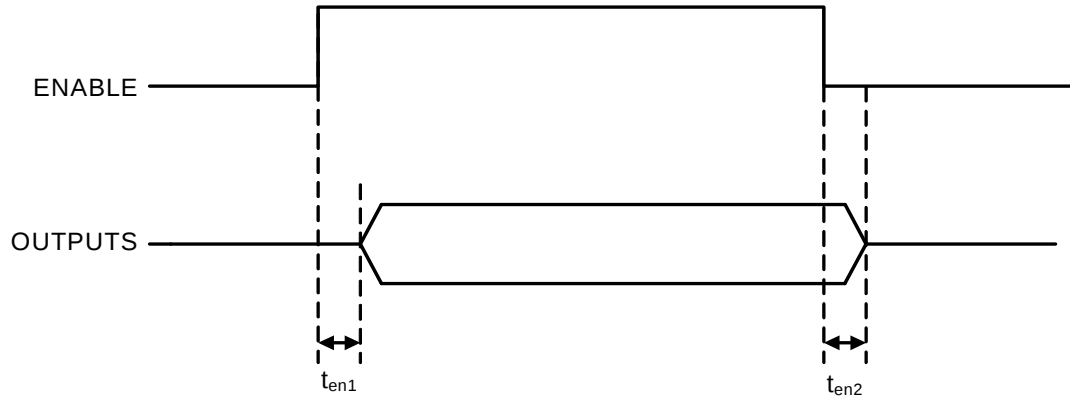
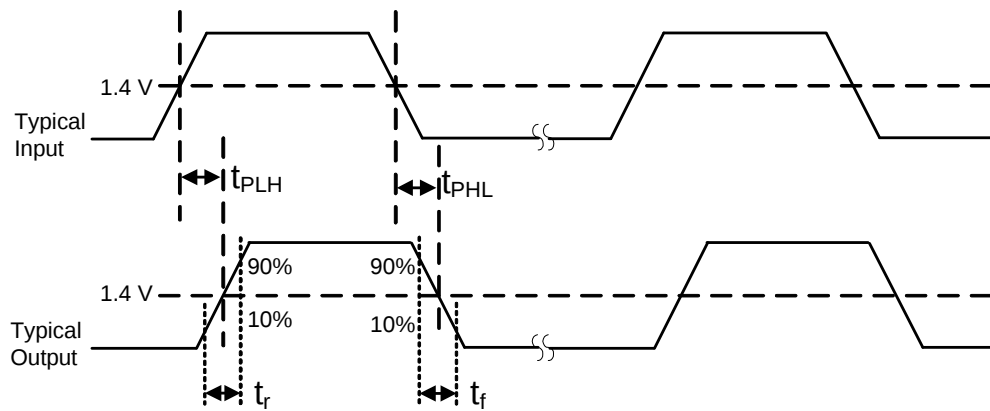


**Figure 1. ENABLE Timing Diagram****Figure 2. Propagation Delay Timing**

2.2. Eye Diagram

Figure 7 illustrates an eye-diagram taken on an Si8650. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8650 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 350 ps peak jitter were exhibited.

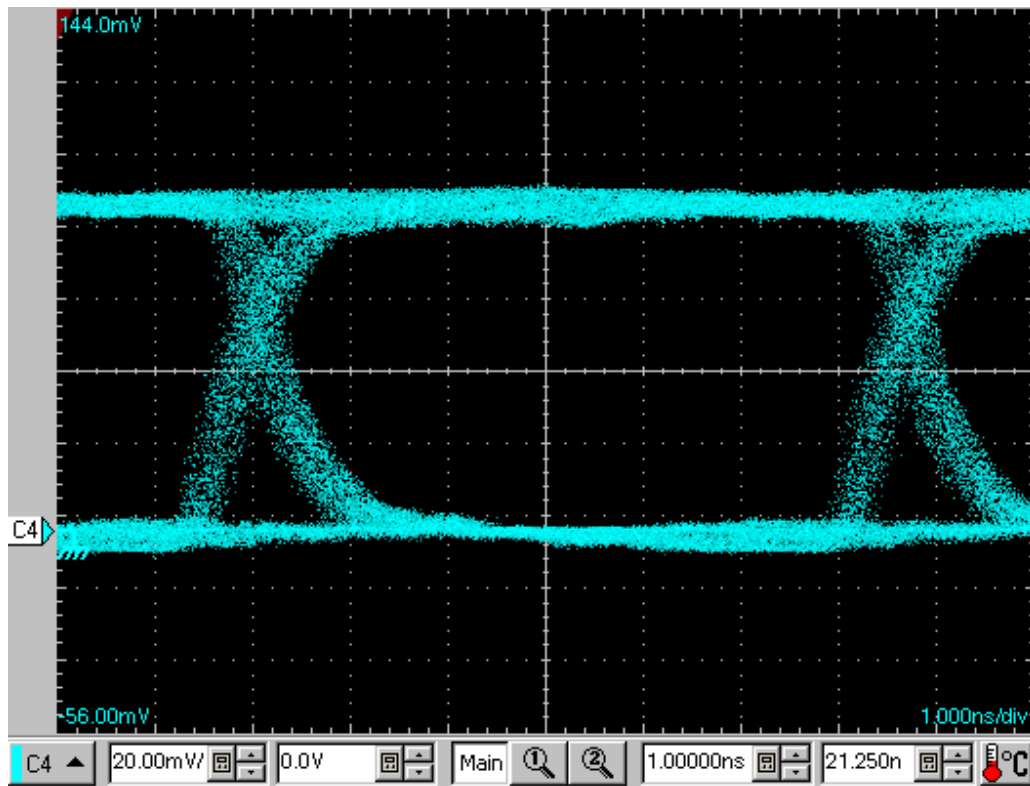
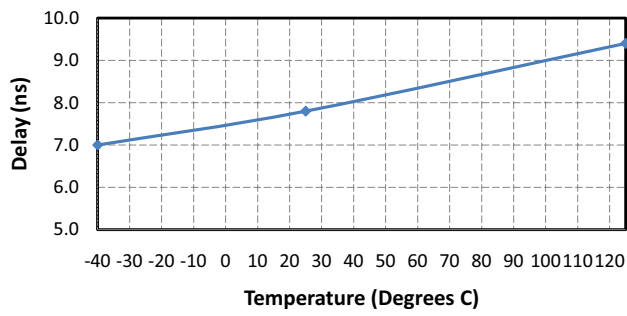


Figure 7. Eye Diagram



**Figure 15. Propagation Delay
vs. Temperature**

Table 17. Package Diagram Dimensions (Continued)

Dimension	Min	Max
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	
Notes: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC. 4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

10. Land Pattern: 16-Pin Narrow Body SOIC

Figure 19 illustrates the recommended land pattern details for the Si865x in a 16-pin narrow-body SOIC. Table 18 lists the values for the dimensions shown in the illustration.

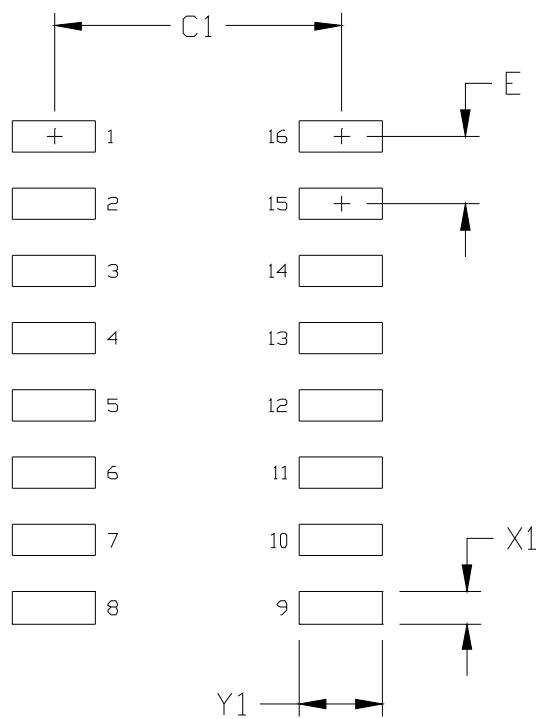


Figure 19. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 18. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55
Notes: 1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion). 2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.		

Table 19. Package Diagram Dimensions (Continued)

Dimension	Min	Max
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	
Notes: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation AB. 4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

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