

# DATA SHEET

## **PDTC123E series**

NPN resistor-equipped transistors;

$R1 = 2.2\text{ k}\Omega$ ,  $R2 = 2.2\text{ k}\Omega$

Product specification  
Supersedes data of 1999 May 21

2003 Apr 10

# NPN resistor-equipped transistors; R1 = 2.2 k $\Omega$ , R2 = 2.2 k $\Omega$

## PDTC123E series

### FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

### APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

### DESCRIPTION

NPN resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	–	50	V
I <sub>O</sub>	output current (DC)	–	100	mA
R1	bias resistor	2.2	–	k $\Omega$
R2	bias resistor	2.2	–	k $\Omega$

### PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP COMPLEMENT
	PHILIPS	EIAJ		
PDTC123EK	SOT346	SC-59	48	PDTA123EK
PDTC123ES	SOT54 (TO-92)	SC-43	TC123E	PDTA123ES
PDTC123ET	SOT23	–	*26 <sup>(1)</sup>	PDTA123ET
PDTC123EU	SOT323	SC-70	*48 <sup>(1)</sup>	PDTA123EU

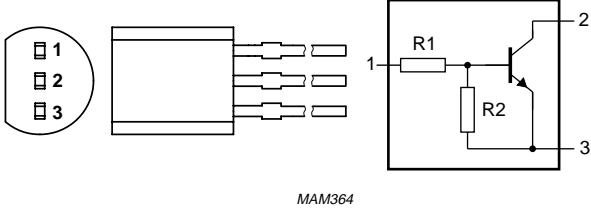
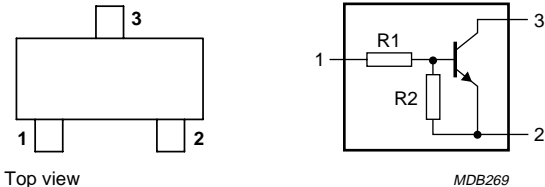
### Note

- \* = p: Made in Hong Kong.  
\* = t: Made in Malaysia.  
\* = W: Made in China.

NPN resistor-equipped transistors;  
R1 = 2.2 kΩ, R2 = 2.2 kΩ

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTC123ES	 <i>MAM364</i>	1 2 3	base collector emitter
PDTC123EK PDTC123ET PDTC123EU	 Top view <i>MDB269</i>	1 2 3	base emitter collector

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CBO</sub>	collector-base voltage	open emitter	–	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	10	V
V <sub>I</sub>	input voltage				
	positive		–	+12	V
	negative		–	–10	V
I <sub>O</sub>	output current (DC)		–	100	mA
I <sub>CM</sub>	peak collector current		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1			
	SOT54		–	500	mW
	SOT23		–	250	mW
	SOT346		–	250	mW
	SOT323		–	200	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C

### Note

1. Refer to standard mounting conditions.

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	in free air; note 1		
	SOT54		250	K/W
	SOT23		500	K/W
	SOT346		500	K/W
	SOT323		625	K/W

### Note

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**CHARACTERISTICS**

T<sub>amb</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0	–	–	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0	–	–	1	$\mu$ A
		V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0; T <sub>j</sub> = 150 °C	–	–	50	$\mu$ A
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0	–	–	2	mA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 20 mA	30	–	–	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 10 mA; I <sub>B</sub> = 0.5 mA	–	–	150	mV
V <sub>i(off)</sub>	input-off voltage	I <sub>C</sub> = 1 mA; V <sub>CE</sub> = 5 V	–	1.2	0.5	V
V <sub>i(on)</sub>	input-on voltage	I <sub>C</sub> = 20 mA; V <sub>CE</sub> = 0.3 V	2	1.6	–	V
R1	input resistor		1.54	2.2	2.86	k $\Omega$
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C <sub>c</sub>	collector capacitance	I <sub>E</sub> = I <sub>e</sub> = 0; V <sub>CB</sub> = 10 V; f = 1 MHz	–	–	2.5	pF

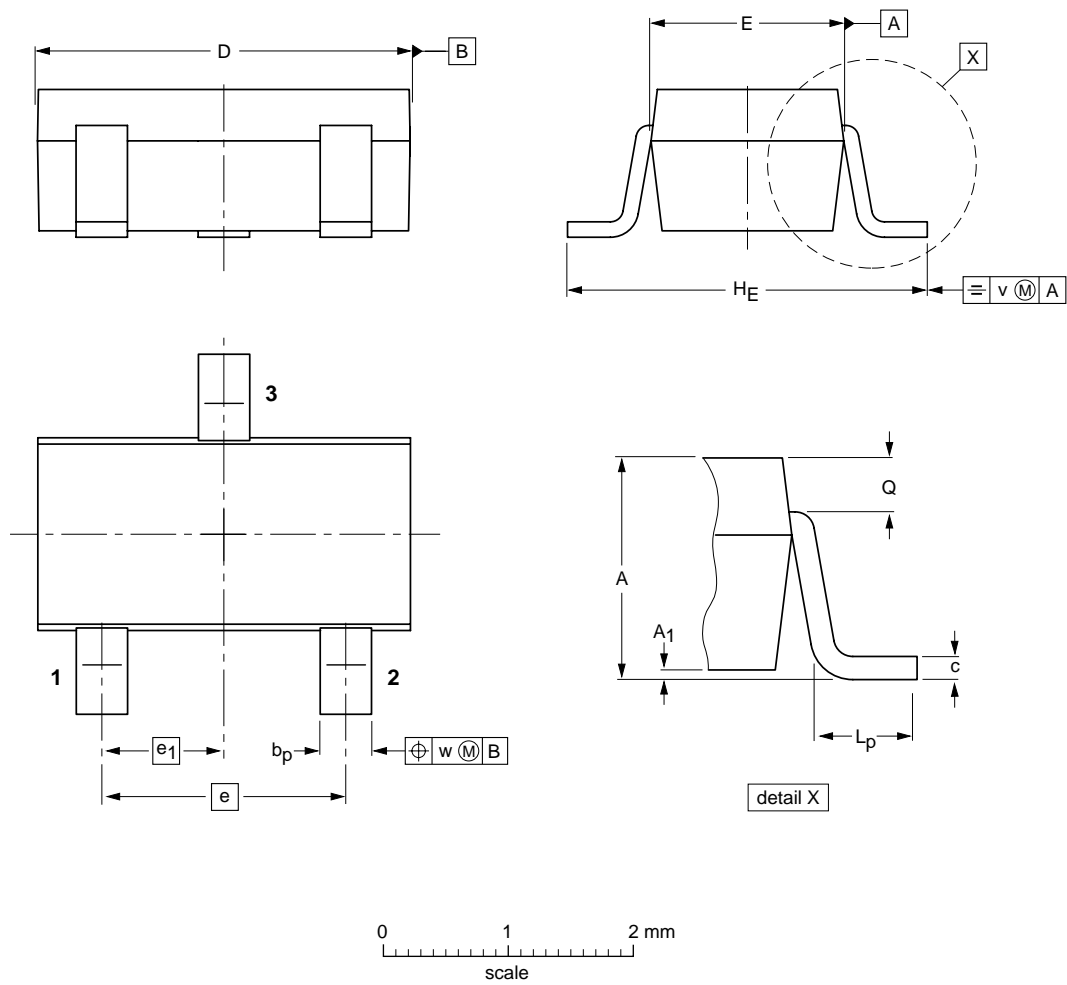
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PACKAGE OUTLINES


Plastic surface mounted package; 3 leads

SOT346



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.3 1.0	0.1 0.013	0.50 0.35	0.26 0.10	3.1 2.7	1.7 1.3	1.9	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2

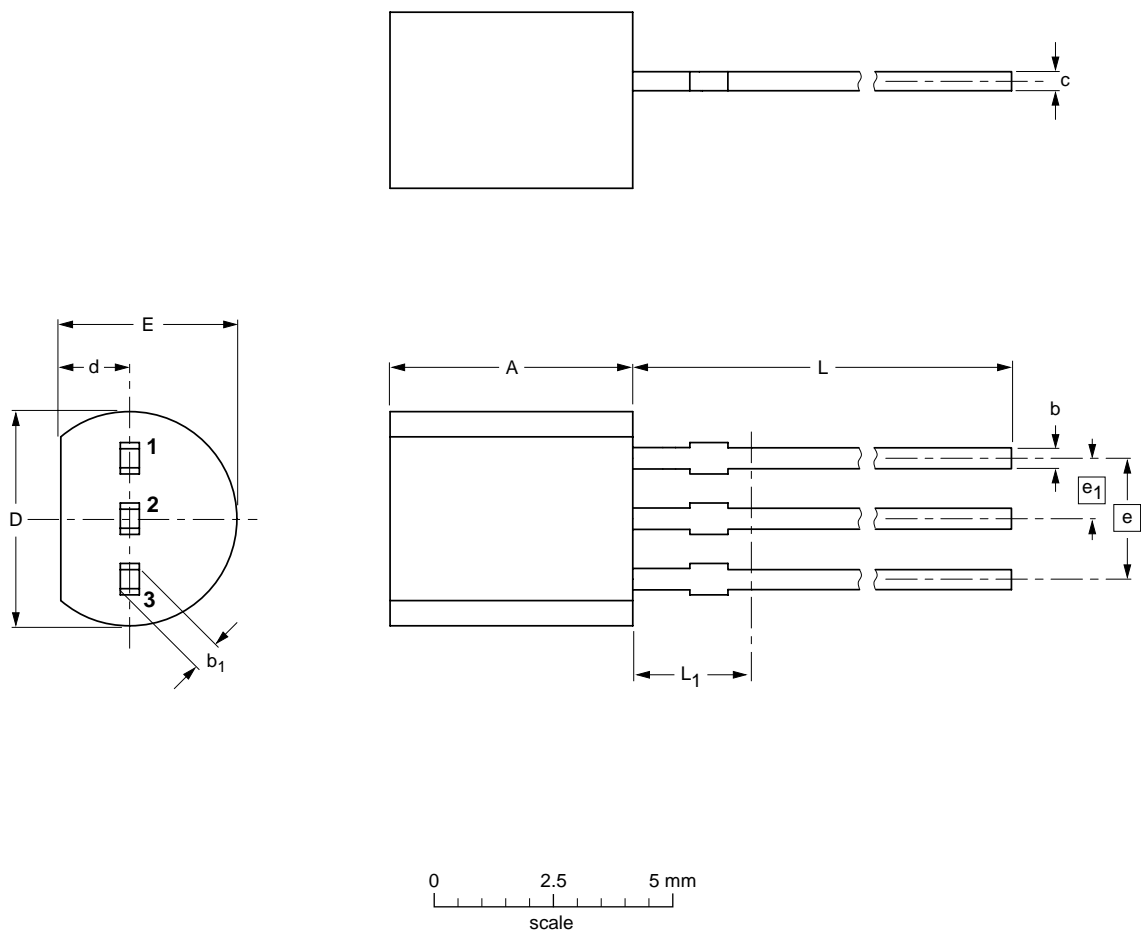
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT346		TO-236	SC-59			98-07-17

NPN resistor-equipped transistors;  
R1 = 2.2 kΩ, R2 = 2.2 kΩ

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Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup>
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

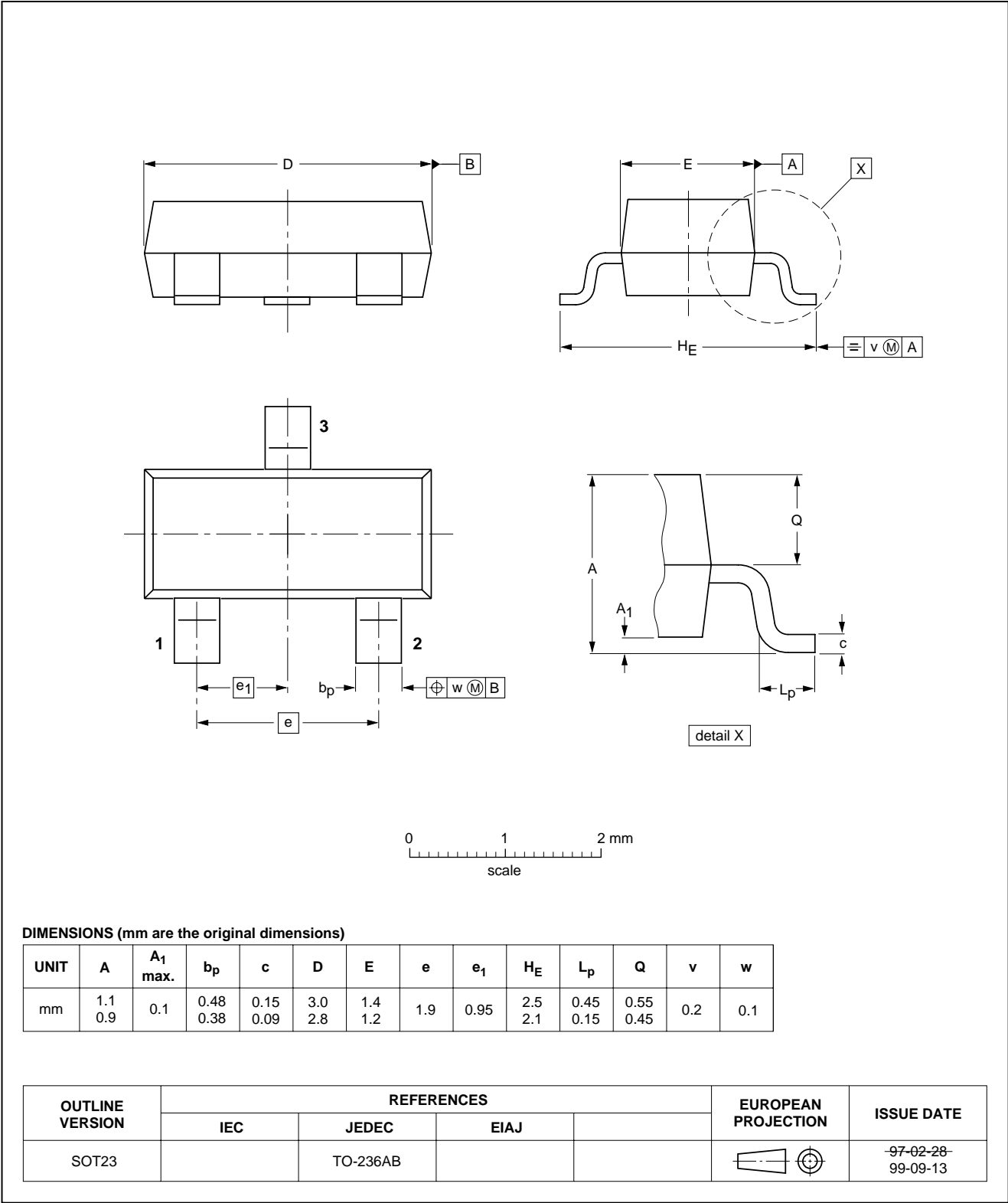
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

NPN resistor-equipped transistors;  
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PDTC123E series

Plastic surface mounted package; 3 leads

SOT23



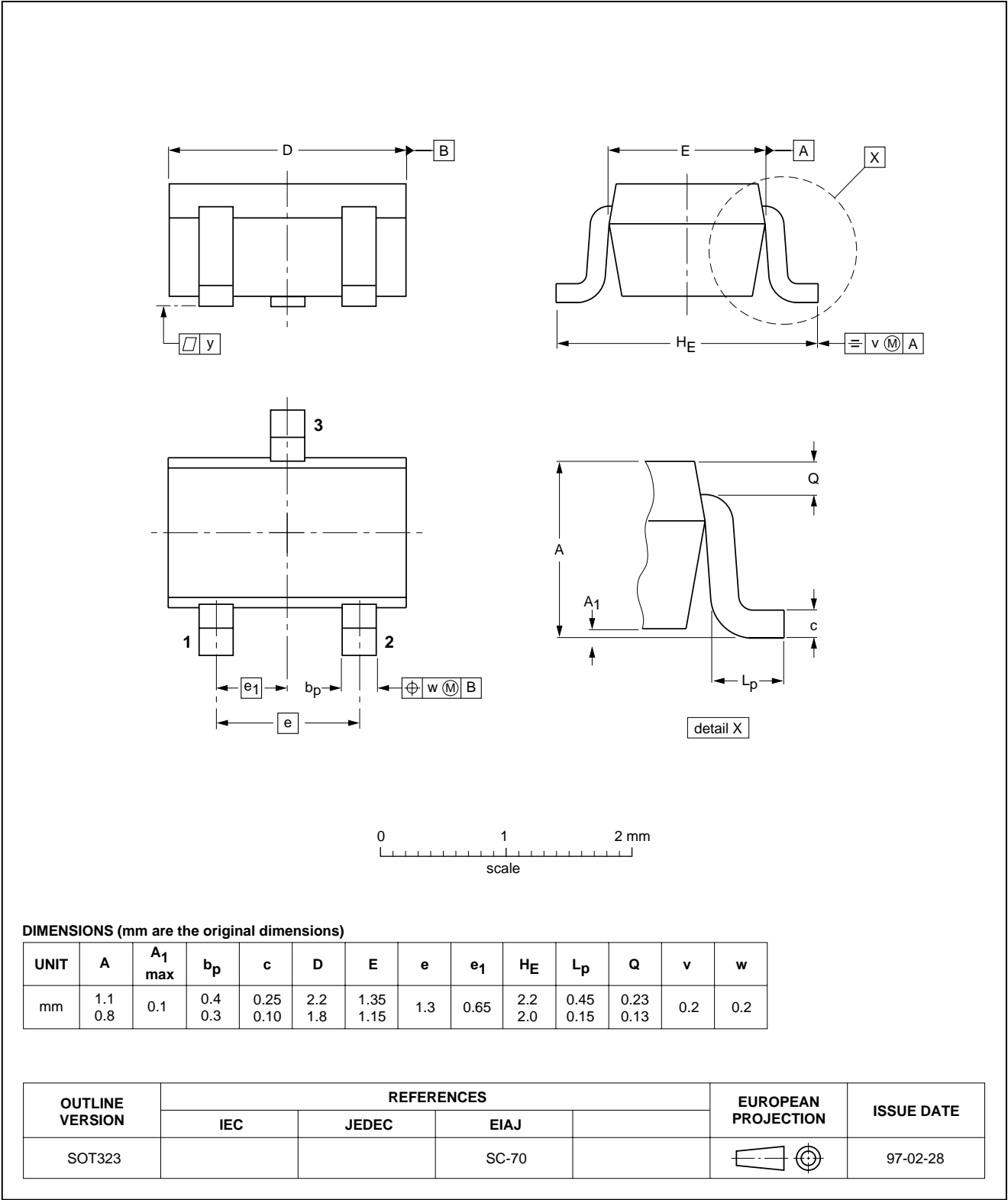


NPN resistor-equipped transistors;  
R1 = 2.2 kΩ, R2 = 2.2 kΩ

PDTC123E series

Plastic surface mounted package; 3 leads

SOT323



NPN resistor-equipped transistors;  
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#### DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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PDTC123E series

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**NOTES**

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Printed in The Netherlands

613514/04/pp12

Date of release: 2003 Apr 10

Document order number: 9397 750 11014

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