Secondary Side, Off-Line Battery Charger Controllers

ADP3810/ADP3811

FEATURES

Programmable Charge Current
High Precision Battery Voltage Limit
Precision 2.000 V Reference
Low Voltage Drop Current Sense: 300 mV Full Scale
Full Operation in Shorted and Open Battery Conditions
Drives Diode-Side of Optocoupler
Wide Operating Supply Range: 2.7 V to 16 V
Undervoltage Lockout
SO-8 Package
ADP3810
- **Internal Precision Voltage Divider for Battery Sense**
- **Four Final Battery Voltage Options Available: 4.2 V, 8.4 V, 12.6 V, 16.8 V**

ADP3811
- **Adjustable Final Battery Voltage**

APPLICATIONS

Battery Charger Controller for:
- **LiIon Batteries (ADP3810)**
- **NiCad, NiMH Batteries (ADP3811)**

GENERAL DESCRIPTION

The ADP3810 and ADP3811 combine a programmable current limit with a battery voltage limit to provide a constant current, constant voltage battery charger controller. In secondary side, off-line applications, the output directly drives the diode side of an optocoupler to give isolated feedback control of a primary side PWM. The circuitry includes two gain (g_m) stages, a precision 2.0 V reference, a control input buffer, an Undervoltage Lock Out (UVLO) comparator, an output buffer and an overvoltage comparator.

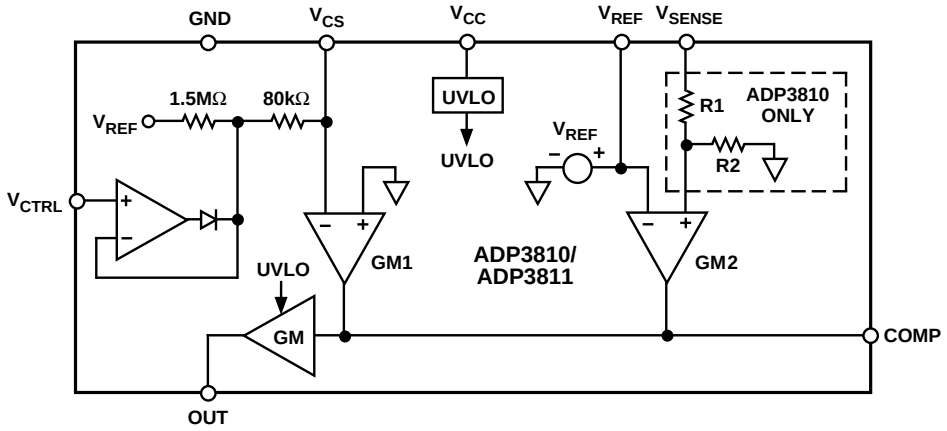
The current limit amplifier senses the voltage drop across an external sense resistor to control the average current for charging a battery. The voltage drop can be adjusted from 25 mV to 300 mV, giving a charging current limit from 100 mA to 1.2 amps with a 0.25 Ω sense resistor. An external dc voltage on the V_{CTRL} input sets the voltage drop. Because this input is high impedance, a filtered PWM output can be used to set the voltage.

As the battery voltage approaches its voltage limit, the voltage sense amplifier takes over to maintain a constant battery voltage. The two amplifiers essentially operate in an "OR" fashion. Either the current is limited, or the voltage is limited.

The ADP3810 has internal thin-film resistors that are trimmed to provide a precise final voltage for LiIon batteries. Four voltage options are available, corresponding to 1-4 LiIon cells as follows: 4.2 V, 8.4 V, 12.6 V and 16.8 V.

The ADP3811 omits these resistors allowing any battery voltage to be programmed with external resistors.

FUNCTIONAL BLOCK DIAGRAM



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ADP3810/ADP3811–SPECIFICATIONS ($-40°C \le T_A \le +85°C$, V_{CC} = 10.0 V, unless otherwise noted)

Parameter	Conditions	Symbol	ADP3810 Min	ADP3810 Typ	ADP3810 Max	Units
CURRENT SENSE[1]						
Full-Scale Current Sense Voltage	V_{CTRL} = 1.2 V		–315	–300	–285	mV
Minimum Current Sense Voltage	0.0 V ≤ V_{CTRL} ≤ 0.1 V		–32	–25	–18	mV
Current Programming Input Range		V_{CTRL}	0.0		1.2	V
Gain (V_{OUT}/V_{CS})	R_L = 1 kΩ	A_{VCS}	74	86		dB
Control Input Bias Current	V_{CTRL} Pin	I_{BCTRL}		10	40	nA
VOLTAGE SENSE						
Accuracy[2]—ADP3810			–1.0		+1.0	%
Input Resistance—ADP3810	4.2 V Option	R_{IN}		210k		Ω
Input Resistance—ADP3810	8.4 V Option	R_{IN}		420k		Ω
Input Resistance—ADP3810	12.6 V Option	R_{IN}		630k		Ω
Input Resistance—ADP3810	16.8 V Option	R_{IN}		840k		Ω
Offset Voltage—ADP3811		V_{OS}	–2.5		+2.5	mV
Bias Current—ADP3811		I_B		1	10	nA
Gain (V_{OUT}/V_{SENSE})[3]	R_L = 1 kΩ	A_{VBAT}	60	74		dB
REFERENCE						
Output Voltage	C_L = 0.1 μF[4]	V_{REF}		2.000		V
Accuracy						
ADP3810			–1.0		+1.0	%
ADP3811			–1.8		+1.8	%
Load Regulation	I_{LOAD} = 0 mA to 5 mA		–0.25		+0.25	%
Line Regulation	V_{CC} = 2.7 V to 16 V			0.004	0.02	%/V
Output Voltage Noise	0.1 Hz to 10 Hz	e_N		35		μV p-p
Load Current (Sourcing)		I_L	5	10		mA
OUTPUT						
Output Current	V_{CC} = 2.7 V	I_{OUT}	4	6		mA
Saturation Voltage	I_{OUT} = 4 mA, V_{CC}–V_{OUT}	V_{SAT}		0.1	0.4	V
Gain (V_{OUT}/V_{COMP})	R_L = 1 kΩ	A_{VOUT}		6		V/V
UNDERVOLTAGE LOCKOUT						
Trip Point-On				2.65	2.7	V
Trip Point-Off			2.5	2.6		V
POWER SUPPLY						
Operating Range			2.7		16	V
Quiescent Current	V_{CC} ≥ 2.7 V	I_Q		1.5	3	mA
Turn-Off Current	V_{CC} ≤ 2.5 V			0.5	1	mA
OVERVOLTAGE COMPARATOR						
Threshold						
ADP3810	Percent Above Full Scale[5]	V_{OV}%		6		%
ADP3811	Percent Above Full Scale[5]	V_{OV}%		6		%
Response Time	I_{OUT} from 0 mA to 2 mA	t_r		8		μs

NOTES

[1]20 kΩ resistor from current sense voltage to V_{CS} pin.

[2]Applies to 4.2 V, 8.4 V, 12.6 V and 16.8 V options. Includes all error from offset voltage, bias current, resistor divider and voltage reference.

[3]Does not include attenuation of input resistor divider for ADP3810.

[4]0.1 μF load capacitor required for reference operation.

[5]Full scale is the programmed final battery voltage: 4.2 V, 8.4 V, 12.6 V or 16.8 V for the ADP3810 or 2.0 V at V_{SENSE} for the ADP3811.

All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Specifications subject to change without notice.

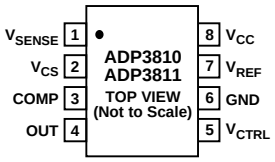
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . –0.4 V to 18 V
V_{CTRL}, V_{CS} Input Range . . . . . –0.4 V to V_{CC}
V_{SENSE} Input Range (ADP3811) . . . . . –0.4 V to V_{CC}
V_{SENSE} Input Range (ADP3810) . . . . . –0.4 V to 20 V
Maximum Power Dissipation . . . . . 500 mW
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to 150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

ORDERING GUIDE

Model	Temperature Range	Package Option	Battery Voltage
ADP3810AR-4.2	–40°C to +85°C	SO-8	4.2 V
ADP3810AR-8.4	–40°C to +85°C	SO-8	8.4 V
ADP3810AR-12.6	–40°C to +85°C	SO-8	12.6 V
ADP3810AR-16.8	–40°C to +85°C	SO-8	16.8 V
ADP3811AR	–40°C to +85°C	SO-8	Adjustable

PIN CONFIGURATION



PIN DESCRIPTION

Mnemonic	Function
V_{SENSE}	Battery Voltage Sense Input.
V_{CS}	Current Sense Input.
V_{REF}	Reference Output. Nominally 2.0 V.
COMP	External Compensation Pin.
OUT	Optocoupler Current Output Drive.
V_{CTRL}	DC Control Input to Set Current Limit, 0 V to 1.2 V.
V_{CC}	Positive Supply.
GND	Ground Pin.

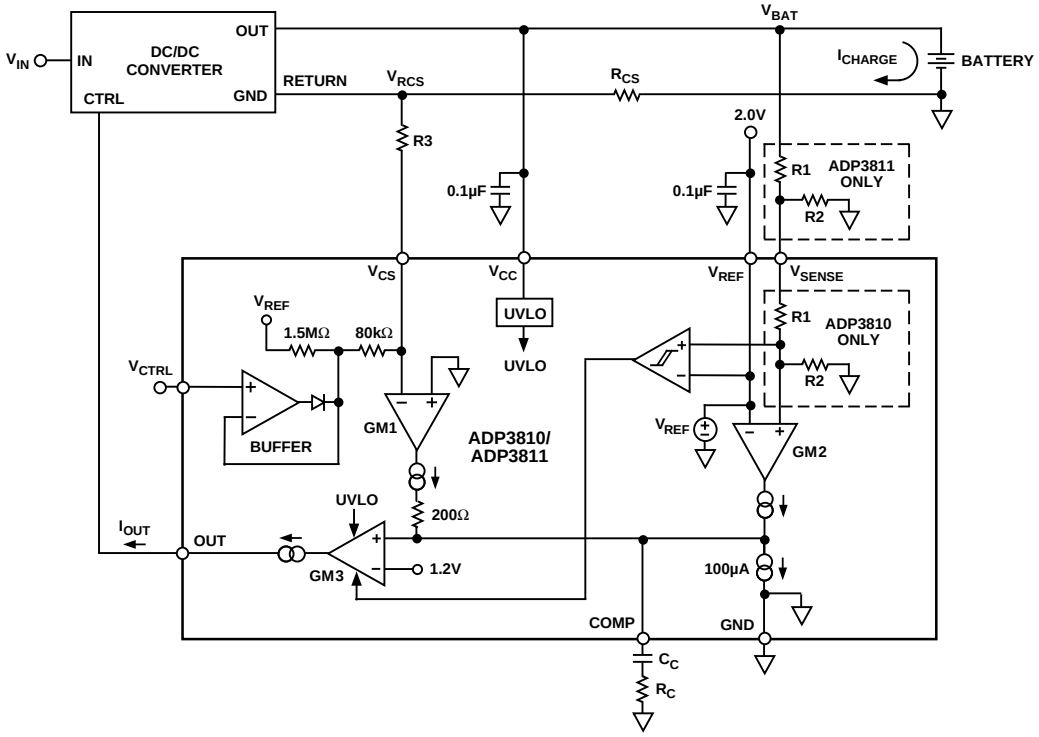


Figure 1. Simplified Battery Charger

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3810/ADP3811 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ADP3810/ADP3811–Typical Performance Characteristics

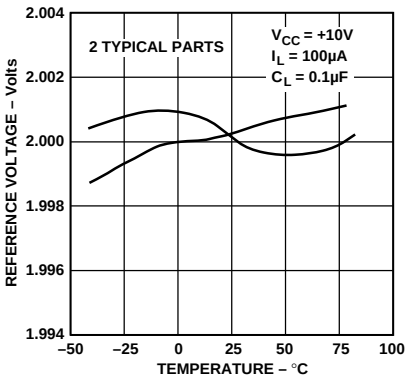


Figure 2. Reference Output Voltage vs. Temperature for Two Typical Parts

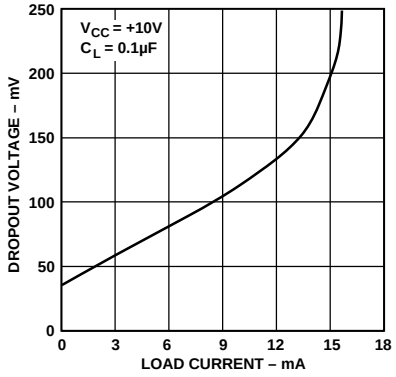


Figure 3. Reference Drop-Out Voltage (V_{CC}–V_{REF}) vs. Load Current

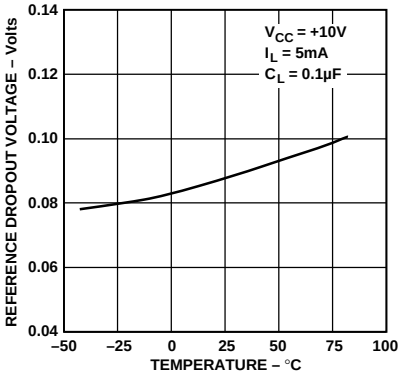


Figure 4. Reference Dropout Voltage vs. Temperature

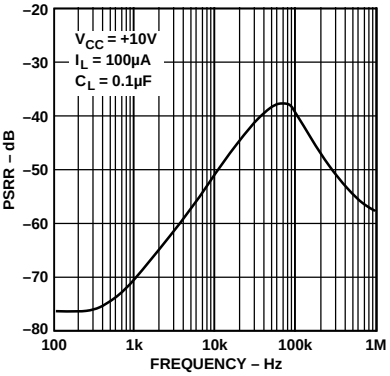


Figure 5. Reference PSRR vs. Frequency

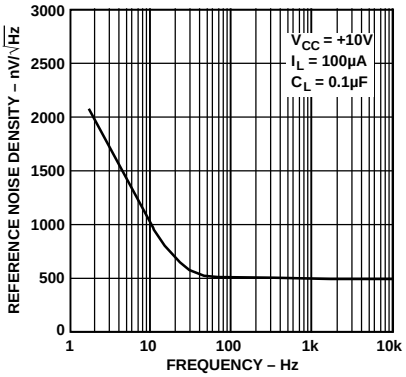


Figure 6. Reference Noise Density vs. Frequency

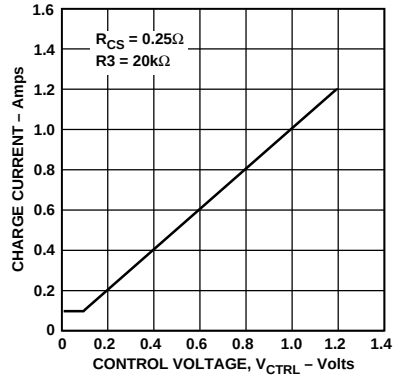


Figure 7. Charge Current vs. Control Voltage

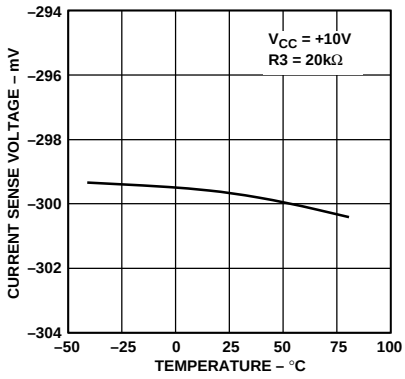


Figure 8. Full-Scale Current Sense Voltage vs. Temperature

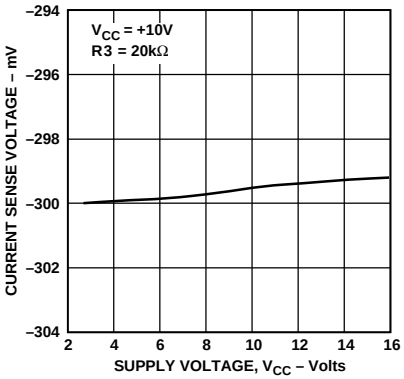


Figure 9. Full-Scale Current Sense Voltage vs. V_{CC}

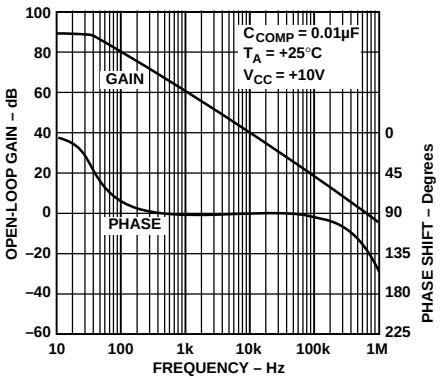


Figure 10. GM1 Open-Loop Gain and Phase vs. Frequency

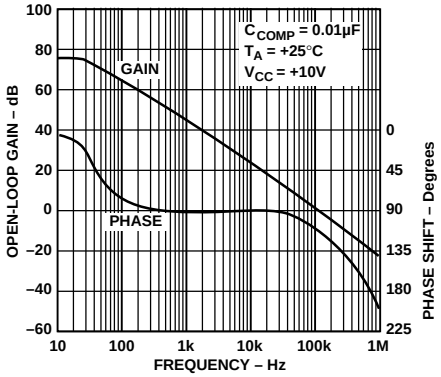


Figure 11. GM2 Open-Loop Gain and Phase vs. Frequency

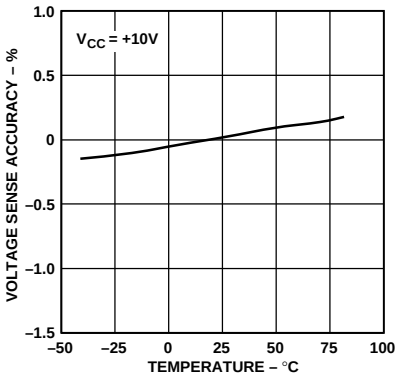


Figure 12. ADP3810 Voltage Sense Accuracy vs. Temperature

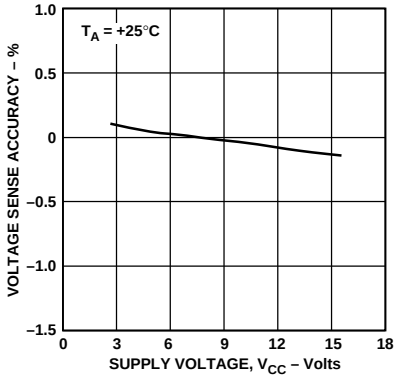


Figure 13. ADP3810 Voltage Sense Accuracy vs. V_{CC}

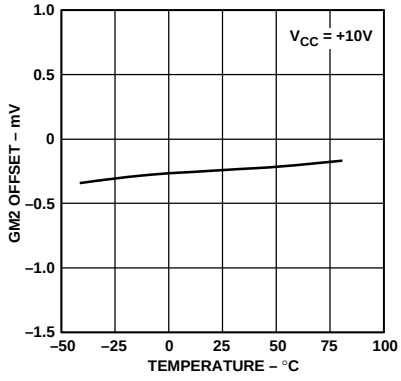


Figure 14. ADP3811 GM2 Offset vs. Temperature

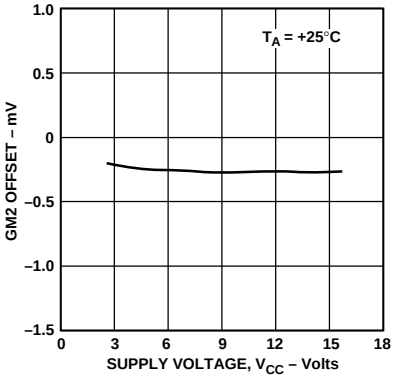


Figure 15. ADP3811, GM2 Offset vs. V_{CC}

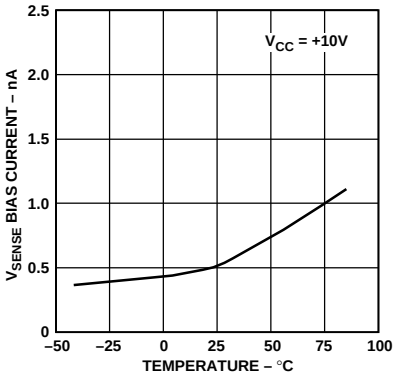


Figure 16. ADP3811 V_{SENSE} Bias Current vs. Temperature

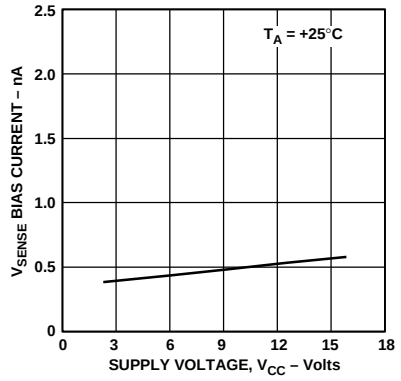


Figure 17. ADP3811 V_{SENSE} Bias Current vs. V_{CC}

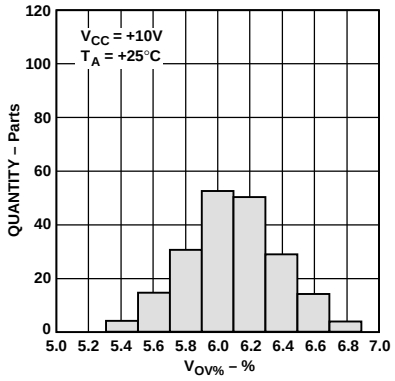


Figure 18. Overvoltage Comparator Distribution ($V_{OV\%}$)

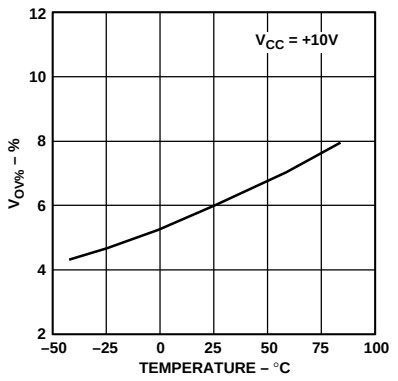


Figure 19. Overvoltage Comparator Threshold ($V_{OV\%}$) vs. Temperature

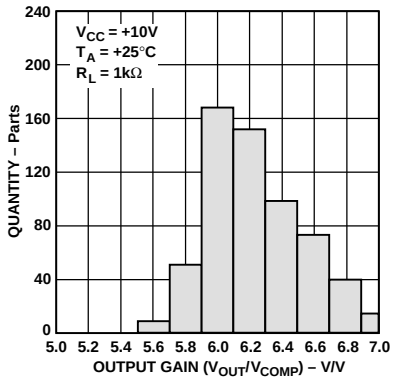


Figure 20. Output Gain (V_{OUT}/V_{COMP}) Distribution

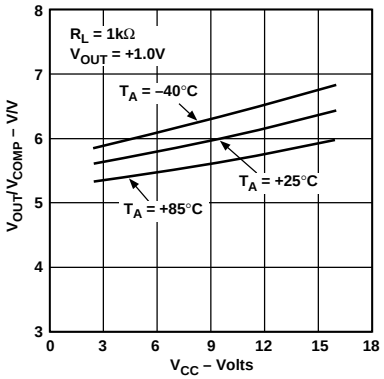


Figure 21. Output Gain (V_{OUT}/V_{COMP}) vs. V_{CC}

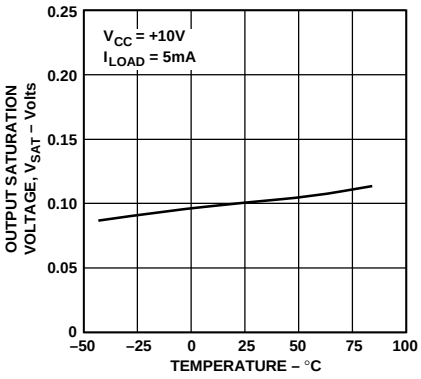


Figure 22. V_{SAT} vs. Temperature

APPLICATIONS SECTION

Functional Description

The ADP3810 and ADP3811 are designed for charging NiCad, NiMH and LiIon batteries. Both parts provide accurate voltage sense and current sense circuitry to control the charge current and final battery voltage. Figure 1 shows a simplified battery charging circuit with the ADP3810/ADP3811 controlling an external dc-dc converter. The converter can be one of many different types such as a Buck converter, Flyback converter or a linear regulator. In all cases, the ADP3810/ADP3811 maintains accurate control of the current and voltage loops, enabling the use of a low cost, industry standard dc-dc converter without compromising system performance. Detailed realizations of complete circuits including the dc-dc converter are included later in this data sheet.

The ADP3810 and ADP3811 contain the following blocks (shown in Figure 1):

- Two "GM" type error amplifiers control the current loop (GM1) and the voltage loop (GM2).
- A common COMP node is shared by both GM amplifiers such that an RC network at this node helps compensate both control loops.
- A precision 2.0 V reference is used internally and is available externally for use by other circuitry. The 0.1 µF bypass capacitor shown is required for stability.
- A current limited buffer stage (GM3) provides a current output, I_{OUT}, to control an external dc-dc converter. This output can directly drive an optocoupler in isolated converter applications. The dc-dc converter must have a control scheme such that higher I_{OUT} results in lower duty cycle. If this is not the case, a simple, single transistor inverter can be used for control phase inversion.
- An amplifier buffers the charge current programming voltage, V_{CTRL}, to provide a high impedance input.
- An UVLO circuit shuts down the GM amplifiers and the output when the supply voltage (V_{CC}) falls below 2.7 V. This protects the charging system from indeterminate operation.
- A transient overshoot comparator quickly increases I_{OUT} when the voltage on the "+" input of GM2 rises over 120 mV above V_{REF}. This clamp shuts down the dc-dc converter to quickly recover from overvoltage transients and protect external circuitry.

Description of Battery Charging Operation

The IC based system shown in Figure 1 charges a battery with a dc current supplied by a dc-dc converter, which is most likely a switching type supply but could also be a linear supply where feasible. The value of the charge current is controlled by the feedback loop comprised of R_{CS}, R3, GM1, the external dc-dc converter and a dc voltage at the V_{CTRL} input. The actual charge current is set by the voltage, V_{CTRL}, and is dependent upon the choice for the values of R_{CS} and R3 according to the formula below:

$$I_{CHARGE} = \frac{1}{R_{CS}} \times \frac{R3}{80\,k\Omega} \times V_{CTRL}$$

Typical values are R_{CS} = 0.25 Ω and R3 = 20 kΩ, which result in a charge current of 1.0 A for a control voltage of 1.0 V. The 80 kΩ resistor is internal to the IC, and it is trimmed to its absolute value. The positive input of GM1 is referenced to ground, forcing the V_{CS} pin to a virtual ground.

The resistor R_{CS} converts the charge current into the voltage at V_{RCS}, and it is this voltage that GM1 is regulating. The voltage at V_{RCS} is equal to –(R3/80 kΩ) V_{CTRL}. When V_{CTRL} equals 1.0 V, V_{RCS} equals –250 mV. If V_{RCS} falls below its programmed level (i.e., the charge current increases), the negative input of GM1 goes slightly below ground. This causes the output of GM1 to source more current and drive the COMP node high, which forces the current, I_{OUT}, to increase. A higher I_{OUT} decreases the drive to the dc-dc converter, reducing the charging current and balancing the feedback loop.

As the battery approaches its final charge voltage, the voltage loop takes over. The system becomes a voltage source, floating the battery at constant voltage thereby preventing overcharging. The constant voltage feature also protects the circuitry that is actually powered by the battery from overvoltage if the battery is removed. The voltage loop is comprised of R1, R2, GM2 and the dc-dc converter. The final battery voltage is simply set by the ratio of R1 and R2 according to the following equation (V_{REF} = 2.000 V):

$$V_{BAT} = 2.000\,V \times \left(\frac{R1}{R2} + 1\right)$$

If the battery voltage rises above its programmed voltage, V_{SENSE} is pulled above V_{REF}. This causes GM2 to source more current, raising the COMP node voltage and I_{OUT}. As with the

current loop, the higher I_{OUT} reduces the duty cycle of the dc-dc converter and causes the battery voltage to fall, balancing the feedback loop.

Each GM stage is designed to be asymmetrical so that each amplifier can only source current. The outputs are tied together at the COMP node and loaded with an internal constant current sink of approximately 100 μA. Whichever amplifier sources more current controls the voltage at the COMP node and therefore controls the feedback. This scheme is a realization of an analog "OR" function where GM1 or GM2 has control of the dc-dc converter and the charging circuitry. Whenever the circuit is in full current limiting or full voltage limiting, the respective GM stage sources an identical amount of current to the fixed current sink. The other GM stage sources zero current and is out of the loop. In the transition region, both GM stages source some of the current to comprise the full amount of the current sink. The high gains of GM1 and GM2 ensure a smooth but sharp transition from current control to voltage control. Figure 24 shows a graph of the transition from current to voltage mode, that was measured on the circuit in Figure 23 as detailed below. Notice that the current stays at its full programmed level until the battery is within 200 mV of the final programmed voltage (10 V in this case), which maintains fast charging through almost all of the battery voltage range. This improves the speed of charging compared to a scheme that reduces the current at lower battery voltages.

The second element in a battery charging system is some form of a dc-dc converter. To achieve high efficiency, the dc-dc converter can be an isolated off-line switching power supply, or it can be an isolated or nonisolated Buck or other type of switching power supply. For lower efficiency requirements, a linear regulator fed from a wall adapter can be used. In the above discussion, the current, I_{OUT}, controls the duty cycle of a switching supply; but in the case of the linear regulator, I_{OUT} controls the pass transistor drive. Examples of these topologies are shown later in this data sheet. If an off-line supply such as a flyback converter is used, and isolation between the control logic and the ADP3810/ADP3811 is required, an optocoupler can be inserted between the ADP3810/ADP3811 output and the control input of the primary side PWM.

Charge Termination

If the system is charging a LiIon battery, the main criteria to determine charge termination is the absolute battery voltage. The ADP3810, with its accurate reference and internal resistors, accomplishes this task. The ADP3810's guaranteed accuracy specification of ±1% of the final battery voltage ensures that a LiIon battery will not be overcharged. This is especially important with LiIon batteries because overcharging can lead to catastrophic failure. It is also important to insure that the battery be charged to a voltage equal to its optimal final voltage (typically 4.2 V per cell). Stopping at less than 1% of full-scale results in a battery that has not been charged to its full mAh capacity, reducing the battery's run time and the end equipment's operating time.

The ADP3810/ADP3811 does not include circuitry to detect charge termination criteria such as $-\Delta V/\Delta t$ or $\Delta T/\Delta t$, which are common for NiCad and NiMH batteries. If such charge termination schemes are required, a low cost microcontroller can be added to the system to monitor the battery voltage and temperature. A PWM output from the microcontroller can subsequently program the V_{CTRL} input to set the charge current. The high impedance of V_{CTRL} enables the inclusion of an RC filter to integrate a PWM output into a dc control voltage.

Compensation

The voltage and current loops have significantly different natural and crossover frequencies in a battery charger application, so the two loops most likely need different pole/zero feedback compensation. Figure 1 shows a single RC network from the COMP node to ground. This is primarily for low frequency compensation (f_C< 100 Hz) of the voltage loop. Since the COMP node is shared by both GM stages, this compensation also affects the current loop. The internal 200 Ω resistor does change the zero location of the compensation for the current loop with respect to the voltage loop. To provide a separate higher frequency compensation (f_C ~ 1 kHz–10 kHz), a second series RC may be needed. A detailed calculation of the compensation values is given later in this data sheet.

ADP3810 and ADP3811 Differences

The main difference between the ADP3810 and the ADP3811 is illustrated in Figure 1. The resistors R1 and R2 are external for the ADP3811 and internal for the ADP3810. The ADP3810 is specifically designed for LiIon battery charging, and thus, the internal resistors are precision thin-film resistors laser trimmed for LiIon cell voltages. Four different final voltage options are available in the ADP3810: 4.2 V, 8.4 V, 12.6 V, and 16.8 V. For slightly different voltages to accommodate different LiIon chemistries, please contact the factory. The ADP3811 does not include the internal resistors, allowing the designer to choose any final battery voltage by appropriately selecting the external resistors. Because the ADP3810 is specifically for LiIon batteries, the reference is trimmed to a tighter accuracy specification of ±1% instead of ±2% for the ADP3811.

V_{CTRL} Input and Charge Current Programming Range

The voltage on the V_{CTRL} input determines the charge current level. This input is buffered by an internal single supply amplifier (labeled BUFFER) to allow easy programmability of V_{CTRL}. For example, for a fixed charge current, V_{CTRL} can be set by a resistor divider from the reference output. If a microcontroller is setting the charge current, a simple RC filter on V_{CTRL} enables the voltage to be set by a PWM output from the micro. Of course, a digital-to-analog converter could also be used, but the high impedance input makes a PWM output the economical choice. The bias current of V_{CTRL} is typically 25 nA, which flows out of the pin.

The guaranteed input voltage range of the buffer is from 0.0 V to 1.2 V. When V_{CTRL} is in the range of 0.0 V to 0.1 V, the output of the internal amplifier is fixed at 0.1 V. This corresponds to a charge current of 100 mA for R_{CS} = 0.25 Ω, R3 = 20 kΩ. The graph of charge current versus V_{CTRL} in Figure 7 shows this relationship. Figure 1 shows a diode in series with the buffer's output and a 1.5 MΩ resistor from V_{REF} to this output. The diode prevents the amplifier from sinking current, so for small input voltages the buffer has an open output. The 1.5 MΩ resistor forms a divider with the internal 80 kΩ resistor to fix the output at 0.1 V, i.e., about 10% of the maximum current. This corresponds to the typical trickle charge current level for NiCad batteries. When V_{CTRL} rises above 0.1 V, the buffer sources current and the output follows the input. The total range of V_{CTRL} from 0.0 V. to 1.2 V results in a charge current range from 100 mA to 1.2 A (for R_{CS} = 0.25 Ω, R3 = 20 kΩ). Larger

charge current levels can be obtained by either reducing the value of R_{CS} or increasing the value of R3. The main penalty of increasing R3 is lower efficiency due to the larger voltage drop across R_{CS}, and the penalty of decreasing R_{CS} is lower accuracy (but higher efficiency) as discussed below.

V_{REF} Output

The internal band gap reference is not only used internally for the voltage and current loops, but it is also available externally if an accurate voltage is needed. The reference employs a pnp output transistor for low dropout operation. Figure 3 shows a typical graph of dropout voltage versus load current. The reference is guaranteed to source 5 mA with a dropout voltage of 400 mV or less. The 0.1 µF capacitor on the reference pin is integral in the compensation of the reference and is therefore required for stable operation. If desired, a larger value of capacitance can also be used for the application, but a smaller value should not be used. This capacitor should be located close to the V_{REF} pin. Additional reference performance graphs are shown in Figures 2 through 6.

Output Stage

The output stage performs two important functions. It is a buffer for the compensation node, and as such, it has a high impedance input. It is also a GM stage. The OUT pin is a current output to enable the direct drive of an optocoupler for isolated applications. The gain from the COMP node to the OUT pin is approximately 5 mA/V. With a load resistor of 1 kΩ, the voltage gain is equal to five as specified in the data sheet. A different load resistor results in a gain equal to $R_L \times$ (5 mA/V). Figures 20 and 21 show how the gain varies from part to part and versus the supply voltage, respectively. The guaranteed output current is 5 mA, which is much more than the typical 1 mA to 2 mA required in most applications.

Current Loop Accuracy Considerations

The accuracy of the current loop is dependent on several factors such as the offset of GM1, the offset of the V_{CTRL} buffer, the ratio of the internal 80 kΩ compared to the external 20 kΩ resistor, and the accuracy of R_{CS}. The specification for current loop accuracy states that the full-scale current sense voltage, V_{RCS}, of –300 mV is guaranteed to be within 15 mV of this value. This assumes an exact 20 kΩ resistor for R3. Any errors in this resistor will result in further errors in the charge current value. For example, a 5% error in resistor value will add a 5% error to the charge current. The same is true for R_{CS}, the current sense resistor. Thus, 1% or better resistors are recommended.

As mentioned above, decreasing the value of R_{CS} increases the charge current. Since it is V_{RCS} that is specified, the actual value of R_{CS} is not accounted for in the specification. An example where R_{CS} = 0.1 Ω illustrates its impact on the accuracy of the charge current. The range of V_{RCS} is from –25 mV ± 5 mV to –300 mV ± 15 mV. This results in a charge current range from 250 mA ± 50 mA to 3 A ± 150 mA, as opposed to a charge current range of 100 mA ± 20 mA to 1.2 A ± 60 mA for R_{CS} = 0.25 Ω. Thus, not only is the minimum current changed, but the absolute variation around the set point is increased (although the percentage variation is the same).

Voltage Loop Accuracy Considerations

The accuracy of the voltage loop is dependent on the offset of GM2, the accuracy of the reference voltage, the bias current of GM2 through R1 and R2, and the ratio of R1/R2. For the demanding application of charging LiIon batteries, the accuracy of the ADP3810 is specified with respect to the final battery voltage. This is tested in a full feedback loop so that the single accuracy specification given in the specification table accounts for all of the errors mentioned above. For the ADP3811, the resistors are external, so the final voltage accuracy needs to be determined by the designer. Certainly, the tolerance of the resistors has a large impact on the final voltage accuracy, and 1% or better is recommended.

Supply Range

The supply range is specified from 2.7 V to 16 V. However, a final battery voltage option for the ADP3810 is 16.8 V. The 16.8 V is divided down by the thin film resistors to 2.0 V internally. Thus, the input to GM2 never sees much more than 2.0 V, which is well below the V_{CC} voltage limit. In fact, V_{CC} can be fixed to 2.7 V and the ADP3810 will still control the charging of a 16.8 V battery stack. The ADP3811, with external resistors, can charge batteries to voltages well in excess of its supply voltage. However, if the final battery voltage is above 16 V, V_{CC} cannot be supplied directly from the battery as it is in Figure 1. Alternative circuits must be employed as will be discussed later. Decoupling capacitors should be located close to the supply pin. The actual value of the capacitors depends on the application, but at the very least a 0.1 µF capacitor should be used.

OFF-LINE, ISOLATED, FLYBACK BATTERY CHARGER

The ADP3810 and ADP3811 are ideal for use in isolated chargers. Because the output stage can directly drive an optocoupler, feedback of the control signal across an isolation barrier is a simple task. Figure 23 shows a complete flyback battery charger with isolation provided by the flyback transformer and the optocoupler. The essential operation of the circuit is not much different from the simplified circuit described in Figure 1. The GM1 loop controls the charge current, and the GM2 loop controls the final battery voltage. The dc-dc converter block is comprised of a primary side PWM circuit and flyback transformer, and the control signal passes through the optocoupler.

The circuit in Figure 23 incorporates all of the features necessary to assure long battery life with rapid charging capability. By using the ADP3810 for charging LiIon batteries, or the ADP3811 for NiCad and NiMH batteries, component count is minimized, reducing system cost and complexity. With the circuit as presented or with its many possible variations, designers no longer need to compromise charging performance and battery life to achieve a cost effective system.

Primary Side Considerations

A typical current-mode flyback PWM controller was chosen for the primary control circuit for several reasons. First and most importantly, it is capable of operating from very small duty cycles to near the maximum designed duty cycle. This makes it a good choice for a wide input ac supply voltage variation requirement, which is usually between 70 V–270 V ac for world wide applications. Add to that the additional requirement of 0% to 100% current control, and the PWM duty cycle must have a wide range. This charger achieves these ranges while maintaining stable feedback loops.

The detailed operation and design of the primary side PWM is widely described in the technical literature and is not detailed here. However, the following explanation should make clear the reasons for the primary side component choices. The PWM frequency is set to around 100 kHz as a reasonable compromise

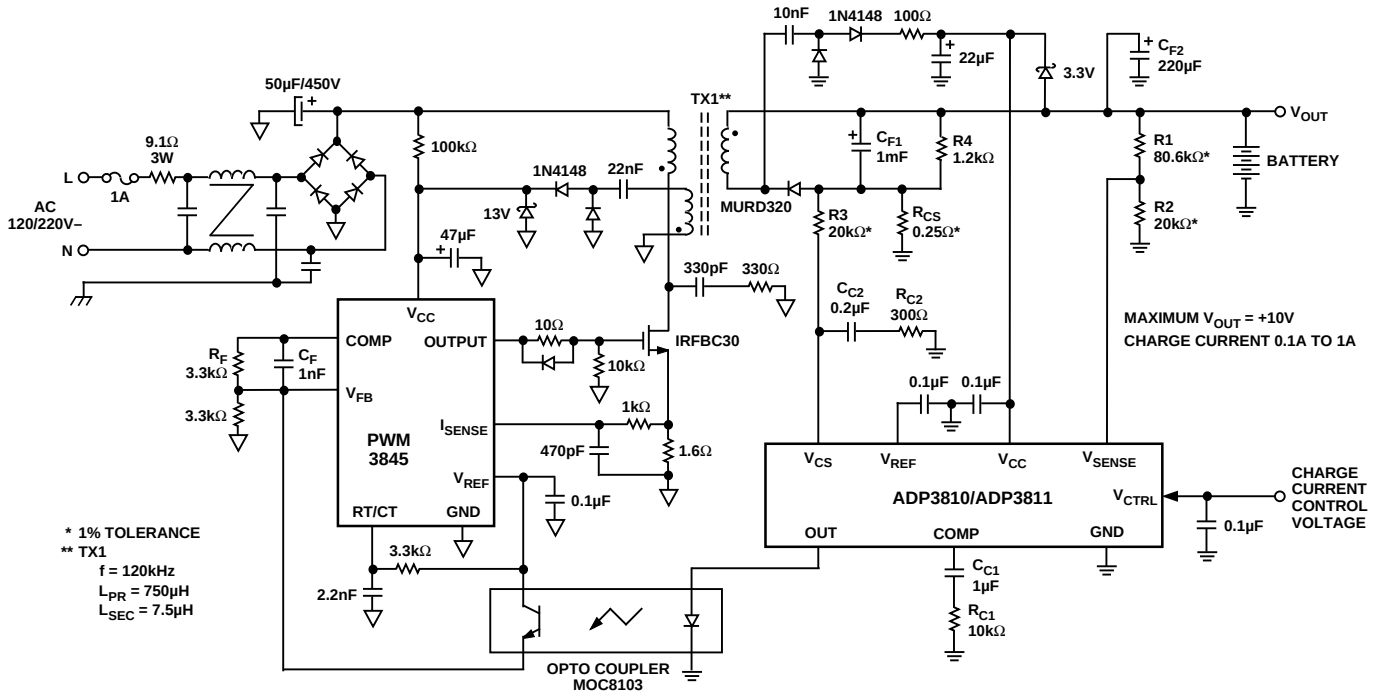


Figure 23. ADP3810/ADP3811 Controlling an Off-Line, Flyback Battery Charger

between inductive and capacitive component sizes, switching losses and cost.

The primary PWM-IC circuit derives its starting V_{CC} through a 100 kΩ resistor directly from the rectified ac input. After start-up, a conventional bootstrapped sourcing circuit from an auxiliary flyback winding wouldn't work, since the flyback voltage would be reduced below the minimum V_{CC} level specified for the 3845 under a shorted or discharged battery condition. Therefore, a voltage doubler circuit was developed (as shown in Figure 23) that provides the minimum required V_{CC} for the IC across the specified ac voltage range even with a shorted battery.

While the signal from the ADP3810/ADP3811 controls the average charge current, the primary side should have a cycle by cycle limit of the switching current. This current limit has to be designed so that, with a failed or malfunctioning secondary circuit or optocoupler, the primary power circuit components (the FET and transformer) won't be overstressed. In addition, during start-up or for a shorted battery, V_{CC} to the ADP3810/ADP3811 won't be present. Thus, the primary side current limit is the only control of the charge current. As the secondary side V_{CC} rises above 2.7 V, the ADP3810/ADP3811 takes over and controls the average current. The primary side current limit is set by the 1.6 Ω current sense resistor connected between the power NMOS transistor, IRFBC30, and ground.

The current drive of the ADP3810/ADP3811's output stage directly connects to the photodiode of an optocoupler with no additional circuitry. With 5 mA of output current, the output stage can drive a variety of optocouplers. An MOC8103 is shown as an example. The current of the photo-transistor flows through the 3.3 kΩ feedback resistor, R_{FB}, setting the voltage at the 3845's COMP pin, thus controlling the PWM duty cycle. The controlled switching regulator should be designed as shown so that more LED current from the optocoupler reduces the duty cycle of the converter. Approximately 1 mA should be the maximum current needed to reduce the duty cycle to zero. The difference between the 5 mA drive and the 1 mA requirement leaves ample margin for variations in the optocoupler gain.

Secondary Side Considerations

For the lowest cost, a current-mode flyback converter topology is used. Only a single diode is needed for rectification (MURD320 in Figure 23), and no filter inductor is required. The diode also prevents the battery from back driving the charger when input power is disconnected. A 1 mF capacitor filters the transformer current, providing an average dc current to charge the battery. The resistor, R_{CS}, senses the average current which is controlled via the V_{CS} input. In this case, the charging current has high ripple due to the flyback architecture, so a low-pass filter (R3 and C_{C2}) on the current sense signal is needed. This filter has an extra inverted zero due to R_{C2} to improve the phase margin of the loop. The 1 mF capacitor is connected between V_{OUT} and the 0.25 Ω sense resistor. To provide additional decoupling to ground, a 220 μF capacitor is also connected to V_{OUT}. Output ripple voltage is not critical, so the output capacitor was selected for lowest cost instead of lowest ripple. Most of the ripple current is shunted by the parallel battery, if connected. If needed, high frequency ringing caused by circuit parasitics can be damped with a small RC snubber across the rectifier.

The V_{CC} source to the ADP3810/ADP3811 can come from a direct connection to the battery as long as the battery voltage remains below the specified 16 V operating range. If the battery voltage is less then 2.7 V (e.g., with a shorted battery, or a battery discharged below it's minimum voltage), the ADP3810/ADP3811 will be in Undervoltage Lock Out (UVLO) and will not drive the optocoupler. In this condition, the primary PWM circuit will run at its designed current limit. The V_{CC} of the ADP3810/ADP3811 can be boosted using the circuit shown in Figure 23. This circuit keeps V_{CC} above 2.7 V as long as the

battery voltage is at least 1.5 V with a programmed charge current of 0.1 A. For a higher programmed charge current, the battery voltage can drop below 1.5 V, and V_{CC} is still maintained above 2.7 V. This is because of the additional energy in the flyback transformer, which transfers more energy through the 10 nF capacitor to V_{CC}. The 22 μF bypass capacitor on V_{CC} stores the energy transferred through the 10 nF capacitor.

Secondary Side Component Calculations

Design Criteria:

Charging a 6 cell NiCad battery.

Max Individual Cell Voltage:	$V_{CELLMAX}$ = 1.67 V
Max Battery Stack Voltage:	$V_{OMAX} = 6 \times 1.67$ V = 10 V
Max Charge Current:	I_{OMAX} = 1 A
Max Control Voltage:	V_{CTRL} = 1 V (for I_{OMAX} = 1 A)
R_S Fixed Value:	R_S = 20 kΩ
Pick a Value for R1:	R1 = 80.6 kΩ

The voltage limit of 10 V is approximately 10% above the maximum fully charged voltage when –ΔV/Δt termination is used. This limit gives a second level of protection without interfering with –ΔV/Δt charge termination.

Component Value Calculations:

Current Sense Resistor:	$R_{CS} = V_{CTRL}/(4 \times I_{OMAX}) = 1/(4 \times 1)$ = 0.25 W, 1%, 0.5 W
Battery Divider, R2:	$R2 = V_{REF} \times R1/(V_{OMAX}–V_{REF})$ R2 = 2 × 80.6 kΩ/(10 V–2 V) = 20.15 kΩ, Pick 20.0 kΩ

The final voltage and charge current accuracy is dependent upon the resistor tolerances. Choose appropriate tolerances for the desired accuracy. One percent accuracy is recommended.

Charger Performance Summary

The charger circuit properly executes the charging algorithm exhibiting stable operation regardless of battery conditions, including an open circuit load. The circuit can charge to other battery voltages by modifying only the battery voltage sense divider. As would be expected, circuit efficiency is best at high battery voltages. Replacing the output blocking rectifier diode with a Schottky would improve efficiency if the Schottky's leakage could be tolerated, and its reverse voltage rating met the application requirement.

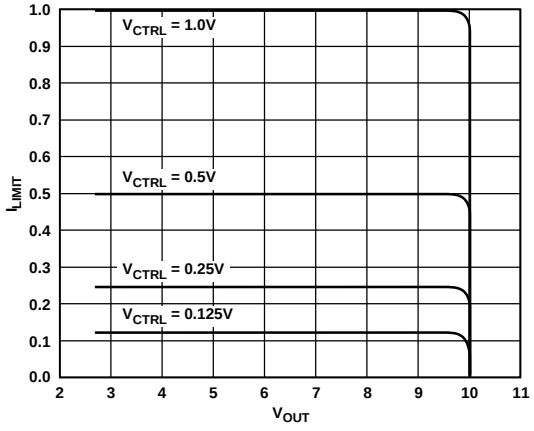


Figure 24. Charge Current vs. Battery Voltage at Four Settings for the Flyback Charger in Figure 23

The Battery Charge Current vs. Battery Voltage characteristics for four different charge current settings are given in Figure 24. The high gain of the internal amplifiers ensures the sharp transition between current mode and voltage mode regardless of the charge current setting. The fact that the current remains at full charging until the battery is very close to its final voltage ensures fast charging times.

The transient performance for various turn-on and turn-off conditions is detailed in Figures 25, 26 and 27. Figure 25 shows the output voltage when power is applied with no battery connected. As shown, the output voltage quickly rises and overshoots its set voltage. The internal comparator responds to this and clamps the voltage giving a quick recovery. Without the internal comparator, an external zener would be required to clamp the voltage to the LED anode. Figure 26 shows the battery current when connecting and disconnecting a battery. The actual trace shown is the voltage across R_{CS}, which is negative for current flowing into the battery. There is an overshoot when the battery is connected, but the loop quickly takes control and limits the average current to the programmed 0.75 A. When the battery is removed, the current quickly returns to zero. The solid band on the scope is due to the current rising and falling with the switching of the PWM. The time scale is too slow to show the detail of this. Figure 27 shows the output voltage when a battery stack charged to 6 V is connected and then disconnected. As expected, when the battery is connected, the voltage immediately goes to 6 V. When the battery is disconnected, the voltage returns to the programmed float voltage of 10 V. Again, a small overshoot is present that is clamped by the internal comparator.

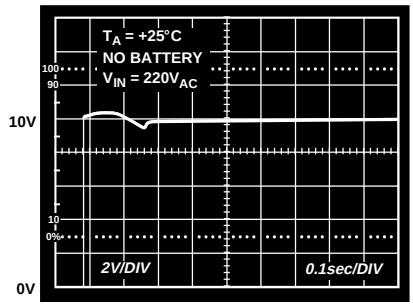


Figure 25. Flyback Charger Output Voltage Transient at Power Turn On, No Battery Attached

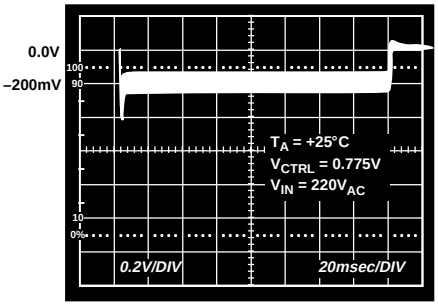


Figure 26. Charge Current Transient Response to Battery Connect/Disconnect

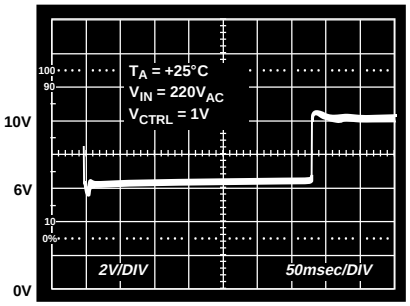


Figure 27. Output Voltage Transient Response to Battery Connect/Disconnect

NONISOLATED TOPOLOGIES

Buck Switching Regulators

The ADP3810/ADP3811 and the ADP1148 can be combined to create a high efficiency buck regulator battery charger as shown in Figure 28. The ADP1148 is a high efficiency, synchronous, step-down regulator that controls two external MOSFETs as shown. Similar to the previous flyback circuit, the ADP3810 controls the average charge current and the final battery voltage, and the ADP1148 controls the cycle by cycle current. The following discussion explains the functionality of the circuit but does not go into detail on the ADP1148. For more information, the ADP1148 data sheet details the operation of the device and gives formulas for choosing the external components.

The resistor R_{SENSE} sets the cycle by cycle current limit to 1.5 A, which is far enough above the 1 A average current of the ADP3810 loop to avoid interfering but still provides a safe maximum current to protect the external components. The ADP3810 uses a 0.25 Ω resistor, R_{CS}, to sense the battery current. As before, a 20 kΩ resistor is needed between R_{CS} and the V_{CS} input of the ADP3810. The RC network from V_{CS} to ground performs the dual function of filtering and compensation.

The voltage loop directly senses the battery voltage. Since the ADP3810 is used in this circuit instead of the ADP3811, V_{SENSE} is connected directly to the battery. The internal resistors set the battery voltage to 8.4 V in this case. Of course, other voltage options could be used, or the ADP3811 could be substituted with external resistors for a user set voltage. Notice the two grounds in the circuit. One ground is for the high current return to the V_{IN} source and the other ground for the ADP3810 circuitry. R_{CS} separates the two grounds, and it is important to keep them separate as shown.

The adjustable version of the ADP1148 is used in this circuit instead of a fixed output version. The output voltage is fed back into the V_{FB} pin, which is set to regulate at $V_{BAT\ MAX}$ + 0.5 V. Doing so provides a secondary, higher voltage limit without interfering with normal circuit operation. The control output of the ADP3810 is connected through a 560 Ω resistor to the SENSE+ input of the ADP1148. The current, I_{OUT}, adjusts the dc level on the SENSE+ pin, which is added to the current ramp across R_{SENSE}. Higher I_{OUT} increases the voltage on SENSE+ and reduces the duty cycle of the 1148, giving negative feedback.

The circuit as shown can quickly and safely charge LiIon batteries while maintaining high efficiency. The efficiency of the ADP1148 is only degraded slightly by the addition of the ADP3810 and external circuitry. The 1.5 mA of supply current lowers the overall efficiency by approximately 1%–2% for maximum output current. The 0.25 Ω sense resistor further lowers the efficiency due to the $I^2 \times R_{CS}$ power loss at high output currents. See the efficiency discussion in the ADP1148 data sheet for more information.

Linear Regulator

A third charging circuit is shown in Figure 29. In this case, the switching supply is replaced with a linear regulator. The ADP3811 drives the gate of an N-channel MOSFET using an external 2N3904. As before, the ADP3811 senses the charge current through a 0.25 Ω resistor. When the current increases above the limit, the internal GM amplifier causes the output to go high. This puts more voltage across R8, increasing the current in Q1. As the current increases, the gate of M1 is pulled lower, reducing the gate to source voltage and decreasing the charge current to complete the feedback loop. Because the ADP3811 has a current output, an external 1 kΩ resistor is needed from the OUT pin to ground in order to convert the current to a voltage.

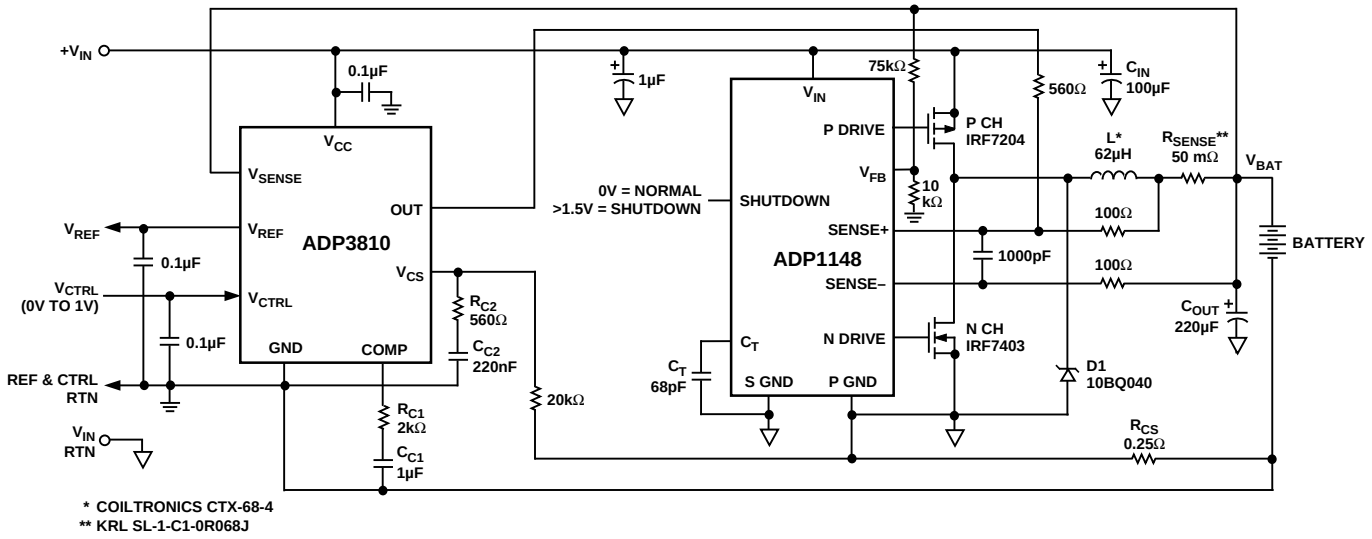


Figure 28. High Efficiency Buck Battery Charger

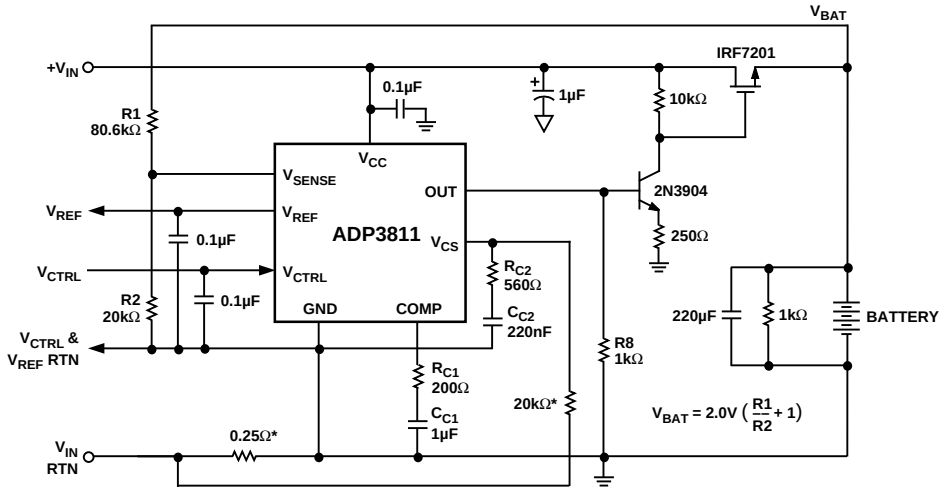
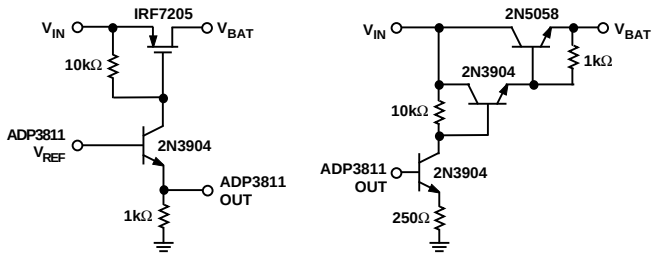


Figure 29. ADP3811 Controlling a Linear Battery Charger

The trade-off between using a linear regulator as shown versus using a flyback or buck type of charger is efficiency versus simplicity. The linear charger in Figure 29 is very simple, and it uses a minimal amount of external components. However, the efficiency is poor, especially when there is a large delta between the input output voltages. The power loss in the pass transistor is equal to $(V_{IN}–V_{BAT}) \times I_{CHARGE}$. Since the circuit is powered from a wall adapter, efficiency may not be a big concern, but the heat dissipated in the pass transistor could be excessive.

An important specification for this circuit is the dropout voltage, which is the difference between the input and output voltage at full charge current. There must be enough voltage to keep the N-channel MOSFET on. In this case, the dropout voltage is approximately 2.2 V for a 0.5 A output current. Two alternative



a. P-Channel MOSFET *b. NPN Darlington*

Figure 30. Alternative Pass Transistor for Linear Regulator

realizations of the pass element are shown in Figure 30. In case (a), the pass transistor is a P-channel MOSFET. This provides a lower dropout voltage so that V_{BAT} can be within a few hundred millivolts of V_{IN}. In case (b), a Darlington configuration of two npn transistors is used. The dropout voltage of this circuit is approximately 2 V for a 0.5 A charge current.

STABILIZATION OF FEEDBACK LOOPS

The ADP3810/ADP3811 uses two transconductance error amplifiers with "merged" output stages to create a shared compensation point (COMP) for both the current and voltage loops as explained previously. Since the voltage and current loops have significantly different natural crossover frequencies in a battery charger application, the two loops need different inverted zero feedback loop compensations that can be accomplished by two series RC networks. One provides the needed low frequency (typical f_C < 100 Hz) compensation to the voltage loop, and the other provides a separate high frequency (f_C ~ 1 kHz–10 kHz) compensation to the current loop. In addition, the current loop input requires a ripple reduction filter on the V_{CS} pin to filter out switching noise. Instead of placing both RC networks on the COMP pin, the current loop network is placed between V_{CS} and ground as shown in Figure 23 (C_{C2} and R_{C2}). Thus, it performs two functions, ripple reduction and loop compensation.

Loop Stability Criteria for Battery Charger Applications

1. The voltage loop has to be stable when the battery is removed or floating.
2. The current loop has to be stable when the battery is being charged within its specified charge current range.
3. Both loops have to be stable within the specified input source voltage range.

Flyback Charger Compensation

Figure 31 shows a simplified form of a battery charger system based on the off-line flyback converter presented in Figure 23. With some modifications (no optocoupler, for example), this model can also be used for converters such as a Buck Converter (Figure 28) or a Linear Regulator (Figure 29). GM1 and GM2 are the internal GM amplifiers of the ADP3810/ADP3811, and GM3 is the buffered output stage that drives the optocoupler. The primary side in Figure 23 is represented here by the "Power Stage," which is modeled as GM4, a linear voltage controlled current source model of the flyback transformer and switch. The "Voltage Error Amplifier" block is the internal error amplifier of the 3845 PWM-IC (R_F = 3.3 kΩ in Figure 23), and it is followed by an internal resistor divider. The optocoupler is modeled as a current controlled current source as shown. Its output current develops a voltage, V_X, across R_F. The gain values of all the blocks are defined below.

This linear model makes the calculation of compensation values a manageable task. It also has the great benefit of allowing the simulation of the ac response using a circuit simulator, such as PSpice or MicroCap. For computer modeling, the GM

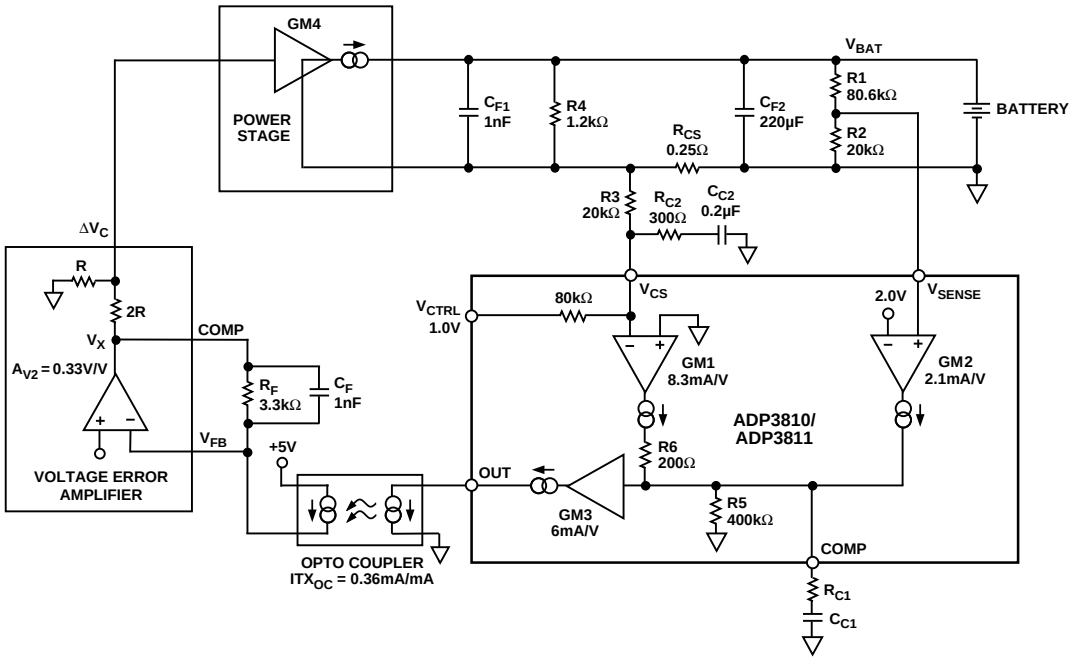


Figure 31. Block Diagram of the Linearized Feedback Model

amplifiers are represented by voltage controlled current sources, the optocoupler by a current controlled current source, and the error amplifier by a voltage controlled voltage source.

Design Criteria

Charging a 6 cell NiCad battery.

Max Battery Stack Voltage: $V_{OMAX} = 6 \times 1.67\ V = 10\ V$

Max Charge Current: $I_{OMAX} = 1\ A$

R_S Fixed Value: $R_S = 20\ k\Omega$

Pick a value for R1: $R1 = 80.6\ k\Omega$

Calculated Current Sense Resistor: $R_{CS} = 0.25\ \Omega$

Calculated Voltage Sense Divider: $R2 = 20\ k\Omega$

Output Filter Cap: $C_{F1} = 1\ mF$ (ESR = 0.1 Ω)

2nd Filter Cap: $C_{F2} = 200\ \mu F$ (ESR = 0.2 Ω)

Gain of Each Block

ADP3810/ADP3811 V_{CS} Input: GM1 = 8.3 mA/V

ADP3810/ADP3811 V_{SENSE} Input: GM2 = 2.1 mA/V

ADP3810/ADP3811 Output Buffer: GM3 = 6 mA/V

Optocoupler: $ITX_{oc} = 0.36\ mA/mA$

Voltage Error Amplifier: $A_{V2} = \Delta V_C/V_X = 0.333$

Power Stage (General): $GM4 = \left(\frac{\Delta I_{OMAX}}{\Delta V_C}\right)\sqrt{\frac{V_{OMAX}}{I_{OMAX} \times R_{LOAD}}}$

Power Stage (Voltage Loop): GM4 = 0.091 A/V

Power Stage (Current Loop): GM4 = 1.0 A/V

The gains for the ADP3810/ADP3811 GM amplifiers are based on typical measurements of the IC's open-loop gain, and they are expressed in units of milliamps per volt. The dc voltage gain of these stages is the value of GM times the load resistance. At the COMP pin, the internal load resistance, R5, is typically 400 kΩ. The optocoupler gain is the typical value taken from the MOC8103 data sheet. The voltage error amplifier gain is due to the resistor divider internal to the 3845 only. V_X is the output of the internal amplifier, as labeled in Figure 31. The actual op amp is assumed to have sufficient open-loop gain and bandwidth compared to the system bandwidth; as a result, it can be considered an ideal transimpedance amplifier. The pole created by the 1 nF capacitor in parallel with R_F is high enough in frequency to not affect the compensation.

The power stage gain equation is linearized based on primary side current mode control with the flyback transformer operating with discontinuous inductor current. ΔI_{OMAX} is the maximum change in output current, which is equal to I_{OMAX}–I_{OMIN}. Since the minimum current is 0.0 A, $\Delta I_{OMAX} = I_{OMAX} = 1\ A$. The maximum change in control voltage is set by internal circuitry within the 3845 to $\Delta V_C = 1\ V$. The load resistor, R_{LOAD}, is different for the voltage and current loop cases. For the voltage loop without the battery, the effective load is R4, but for the current loop, the effective load is R_{CS}. In the current loop, the voltage limit has not been reached, so the maximum output voltage is equal to the maximum output current times the load resistor. Thus, the entire expression under the square root reduces to 1.0. Substituting these values into the general equation for the power stage yields the specific gain values shown for GM4.

When calculating the loop gain for the voltage loop and the current loop, there are two main differences. First, GM2 applies only to the voltage loop, and GM1 applies only to the current loop. Use the appropriate GM input stage for the particular loop calculations. Second, there are three battery conditions to consider. For the current loop, the battery is present and uncharged. Thus, the battery is modeled as a very large capacitance (greater than 1 Farad). For the voltage loop, the battery is

either present or absent. If the battery is present, its large capacitance creates a very low frequency dominant pole, giving a single pole system. The more demanding case is when the battery is removed. Now the output pole is dependent upon the filter capacitors, C_{F1} and C_{F2}. This pole is higher in frequency, and more care must be taken to stabilize the loop response. All three cases are described in detail below.

The following calculations for compensation components help to realize stable voltage and current loops. In practical designs, checking the stability using a network analyzer or a Feedback Loop Analyzer is always recommended. The calculated component values serve as good starting values for a measurement-based optimization. The component values shown in Figure 23 are slightly different from the calculated values based on this optimization procedure.

To simplify the analysis further, the loop gain is split into two components: the gain from the battery to the ADP3810/ADP3811's COMP pin and the gain from the COMP pin back to the battery. Because the compensation of each loop depends upon the RC network on the COMP pin, it is a convenient choice for dividing the loop calculations.

Definitions:

Modulator Gain: G_{MOD} = gain in dB from the COMP pin to V_{BAT}.
Error Amplifier: G_{EA} = gain in dB from V_{BAT} to the COMP pin.
Loop Gain: $G_{LOOP} = G_{MOD} + G_{EA}$.
Modulator Pole: f_{PM}, The pole present at the output of the modulator.
Modulator Zero: f_{ZM}, The zero due to the ESR, R_{F1}, of the filter cap, C_{F1}.

Voltage Loop Compensation, No Battery

Step 1. Calculate the dc loop gain (G_{LOOP}), f_{PM}, and f_{ZM}:

$$G_{MOD} = 20 \times \log\left[GM3 \times ITX_{OC} \times R_F \times A_{V2} \times GM4 \times R4\right]$$

$$G_{MOD} = 20 \times \log\left[\begin{array}{l} 6\ mA/V \times 0.36 \times 3.3\ k\Omega \times \\ 0.333 \times 0.091\ A/V \times 1.2\ k\Omega \end{array}\right] = 48.3\ dB$$

$$G_{EA} = 20 \times \log\left[\frac{R2}{R1+R2} \times GM2 \times R5\right]$$

$$G_{EA} = 20 \times \log\left[\frac{20\ k\Omega}{80\ k\Omega + 20\ k\Omega} \times 2.1\ mA/V \times 400\ k\Omega\right] = 48.5\ dB$$

$$G_{LOOP} = 44.5\ dB + 48.3\ dB = 96.8\ dB$$

$$f_{PM} = \frac{1}{2\pi \times R4 \times \left(C_{F1} + C_{F2}\right)} = \frac{1}{2\pi \times 1.2\ k\Omega \times \left(1.22\ mF\right)} = 0.11\ Hz$$

$$f_{ZM} = \frac{1}{2\pi \times R_{F1} \times C_{F1}} = \frac{1}{2\pi \times 0.1\ \Omega \times 1.0\ mF} = 1.6\ kHz$$

In reality, the interaction of C_{F1} and C_{F2} and their ESRs create an additional pole/zero pair, but because the value of R_{F1} (ESR of C_{F1}) and R_{F2} (ESR of C_{F2}) are similar, they tend to cancel each other out. Furthermore, the loop crossover is an order of magnitude lower in frequency, so the additional pole and zero have little effect on the loop response.

Step 2. Pick the voltage and current loop crossover frequencies, f_{CV} and f_{CI}:

To avoid interference between the voltage loop and the current loop, use f_{CV} < 1/10 of f_{CI}, the current loop crossover. The current loop crossover f_{CI} is chosen to be ~ 1.9 kHz to provide a fast current limiting response time, so pick f_{CV} ~ 100 Hz.

Step 3. Calculate G_{MOD} at f_{CV}:

The modulator gain of 46.7 dB is the dc gain. The modulator pole reduces this gain above f_{PM}.

$$G_{MOD}(100\ Hz) = G_{MOD}(dc) - 20 \times \log\sqrt{1 + \left(\frac{f_{CV}}{f_{PM}}\right)^2}$$

$$G_{MOD}(100\ Hz) = 48.3\ dB - 20 \times \log\sqrt{1 + \left(\frac{100}{0.11}\right)^2} = -10.9\ dB$$

Step 4. Calculate gain loss of G_{EA} at f_{CV}:

To have the feedback loop gain cross over 0 dB at f_{CV} = 100 Hz, G_{EA} (100 Hz) should be +10.9 dB. Thus, the total gain loss of G_{EA} needed at crossover is:

$$G_{LOSS} = G_{EA}(dc) - G_{EA}(100\ Hz) = 48.5\ dB - 10.9\ dB = 37.6\ dB$$

Step 5. Determine f_P needed to achieve G_{LOSS}:

To achieve this G_{LOSS} we need to add a pole, which is located at the COMP pin. GM2 has practically no parasitic loss in gain at 100 Hz. Its first parasitic pole occurs at approximately 500 kHz as shown in Figure 11. Thus, the entire gain loss must be realized with an external compensation capacitor, C_{C1}, that sets the pole, f_{P1}.

$$f_{P1} = \frac{f_{CV}}{\sqrt{10^{\left(\frac{G_{LOSS}}{10}\right)} - 1}} = 1.3\ Hz$$

Step 6. Calculate C_{CI} based upon f_P:

$$C_{C1} = \frac{1}{2\pi \times R5 \times f_{P1}} \approx 0.3\ \mu F$$

Step 7. Calculate the loop phase margin, Φ_M:

The loop phase margin is a combination of the phase of the modulator pole and zero and the error amplifier pole.

$$\Phi_M = 180 - arc\tan\left(\frac{f_{CV}}{f_{P1}}\right) - arc\tan\left(\frac{f_{CV}}{f_{PM}}\right) + arc\tan\left(\frac{f_{CV}}{f_{ZM}}\right) \approx 0°$$

Step 8. Calculate R_{CI} to stabilize the loop:

The sum of phase losses of the modulator and error amplifier results in a loop phase of 0°, which is unacceptable for loop stability. To stabilize the feedback loop, we have to add a phase boosting zero to the error amplifier by inserting a resistor (R_{C1}) in series with the capacitor C_{C1}. If the desired phase margin is ϕ_M = 60 degrees, the frequency of the zero can be calculated:

$$f_{Z1} = f_{CV}/\tan\phi_M = 57\ Hz$$

From this, the R_{C1} resistor is calculated:

$$R_{C1} = \frac{1}{2\pi \times f_{Z1} \times C_{C1}} \approx 10\ k\Omega$$

Step 9. Iterate C_{CI}:
Because f_{Z1} is very close to f_{CV}, it will increase the error amplifier gain in a nonnegligible amount at the 0 dB point. The increase in gain is calculated as:

$$20\times\log\sqrt{1+\left(\frac{f_{Z1}}{f_{CV}}\right)^2}=7.1\,dB$$

Now, the total error amplifier gain loss required is:

$$G_{LOSS} = 37.6\ dB + 7.1\ dB = 44.7\ dB$$

With this, the new f_{P1} can be calculated from the equation in Step 5.

$$f_{P1} = 0.58\ Hz$$

Finally, C_{C1} is recalculated using the equation in Step 6.

$$C_{C1}=\frac{1}{2\pi\times 400\,k\Omega\times 0.58\ Hz}\approx 0.7\,\mu F$$

Following these steps gives a cookbook method for calculating the compensation components for the voltage loop. As mentioned above, these components can be optimized in the actual circuit. The results of a PSpice[1] analysis of the loop is shown in Figure 32. The open loop gain of the loop is 108 dB as calculated. The crossover frequency is 100 Hz with a phase margin of 52°. The graph shows the phase leveling off at 90°. In reality the phase will continue to fall as higher frequency parasitic poles take effect.

[1]PSpice is a trademark of MicroSim Corporation.

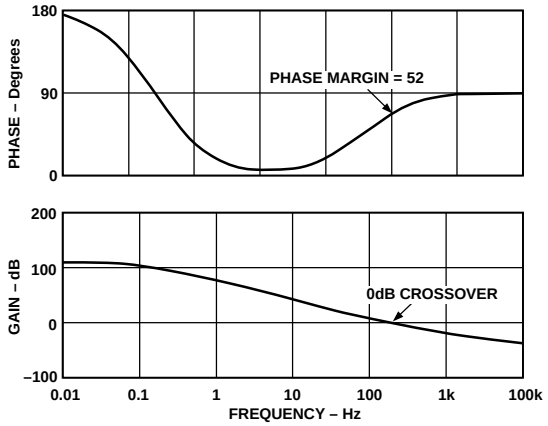


Figure 32. Voltage Loop Gain/Phase Plots

Voltage Loop Compensation, Battery Present
When the battery has finished charging and is still connected to the charging circuitry, the system is said to be "floating" the battery. The loop is maintaining a constant output voltage equal to the battery voltage, and the output current has dropped to nearly zero. This case is actually the easiest to compensate because the battery's capacitance creates a very low frequency dominant pole, giving a single pole response. For example, if the battery is modeled as a 10 Farad capacitor, the dominant pole will be $1/(2\pi\times 1.2\ k\Omega\times 10\ F) = 0.013$ MHz. This very low frequency pole causes the system to cross over 0 dB at less than 10 Hz, giving a stable single pole system. The compensation components have little effect on this response, so no further calculations are needed for this case.

Current Loop Compensation
Now that the voltage loop compensation is complete, it is time to add the compensation for the current loop. The definitions for modulator gain and error amplifier gain are the same as before; but now, the controlling error amplifier is GM1 in Figure 31, as opposed to GM2, for the voltage loop. Otherwise, the calculations are very similar.

Step 10. Calculate the dc loop gain (G_{LOOP}), f_{PM}, and f_{ZM}:

$$G_{MOD}=20\times\log\left[GM3\times ITX_{OC}\times R_F\times A_{V2}\times GM4\times R_{CS}\right]$$

$$G_{MOD}=20\times\log\left[\begin{matrix}6\,mA/V\times 0.36\times 3.3\,k\Omega\times\\ 0.333\times 1.0\ A/V\times 0.25\,\Omega\end{matrix}\right]=-4.5\,dB$$

$$G_{EA}=20\times\log\left[GM1\times R5\right]=20\log\left[8.3\,mA/V\times 400\,k\Omega\right]=70.4\,dB$$

$$G_{LOOP} = -6.1\ dB + 70.4\ dB = 64.3\ dB$$

$$f_{PM}=\frac{1}{2\pi\times\left(R_{CS}+R_{F1}\right)\times C_{F1}}=\frac{1}{2\pi\times 0.35\,\Omega\times 1\,mF}=450\ Hz$$

$$f_{ZM}=\frac{1}{2\pi\times R_{F1}\times C_{F1}}=\frac{1}{2\pi\times 0.1\,\Omega\times 1\,mF}=1.6\,kHz$$

Step 11. Pick the current loop crossover frequency, f_{CI}:
From Step 2 in the voltage loop calculations, f_{CI} ~ 1.9 kHz.

Step 12. Calculate G_{MOD} at f_{CI}:
The modulator gain of –4.5 dB is the dc gain. The modulator pole reduces this gain above f_{PM}.

$$G_{MOD}\left(1.9\,kHz\right)=G_{MOD}\left(dc\right)-20\times\log\sqrt{1+\left(\frac{f_{CI}}{f_{PM}}\right)^2}+20\times\log\sqrt{1+\left(\frac{f_{CI}}{f_{ZM}}\right)^2}$$

$$G_{MOD}\left(1.9\,kHz\right)=-4.5\,dB-12.7\,dB+3.8\,dB=-13.4\,dB$$

If the 1 mF capacitor has a much higher ESR, e.g., 1 Ω, the modulator zero, f_{ZM}, will be lower in frequency than the modulator pole, f_{PM}. This causes the loop gain and bandwidth to increase and could cause instability. One possible solution to this scenario is to use a much higher value (47 nF) for the C_F = 1 nF capacitor. The pole of this capacitor would then be in the 1 kHz range and would reduce the loop gain. If the ESR is much less than 0.1 Ω, the bandwidth of the loop will decrease slightly.

Step 13. Calculate gain loss of G_{EA} at f_{CI}:
The gain loss of G_{EA} in the current loop is a combination of the loss due to C_{C1}, R_{C1} and the additional loss from C_{C2}, R_{C2}. To calculate the contribution of gain roll-off needed from C_{C2}, R_{C2}, the effective gain of G_{EA} must first be calculated. Since the gain is calculated at 1.9 kHz, the impedance of C_{C1} is 120 Ω. Thus, the gain becomes:

$$G_{EA}\left(1.9\,kHz\right)=20\times\log\left[GM1\times\left(R6+R_{C1}+120\,\Omega\right)\right]$$

$$G_{EA}\left(1.9\,kHz\right)=20\times\log\left[8.3\,mA/V\times\left(10320\,\Omega\right)\right]=38.9\,dB$$

$$G_{LOSS} = G_{EA}(1.9\ kHz) - G_{MOD}(1.9\ kHz)$$
$$= 38.9\ dB - 13.4\ dB = 25.5\ dB$$

Step 14. Calculate value of R_{C2} to realize G_{LOSS}:
Assuming that C_{C2} is a short, R_{C2} forms a resistor divider with R3, reducing the loop gain. To calculate R_{C2}, simply set the resistor ratio to give an attenuation of 25.5 dB, which is a loss of 1/20.

$$R_{C2} = \frac{R3}{20-1} = 1\,k\Omega$$

To provide some margin in the circuit for gain fluctuations in the various stages, the final value of R_{C2} was adjusted down to 300 Ω.

Step 15. Calculate the value of C_{C2}:
To maintain high dc gain, a capacitor, C_{C2}, is connected in series with R_{C2}. The zero provided by this RC network should be close to f_{CI} to provide a phase boost at crossover:

$$f_{Z2} \approx 1.9\,kHz$$

$$C_{C2} = \frac{1}{2\pi \times f_{Z2} \times R_{C2}} = \frac{1}{2\pi \times 1.9\,kHz \times 300\,\Omega} \approx 200\,nF$$

The pole frequency due to C_{C2} and R3 can now be calculated as:

$$f_{P2} = \frac{1}{2\pi \times C_{C2} \times R3} = 40\,Hz$$

Step 16. Check the current loop phase margin:

$$\Phi_M = 180 - arc\tan\left(\frac{f_{CI}}{f_{P2}}\right) + arc\tan\left(\frac{f_{CI}}{f_{Z2}}\right) - arc\tan\left(\frac{f_{CI}}{f_{PM}}\right) + arc\tan\left(\frac{f_{CI}}{f_{ZM}}\right) + arc\tan\left(\frac{f_{CI}}{f_{P1}}\right) + arc\tan\left(\frac{f_{CI}}{f_{Z3}}\right)$$

$$\Phi_M \approx 115°$$

The above formula subtracts the phase of each pole and adds the phase of each zero. The poles and zeros come in pairs, f_{P2}/f_{Z2} calculated in Step 15 from C_{C2}/R_{C2}; f_{PM}/f_{ZM} calculated in Step 10 due to the output filter cap; and f_{P1}/f_{Z3} due to C_{C1}/R_{C1}. f_{P1} is the same pole that was calculated in Step 9, and f_{Z3} needs to be recalculated with the addition of the internal 200 Ω resistor as follows:

$$f_{Z3} = \frac{1}{2\pi \times C_{C1} \times (R_{C1} + R6)} = 78\,Hz$$

The final phase margin of 115° is more than adequate for a stable current loop. In reality, higher order parasitic poles reduce the phase margin to significantly less than 115° for a 1.9 kHz crossover. The same was not the case for the voltage loop because the cross over frequency of 100 Hz was well below the parasitic poles.

A PSpice analysis of the resulting loop gain and phase for the values calculated is shown in Figure 33.

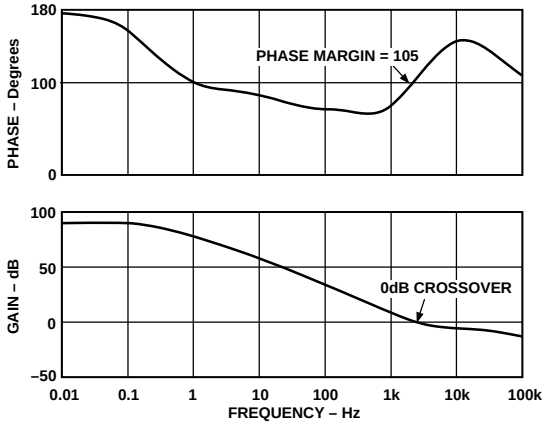


Figure 33. Current Loop Gain/Phase Plots

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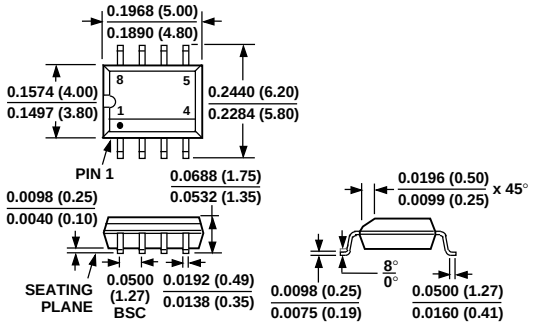
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Small Outline IC (SO-8)



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