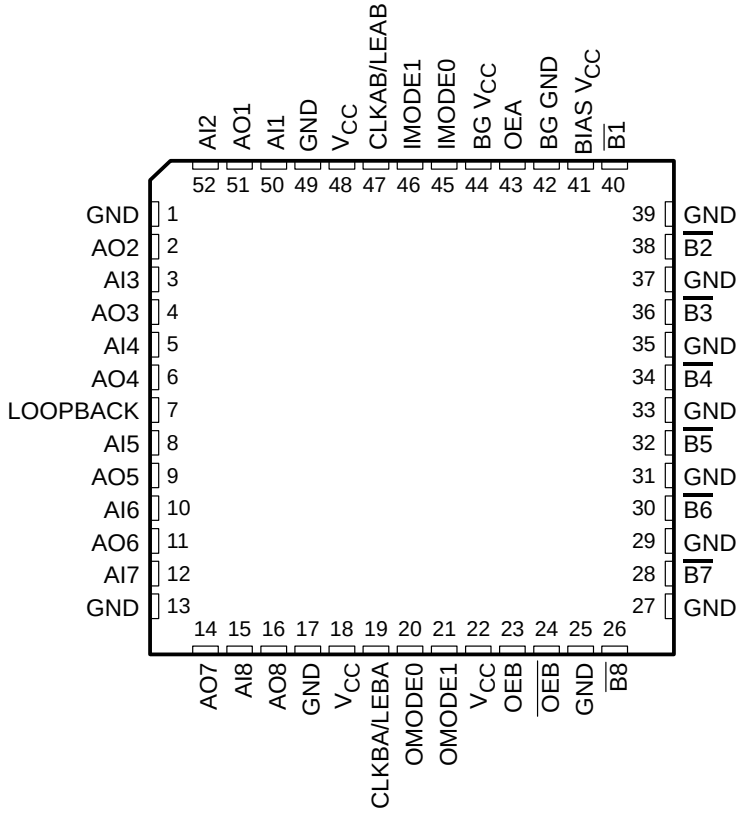
- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **High-Impedance State During Power Up and Power Down**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**

RC PACKAGE
(TOP VIEW)



description

The SN74FB2033A is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level A port. The common-I/O, open-collector $\overline{B}$ port operates at backplane transceiver logic (BTL) signal levels.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock inputs serve as active-high transparent latch enables.

description (continued)

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, $\overline{B}$-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.

The AO port-enable/-disable control is provided by OEA. When OEA is low or when V_{CC} is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The $\overline{B}$ port is controlled by OEB and $\overline{OEB}$. If OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.5 V, the $\overline{B}$ port is inactive. If OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active.

BG V_{CC} and BG GND are the bias-generator reference inputs.

The A-to-B and B-to-A logic elements are active, regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive ($\overline{B}$ port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on V_{OH} during a low-to-high transition. The other clamps out ringing below the BTL V_{OL} voltage of 0.75 V. Both clamps are active only during ac switching and do not affect the BTL outputs during steady-state conditions.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFP – RC	Tube	SN74FB2033ARC	FB2033A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

FUNCTION/MODE

INPUTS								FUNCTION/MODE
OEA	OEB	$\overline{OEB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	
L	L	X	X	X	X	X	X	Isolation
L	X	H	X	X	X	X	X	
X	H	L	L	L	X	X	X	AI to $\overline{B}$, buffer mode
X	H	L	L	H	X	X	X	AI to $\overline{B}$, flip-flop mode
X	H	L	H	X	X	X	X	AI to $\overline{B}$, latch mode
H	L	X	X	X	L	L	L	$\overline{B}$ to AO, buffer mode
H	X	H	X	X	L	L	L	
H	L	X	X	X	L	H	L	$\overline{B}$ to AO, flip-flop mode
H	X	H	X	X	L	H	L	
H	L	X	X	X	H	X	L	$\overline{B}$ to AO, latch mode
H	X	H	X	X	H	X	L	
H	L	X	X	X	L	L	H	AI to AO, buffer mode
H	X	H	X	X	L	L	H	
H	L	X	X	X	L	H	H	AI to AO, flip-flop mode
H	X	H	X	X	L	H	H	
H	L	X	X	X	H	X	H	AI to AO, latch mode
H	X	H	X	X	H	X	H	
H	H	L	X	X	X	X	L	AI to $\overline{B}$, $\overline{B}$ to AO

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEA	OEB	$\overline{OEB}$	AO	$\overline{B}$
L	X	X	Hi Z	
H	X	X	Active	
X	L	L		Inactive (H)
X	L	H		Inactive (H)
X	H	L		Active
X	H	H		Inactive (H)

BUFFER

INPUT	OUTPUT
L	H
H	L

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	H
H	H	L
L	X	Q_0

Function Tables (Continued)

LOOPBACK

LOOPBACK	Q†
L	$\overline{B}$ port
H	Point P‡

† Q is the input to the B-to-A logic element.
‡ P is the output of the A-to-B logic element (see functional block diagram).

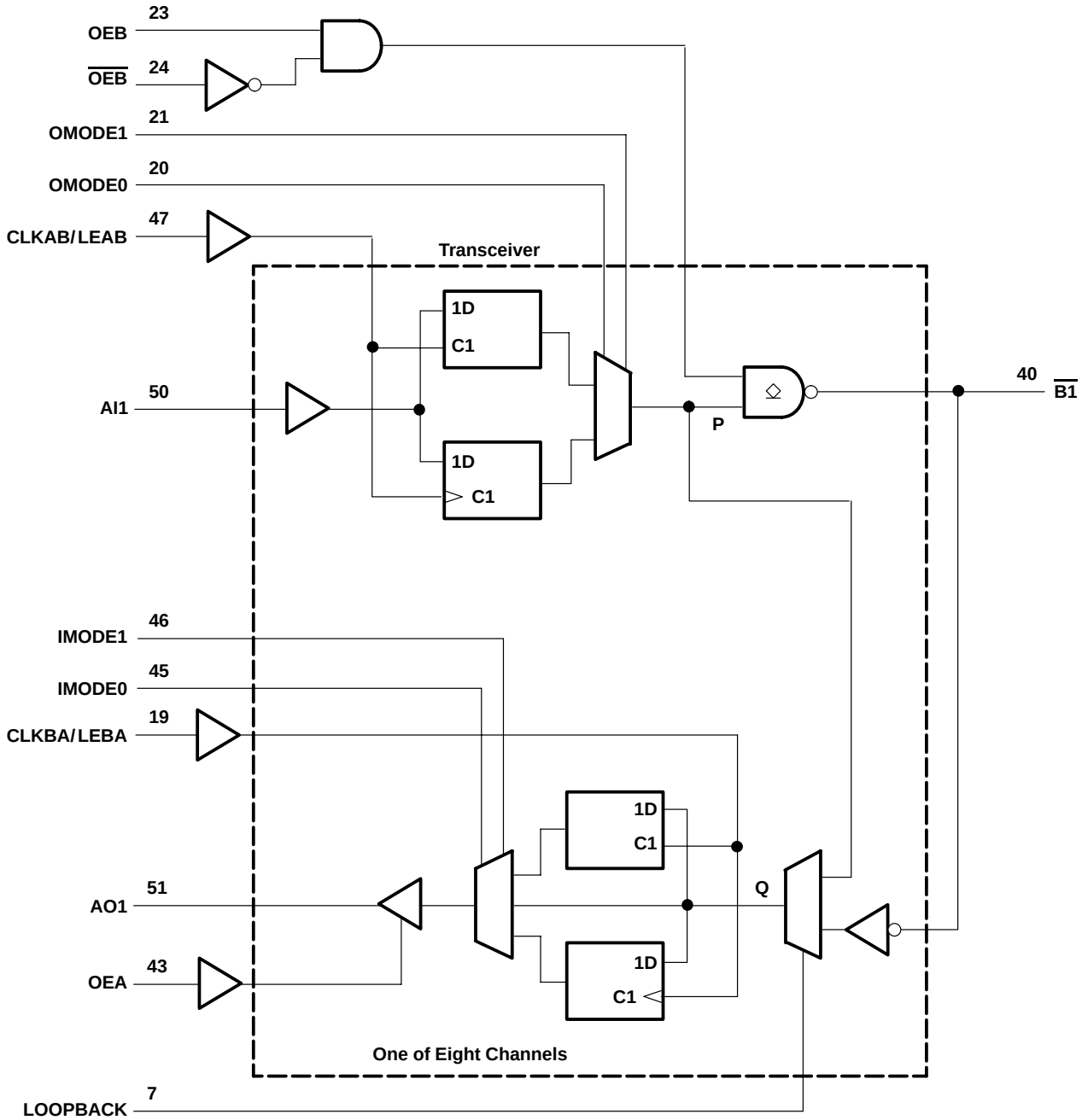
SELECT

INPUTS		SELECTED LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q_0
↑	L	H
↑	H	L

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current range, V_I: Except $\overline{B}$ port . . . . . –1.2 V to 7 V
$\overline{B}$ port . . . . . –1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, V_O . . . . . –0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O: A port . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . . –40 mA
$\overline{B}$ port . . . . . –18 mA
Current applied to any single output in the low state, I_O: A port . . . . . 48 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 44°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}, BG V_{CC}	Supply voltage		4.75	5	5.25	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{OH}	High-level output current	AO port			–3	mA
I_{OL}	Low-level output current	AO port			24	mA
		$\overline{B}$ port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Except $\overline{B}$ port			10	ns/V
T_A	Operating free-air temperature		0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC}(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}	AO port	V_{CC} = 4.75 V to 5.25 V,	I_{OH} = –10 µA			V_{CC}–1.1	V
		V_{CC} = 4.75 V	I_{OH} = –3 mA	2.5	2.85	3.4	
			I_{OH} = –32 mA	2			
V_{OL}	AO port	V_{CC} = 4.75 V	I_{OL} = 20 mA		0.33	0.5	V
			I_{OL} = 55 mA			0.8	
	$\overline{B}$ port	V_{CC} = 4.75 V	I_{OL} = 100 mA	0.75		1.1	
			I_{OL} = 4 mA	0.5			
I_I	Except $\overline{B}$ port	V_{CC} = 0,	V_I = 5.25 V			100	µA
I_{IH}	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 2.7 V			50	µA
	$\overline{B}$ port‡	V_{CC} = 0 to 5.25 V,	V_I = 2.1 V			100	
I_{IL}	Except $\overline{B}$ port	V_{CC} = 5.25 V	V_I = 0.5 V			–50	µA
	$\overline{B}$ port‡		V_I = 0.75 V			–100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.25 V,	V_O = 2.1 V			100	µA
I_{OZPU}		V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			50	µA
I_{OZPD}		V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			–50	µA
I_{OZH}	AO port	V_{CC} = 5.25 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC} = 5.25 V,	V_O = 0.5 V			–50	µA
I_{OS}§	AO port	V_{CC} = 5.25 V,	V_O = 0	–40	–80	–150	mA
I_{CC}	All outputs on	V_{CC} = 5.25 V,	I_O = 0		45	70	mA
C_i	AI port and control inputs	V_I = 0.5 V or 2.5 V			5		pF
C_o	AO port	V_O = 0.5 V or 2.5 V			5		pF
C_{io}	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC} = 0 to 4.75 V				6	pF
		V_{CC} = 4.75 V to 5.25 V				6	

† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion characteristics over recommended operating free-air temperature range (see Note 3)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		10	µA
		V_{CC} = 4.5 V to 5.5 V				10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V			100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100	

NOTE 3: The power-up sequence is GND, BIAS V_{CC}, V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency			150		150	MHz
t_w	Pulse duration	CLKAB/LEAB or CLKBA/LEBA	3.3		3.3		ns
t_{su}	Setup time	Data before CLKAB/LEAB or CLKBA/LEBA↑	2.7		2.7		ns
t_h	Hold time	Data after CLKAB/LEAB or CLKBA/LEBA↑	0.7		0.7		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	AI (through mode)	$\overline{B}$	2.3	3.6	4.6	2.3	5.6	ns
t_{PHL}			1.9	3	4.2	1.9	4.5	
t_{PLH}	$\overline{B}$ (through mode)	AO	2.5	4.2	5.5	2.5	6.1	ns
t_{PHL}			3	4.2	5.6	3	5.7	
t_{PLH}	AI (transparent)	$\overline{B}$	2.3	3.6	4.6	2.3	5.6	ns
t_{PHL}			1.9	3	4.1	1.9	4.5	
t_{PLH}	$\overline{B}$ (transparent)	AO	2.5	4.2	5.5	2.5	6.1	ns
t_{PHL}			3	4.2	5.6	3	5.7	
t_{PLH}	OEB	$\overline{B}$	2.4	3.7	4.7	2.4	5.8	ns
t_{PHL}			1.8	3	4.1	1.8	4.4	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	2	3.4	4.3	2	5.2	ns
t_{PHL}			2	3.3	4.4	2	4.8	
t_{PZH}	OEA	AO	2	3.5	4.6	2	5.1	ns
t_{PZL}			2.7	4.2	5.1	2.7	5.4	
t_{PHZ}	OEA	AO	2.1	4	5	2.1	5.5	ns
t_{PLZ}			1.6	2.8	3.9	1.6	4.3	
t_{PLH}	CLKAB/LEAB	$\overline{B}$	3	4.7	5.8	3	6.9	ns
t_{PHL}			2.8	4.3	5.6	2.8	6.1	
t_{PLH}	CLKBA/LEBA	AO	2	3.6	4.9	2	5.4	ns
t_{PHL}			2.2	3.5	4.7	2.2	5.1	
t_{PLH}	OMODE	$\overline{B}$	2.4	5	6.1	2.4	7.2	ns
t_{PHL}			2.4	4.5	6	2.4	6.7	
t_{PLH}	IMODE	AO	1.8	4	5.3	1.8	5.9	ns
t_{PHL}			2.3	4.1	5.2	2.3	5.4	
t_{PLH}	LOOPBACK	AO	2.4	5	7	2.4	8	ns
t_{PHL}			3.1	4.6	5.7	3.1	5.9	
t_{PLH}	AI	AO	1.9	3.7	5.5	1.9	6.1	ns
t_{PHL}			2.6	4.2	5.6	2.6	5.8	
t_r	Rise time,1.3 V to 1.8 V, $\overline{B}$ port		0.5	1.2	2.1	0.5	3	ns
t_f	Fall time, 1.8 V to 1.3 V, $\overline{B}$ port		0.5	1.4	2.3	0.5	3	
t_r	Rise time, 10% to 90%, AO		2	3.3	4.2	2	5	ns
t_f	Fall time, 90% to 10%, AO		1	2.5	3.4	1	5	
$\overline{B}$-port input pulse rejection						1		ns

output-voltage characteristics

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OHP}	Peak output voltage during turnoff of 100 mA into 40 nH	$\overline{B}$ port	See Figure 1		4.5	V
V_{OHV}	Minimum output voltage during turnoff of 100 mA into 40 nH	$\overline{B}$ port	See Figure 1	1.62		V
V_{OLV}	Minimum output voltage during high-to-low switch	$\overline{B}$ port	I_{OL} = –50 mA	0.3		V

PARAMETER MEASUREMENT INFORMATION

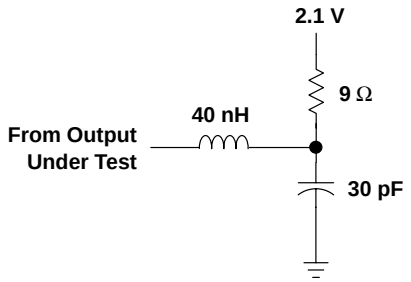
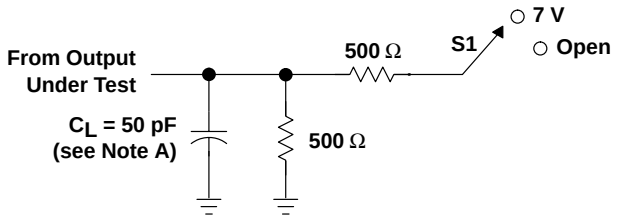
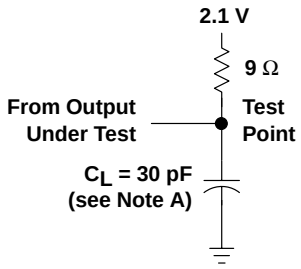


Figure 1. Load Circuit for V_{OHP} and V_{OHV}

PARAMETER MEASUREMENT INFORMATION

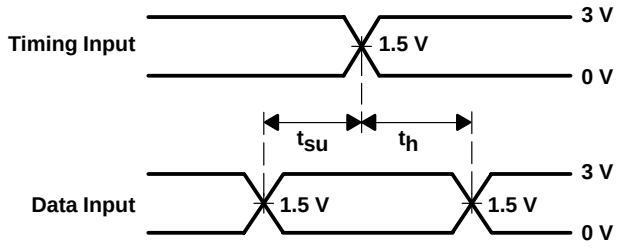


LOAD CIRCUIT FOR A OUTPUTS

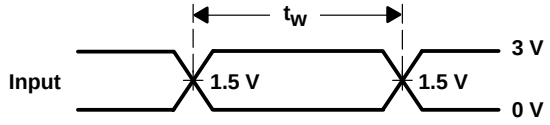


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

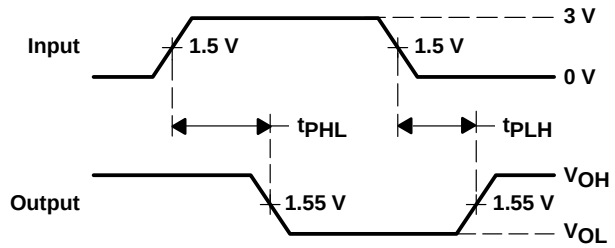
LOAD CIRCUIT FOR B OUTPUTS



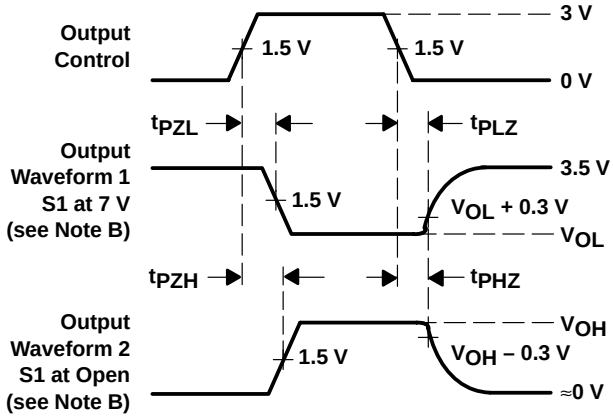
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



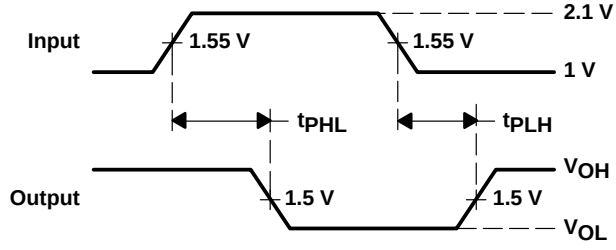
VOLTAGE WAVEFORMS
PULSE DURATION



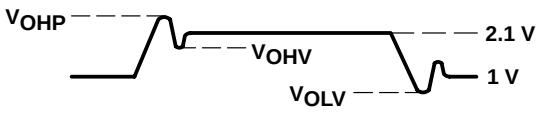
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns; BTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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