

Octal D-type transparent latch with 5-volt tolerant inputs/outputs; 3-state

74LVC573A
74LVCH573A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic.
- Wide supply voltage range of 2.7 V to 3.6 V.
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages upto 5.5 V
- CMOS low power consumption
- Direct Interface with TTL levels
- Flow-through pin-out architecture
- Bushold on all data inputs (LVCH573A only).

DESCRIPTION

The 74LVC(H)573A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment. The 74LVC(H)573A is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches. The '573' consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches. The '573' is functionally identical to the '373', but the '373' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n ; LE to Q_n	$C_L = 50\text{ pF}$ $V_{CC} = 3.3\text{ V}$	4.3 4.6	ns
C_i	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is $V_i = \text{GND to } V_{CC}$.

ORDERING INFORMATION

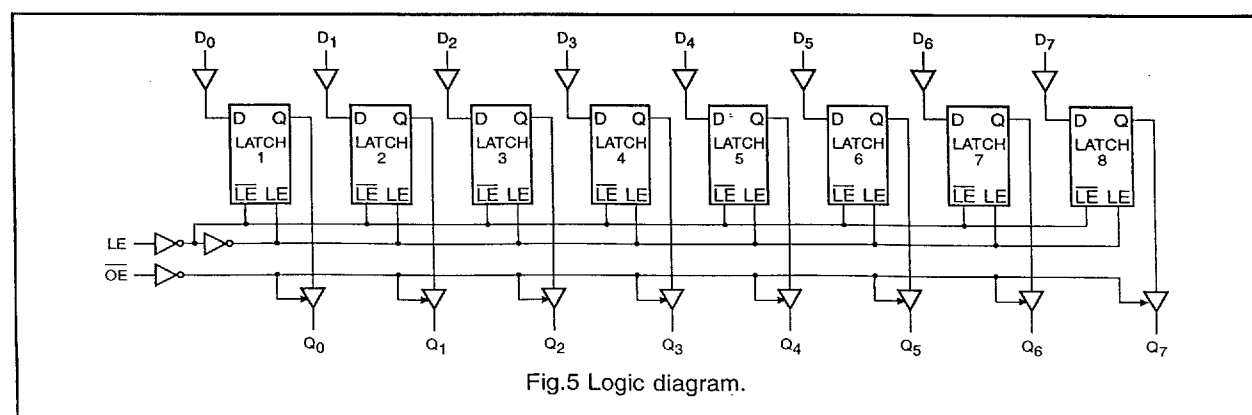
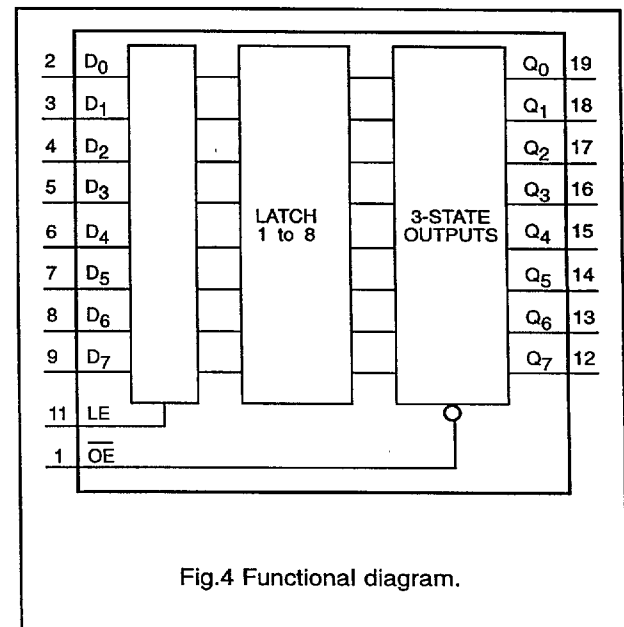
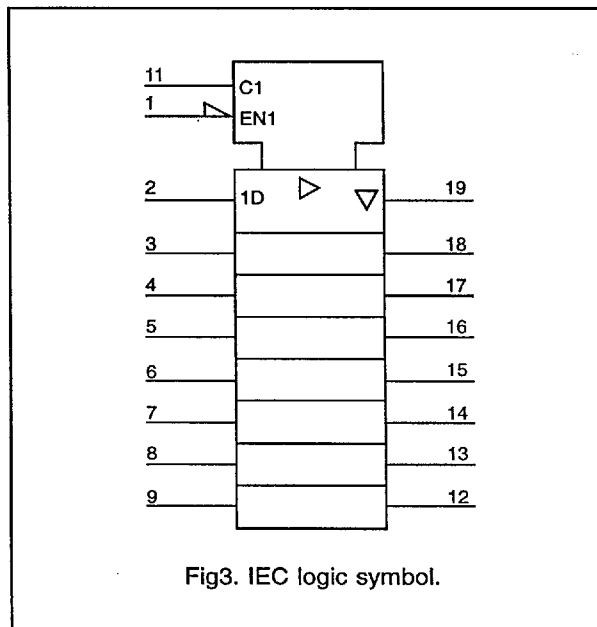
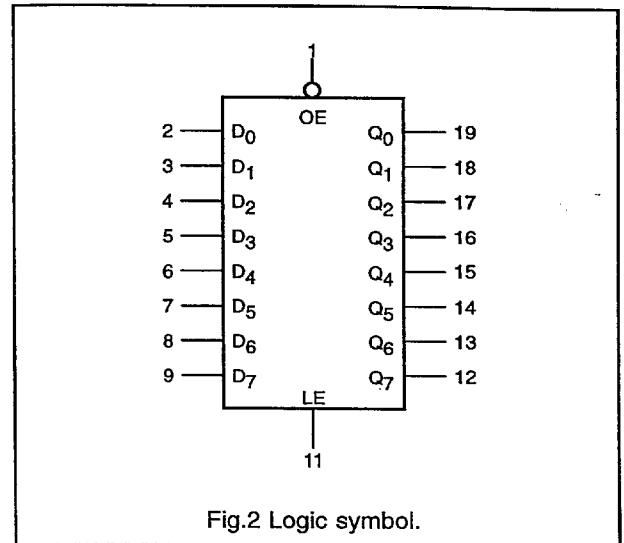
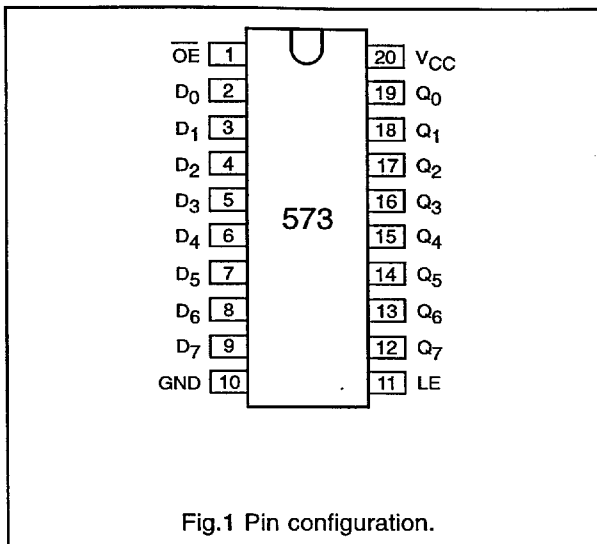
TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC(H)573AD	20	SO	plastic	SOT163-1
74LVC(H)573ADB	20	SSOP	plastic	SOT339-1
74LVC(H)573APW	20	TSSOP	plastic	SOT360-1

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q_0 to Q_7	3-state latch outputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V_{CC}	positive supply voltage

Octal D-type transparent latch with 5-volt tolerant inputs/outputs; 3-state

74LVC573A
74LVCH573A



Octal D-type transparent latch with 5-volt tolerant inputs/outputs; 3-state

74LVC573A
74LVCH573A

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS Q ₀ to Q ₇
	$\overline{OE}$	LE	D _n		
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition

X = don't care

Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74LVC(H)573A

For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC(H)573A

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

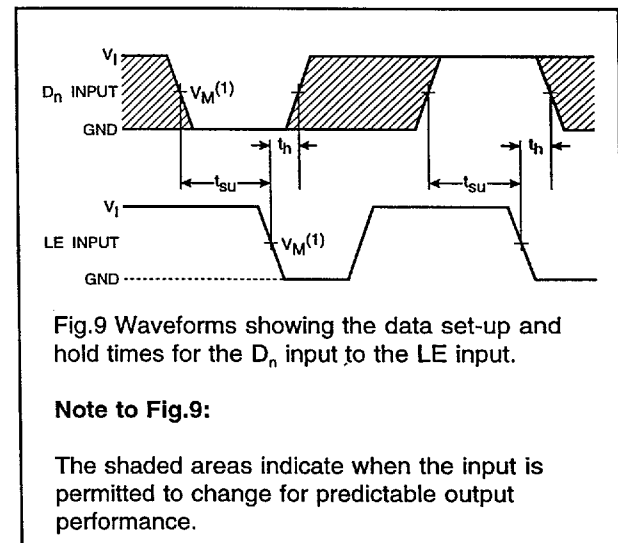
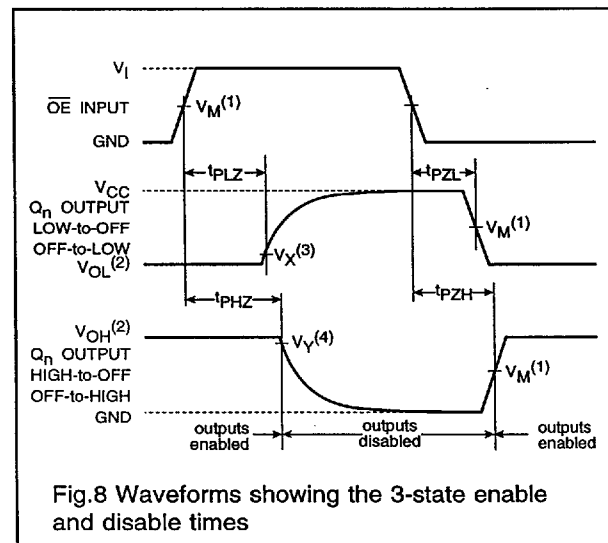
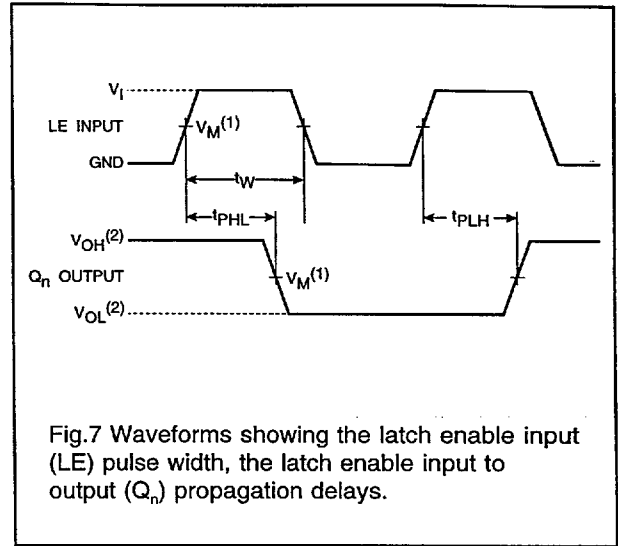
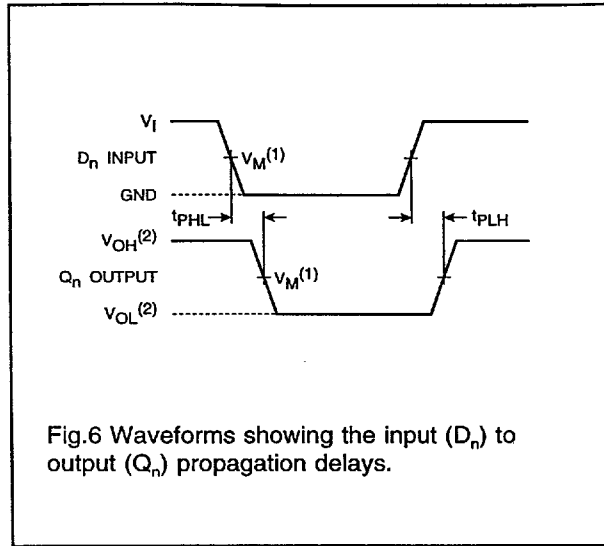
SYMBOL	PARAMETER	T _{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V _{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t _{PHL} /t _{PLH}	propagation delay D _n to Q _n	— 1.5 1.5	21 4.7 4.3*	— 8.0 7.5	ns	1.2 2.7 3.0 to 3.6	Figs 6, 10
t _{PHL} /t _{PLH}	propagation delay LE to Q _n	— 1.5 1.5	23 5.3 4.6*	— 9.0 8.0	ns	1.2 2.7 3.0 to 3.6	Figs 7, 10
t _{PZH} /t _{PZL}	3-state output enable time OE to Q _n	— 1.5 1.5	17 4.4 3.8*	— 8.5 7.5	ns	1.2 2.7 3.0 to 3.6	Figs 8, 10
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Q _n	— 1.5 1.5	8.0 4.0 3.5*	— 6.5 6.0	ns	1.2 2.7 3.0 to 3.6	Figs 8, 10
t _W	LE pulse width HIGH	— —	3.0 3.0*	— —	ns	2.7 3.0 to 3.6	Fig.7
t _{su}	set-up time D _n to LE	1.0 1.0	0.2 0.2*	— —	ns	2.7 3.0 to 3.6	Fig.9
t _h	hold time D _n to LE	1.0 1.0	0 0*	— —	ns	2.7 3.0 to 3.6	Fig.9

Notes: All typical values are measured at T_{amb} = 25 °C.* Typical values are measured at V_{CC} = 3.3 V.

Octal D-type transparent latch with 5-volt tolerant inputs/outputs; 3-state

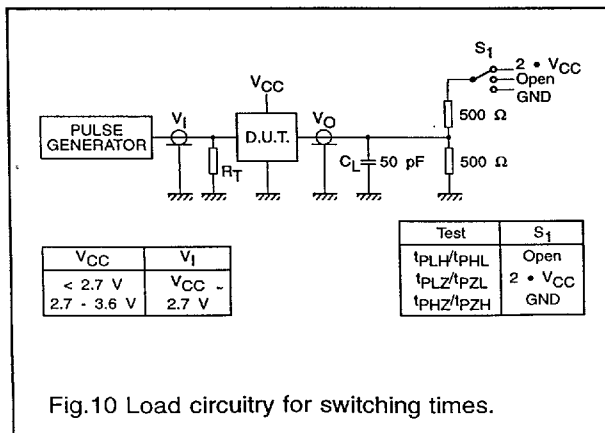
74LVC573A 74LVCH573A

AC WAVEFORMS



Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.



- Notes:**
- (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 - (2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
 - (3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 - (4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V