STLC4420A

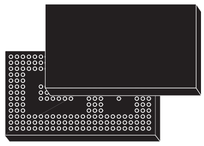
Single chip 802.11b/g/a WLAN radio

Feature summary

- Extremely small footprint
- Low power consumption
- High performance dual band solution,operating at 2.4 GHz and at 5 GHz
- Fully compliant with the IEEE 802.11b ,802.11g and 802.11a WLAN standards
- Support for 54, 48, 36, 24, 18, 12, 9, and 6Mbps OFDM, 11 and 5.5Mbps CCK and legacy 2 and 1Mbps data rates at 2.4 GHz
- Support for 54, 48, 36, 24, 18, 12, 9, and 6Mbps OFDM at 5 GHz
- Single chip 802.11b/g/a WLAN solution with fully integrated:
  - Zero IF (ZIF) transceiver,
  - Voltage controlled oscillator (VCO),
  - High-speed A/ D and D/A converters,
  - Radio power management unit (PMU),
  - OFDM and CCK baseband processor,
  - ARM9 media access controller (MAC),
  - SPI serial host interface (up to 48Mbps)
  - PA bias control
  - Flexible integrated power management unit
  - Glueless FEM interface
- Intelligent power control, including 802.11 power save mode
- Fully integrated Bluetooth coexistence
- Mode selectable SPI or SDIO host interface (up to 48Mbps)

Applications

- Cellular phones
- Personal digital assistants (PDA)
- Portable computers
- Hand-held data transfer devices
- Cameras
- Computer peripherals
- Cable replacement



LFBGA228 (12.5x7x1.4mm)

Description

The STLC4420A is a single chip dual band WLAN solution for embedded, low-power, high performance and very small form factor mobile applications. The product conforms to the IEEE 802.11b, 802.11g and 802.11a protocols operating in the 2.4 GHz and 5 GHz frequency band, supporting OFDM data rates of 54, 48, 36, 24, 18, 12, 9, and 6Mbps in the both bands and CCK data rates of 11 and 5.5Mbps and legacy data rates of 2 and 1Mbps at 2.4 GHz.

The STLC4420A is a fully integrated wireless radio including a ZIF transceiver, RF synthesizer/VCO, high-speed data converters, an OFDM/CCK digital baseband processor, an ARM9-based MAC and a complete power management unit with integrated PA bias control. An external dual band FEM completes a highly integrated chip set solution.

Host control is provided by a flexible serial interface (SPI or SDIO) supporting bit rates of 48Mbps. For maximum flexibility, the STLC4420A accepts system reference clock frequencies of 19.2, 26, 38.4 and 40 MHz. A reference design evaluation platform of hardware and software is provided to system integrators to rapidly enable wireless connectivity to mobile platforms..

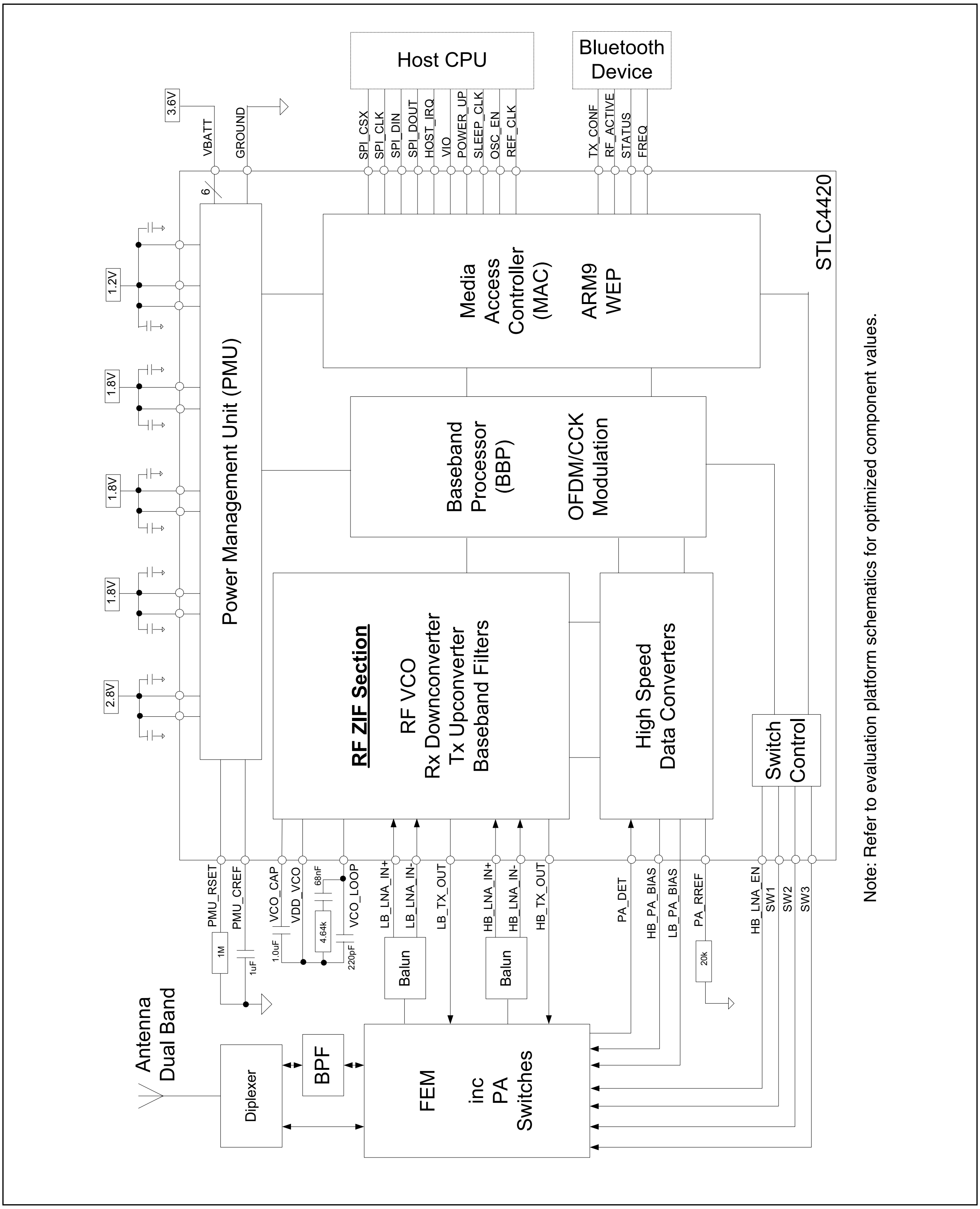
Order codes

Part number	Op. Temp. range, °C	Package
STLC4420A	-30 to 85	LFBGA228

Contents

1 Block diagram and application circuit

Figure 1. STLC4420A block diagram and application circuit (standard front end module)



2 Pin descriptions

Figure 2. STLC4420A pin connections

	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	PA_RREF	PA_RREF	RSRV_NC	VDDA_SYNTH	HB_TX_OUT	LB_TX_OUT	TX_GND	HB_LNA_IN-	HB_LNA_IN+	LB_LNA_IN-	LB_LNA_IN+	AGND	VDDA	1
2	PA_BIAS24	PA_BIAS24	RSRV_NC	TX_GND	TX_GND	VDDA	TX_GND	LNA_SHIELD	LNA_SHIELD	LNA_SHIELD	LNA_SHIELD	AGND	VDDA	2
3	VDD_BIAS	AGND	PA_BIAS5	VDDS_PRESR	AGND	TX_GND	TX_GND	AGND	AGND	AGND	LNA_SHIELD	AGND	VDDA	3
4	HISPEED_BUS_SEL	RSRV_NC	RSRV_NC								AGND	AGND	VDD_QLO	4
5	AGND	MODE0	RSRV_NC								AGND	AGND	VCO_LOOP	5
6	AGND	POR_V4I	MODE1			AGND	AGND	AGND			AGND	AGND	VDD_VCO	6
7	VDDA	POR_V4O	RSRV_NC			AGND	AGND	AGND			AGND	AGND	VCO_CAP	7
8	AGND	RSRV_NC	AGND			AGND	AGND	AGND			AGND	AGND	VDDA	8
9	VDDD	DGND	AGND			AGND	AGND	AGND			AGND	I_TEST-	I_TEST+	9
10	REF_CLK	RSRV_NC	AGND			AGND	AGND	AGND			AGND	Q_TEST-	Q_TEST+	10
11	AGND	FB_V2	AGND			AGND	AGND	AGND			AGND	AGND	VDDA	11
12	VDDA	V2OUT	AGND								AGND	PA_DET0	PA_DET1	12
13	OSC_EN	VDDA_PLL	VDDD								AGND	VCC_LNA	SW1	13
14	VBATV2	VBATV4	DGND	RSRV_NC	RSRV_NC	RSRV_NC	RSRV_NC	DGND	VDDD	RSRV_NC	FB_V2X	V2XOUT	SW2	14
15	V1OUT	HB_VPA	DGND	DGND	DGND	DGND	EMU_GND	DGND	VDDD	GPIO5	VBAT	VDDD	SW3	15
16	VBAT_V1	V4OUT	DGND	RSRV_NC	GNDA_PLL	RSRV_NC	VDDD	EMU_DGND	VDD_CORE	RSRV_NC	GP2_12	VBAT_V2X	SW4	16
17	LB_VPA	VDD_CORE	POR_V2O								GP2_10	SPI_DOUT	DGND	17
18	VDDD	SER_MODE	POR_V2I								GP2_9	GPIO4	HOST_IRQ	18
19	RSRV_NC	VDD_CORE	RSRV_NC			DGND	DGND	DGND			VDD_CORE	TX_CONF	STATUS	19
20	TMS	STANDBY1	TCLK								UART_SOUT	VIO	SPI_CSX	20
21	VDD_CORE	VDDD	RSRV_NC								FREQ	VDD_CORE	UART_SIN	21
22	TRSTN	GP1_3	GPIO7	TDI	VDDD	GP2_13	GPIO8	DGND	DGND	VI2C	DGND	SPI_CLK	GP2_8	22
23	RSRV_NC	GPIO6	GPIO1	GP1_7	EMU_CREF	POWER_UP	VDIG	RSRV_NC	DGND	EMU_SCL	GP1_4	LF_XTAL_IN	VDD_CORE	23
24	DGND	STANDBY2	GPIO3	RSRV_GND	IRES	TDO	V4_OUT_SEL	DAT2	RF_ACTIVE	SPI_DIN	EMU_SDA	DGND	DGND	24
	N	M	L	K	J	H	G	F	E	D	C	B	A	

2.1 Signal description

Table 1. STLC4420A signal descriptions

Pin name	Pin number	Type	Internal resistor	Function
RF front end interface pins				
LB_LNA_IN-	D1	RF input	100Ω RF Differential	Low band (2.4 GHz) 100Ω RF differential RX inputs.
LB_LNA_IN+	C1	RF input		
HB_LNA_IN-	F1	RF input	100Ω RF Differential	High band (5 GHz) 100Ω RF differential RX inputs.
HB_LNA_IN+	E1	RF input		
LNA_SHIELD	C2, C3,D2, E2, F2	RF shield	-	Low noise amplifier (LNA) input shield pins.
LB_TX_OUT	H1	RF output	-	50Ω RF transmit (TX) low band (2.4 GHz) single ended output.
HB_TX_OUT	J1	RF output	-	50Ω RF transmit (TX) low band (5 GHz) single ended output.
SW1	A13	digital output	-	Complementary transmit/receive antennaswitch control outputs. I/O level determined by VDDA supply input.
SW2	A14	digital output	-	
SW3	A15	digital output	-	
SW4	A16	digital output	-	
PA_BIAS24	N2, M2	analog output	-	Power amplifier bias control (2.4 GHz). DAC full-scale output current determined by PA_RREF resistor.
PA_BIAS5	L3	analog output	-	Power amplifier bias control (5 GHz). DAC full-scale output current determined by PA_RREF resistor.
PA_RREF	N1, M1	analog reference	-	Analog reference resistor. A 20K ohm typical resistor sets the PA_BIAS full-scale output current.
PA_DET0	B12	analog input	Resistor ladder	PA Detector Input 0. (2.4 GHz)
PA_DET1	A12	analog input		PA Detector Input 1. (5 GHz)
Host interface and clock pins				
DAT2	F24	1.8 V (VIO) digital I/O		SDIO data I/O bit 2. Not used in SPI mode.
HOST_IRQ	A18	1.8 V digital output, VIO domain		Host interrupt request. Typically asserted to request a SPI data transfer. In SDIO mode pin = DAT1.
POWER_UP	H23	1.8 V digital input	1MΩ Pull-Down	Power up enable from host
OSC_EN	N13	1.8 V digital output	No Pull	Oscillator enable output. Initially driven high upon powerup, under firmware control after initialization.

Table 1. STLC4420A signal descriptions (continued)

Pin name	Pin number	Type	Internal resistor	Function
REF_CLK	N10	Clock input	-	Reference clock input (19.2, 26.0, 38.4 or 40.0 MHz). Use a 1000pF typical series blocking capacitor.
LF_XTAL_IN	B23	1.8 V (VIO) digital input		32KHz typical sleep clock input from host.
SPI_CLK	B22	1.8 V (VIO) digital input		SPI clock from host
SPI_CSX	A20	1.8V (VIO) digital input		SPI chip select from host
SPI_DIN	D24	1.8 V (VIO) digital I/O		SPI data input for 4-wire modes. In 3-wire modes, this is the data input/output signal.
SPI_DOUT	B17	1.8 V (VIO) digital output		SPI data output for 4-wire modes only. In SDIO mode pin = DAT0.
FREQ	C21	1.8 V (VIO) GPIO (input)	No Pull	Firmware controlled GPIO typically implementing Bluetooth coexistence FREQ input function. Assigned to ARM MAC GP2-6.
RF_ACTIVE	E24	1.8 V (VIO) GPIO (input)	No Pull	Firmware controlled GPIO typically implementing Bluetooth coexistence RF_ACTIVE input function. Assigned to ARM MAC GP2-5.
STATUS	A19	1.8 V (VIO) GPIO (input)	No Pull	Firmware controlled GPIO typically implementing Bluetooth coexistence STATUS input function. Assigned to ARM MAC GP2-4.
TX_CONF	B19	1.8 V (VIO) GPIO (output)	No Pull	Firmware controlled GPIO typically implementing Bluetooth coexistence TX_CONF output function. Assigned to ARM MAC GP2-3.
MODE0	M5	1.8 V digital input		MODE strapping pins are pimarily used to properly initialize the PLL for following REF_CLK frequencies. Connect appropriate pin to ground plane for a logic 0 input or to 1.8V power plane (through a 4kohm resistor) for a logic 1. MODE(1:0) = 00 => 19.2 MHz MODE(1:0) = 01 => 40 MHz default, no pull needed MODE(1:0) = 10 => 26 MHz MODE(1:0) = 11 => 38.4 MHz (Note: M5=RX0, L6=RX1)
MODE1	L6	1.8 V digital input		
HISPEED_ BUS_SEL	N4	1.8 V digital input		High speed internal bus selection input. Needs to be pulled down through 2.5K ohm to set the proper high speed bus mode. (Note: N4 = ANTSELTST+)

Table 1. STLC4420A signal descriptions (continued)

Pin name	Pin number	Type	Internal resistor	Function
Power supply pins				
POR_V2O	L17	1.8V (V2) Digital Input		BB/MAC Power on Reset Input
POR_V2I	L18	1.8V (V2) Digital Output		EMU Power on Reset Output. A more detailed description could be added from the ST EMU spec
POR_V4I	M6	2.8V (V4) Digital Input		Transceiver Power on Reset Input
POR_V4O	M7	2.8V (V4) Digital Output		EMU Power on Reset Output. A more detailed description could be added from the ST EMU spec
VBATV2X	B16	Supply Input (3.6V)		Battery supply inputs for regulator V2X of the EMU. Decouple . Decouple to a solid ground plane using a ceramic capacitor located as close a possible to the VBAT pins.
VBATV2	N24			Battery supply inputs for regulator V2 of the EMU. Decouple to a solid ground plane using a ceramic capacitor located as close a possible to the VBAT pins.
VBATV1	N16			Battery supply input for regulator V1 of the EMU. Decouple to a solid ground plane using a ceramic capacitor located as close a possible to the VBAT pins.
VBATV4	M14			Battery supply input for regulator V4 of the EMU. Decouple to a solid ground plane using a ceramic capacitor located as close a possible to the VBAT pins.
STANDBY1	M20	1.8 Digital Output		Indicates power regulator standby status with STANDBY_1. A more detailed description should be taken from the ST EMU specification
STANDBY2	M24	1.8 Digital Output		Indicates power regulator standby status with STANDBY_1. A more detailed description should be taken from the ST EMU specification
SER_MODE	M18	1.8V (VIO) Digital Input		Selects Serial Host Interface Mode. Set to Logic High for SPI mode, set to Logic Low for SDIO mode
VBAT	C15	Supply Input (3.6V)	-	Battery supply inputs. Decouple to a solid ground plane using a ceramic capacitor located as close a possible to the VBAT pins.
VDIG	G23	Supply Input (3.3V)	-	Supply pin for SW1 to SW4 digital output drivers. (3.6V Nominal)

Table 1. STLC4420A signal descriptions (continued)

Pin name	Pin number	Type	Internal resistor	Function
VI2C	D22	Digital supply input		Digital 1.8V I/O power supply input pin dedicated to the EMU I2C bus interface. Connect to ground if the I2C interface of the EMU is not connected (EMU_SCL, EMU_SDA)
VIO	B20	Supply input (1.8 V)	-	Host digital I/O supply input for SPI and Bluetooth interfaces.
V1OUT	N15	Regulator output	-	Linear regulator 1.8V output.
V2OUT	M12	Regulator output	-	Linear regulator 1.8V output.
V2XOUT	B14	Regulator output	-	Linear regulator 1.2V output.
V4OUT	M16	Regulator output	-	Linear regulator output selectable for 2.81V or 3.11V. Output voltage controlled by V4_OUTSEL pin G24.
V4_OUTSEL	G24	1.8 V digital input	-	Control input for selection of V4OUT regulator output voltage. Logic 0 = 0=2.81V, 1= 3.11V
FB_V2	M11	Regulator sense	-	Sense line for V2 regulator. Connect to V2OUT pin M12 with a short trace.
FB_V2X	C14	Regulator sense	-	Sense line for V2X regulator. Connect to V2XOUT pin B14 with a short trace.
EMU_CREF	J23	Analog reference	-	Reference capacitor for internal Power Management Unit (PMU). Connect a 1uF capacitor to a solid board gound plane.
IRES	J24	Analog reference		Reference resistor for the internal Power Management Unit (EMU). Connect a 1MΩ resistor to a solid board ground plane.
VDDA	A1, A2, A3, A8, A11, H2, N7, N12	Analog supply input	-	Analog 1.8V supply input pins. Decouple to a solid ground plane using ceramic capacitors located as close a possible to the appropriate pins. Refer to evaluation platform schematics.
VDDA_SYNTH	K1			
VDDS_PRESR	K3			
VCC_LNA	B13			
HB_VPA	M15	3.0 V digital output		High Band PA Enable
LB_VBA	N17	3.0 V digital output		Low Band PA Enable
VDDA_PLL	M13	Analog supply input	-	Phase Locked Loop supply = 1.8V

Table 1. STLC4420A signal descriptions (continued)

Pin name	Pin number	Type	Internal resistor	Function
VDD_QLO	A4	Analog supply input	-	Analog 1.8V supply input for RF Quadrature Local Oscillator (QLO). Decouple to a solid ground plane using a ceramic capacitor located as close as possible to the pin. Refer to evaluation platform schematics.
VDD_VCO	A6	Analog supply input	-	Analog 1.8V supply input for the RF Voltage Controlled Oscillator (VCO). Typically connected to V1OUT pin N15. Decouple to a solid ground plane using a ceramic capacitor located as close as possible to the pin. Refer to evaluation platform schematics.
VDD_BIAS	N3	Analog supply input	-	Analog supply input for BIAS control ciruits. Typically connected to V4OUT pin M16. Decouple to a solid ground plane using a ceramic capacitor located as close as possible to the pin. Refer to evaluation platform schematics.
VDDD	B15, J22, M21, N18, E14, E15, L13, N9,G16	Digital supply input	-	Digital 1.8V I/O power supply input pins. Decouple to a solid ground plane using ceramic capacitors located as close a possible to the appropriate pins. Refer to evaluation platform schematics.
AGND	B1-B8,B11, C4-C13, D3, E3, F3, F6-F11, G6-G11, H6-H11, J3, L8-L12, M3, N5, N6, N8, N11	Analog ground	-	All AGND pins must be connected together through a solid ground plane. For optimal performance, refer to the evaluation platform layout for the proper AGND and DGND grounding scheme.
TX_GND	G1, G2, G3, H3, J2, K2	Analog ground	-	All TX_GND pins must be connected together through a solid ground plane. For optimal performance, refer to the evaluation platform layout for the proper grounding scheme.
VDD_CORE	A23, B21, C19, E16, M17, M19, N21	Digital supply input	-	Digital 1.2V core supply. Decouple to a solid ground plane using ceramic capacitors located as close a possible to the appropriate pins. Refer to evaluation platform schematics.
DGND	A17,L14, L15, L16, M9, K15, J15, H15, H19, G19, F14, F15, F19, F22, E22, C22, E23, N24, B24, A24	Digital ground	-	All DGND pins must be connected together through a common solid ground plane. For maximum performance, refer to the evaluation platform layout for the proper AGND and DGND grounding scheme.

Table 1. STLC4420A signal descriptions (continued)

Pin name	Pin number	Type	Internal resistor	Function
EMU_GND	G15	Ground		Ground of the EMU.
EMU_DGND	F16	Digital Ground		Ground of the EMU level shifter.
GNDA_PLL	J16			
Miscellaneous Pins				
GPIO8	G22	1.8V (VDDD) GPIO	No Pull	Firmware controlled 1.8V digital GPIO Assigned to ARM MAC GP2-11. Float for proper operation.
GPIO7	L22	1.8V (VDDD) GPIO	No Pull	Firmware controlled 1.8V digital GPIO. Assigned to ARM MAC GP2-1. Can optionally be used as a serial data line (SDA) for external 1.8V serial FLASH device.
GPIO6	M23	1.8V (VIO) GPIO	40uA Pull-Down	Firmware controlled 1.8V digital GPIO. Assigned to ARM MAC GP2-0. Can optionally be used as a serial clock line (SCL) for external 1.8V serial FLASH device.
GPIO5	D15	1.8V (VIO) GPIO	Pull-Up	Firmware controlled 1.8V digital GPIO. Assigned to ARM MAC GP1-13. (Radio_PE). Float for proper operation.
GPIO4	B18	1.8V (VIO) GPIO	Pull-Up	Firmware controlled 1.8V digital GPIO -- float for proper operation. Assigned to ARM MAC GP1-15. (FAAmode_n)
GPIO3	L24	1.8V (VDDD) GPIO	40uA Pull-Down	Firmware controlled 1.8V digital GPIO -- float for proper operation. Assigned to ARM MAC GP2-2. (LED2/TR_SW_Bar)
GPIO1	L23	1.8V (VDDD) GPIO	No Pull	Firmware controlled 1.8V digital GPIO -- float for proper operation. Assigned to ARM MAC GP2-15 (FAA_HDRn).
GP1_3	M22	1.8V (VDDD) GPIO	No Pull	Firmware controlled 1.8V digital GPIO Assigned to ARM MAC GP1-3. Float for proper operation.
GP1_7	K23	1.8V (VDDD) GPIO	No Pull	Firmware controlled 1.8V digital GPIO Assigned to ARM MAC GP1-7. Float for proper operation.
GP2_13	H22	1.8V (VDDD) GPIO	No Pull	Firmware controlled 1.8V digital GPIO Assigned to ARM MAC GP2-13. Float for proper operation.
GP2_12	C16	1.8V (VDDD) GPIO	No Pull	Firmware controlled 1.8V digital GPIO Assigned to ARM MAC GP2-12. Float for proper operation.

Table 1. STLC4420A signal descriptions (continued)

Pin name	Pin number	Type	Internal resistor	Function
GP2_10	C17	1.8V (VDDD) GPIO	No Pull	Firmware controlled 1.8V digital GPIO Assigned to ARM MAC GP2-10. Float for proper operation.
GP2_9	C18	1.8V (VDDD) GPIO	No Pull	Firmware controlled 1.8V digital GPIO Assigned to ARM MAC GP2-9. Float for proper operation.
GP1_4	C23	1.8V (VDDD) GPIO	No Pull	Firmware controlled 1.8V digital GPIO Assigned to ARM MAC GP1-4. Float for proper operation.
GP2_8	A22	1.8V (VDDD) GPIO	No Pull	Firmware controlled 1.8V digital GPIO Assigned to ARM MAC GP2-8. Float for proper operation.
I_TEST-	B9	Reserved	-	Reserved analog test pins -- float for proper operation.
I_TEST+	A9		-	
Q_TEST-	B10		-	
Q_TEST+	A10		-	
VCO_CAP	A7	Miscellaneous	-	RF VCO core decoupling pin. Decouple this pin through a ceramic capacitor to VDD_VCO pin A6. Refer to evaluation platform schematics for optimal capacitor value.
VCO_LOOP	A5	Miscellaneous	-	VCO loop filter pin. Connect this pin to thru a loop filter network to VDD_VCO pin A6. Refer to evaluation platform schematics for optimal filter network.
EMU_SCL	D23	Miscellaneous		Optional EMU programming I2C clock
EMU_SDA	C24	Miscellaneous		Optional EMU programming I2C data/address
RSRV_GND	K24	Reserved	-	Reserved pin. Connect to ground plane for proper operation.
RSRV_NC	D14, D16, G14, H14, H16, J14, K16, L1, L2, L4, L5, L7, M4, M8, M10, N19, N23, F23, L21, L19, K14	Reserved	-	Reserved pins. Float for proper operation.
TCLK	L20	JTAG	Pull-Up	JTAG clock
TDI	K22	JTAG	No-Pull	JTAG data input
TDO	H24	JTAG	No-Pull	JTAG data output
TMS	N20	JTAG	Pull-Up	JTAG test mode select
TRSTN	N22	JTAG	Pull-Up	JTAG reset

Table 1. STLC4420A signal descriptions (continued)

Pin name	Pin number	Type	Internal resistor	Function
UART_SIN	A21	1.8V (VDDD) digital input	Pull-Down	UART serial input
UART_SOUT	C20	1.8V (VDDD) digital output	No-Pull	UART serial output

3 Electrical specifications

Note: The STLC4420 has an ESD classification of Class TBD.

Warning: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Table 2. General electrical specifications

Parameter		Test condition / comment	Min.	Typ.	Max.	Units
Absolute maximum ratings						
PMU VBATT (V_{cc})			-0.3	-	7.0	V
Voltage on any other pin		Within shared voltage rails	-0.3	-	V_{cc} + 0.3	V
V_{cc} to V_{cc} decouple			-0.3	-	+0.3	V
Any GND to GND			-0.3	-	+0.3	V
Operating conditions and input power specifications						
Operating temperature range			-30		85	^{o}C
VBATT supply	Input supply voltage	Power Management Unit VBATT supply input	3.0	3.6	5.5	V
	Average continuous tx current	Continuous Transmitting @ 54Mbps, VBATT = 3.6 V		TBD		mA
	Average continue rx current	Receiving Valid Packets @ 54Mbps, VBATT = 3.6 V		TBD		mA
	Average standby mode current	VBATT = 3.6 V		85		µA
VDIG supply	Input supply voltage	Power management unit VDIG supply for digital buffers	3	3.6	VBATT	V
	Input supply current	VDIG = 3.6 V, Typical load is application dependent	-	-	-	mA
VIO supply	Input supply voltage	VIO input supply determines Host CMOS logic levels for: SPI_CSX, SPI_CLK, SPI_DIN, SPI_DOUT, HOST_IRQ, SLEEP_CLK, FREQ, RF_ACTIVE, STATUS, TX_CONF, GPIO4, GPIO5, GPIO6	1.62	1.8	1.98	V
	Input supply current	VIO = 1.8 V	-	-	10	mA

Table 2. General electrical specifications (continued)

Parameter		Test condition / comment	Min.	Typ.	Max.	Units
Internal power management unit (PMU) specifications						
PMU_CREF		PMU reference capacitor	-30%	1	+30%	uF
PMU_RSET		PMU reference resistor	-1%	1	+1%	MΩ
V1OUT Linear Regulator	Output Voltage	Active Mode Low Power Mode	1.757 1.759	1.8 1.8	1.841 1.847	V
	Peak Output Current	Active Mode Low Power Mode			50 5	mA
	External Output Load Capacitor	Typical ESR = 0.1 ohm	-35%	1	+35%	uF
V2OUT Linear Regulator	Output Voltage	Active Mode Low Power Mode	1.759 1.74	1.8 1.8	1.844 1.860	V
	Peak Output Current	Active Mode Low Power Mode			300 5	mA
	External Output Load Capacitor	Typical ESR = 0.1 ohm	-35%	2.2	+35%	uF
V2XOUT Linear Regulator	Output Voltage	Active Mode Low Power Mode	1.159 1.150	1.2 1.2	1.244 1.250	V
	Peak Output Current	Active Mode Low Power Mode			280 20	mA
	External Output Load Capacitor	Typical ESR = 0.1 ohm	-35%	2.2	+35%	uF
V4OUT Linear Regulator	Output Voltage	Active Mode: V4_OUTSEL=0 V4_OUTSEL=1 Low Power Mode: V4_OUTSEL=0 V4_OUTSEL=1	 2.726 3.016 2.726 3.016	 2.81 3.11 2.81 3.11	 2.894 3.203 2.894 3.203	V
	Peak Output Current	Active Mode Low Power Mode			30 5	mA
	External Output Load Capacitor	Typical ESR = 0.1 ohm	-35%	1	+35%	uF
Receiver specifications 802.11b/g (802.11a TBC)						
	RX RF Frequency Range	802.11 b/g	2300		2500	MHz
		802.11 a	4900		5850	
	RX LO Frequency Range		4600		5000	MHz
	RF Input VSWR	Differential, 100 Ohms reference	2:1			
	RX LO Phaser Jitter	50KHz to 10MHz, RMS LO/2		1.25		Deg

Table 2. General electrical specifications (continued)

Parameter		Test condition / comment	Min.	Typ.	Max.	Units
	LO to LNA Input Feed through	At LO/2 Frequency. RF front end properly matched and isolated			-70	dBm
		At LO Frequency. RF front end properly matched and isolated			-50	dBm
	Maximum RX input Level	b/g Band only. RF front end properly matched	-23	-10		dBm
	Adjacent ChannelRejection	CCK CH6	35	37		
		OFDM 54Mbits Ch6	-1	11		
	TX to RX Input Leakage	During transmit mode, affecting TX distortion		+5		dBm
	DSB NF	High Gain RX Mode, -90dBm input, b and g Band only, front end losses not included		5	7	dB
	IP3 Input		-17	-16		dBm
	IP2 Input			+13		dBm
	DSB NF	Low Gain RX Mode, -20dBm input, b and g Band only, front end losses not included		29.8		dB
	IP3 Input			+9		dBm
	IP2 Input			+33		dBm
	RF Hi/Lo Gain Switching Point	b/g Band only. RF front end properly matched.		-38		dBm
	Receive Sensitivity, b and g band, front end losses not included	6Mbps OFDM, 10% PER	-85	-90		dBm
		9Mbps OFDM, 10% PER		-88		dBm
		12Mbps OFDM, 10% PER		-87		dBm
		18Mbps OFDM, 10% PER		-84		dBm
		24Mbps OFDM, 10% PER		-80		dBm
		36Mbps OFDM, 10% PER		-76		dBm
		48Mbps OFDM, 10% PER		-73		dBm
		54Mbps OFDM, 10% PER	-68	-71		dBm
		1Mbps BPSK, 8% PER	-89	-96		dBm
		2Mbps QPSK, 8% PER		-91		dBm
		5.5Mbps CCK, 8% PER		-90		dBm
		11Mbps CCK, 8% PER	-82	-86		dBm

Table 2. General electrical specifications (continued)

Parameter		Test condition / comment	Min.	Typ.	Max.	Units
	Multipath Delay Spread	6Mbps, 10% PER		820		ns
		9Mbps, 10% PER		430		ns
		12Mbps, 10% PER		630		ns
		18Mbps, 10% PER		405		ns
		24Mbps, 10% PER		320		ns
		36Mbps, 10% PER		210		ns
		48Mbps,10% PER		160		ns
		54Mbps, 10% PER		120		ns
		1Mbps BPSK and 2Mbps QPSK, 8% PER		250		ns
		5.5 and 11Mbps CCK, 8% PER		100		ns
Transmitter specifications 802.11b/g (802.11a TBC)						
	TX RF Frequency Range	802.11 b/g	2300		2500	MHz
		802.11 a	4900		5850	
	TX LO Frequency Range		4600		5000	MHz
	RF Output VSWR	Note: Over AGC range, b and g Bands only			2:1	
	TX LO Phase Jitter	50KHz to 10MHz, RMS, LO/2		1.25		Deg
	TX AGC Control Dynamic Range		40			dB
	TX AGC Control Step Size	Monotonic			2	dBm
	CCK Output Power	At 0 control attenuation. RF front end properly matched	5		8	dBm
	CCK Output Power	Case 1: Set TX AGC to obtain this Pout.		3		dBm
	OFDM Output Power			-6		dBm
	Output Noise Floor	Carrier offsets 0 to 10MHz			-135	dBm/Hz
		Carrier offsets >20MHz			-138	dBm/Hz
	CCK Output Power	Case 2: Set TX AGC to obtain this Pout		-7		dBm
	OFDM Output Power			-16		dBm
	Output Noise Floor	Carrier offsets 0 to 10MHz			-137.5	dBm/Hz
		Carrier offsets >20MHz			-140.5	dBm/Hz

Table 2. General electrical specifications (continued)

Parameter		Test condition / comment	Min.	Typ.	Max.	Units
	CCK Output Power	Case 3: Set TX AGC to obtain this Pout		-17		dBm
	OFDM Output Power			-26		dBm
	Output Noise Floor	Carrier offsets 0 to 10MHz			-140	dBm/Hz
		Carrier offsets >20MHz			-143	dBm/Hz
	CCK Output Power	Case 4: Set TX AGC to obtain this Pout		-27		dBm
	OFDM Output Power			-36		dBm
	Output Noise Floor	Carrier offsets 0 to 10 MHz			-142.5	dBm/Hz
		Carrier offsets >20 MHz			-145.5	dBm/Hz
	CCK Output Power	Case 5: Set TX AGC to obtain this Pout		-37		dBm
	OFDM output power			-46		dBm
	Output noise floor	Carrier offsets 0 to 10 MHz			-145	dBm/Hz
		Carrier offsets >20 MHz			-148	dBm/Hz
External power amplifier detector ADC specifications						
	Full scale input voltage	At input of ADC	0		1.0	V
	Maximum input voltage	At PA_DETx input -- 16 tap resistive divider tap node			VDDA	V
	Input resistance			30K		Ohm
	Input capacitance				0.5	pF
External power amplifier BIAS DAC specifications						
	Full scale output current	At voltage output compliance > 1.8 V		2.5		mA
		At voltage output compliance = 1.8 V		5		mA
	Output voltage compliance *Note: An external resistor at PA_RREF pin determines the full scale output current.*	At -40°C, full scale output current < 2.5mA, VDD_BIAS = 3.15 V			2.85	V
		At +25°C, full scale output current < 2.5mA, VDD_BIAS = 3.15 V			2.75	V
		At +100°C, full scale output current < 2.5mA, VDD_BIAS = 3.15 V			2.55	V
		Full temperature range, scale output current <= 5mA, VDD_BIAS = 3.15 V			1.8	V

Table 2. General electrical specifications (continued)

Parameter		Test condition / comment	Min.	Typ.	Max.	Units
	BIAS DAC supply voltage		2.8		3.15	V
SPI_DOUT	Tdod	SPI_DOUT delay from transmit edge of SPI_CLK	0		7	ns
	Tdozh	SPI_DOUT delay before HI-Z state from rising edge of SPI_CSX	0			ns
	Tdozd	SPI_DOUT delay before driven from HI-Z state on falling edge of SPI_CSX			10	ns

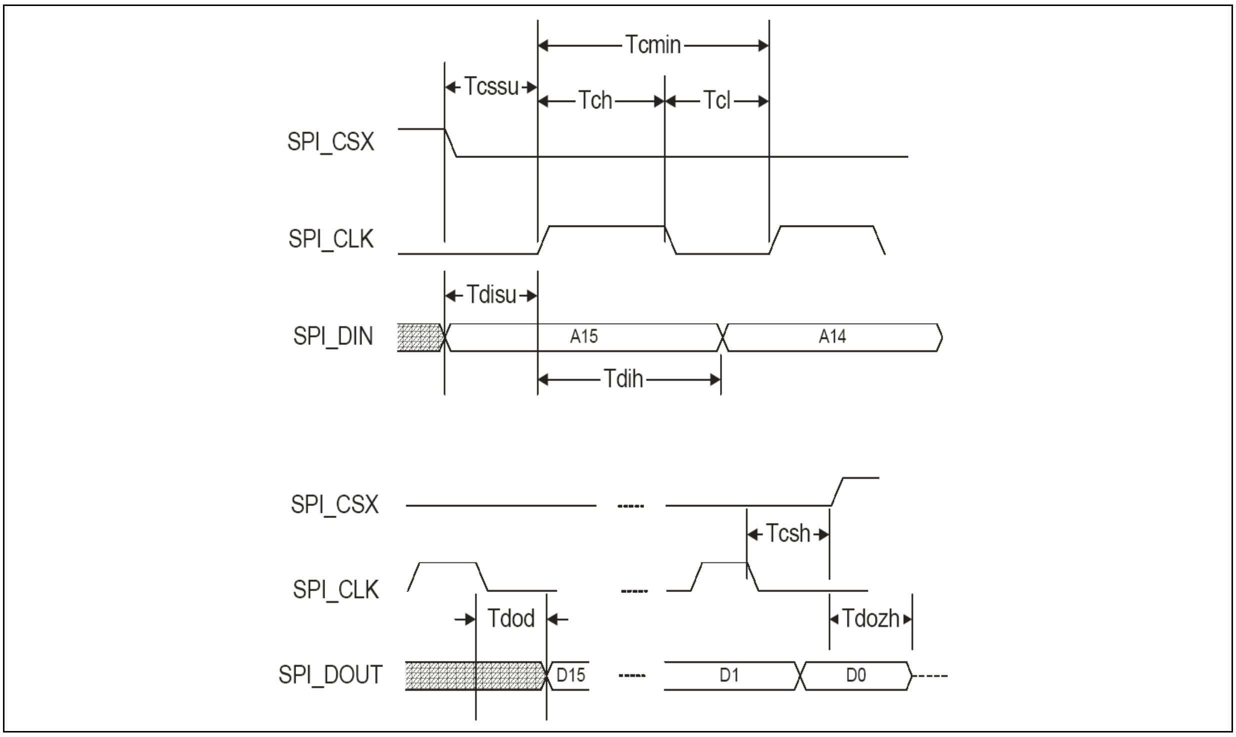
Table 3. Host interface specifications

Parameter		Test condition / comment	Min.	Typ.	Max.	Units
Digital interface specifications						
POWER_UP Input	VIH	PMU Power up control. Active High.	0.8	-	VBATT	V
	VIL		0	-	0.3	V
	Pull-Down		-	500	-	K ohms
Host CMOS Inputs	VIH	VIO supply domain	0.7*VIO	-	VIO + 0.3	V
	VIL		0	-	0.3*VIO	V
Host CMOS Outputs	VOH	IOH = 0.2mA, VIO supply domain	VIO - 0.2	-	VIO	V
	VOL	IOL = 6mA, VIO supply domain	0	-	0.6	V
	Input Current	VIO supply domain	-1.0	-	+1.0	µA
OSC_EN Input	VOH	IOH <= 2mA	1.4	-	-	V
	VOL	IOL <= 2mA	-	-	0.4	V
REF_CLK Input	Input Level	AC coupled	500	-	1000	mVpp
	Accuracy		-	-	25	ppm
SLEEP_CLK Input	Frequency	VIO supply domain	-	32.768	-	kHz
	Accuracy		-	-	150	ppm
	Duty Cycle		30	-	70	%
SPI timing specifications (refer to *Figure 3*)						
SPI_CLK	Tcmin	SPI_CLK Period	20.8			ns
	Tch	SPI_CLK High Time	10.4			ns
	Tcl	SPI_CLK Low Time	10.4			ns
SPI_CSX	Tcssu	SPI_CSX Setup time to first clock edge	10.4			ns
	Tcsh	SPI_CSX hold time from last clock edge	10.4			ns

Table 3. Host interface specifications

SPI_DIN	Tdisu	SPI_DIN setup time to receive edge of SPI_CLK	3			ns
	Tdih	SPI_DIN hold time to receive edge of SPI_CLK	0			ns

Figure 3. SPI timing specification



4 Serial host interface

4.1 Host pins

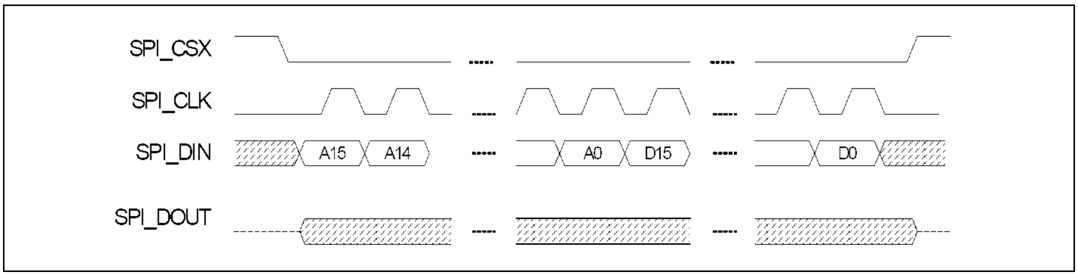
The Serial Host Interface consists of the following pins:

- SPI_CLK: serial host clock input, 0 to 48 MHz.
- SPI_DIN: serial host data input, sampled on active edge of SPI_CLK.
- SPI_DOUT: serial host data output, driven when asserted low and floating when de-asserted. SPI_DOUT is driven on inactive edge of SPI_CLK.
- SPI_CSX: serial host chip select, active low chip select.
- HOST_IRQ: serial host interrupt, active high interrupt to Host.

The serial host interface has 12 modes of operation controlled by 4 variables. The default 4-Wire mode may be changed by a SPI host write to the device status/ control register. If the host requires a different SPI mode for normal operation, the host may need to toggle the necessary SPI pins using GPIO-style interfacing to perform a 4-Wire write sequence to change the mode.

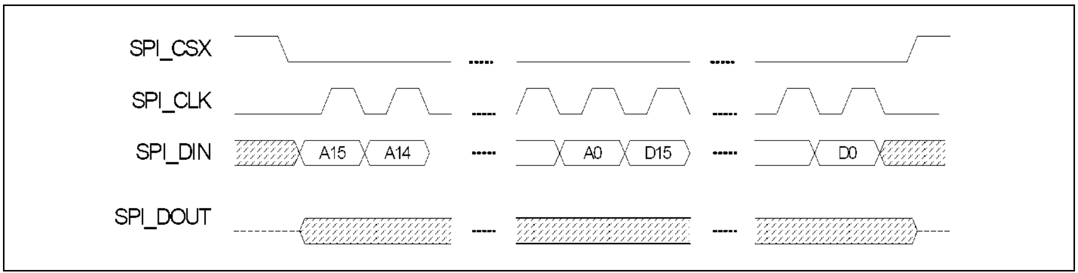
The default 4-Wire single word write is show below in *Figure 4*.

Figure 4. 4-Wire mode single word write



The default 4-Wire single word read is shown below in *Figure 5*.

Figure 5. 4-Wire mode single word read



4.2 SPI mode selection

As shown in *Table 4*, the 12 modes of operation are controlled by 4 variables in the device status/control register.

Table 4. Serial host modes of operation

Invert Clock	Phase Shift	3-Wire-Mode	3-Wire-Adr DataWait	Name
0	0	0	X	4-Wire
1	0	0	X	4-WireInv
0	1	0	X	4WShft
1	1	0	X	4-WireInvShft
0	0	1	0	3-Wire
1	0	1	0	3-WireInv
0	1	1	0	3-WireShft
1	1	1	0	3-WireInvShft
0	0	1	1	3-WireWait1
1	0	1	1	3-WireInvWait1
0	1	1	1	3-WireShftWait1
1	1	1	1	3-WireInvShftWait1

When Invert Clock = 0, SPI_CLK receive edge is the rising edge and SPI_CLK transmit edge is the falling edge.

The SPI_CLK polarity can be reversed by a host write to device status/control register to change the Invert Clock = 1.

In this case, the SPI_CLK transmit edge becomes the rising edge and SPI_CLK receive edge becomes the falling edge.

Figure 6. Single Word Read 4-WireInvMode

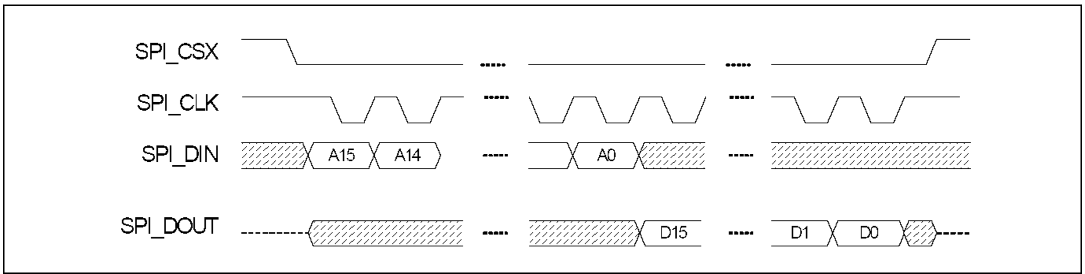


Figure 7. Single Word Read 4-WireShftMode

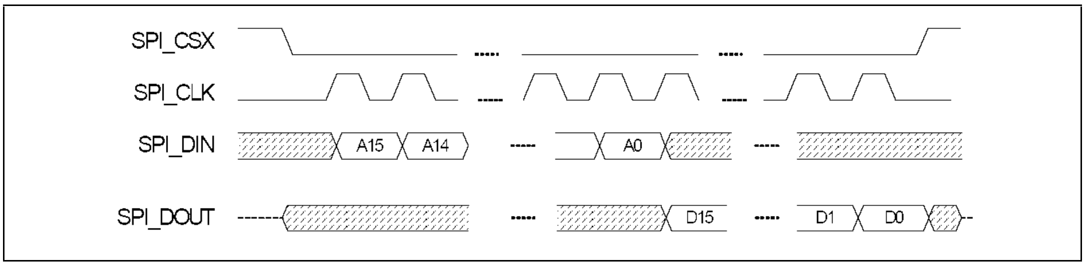


Figure 8. Single Word Read 4-WireInvShftMode

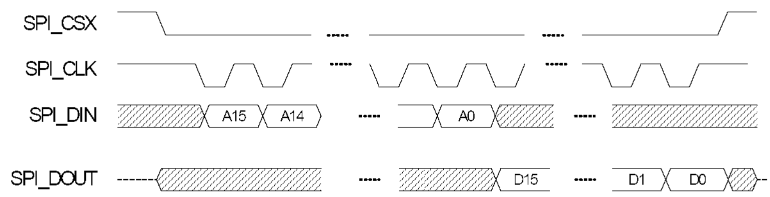


Figure 9. 3-Wire

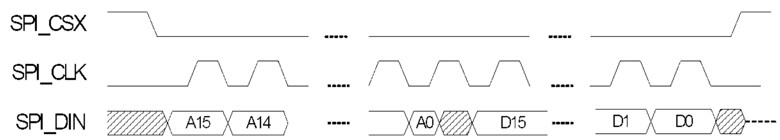


Figure 10. 3-WireInv

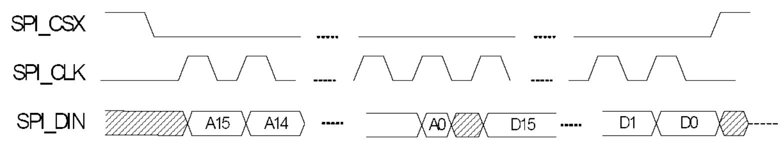


Figure 11. 3-WireShft

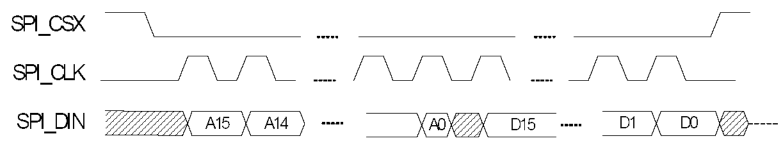


Figure 12. 3-WireInvShft

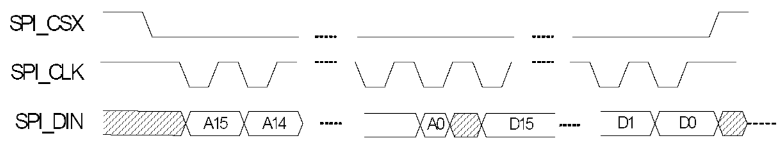


Figure 13. 3-WireWait1

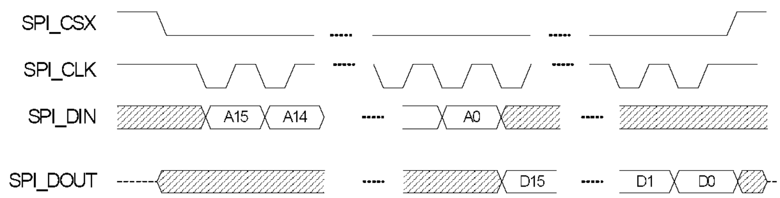


Figure 14. 3-WireInvWait1

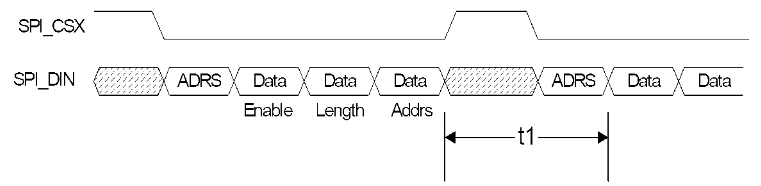


Figure 15. 3-WireShiftWait1

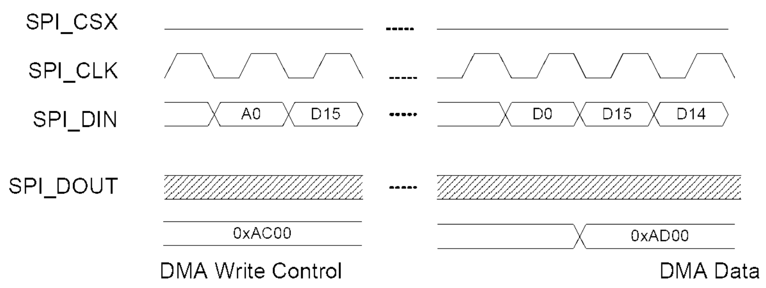
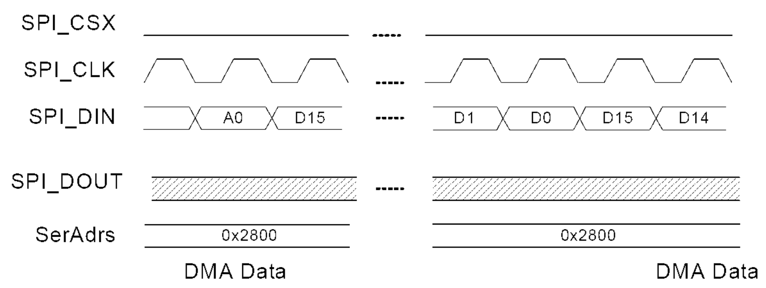


Figure 16. 3-WireInvShftWait1



4.3 AHB masters

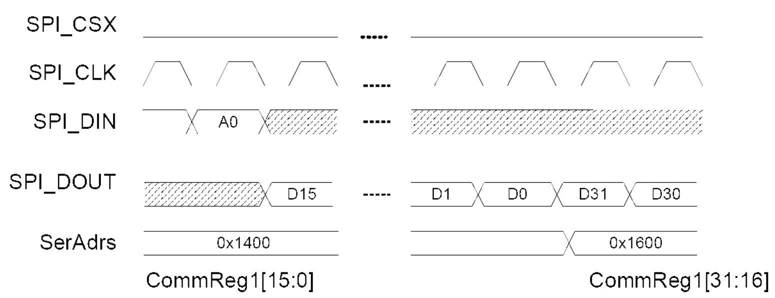
The DMA engines are contained within the Serial Host interface. The DMA engines access data on the device via a pair of AHB masters. AHB1 is connected to the standard AHB bus which is shared with the CPU and DMA controller AHB masters.

The Serial Host has a second AHB master connected to the AHB Ram directly via a AHB2. The Serial Host AHB2 master and the AHB Ram AHB2 slave are the only master and slave on the AHB2 bus. This guarantees sufficient bandwidth for the serial host interface.

When the AHB master is accessing APB registers the ApbAccess bit must be set to force the master to use word (32-bit) transfers so that the APB registers are not set to an indeterminate state by a pair of half-word (16-bit) transfers.

DMA read data is prefetched when the DMA Read Address is written and the DMA Write Enable is asserted. The host must not read DMA Data register before the prefetch completes. There must be 20 ABClock cycles between the end the Data Phase when DMA Read Address is written and the end of Address Phase which selects the DMA Read register.

Figure 17. AHB bus timing



The read data is registered on the 15 SPI_CLK of the address phase. SPI_CSX high time must be 20ABClocks - 15SPI_CLKs. If ABClock period is 100ns (10 MHz) and SPI_CLK period is 40ns then the time between writing DMA write address register and reading the DMA data register is (20 * 100) - (15 * 40) = 1.4us. If the ABClock period is 25ns (40 MHz) then SPI_CSX high time is < 0 for Read data to be valid. In this case, only the Min High time for SPI_CSX must be observed.

4.4 Host registers

The Host can access the registers listed in *Table 5*.

Table 5. Host registers

Domain	A14-A8	Access	Sleep access	Description	Notes
SPI_CLK	X00 0000 X00 0010	RW	RW	ARM interrupt	(1), (2)
ARM	X00 0100 X00 0110	R	--	ARM interrupt enable	
ARM	X00 1000 X00 1010	R	--	Host interrupt	(1)
SPI_CLK	X00 1100 X00 1110	RW	RW	Host interrupt enable	
SPI_CLK	X01 0000 X01 0010	W	--	Host interrupt acknowledge	
Shared	X01 0100 X01 0110	RW	--	GP1 communication	
Shared	X01 1000 X01 1010	RW	--	GP2 communication	
Host	X10 0100 X10 0110	RW	RW	Device control/ status	(1), (2)
Host	X10 1000	RW	--	DMA data	
Shared	X10 1100	RW	--	DMA write control	

Table 5. Host registers (continued)

Domain	A14-A8	Access	Sleep access	Description	Notes
Shared	X10 1110	RW	--	DMA write length	
Shared	X11 0000 X11 0010	RW	--	DMA write base	
Shared	X11 0100	RW	--	DMA read control	
Shared	X11 0110	RW	--	DMA read length	
Shared	X11 1000 X11 1010	RW	--	DMA read base	

1. Readable during Sleep Mode without generating Sleep interrupt. All registers are readable during Sleep Mode. Reading registers not marked as Readable during Sleep will set the ArmAsleep bit in the Host and ARM Interrupt registers.
2. Writable during Sleep Mode. All registers are writable during Sleep mode. Writing registers not marked as writable during Sleep mode requires several 32 kHz clock cycles to complete the write access and will set the ArmAsleep bit in the Host and Arm Interrupt.

The Host accesses each register as a 16-bit register. Registers which are physically 32-bits have 2 addresses in the Host address space. The even address (A9 == 0) is the low 16-bits and the odd address (A9 == 1) is the high 16-bits.

A15 is the read bit. A15 is set for reads and cleared for Writes. For example, to write ARM Interrupt[31:16] address bits 15:0 are set to 16'h0100. Address bits 15:0 are set to 16'h8100 to read ARM Interrupt[31:16]. A7 - A0 are don't care bits and can be set to any value by the Host. It is required that a full 16-bit address be sent. The initial data phase does not begin until the 16-bit address phase has completed.

4.5 Host writes

The Host writes to a 16-bit register by sending a 16 bit Address phase with A15 set to zero. The Address phase is followed by a 16-bit data phase. D15 is the first bit of data phase and D0 is the last bit of the data phase. D15 - D0 are written to the selected register on the active edge of SPI_CLK when D0 is present on SPI_DIN.

When the register is in the ARM or Shared clock domain the write process begins when on the active edge of SPI_CLK when D0 is present on SPI_DIN. The write completes after the data is synchronized into the ABClock domain. This process takes 3 ABClock cycles. ABClocks are 30us each in Sleep mode! Host must ensure 90us delays between writes to non-Sleep accessible registers when device is in Sleep mode.

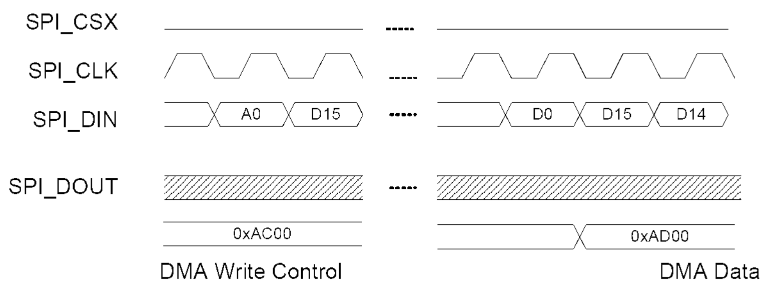
If less than 16 bits are written during the data phase the data is not written to the addressed register. The SPI_CLK may stop at any time. The current phase (address or data) is not interrupted by a stopped (or slowed) SPI_CLK. The logic remains in the current phase until SPI_CLK resumes or SPI_CSX is de-asserted.

4.6 Host multi-word writes

The Host may write to multiple consecutive 16-bit registers by keeping SPI_CSX asserted and continuing to toggle SPI_CLK after the initial 16-bit data phase has completed.

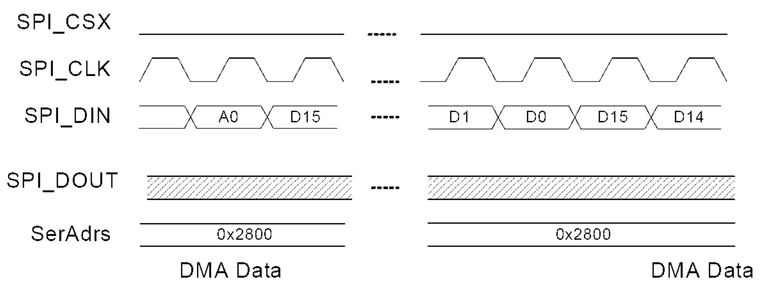
The register address is incremented by 2 at the end of each data phase for all register address except the DMA data register.

Figure 18. Serial host multi-word write



Consecutive writes to the DMA data register are written to the DMA data register with no address increment.

Figure 19. Serial host multi-word write DMA data



4.7 Host reads

The Host reads from a 16-bit register by sending a 16 bit Address phase with A15 set to one. The Address phase is followed by a 16-bit data phase. D15 is the first bit of data phase and D0 is the last bit of the data phase. Data is available on SPI_DOUT.

Any register may be accessed during Sleep mode. However, the usual synchronization mechanism for ARM or Shared clock domain registers is bypassed in Sleep mode. Read data is unpredictable if the ARM writes to the ARM or Shared clock domain register during a Sleep Mode read by the Host.

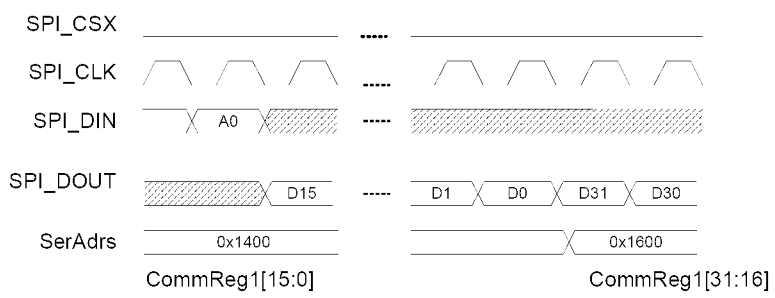
The SPI_CLK may stop at any time. The current phase (address or data) is not interrupted by a stopped (or slowed) SPI_CLK. The logic remains in the current phase until SPI_CLK resumes or SPI_CSX is de-asserted. If less than 16-bits are read by the host during a data phase to any register except the DMA Data register there is no effect on the internal state of the registers. If less than 16-bits are read by the host during a data phase to the DMA Data register the contents of subsequent DMA read accesses are unpredictable until the DMA is disabled and restarted.

4.8 Host multi-word reads

The Host may read from multiple consecutive 16-bit registers by keeping SPI_CSX asserted and continuing to toggle SPI_CLK after the initial 16-bit data phase has completed.

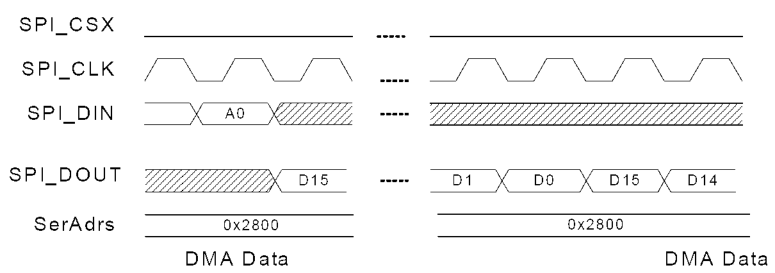
The register address is incremented by 2 at the end of each data phase for all register address except the DMA data register.

Figure 20. Serial host multi-word read



Consecutive reads from the DMA data register are read from the DMA data register with no address increment.

Figure 21. Serial host multi-word read DMA data



4.9 ARM AHB slave access

The ARM accesses the registers of the Serial Host via the AHB slave interface. lists the registers that are implemented. Host only registers are listed for convenience only.

Table 6. ARM register

ARM		Register	
Offset	**Access**	**Description**	**Reference**
0x00	R	ARM Interrupt [31:0]	ARMInt
0x04	W	ARM Interrupt Acknowledge [31:0]	ARMIntAck
0x08	RW	ARM Interrupt Enable [31:0]	ARMIntEn
0x10	RW	Host Interrupt [31:0]	HostInt
0x18	R	Host Interrupt Enable [31:0]	HostIntEn
-	-	Host Interrupt Acknowledge [31:0]	--
0X20	RW	GP1 Communication [31:0]	GP1Com
0x24	RW	GP2 Communication [31:0]	GP2Com
-	-	Device Control/Status [31:0]	--
-	-	DMA Data	--
0x40	RW	DMA Write Control	DMAWriteControl
0x44	RW	DMA Write Length	DMAWriteLength
0x48	RW	DMA Write Base	DMAWriteBase
0x50	RW	DMA Read Control	DMAReadControl
0x54	RW	DMA Read Length	DMAReadLength
0x58	RW	DMA Read Base	DMAReadBase

5 Registers description

5.1 ARM interrupt register

The HOSTMSG bits of this register are written by the Host and generate interrupts to the ARM processor when the corresponding bit is set in the ARM Interrupt Enable register. Writing a logic 1 causes the corresponding interrupt bit to be set. All other bits are unaffected; previously set bits will remain set. This register can be read/written while the device is in sleep Mode (i.e. running off the low frequency oscillator) and not generate an ARM_asleep interrupt.

Note: Both the ARM and Host Interrupt Register have the bit "ARM_ASLEEP". Although only the host generates this bit it is used as an interrupt source to both. When the Host sees this interrupt, it is expected that it will poll the device control/status Register until the SleepMode status bit is de-asserted by ARM before continuing.

The format of the register is defined in *Table 7*.

Table 7. ARM interrupt register

Bit position	Name	Description
31	ARM_ASLEEP	Indicates that an access to hardware registers or device memory (by Host) was attempted while the device was in sleep-mode.
30	DMA wr done	Last Write Occurred
29	DMA rd done	Last Read Occurred
28	DMA rd ready	DMA rd FIFO ready to be read
27:16	Reserved	Not Implemented
15:0	HOSTMSG	General purpose Host Message Interrupts. May be written by the Host to cause an interrupt to the ARM Processor.

5.2 ARM interrupt acknowledge

This register is written by the ARM processor and clears bits in the ARM interrupt register. Writing a logic 1 in any bit position causes the corresponding interrupt bit to be cleared. All other bits are unaffected.

The format of the register is defined in *Table 8*.

Table 8. ARM interrupt acknowledge

Bit position	Name	Description
31	ARM_ASLEEP	Indicates that an access to hardware registers or device memory (by Host) was attempted while the device was in sleep-mode.
30	DMA wr done	Last Write Occurred
29	DMA rd done	Last Read Occurred
28	DMA rd ready	DMA rd FIFO ready to be read

Table 8. ARM interrupt acknowledge (continued)

Bit position	Name	Description
27:16	Reserved	Not Implemented
15:0	HOSTMSG	General purpose Host Message Interrupts. May be written by the Host to cause an interrupt to the ARM processor.

5.3 ARM interrupt enable

The ARM processor writes this register, and enables interrupts from the ARM interrupt register. An interrupt is generated when corresponding bits in both the ARM interrupt register and the ARM interrupt enable register are both logic 1.

The format of the register is defined in *Table 9*.

Table 9. ARM interrupt enable

Bit position	Name	Description
31	ARM_ASLEEP	Indicates that an access to hardware registers or device memory (by Host) was attempted while the device was in sleep-mode.
30	DMA WR done	Last Write Occurred
29	DMA RD done	Last Read Occurred
28	DMA RD ready	DMA rd FIFO ready to be read
27:16	Reserved	Not Implemented
15:0	HOSTMSG	General purpose Host Message Interrupts. Written by the ARM to enable Interrupt on selected bit(s)

5.4 Host interrupt register

The bits of this register reflect the Host interrupt register with the masking by the host interrupt enable register. This register can be written or read while the device is in sleep mode (for example, running off the low frequency oscillator) and not generate an ARM_asleep interrupt.

The format of the register is defined in *Table 10*.

Table 10. Host interrupt register

Bit position	Name	Description
31	ARM_ASLEEP	Indicates that an access to hardware registers or device memory (by Host) was attempted while the device was in sleep-mode.
30	DMA wr done	Last Write Occurred
29	DMA rd done	Last Read Occurred
28	DMA rd ready	DMA rd FIFO ready to be read
27	NotSleep	Not Implemented

Table 10. Host interrupt register

Bit position	Name	Description
26:16	Reserved	Not Implemented
15:0	ARMMSG	General purpose Host Message Interrupts. Written by the ARM to enable Interrupt on selected bit(s)

5.5 Host interrupt enable register

The Host writes this 32-bit register to enable interrupts from the host interrupt register. A Host interrupt is generated if the corresponding bit in both the host interrupt register and the host interrupt enable register are both active.

The format of the register is defined in *Table 11*.

Table 11. Host interrupt enable register

Bit position	Name	Description
31	ARM_ASLEEP	Indicates that an access to hardware registers or device memory (by Host) was attempted while the device was in sleep-mode.
30	DMA wr done	
29	DMA rd done	
28	DMA rd ready	
27	NotSleep	
26:16	Reserved	Not Implemented
15:0	HOSTMSG	General purpose ARM Message Interrupts. Written by the ARM to cause an interrupt to the HOST

5.6 Host interrupt acknowledge register

This 32-bit register is written by the Host, and clears interrupts in the Host Interrupt Register. Writing a logic 1 in any bit position cause the corresponding interrupt bit to be cleared. All other bits are unaffected.

The format of the register is defined in *Table 12*.

Table 12. Host interrupt acknowledge register

Bit position	Name	Description
31	ARM_ASLEEP	Indicates that an access to hardware registers or device memory (by Host) was attempted while the device was in sleep-mode.
30	DMA WR done	Last write occurred
29	DMA RD done	Last read occurred
28	DMA RD ready	DMA RD FIFO ready to be read

Table 12. Host interrupt acknowledge register

Bit position	Name	Description
27:16	Reserved	Not implemented
15:0	HOSTMSG	General purpose host message interrupts. Written by the ARM to enable Interrupt on selected bit(s)

5.7 General purpose 1 and 2 communication registers

These 32-bit general-purpose register can be written or read by either the Host or the ARM processor.

5.8 Device control/status register

The device control/status register is used by the Host to configure the device by writing to bits 31:27. The status of the device is visible to the Host by reading bits 22:6.

The contents of the register are defined in *Table 13*.

Table 13. Device control/status register

Bit number	Name	Description
31	SetHostOverride	When set, tells processor to use boot options set by bits 30 and 29 and override boot strapping options after reset.
30	SetStartHalted	When bit 31 is set, this bit forces CPU to remain idle when reset is de-asserted. (Read/Write)
29	SetRAMBoot	When bit 31 is set, processor boots from RAM. Over-rides TMSEL strapping options (Read/Write)
28	SetHostReset	When set, produces an active high(1) reset level to the ARM (Read/Write) Must be cleared to de-assert(0) reset.
27	SetHostCPUEn	Enables processor after StartHalted has been asserted. (Read/Write)
26:23	Reserved	Not Implemented
22	StartHalted	Indicates that the processor clock was stopped after the previous reset. (Read Only)
21	RestartAsserted	Indicates that OSC Restart is asserted. (Read Only)
20	Reserved	Not Implemented
19	SoftRes	Soft Reset flag - A logic 1 indicates that the previous reset was generated by a write to the PMU system control register bit 0.
18	RTCRes	RTC Reset flag - A logic 1 indicates that the previous reset was generated by the Real Time Clock.
17	HardRes	Hard Reset flag - A logic 1 indicates that the previous reset was generated by asserting the RESET_N pin.

Table 13. Device control/status register

Bit number	Name	Description
16	HostRes	Host Reset flag - A logic 1 indicates that the previous reset was generated by the Host asserting the HostReset bit in this register.
15	SleepMode	SleepMode flag - A logic 1 indicates that the device is in Sleep Mode, i.e. running off the low frequency oscillator. (Read Only)
14:6	ClockDivisor	The clock divisor setting on the PMU clock control register (Read Only)
5	Reserved	Not Implemented
4	UseSerHostOverRide	When asserted, SerHost mode is updated by bits 3:0 1 = Update SerHost mode based on bits 3:0 0 = No change to SerHost mode
3	Host_3_WireAdrDataWait	Number of wait states between Address and Data phase in 3_Wire mode 0 = Zero wait states between Address and Data phase in 3_Wire mode 1 = One wait state between Address and Data phase in 3_Wire mode Read value is currently selected 3_ WireAdrDataWait. May be different that last written value when UseSerHostOverRide is deasserted.
2	Host_3_WireMode	Select 3 wire mode using SPI_DIN for Serial data input and output 0 = Use 4 wire mode, SPI_DIN input only and SPI_DOUT output only 1 = Use 3 wire mode, SPI_DIN for input and output Read value is currently selected 3_ WireMode. May be different that last written value when UseSerHostOverRide is deasserted
1	Host_PhaseShift	Shift SPI_DIN and SPI_DOUT by 1 clock phase 0 = No phase shift 1 = Phase shift SPI_DIN and SPI_DOUT by 1 clock phase Read value is currently selected PhaseShift. May be different that last written value when UseSerHostOverRide is deasserted
0	Host_InvertClock	Select active edge of SPI_CLK 0 = Rising edge of SPI_CLK is active edge 1 = Falling edge of SPI_CLK is active edge Read value is currently selected InvertClock. May be different that last written value when UseSerHostOverRide is deasserted

5.9 DMA data register

The data register allows the Host to read data directly from the RAM, or to write data directly into the RAM. The Read address is post incremented by 2 after each read.

The read length is decremented by 2 after each read.

Data is prefetched into the DMA data register when the DMA Read Address is written (if the DMA Write Enable bit is set). The Write address is post incremented by 2 after each write. The Write Length is decremented by 2 after each write.

It is possible to intermix Reads and Writes to the DMA Data register if the both DMA Read and Write channels are enabled.

The format of the register is defined in *Table 15*.

Table 14. DMA write control register

Bit number	Name	Description
15:0	Data	Data
DMA Data Register		

5.10 DMA write control register

The DMA write control register allows the ARM or the Host to enable the DMA write channel. Both ARM and Host are also able to control when 32-bit APB access are utilized. Only the ARM can modify the HostAllowed bit. When the HostAllowed bit is de-asserted the Host is not allowed to write the DMA Write Control, Length or Base registers.

Only bits 15:0 are accessible by the Host.

The format of the register is defined in *Table 15*.

Table 15. DMA write control register

Bit number	Name	Description
31:8	Reserved	
7	HostAllowed	When bit is set, the Host is allowed to write to DMA write control, length and base registers. HostAllowed bit is only writable by the ARM. HostAllowed default value is '1'. '0' = Host not Allowed to write Control, Length and Base registers. '1' = Host IS Allowed to write Control, Length and Base registers.
6:4	Reserved	
3	ApbAccess	Bit must be asserted when DMA is used to write APB registers. '0' = Access is not to APB register '1' = Access is to APB register
2:1	Reserved	
0	Enable	Specifies the access direction

5.11 DMA write length register

This 16 bit register is programmed with the maximum byte count of the next DMA Write transfer. Only the low-order 16 bits are used. The value programmed can be any number of bytes from 1 to 65535.

The format of the register is defined in *Table 16*.

Table 16. DMA write length register

Bit number	Name	Description
31:16	Reserved	
15:0	Data length	Maximum byte count

5.12 DMA write base address register

The DMA Write Base Address is written to point to the first location for the DMA Data register write in the Devices AHB space. The address will be incremented after every Host access to the Data register. There is no restriction on the Base Address. Byte, Half-word, Word and QuadWord addresses are supported.

The format of the register is defined in *Table 17*.

Table 17. DMA write base address register

Bit number	Name	Description
31:0	DMA Write Base	Address for 1st DMA write

5.13 DMA read control register

The DMA Read Control register allows the ARM or the Host to enable the DMA Read channel. Only the ARM can modify the HostAllowed bit. When the HostAllowed bit is de-asserted the Host is not allowed to write the DMA Read Control, Length or Base registers.

Only bits 15:0 are accessible by the Host.

The format of the register is defined in *Table 18*.

Table 18. DMA read control register

Bit number	Name	Description
31:8	Reserved	
7	HostAllowed	When bit is set, the Host is allowed to write to DMA Read Control, Length and Base registers. HostAllowed bit is only writable by the ARM. HostAllowed default value is '1'. '0' = Host not Allowed to write Control, Length and Base registers. '1' = Host IS Allowed to write Control, Length and Base registers.
6:1	Reserved	
0	Enable	Specifies the access direction

5.14 DMA read length register

This 16 bit register is programmed with the maximum byte count of the next DMA Read transfer. Only the low-order 16 bits are used. The value programmed can be any number of bytes from 1 to 65535. A value of '0' disables the byte count logic, causing any transfers to continue until terminated by clearing the Enable bit.

The format of the register is defined in *Table 19*.

Table 19. DMA read length register

Bit number	Name	Description
31:16	Reserved	
15:0	Data Length	Maximum byte count

5.15 DMA read base address register

The DMA read base address is written to point to the first location for the DMA Data register read in the Devices AHB space. The address will be incremented after every Host access to the Data register. There is no restriction on the Base Address. Byte, Half-word, Word and QuadWord addresses are supported.

The format of the register is defined in *Table 20*.

Table 20. DMA read length register

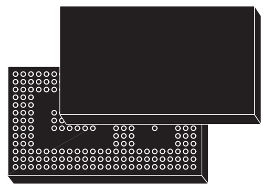
Bit number	Name	Description
31:0	DMA Read Base	Address for 1st DMA read

6 Package information

Figure 22. LFBGA228 mechanical data and package dimensions

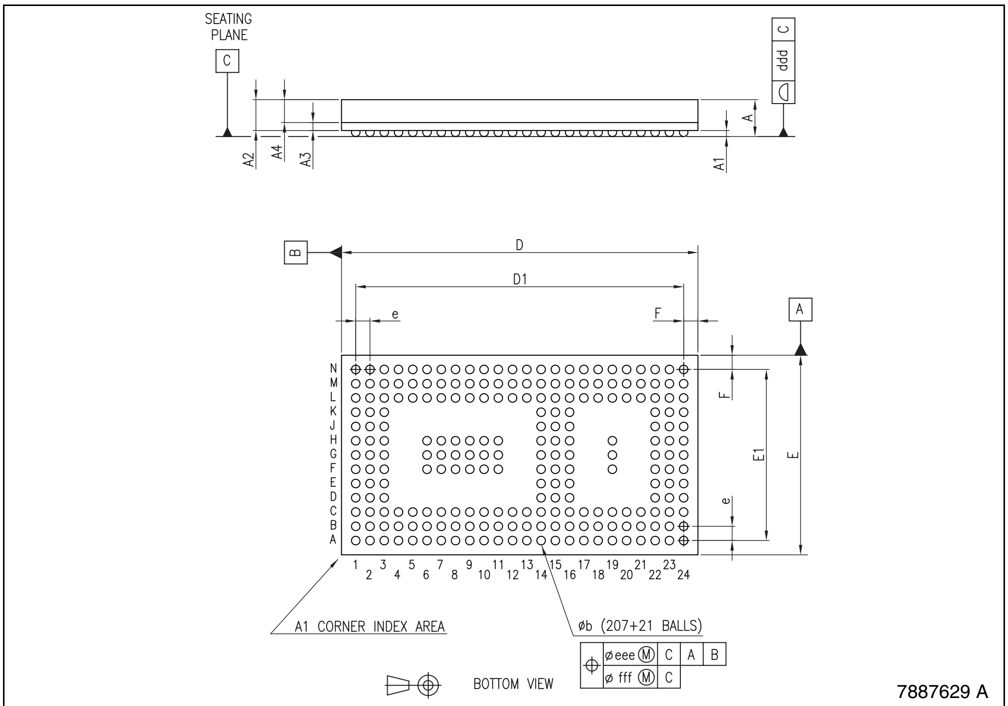
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.40			0.0551
A1	0.15			0.0059		
A2		1.065			0.0419	
A3		0.280			0.0110	
A4			0.800			0.0315
b	0.25	0.30	0.35	0.010	0.012	0.014
D	12.35	12.50	12.65	0.486	0.492	0.498
D1		11.50			0.453	
E	6.85	7.00	7.15	0.270	0.275	0.281
E1		6.00			0.236	
e		0.50			0.020	
F		0.50			0.020	
ddd			0.08			0.003
eee			0.15			0.006
fff			0.05			0.002

OUTLINE AND MECHANICAL DATA



Body: 12.5 x 7 x 1.4mm

LFBGA228 (207+21)
Low **P**rofile **B**all **G**rid **A**rray



Revision history

Table 21. Revision history

Date	Revision	Changes
05-Mar-2006	1	Initial release.