



PROGRAMMABLE OUTPUT POWER FACTOR PREREGULATOR

FEATURES

- Controls Boost Preregulator to Near-Unity Power Factor
- World Wide Line Operation
- Over-Voltage Protection
- Accurate Power Limiting
- Average Current Mode Control
- Improved Noise Immunity
- Improved Feed-Forward Line Regulation
- Leading Edge Modulation
- 150- μ A Typical Start-Up Current
- Low-Power BiCMOS Operation
- 10.8-V to 17-V Operation
- Programmable Output Voltage (Tracking Boost Topology)

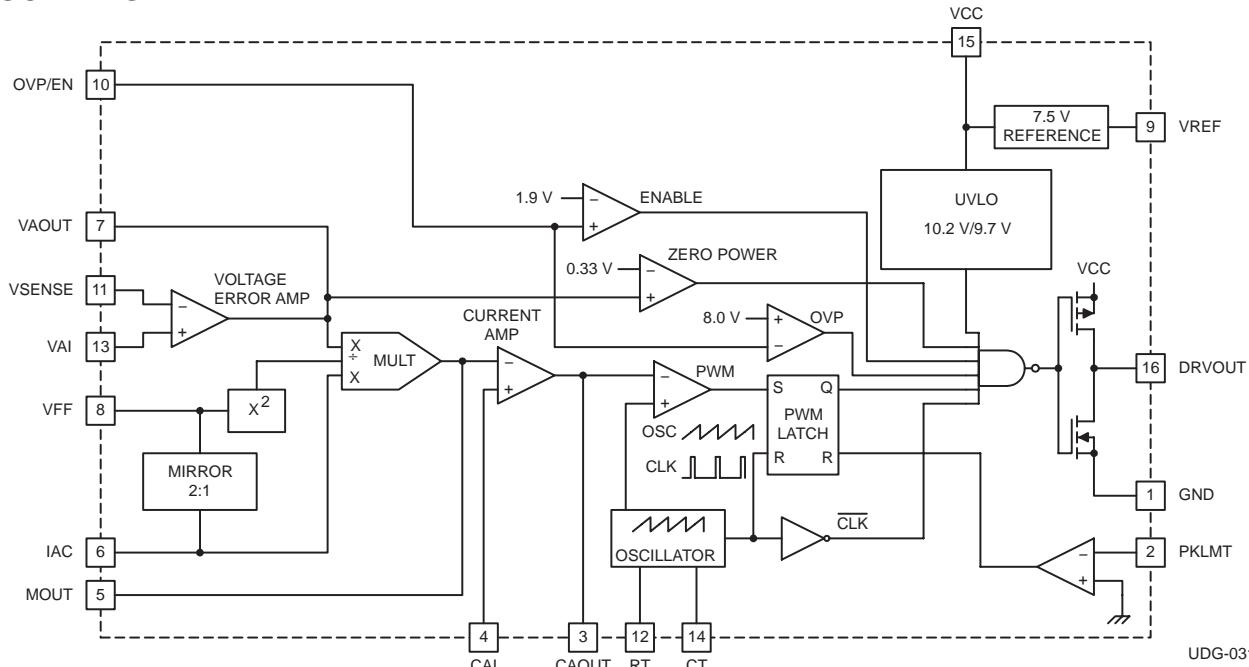
DESCRIPTION

The UCC2819A/UCC3819A provides all the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the ac-input line current waveform to correspond to that of the ac-input line voltage. Average current mode control maintains stable, low distortion sinusoidal line current.

Designed in Texas Instrument's BiCMOS process, the UCC3819A offers new features such as lower start-up current, lower power dissipation, overvoltage protection, a shunt UVLO detect circuitry and a leading-edge modulation technique to reduce ripple current in the bulk capacitor.

The UCC3819A allows the output voltage to be programmed by bringing out the error amplifier noninverting input.

BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

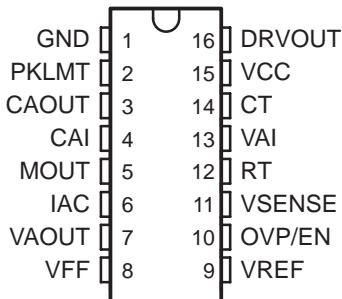
DESCRIPTION (CONTINUED)

The UCC3819A is directly pin for pin compatible with the UCC3819. Only the output stage of UCC3819A has been modified to allow use of a smaller external gate drive resistor values. For some power supply designs where an adequately high enough gate drive resistor can not be used, the UCC3819A offers a more robust output stage at the cost of increasing the internal gate resistances. The gate drive of the UCC3819A remains strong at ± 1.2 A of peak current capability.

Available in the 16-pin D, N, and PW packages.

PIN CONNECTION DIAGRAM

**D, N, AND PW PACKAGES
(TOP VIEW)**



AVAILABLE OPTIONS TABLE

$T_A = T_J$	PACKAGE DEVICES		
	SOIC (D) PACKAGE ⁽¹⁾	PDIP (N) PACKAGE	TSSOP (PW) PACKAGE ⁽¹⁾
0°C to 70°C	UCC3819AD	UCC3819AN	UCC3819APW
-40°C to 85°C	UCC2819AD	UCC2819AN	UCC2819APW

NOTES: (1) The D and PW packages are available taped and reeled. Add R suffix to the device type (e.g. UCC3819ADR) to order quantities of 2,500 devices per reel (D package) and 2,000 devices per reel (for PW package). Bulk quantities are 40 units (D package) and 90 units (PW package) per tube.

THERMAL RESISTANCE TABLE

PACKAGE	θ_{jc} (°C/W)	θ_{ja} (°C/W)
SOIC-16 (D)	22	40 to 70 ⁽¹⁾
PDIP-16 (N)	12	25 to 50 ⁽¹⁾
TSSOP-16 (PW)	14 ⁽²⁾	123 to 147 ⁽²⁾

NOTES: (1) Specified θ_{ja} (junction to ambient) is for devices mounted to 5-inch² FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 inch² aluminum PC board. Test PWB was 0.062 inch thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with a 100-mil x 100-mil probe land area at the end of each trace.
 (2) Modeled data. If value range given for θ_{ja} , lower value is for 3x3 inch. 1 oz internal copper ground plane, higher value is for 1x1-inch. ground plane. All model data assumes only one trace for each non-fused lead.

ABSOLUTE MAXIMUM RATINGSover operating free-air temperature (unless otherwise noted)[†]

	UCCx81xA	UNIT
Supply voltage VCC	18	V
Gate drive current, continuous	0.2	A
Gate drive current	1.2	
Input voltage, CAI, MOUT, SS	8	V
Input voltage, PKLMT	5	
Input voltage, VSENSE, OVP/EN, VAI	10	
Input current, RT, IAC, PKLMT	10	mA
Maximum negative voltage, DRVOUT, PKLMT, MOUT	-0.5	V
Power dissipation	1	W
Junction temperature, T_J	-55 to 150	°C
Storage temperature, T_{Stg}	-65 to 150	
Lead temperature, T_{SOL} (soldering, 10 seconds)	300	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to 70°C for the UCC3819A, -40°C to 85°C for the UCC2819A, $VCC = 12\text{ V}$, $R_T = 22\text{ k}\Omega$, $C_T = 270\text{ pF}$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current					
Supply current, off	$VCC = (\text{VCC turnon threshold} - 0.3\text{ V})$		150	300	µA
Supply current, on	$VCC = 12\text{ V}$, No load on DRVOUT	2	4	6	mA
UVLO					
VCC turnon threshold		9.7	10.2	10.8	V
VCC turnoff threshold		9.4	9.7		
UVLO hysteresis		0.3	0.5		
Voltage Amplifier					
VIO	$\text{VAOUT} = 2.75\text{ V}$, $\text{VCM} = 3.75\text{ V}$	-15		15	mV
VAI bias current	$\text{VAOUT} = 2.75\text{ V}$, $\text{VCM} = 3.75\text{ V}$		50	200	nA
VSENSE bias current	$\text{VSENSE} = \text{VREF}$, $\text{VAOUT} = 2.5\text{ V}$		50	200	
CMRR	$\text{VCM} = 1\text{ V}$ to 7.5 V	50	70		dB
Open loop gain	$\text{VAOUT} = 2\text{ V}$ to 5 V	50	90		
High-level output voltage	$\text{I}_L = -150\text{ }\mu\text{A}$	5.3	5.5	5.6	V
Low-level output voltage	$\text{I}_L = 150\text{ }\mu\text{A}$	0	50	150	mV

NOTES: 1. Ensured by design, Not production tested.
2. Reference variation for $VCC < 10.8\text{ V}$ is shown in Figure 2.

ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to 70°C for the UCC3819A, -40°C to 85°C for the UCC2819A, $V_{CC} = 12\text{ V}$, $R_T = 22\text{ k}\Omega$, $C_T = 270\text{ pF}$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Over Voltage Protection and Enable					
Over voltage reference		V _{REF} +0.48	V _{REF} +0.50	V _{REF} +0.52	V
Hysteresis		300	500	600	mV
Enable threshold		1.7	1.9	2.1	V
Enable hysteresis		0.1	0.2	0.3	
Current Amplifier					
Input offset voltage	$V_{CM} = 0\text{ V}$, $V_{CAOUT} = 3\text{ V}$	-3.5	0	2.5	mV
Input bias current	$V_{CM} = 0\text{ V}$, $V_{CAOUT} = 3\text{ V}$		-50	-100	nA
Input offset current	$V_{CM} = 0\text{ V}$, $V_{CAOUT} = 3\text{ V}$		25	100	
Open loop gain	$V_{CM} = 0\text{ V}$, $V_{CAOUT} = 2\text{ V}$ to 5 V	90			dB
Common-mode rejection ratio	$V_{CM} = 0\text{ V}$ to 1.5 V , $V_{CAOUT} = 3\text{ V}$	60	80		
High-level output voltage	$I_L = -120\text{ }\mu\text{A}$	5.6	6.5	6.8	V
Low-level output voltage	$I_L = 1\text{ mA}$	0.1	0.2	0.5	
Gain bandwidth product	See Note 1		2.5		MHz
Voltage Reference					
Input voltage, (UCC3819A)	$T_A = 0^\circ\text{C}$ to 70°C	7.387	7.5	7.613	V
Input voltage, (UCC2819A)	$T_A = -40^\circ\text{C}$ to 85°C	7.369	7.5	7.631	
Load regulation	$I_{REF} = 1\text{ mA}$ to 2 mA	0		10	mV
Line regulation	$V_{CC} = 10.8\text{ V}$ to 15 V , See Note 2	0		10	
Short-circuit current	$V_{REF} = 0\text{ V}$	-20	-25	-50	mA
Oscillator					
Initial accuracy	$T_A = 25^\circ\text{C}$	85	100	115	kHz
Voltage stability	$V_{CC} = 10.8\text{ V}$ to 15 V	-1%		1%	
Total variation	Line, temp, See Note 1	80		120	kHz
Ramp peak voltage		4.5	5	5.5	V
Ramp amplitude voltage (peak to peak)		3.5	4	4.5	
Peak Current Limit					
PKLMT reference voltage		-15		15	mV
PKLMT propagation delay		150	350	500	ns

NOTES: (1) Ensured by design, Not production tested.

(2) Reference variation for $V_{CC} < 10.8\text{ V}$ is shown in Figure 2.

ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to 70°C for the UCC3819A, -40°C to 85°C for the UCC2819A, $V_{CC} = 12\text{ V}$, $R_T = 22\text{ k}\Omega$, $C_T = 270\text{ pF}$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Multiplier					
I_{MOUT} , high line, low power output current, (0°C to 85°C)	$I_{AC} = 500\text{ }\mu\text{A}$, $V_{FF} = 4.7\text{ V}$, $VA_{OUT} = 1.25\text{ V}$	0	-6	-20	μA
I_{MOUT} , high line, low power output current, (-40°C to 85°C)	$I_{AC} = 500\text{ }\mu\text{A}$, $V_{FF} = 4.7\text{ V}$, $VA_{OUT} = 1.25\text{ V}$	0		-23	
I_{MOUT} , high line, high power output current	$I_{AC} = 500\text{ }\mu\text{A}$, $V_{FF} = 4.7\text{ V}$, $VA_{OUT} = 5\text{ V}$	-70	-90	-105	
I_{MOUT} , low line, low power output current	$I_{AC} = 150\text{ }\mu\text{A}$, $V_{FF} = 1.4\text{ V}$, $VA_{OUT} = 1.25\text{ V}$	-10	-19	-50	
I_{MOUT} , low line, high power output current	$I_{AC} = 150\text{ }\mu\text{A}$, $V_{FF} = 1.4\text{ V}$, $VA_{OUT} = 5\text{ V}$	-268	-300	-346	
I_{MOUT} , I_{AC} limited	$I_{AC} = 150\text{ }\mu\text{A}$, $V_{FF} = 1.3\text{ V}$, $VA_{OUT} = 5\text{ V}$	-250	-300	-400	
Gain constant (K)	$I_{AC} = 300\text{ }\mu\text{A}$, $V_{FF} = 3\text{ V}$, $VA_{OUT} = 2.5\text{ V}$	0.5	1	1.5	1/V
I_{MOUT} , zero current	$I_{AC} = 150\text{ }\mu\text{A}$, $V_{FF} = 1.4\text{ V}$, $VA_{OUT} = 0.25\text{ V}$		0	-2	μA
	$I_{AC} = 500\text{ }\mu\text{A}$, $V_{FF} = 4.7\text{ V}$, $VA_{OUT} = 0.25\text{ V}$		0	-2	
I_{MOUT} , zero current, (0°C to 85°C)	$I_{AC} = 500\text{ }\mu\text{A}$, $V_{FF} = 4.7\text{ V}$, $VA_{OUT} = 0.5\text{ V}$		0	-3	
I_{MOUT} , zero current, (-40°C to 85°C)	$I_{AC} = 500\text{ }\mu\text{A}$, $V_{FF} = 4.7\text{ V}$, $VA_{OUT} = 0.5\text{ V}$		0	-3.5	
Power limit ($I_{MOUT} \times V_{FF}$)	$I_{AC} = 150\text{ }\mu\text{A}$, $V_{FF} = 1.4\text{ V}$, $VA_{OUT} = 5\text{ V}$	-375	-420	-485	μW
Feed-Forward					
VFF output current	$I_{AC} = 300\text{ }\mu\text{A}$	-140	-150	-160	μA
Gate Driver					
Pullup resistance	$I_O = -100\text{ mA}$ to -200 mA		9	12	Ω
Pulldown resistance	$I_O = 100\text{ mA}$		4	10	
Output rise time	$C_L = 1\text{ nF}$, $R_L = 10\text{ }\Omega$, $V_{DRVOUT} = 0.7\text{ V}$ to 9 V		25	50	ns
Output fall time	$C_L = 1\text{ nF}$, $R_L = 10\text{ }\Omega$, $V_{DRVOUT} = 9\text{ V}$ to 0.7 V		10	50	
Maximum duty cycle		93%	95%	100%	
Minimum controlled duty cycle	At 100 kHz			2%	
Zero Power					
Zero power comparator threshold	Measured on VA_{OUT}	0.20	0.33	0.50	V

NOTES: (1) Ensured by design, Not production tested.

(2) Reference variation for $V_{CC} < 10.8\text{ V}$ is shown in Figure 2.

PIN ASSIGNMENTS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CAI	4	I	Current amplifier noninverting input
CAOUT	3	O	Current amplifier output
CT	14	I	Oscillator timing capacitor
DRVOUT	16	O	Gate drive
GND	1	–	Ground
IAC	6	I	Current proportional to input voltage
MOUT	5	I/O	Multiplier output and current amplifier inverting input
OVP/EN	10	I	Over-voltage/enable
PKLMT	2	I	PFC peak current limit
RT	12	I	Oscillator charging current
VAI	13	I	Voltage amplifier non-inverting input
VAOUT	7	O	Voltage amplifier output
VCC	15	I	Positive supply voltage
VFF	8	I	Feed-forward voltage
VSENSE	11	I	Voltage amplifier inverting input
VREF	9	O	Voltage reference output

Pin Descriptions

CAI: Place a resistor between this pin and the GND side of current-sense resistor. This input and the inverting input (MOUT) remain functional down to and below GND.

CAOUT: This is the output of a wide bandwidth operational amplifier that senses line current and commands the PFC pulse-width modulator (PWM) to force the correct duty cycle. Compensation components are placed between CAOUT and MOUT.

CT: A capacitor from CT to GND sets the PWM oscillator frequency according to:

$$f \approx \left(\frac{0.6}{RT \times CT} \right)$$

The lead from the oscillator timing capacitor to GND should be as short and direct as possible.

DRVOUT: The output drive for the boost switch is a totem-pole MOSFET gate driver on DRVOUT. To avoid the excessive overshoot of the DRVOUT while driving a capacitive load, a series gate current-limiting/damping resistor is recommended to prevent interaction between the gate impedance and the output driver. The value of the series gate resistor is based on the pulldown resistance ($R_{pulldown}$ which is 4- Ω typical), the maximum VCC voltage (VCC), and the required maximum gate drive current (I_{max}). Using the equation below, a series gate resistance of resistance 11 Ω would be required for a maximum VCC voltage of 18 V and for 1.2 A of maximum sink current. The source current will be limited to approximately 900 mA (based on the R_{pullup} of 9- Ω typical).

$$R_{GATE} = \frac{VCC - (I_{MAX} \times R_{pulldown})}{I_{MAX}}$$

GND: All voltages measured with respect to ground. VCC and REF should be bypassed directly to GND with a 0.1- μ F or larger ceramic capacitor.

Pin Descriptions (continued)

IAC: This input to the analog multiplier is a current proportional to instantaneous line voltage. The multiplier is tailored for very low distortion from this current input (I_{IAC}) to multiplier output. The recommended maximum I_{IAC} is 500 μ A.

MOUT: The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high-impedance input so the amplifier can be configured as a differential amplifier. This configuration improves noise immunity and allows for the leading-edge modulation operation. The multiplier output current is limited to $(2 \times I_{IAC})$. The multiplier output current is given by the equation:

$$I_{MOUT} = \frac{I_{IAC} \times (V_{VAOUT} - 1)}{V_{VFF}^2 \times K}$$

where $K = \frac{1}{V}$ is the multiplier gain constant.

OVP/EN: A window comparator input that disables the output driver if the boost output voltage is a programmed level above the nominal or disables both the PFC output driver and resets SS if pulled below 1.9 V (typ).

PKLMT: The threshold for peak limit is 0 V. Use a resistor divider from the negative side of the current sense resistor to VREF to level shift this signal to a voltage level defined by the value of the sense resistor and the peak current limit. Peak current limit is reached when PKLMT voltage falls below 0 V.

RT: A resistor from RT to GND is used to program oscillator charging current. A resistor between 10 k Ω and 100 k Ω is recommended. Nominal voltage on this pin is 3 V.

VAI: This input can be tied to the VREF or any other voltage reference (≤ 7.5 V) to set the boost regulator output voltage.

VAOUT: This is the output of the operational amplifier that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5 V to prevent overshoot.

VCC: Connect to a stable source of at least 20 mA between 10 V and 17 V for normal operation. Bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate gate drive signals, the output devices are inhibited unless V_{VCC} exceeds the upper under-voltage lockout voltage threshold and remains above the lower threshold.

VFF: The RMS voltage signal generated at this pin by mirroring 1/2 of the I_{IAC} into a single pole external filter. At low line, the VFF roll should be 14 V.

VSENSE: This is normally connected to a compensation network and to the boost converter output through a divider network.

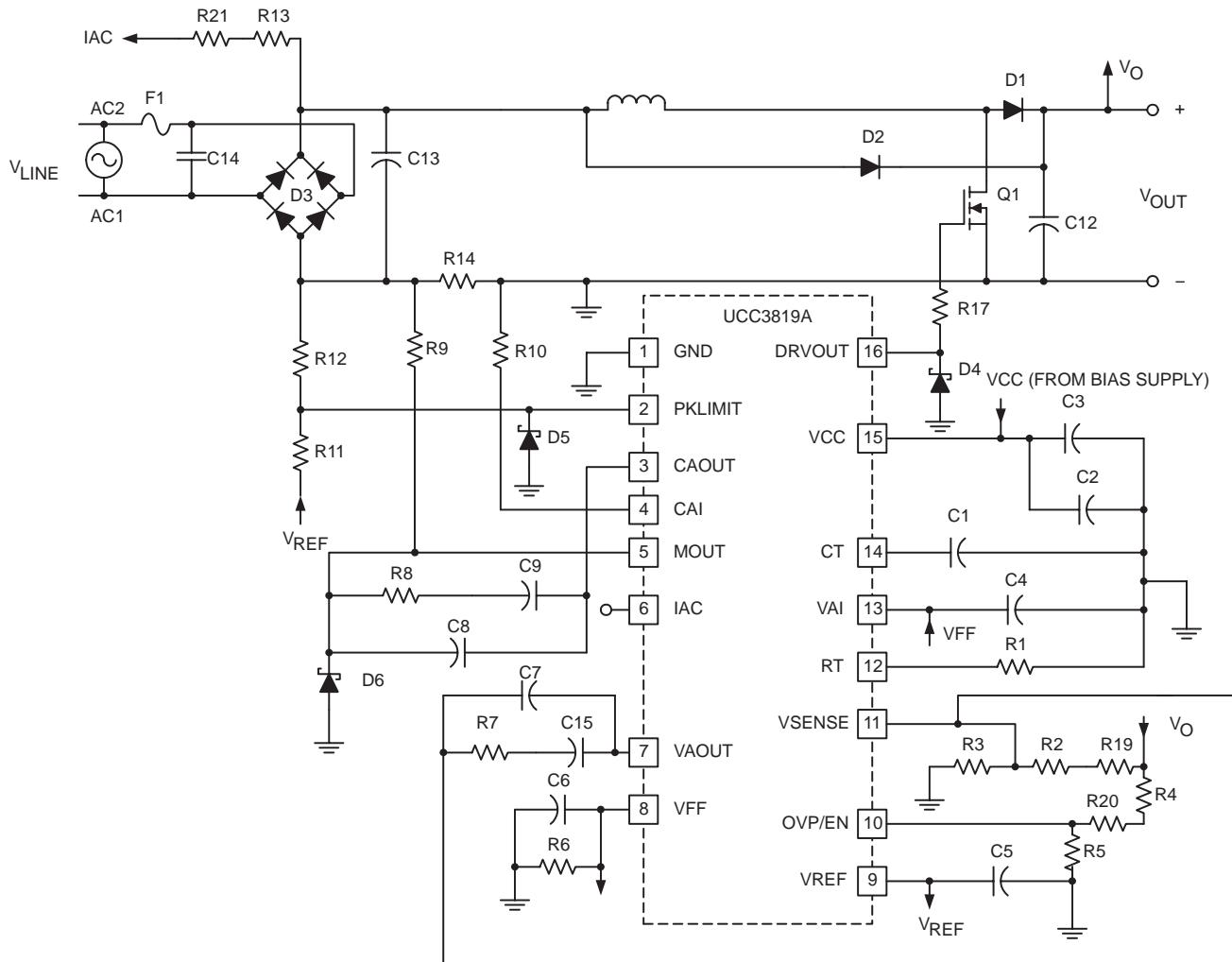
VREF: VREF is the output of an accurate 7.5-V voltage reference. This output is capable of delivering 20 mA to peripheral circuitry and is internally short-circuit current limited. VREF is disabled and remains at 0 V when V_{VCC} is below the UVLO threshold. Bypass VREF to GND with a 0.1- μ F or larger ceramic capacitor for best stability. Please refer to Figures 8 and 9 for VREF line and load regulation characteristics.

APPLICATION INFORMATION

The UCC3819A is based on the UCC3818 PFC preregulator. For a more detailed application information for this part, please refer to the UCC3818 datasheet product folder.

The main difference between the UCC3818 and the UCC3819A is that the non-inverting input of the voltage error amplifier is made available to the user through an external pin (VAI) in the UCC3819A. The SS pin and function were eliminated to accommodate this change.

The benefit of VAI pin is that it can be used to dynamically change the PFC output voltage based on the line voltage (RMS) level or other conditions. Figure 1 shows one suggested implementation of the tracking boost PFC converter as this approach is sometimes referred to. The VAI pin is tied to the VFF pin and hence output voltage scales up with the line voltage. The benefit of this approach is that at lower line voltages the output voltage is lower and that leads to smaller boost inductor value, lower MOSFET conduction losses and reduced component stresses. In order for this feature to work, the downstream converter has to operate over a wider input range.



UDG-01008

Figure 1. Suggested Implementation of UCC3819A in a Tracking Boost PFC Preregulator

APPLICATION INFORMATION

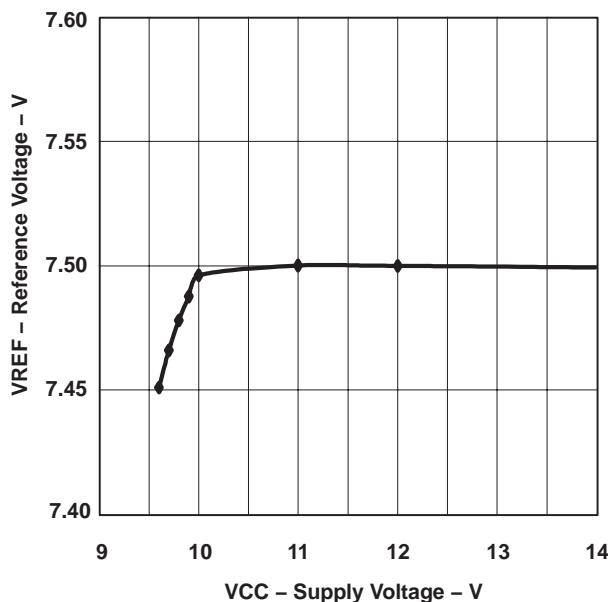
REFERENCE VOLTAGE
vs
SUPPLY VOLTAGE

Figure 2

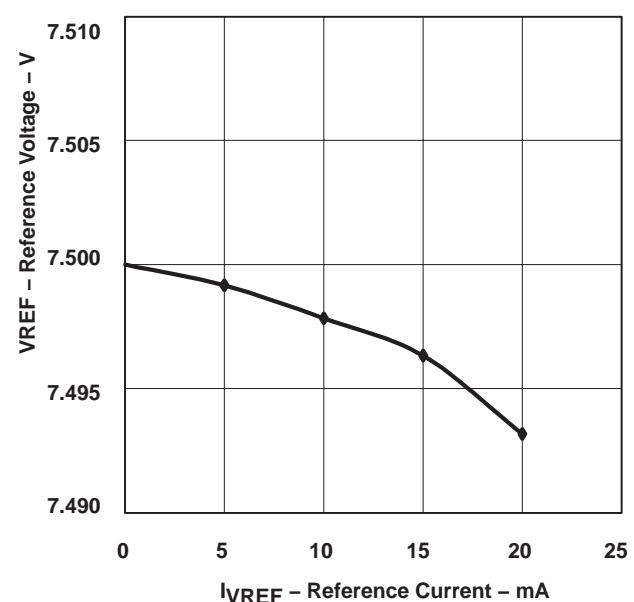
REFERENCE VOLTAGE
vs
REFERENCE CURRENT

Figure 3

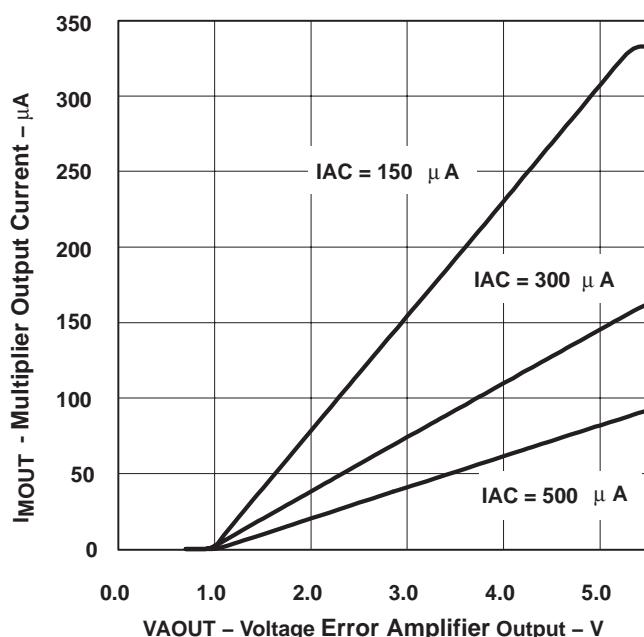
MULTIPLIER OUTPUT CURRENT
vs
VOLTAGE ERROR AMPLIFIER OUTPUT

Figure 4

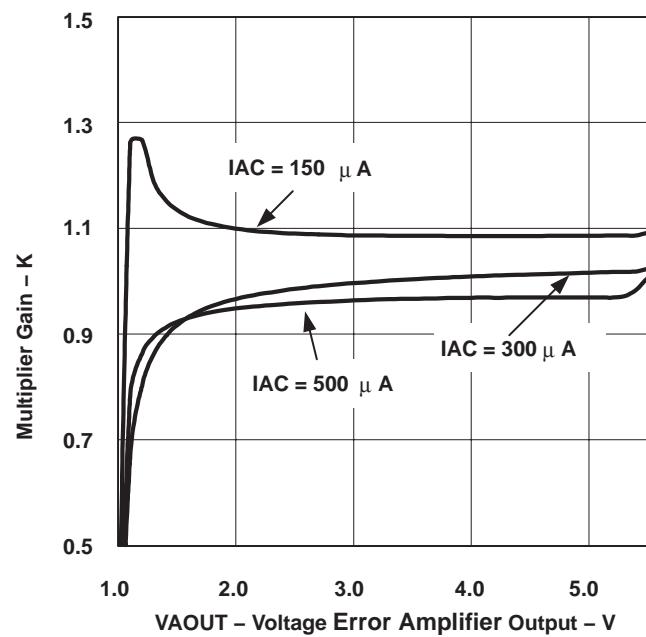
MULTIPLIER GAIN
vs
VOLTAGE ERROR AMPLIFIER OUTPUT

Figure 5

APPLICATION INFORMATION

MULTIPLIER CONSTANT POWER PERFORMANCE

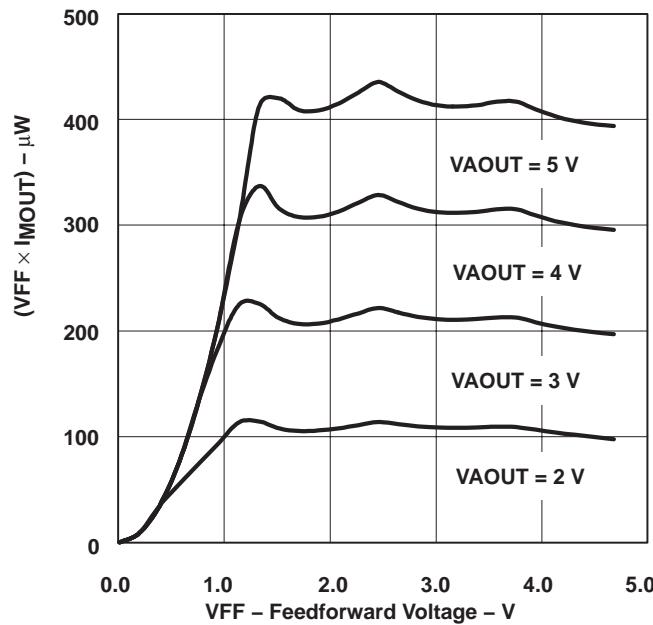


Figure 6

References and Resources:

Application Note: *Differences Between UCC3817A/18A/19A and UCC3817/18/19*, Texas Instruments Literature Number SLUA294

User's Guide: *UCC3817 BiCMOS Power Factor Preregulator Evaluation Board*, Texas Instruments Literature Number SLUU077

Application Note: *Synchronizing a PFC Controller from a Down Stream Controller Gate Drive*, Texas Instruments Literature Number SLUA245

Seminar topic: *High Power Factor Switching Preregulator Design Optimization*, L.H. Dixon, SEM-700, 1990.

Seminar topic: *High Power Factor Preregulator for Off-line Supplies*, L.H. Dixon, SEM-600, 1988.

Related Products

DEVICE	DESCRIPTION	CONTROL METHOD	TYPICAL POWER LEVEL
UCC3817/A,18/A	BiCMOS PFC controller	ACM(2)	75 W to 2 kW+
UC3854	PFC controller	ACM(2)	200 W to 2 kW+
UC3854A/B	Improved PFC controller	ACM(2)	200 W to 2 kW+
UC3855A/B	High performance soft switching PFC controller	ACM(2)	400 W to 2 kW+
UCC38050/1	Transition mode PFC controller	CRM(1)	50 W to 400 W
UCC28510/11/12/13	Advanced PFC+PWM combo controller	ACM(2)	75 W to 1kW+
UCC28514/15/16/17	Advanced PFC+PWM combo controller	ACM(2)	75 W to 1kW+

NOTES: (1). Critical conduction mode

(2). Average current mode

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2819AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2819AD	Samples
UCC2819ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2819AD	Samples
UCC2819ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2819AD	Samples
UCC2819ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2819AD	Samples
UCC2819APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2819A	Samples
UCC2819APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2819A	Samples
UCC2819APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2819A	Samples
UCC2819APWRG4	ACTIVE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85		Samples
UCC3819AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3819AD	Samples
UCC3819ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3819AD	Samples
UCC3819ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3819AD	Samples
UCC3819ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3819AD	Samples
UCC3819APW	OBsolete	TSSOP	PW	16		TBD	Call TI	Call TI	0 to 70	3819A	
UCC3819APWG4	OBsolete	TSSOP	PW	16		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

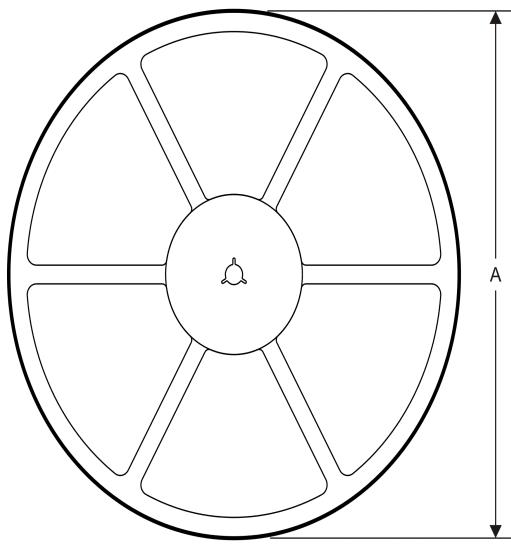
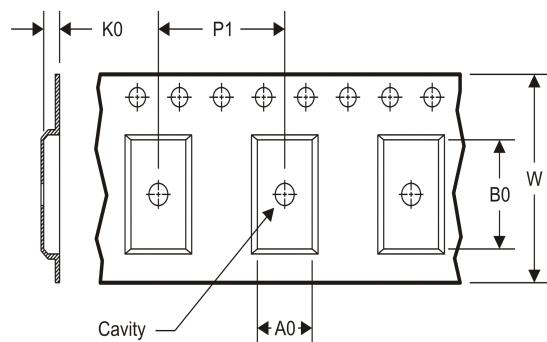
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

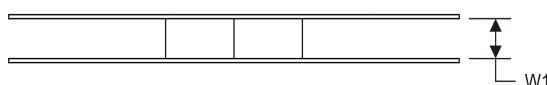
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers


TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2819ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC2819APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
UCC3819ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

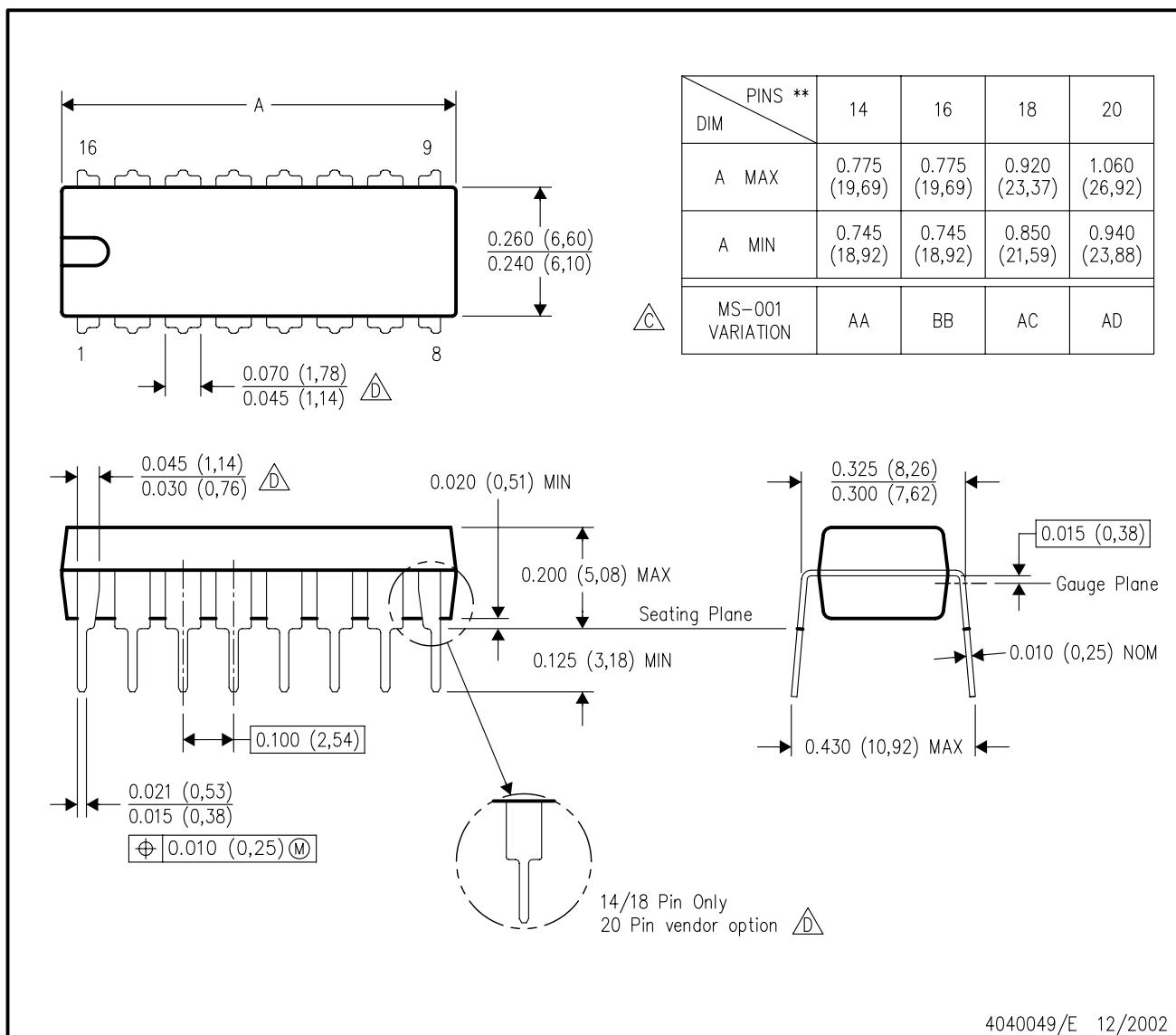

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2819ADR	SOIC	D	16	2500	333.2	345.9	28.6
UCC2819APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
UCC3819ADR	SOIC	D	16	2500	333.2	345.9	28.6

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



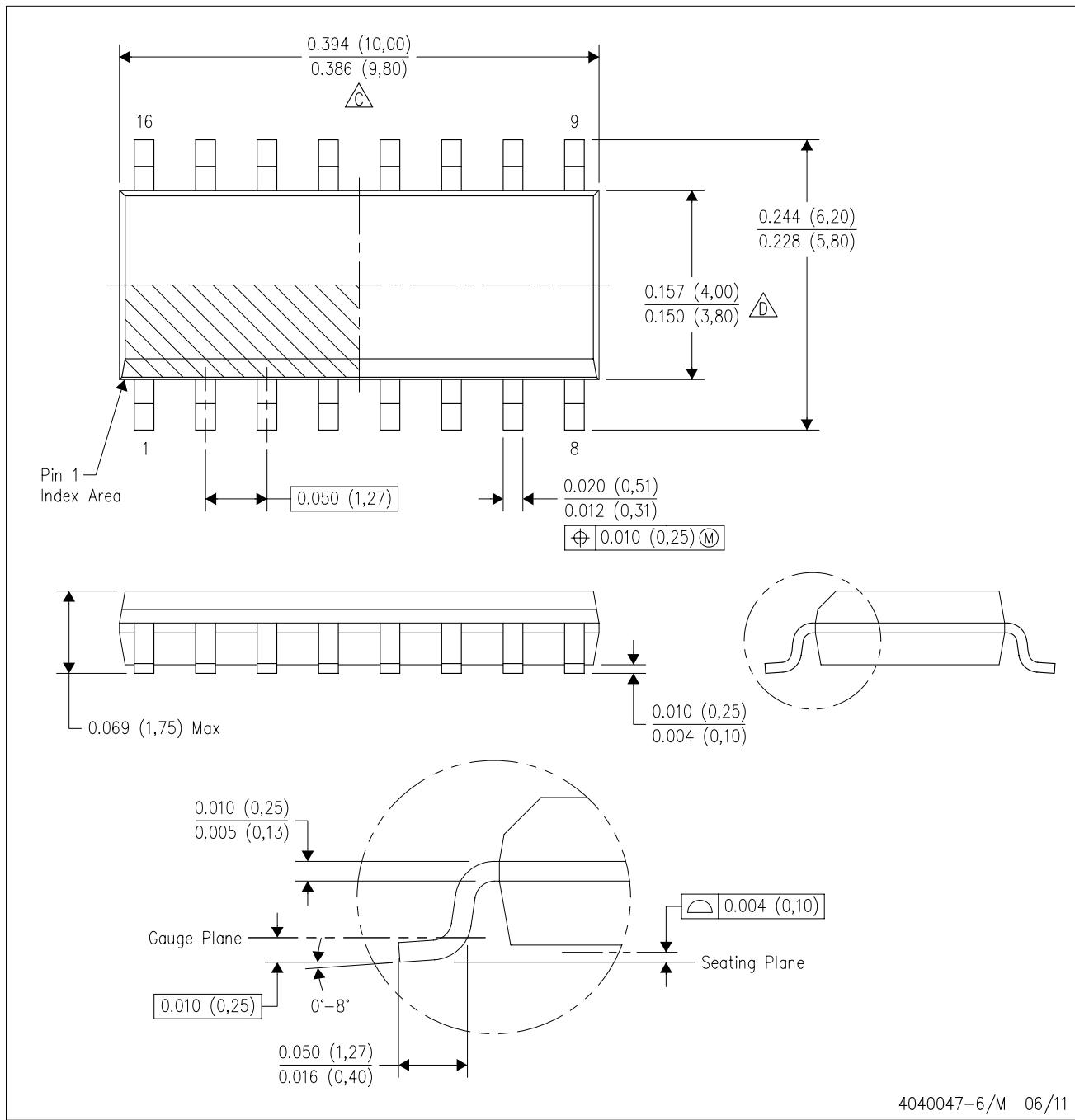
NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

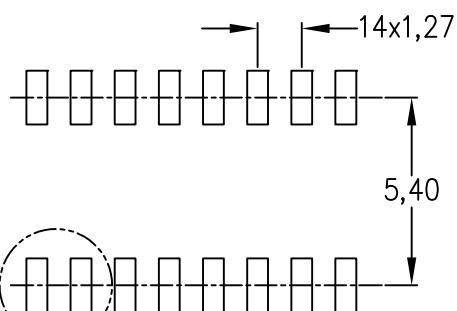
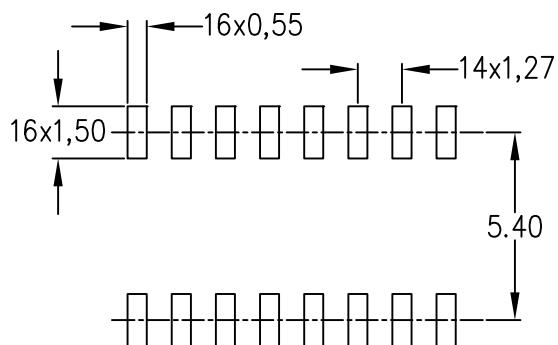
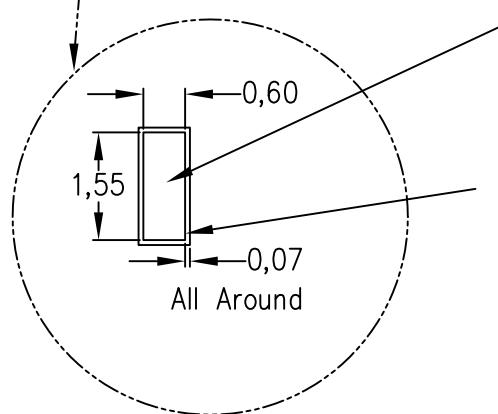
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

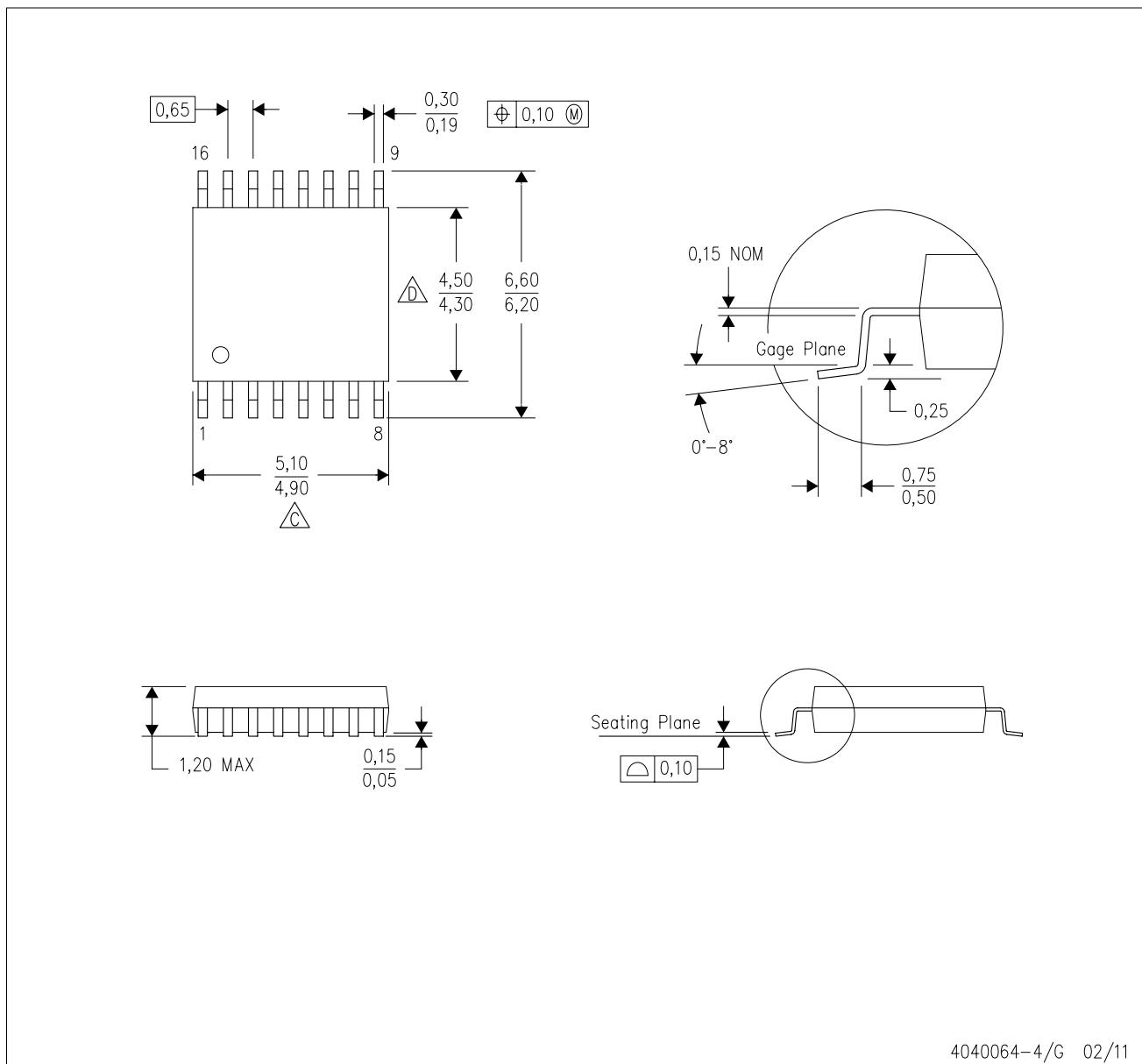
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

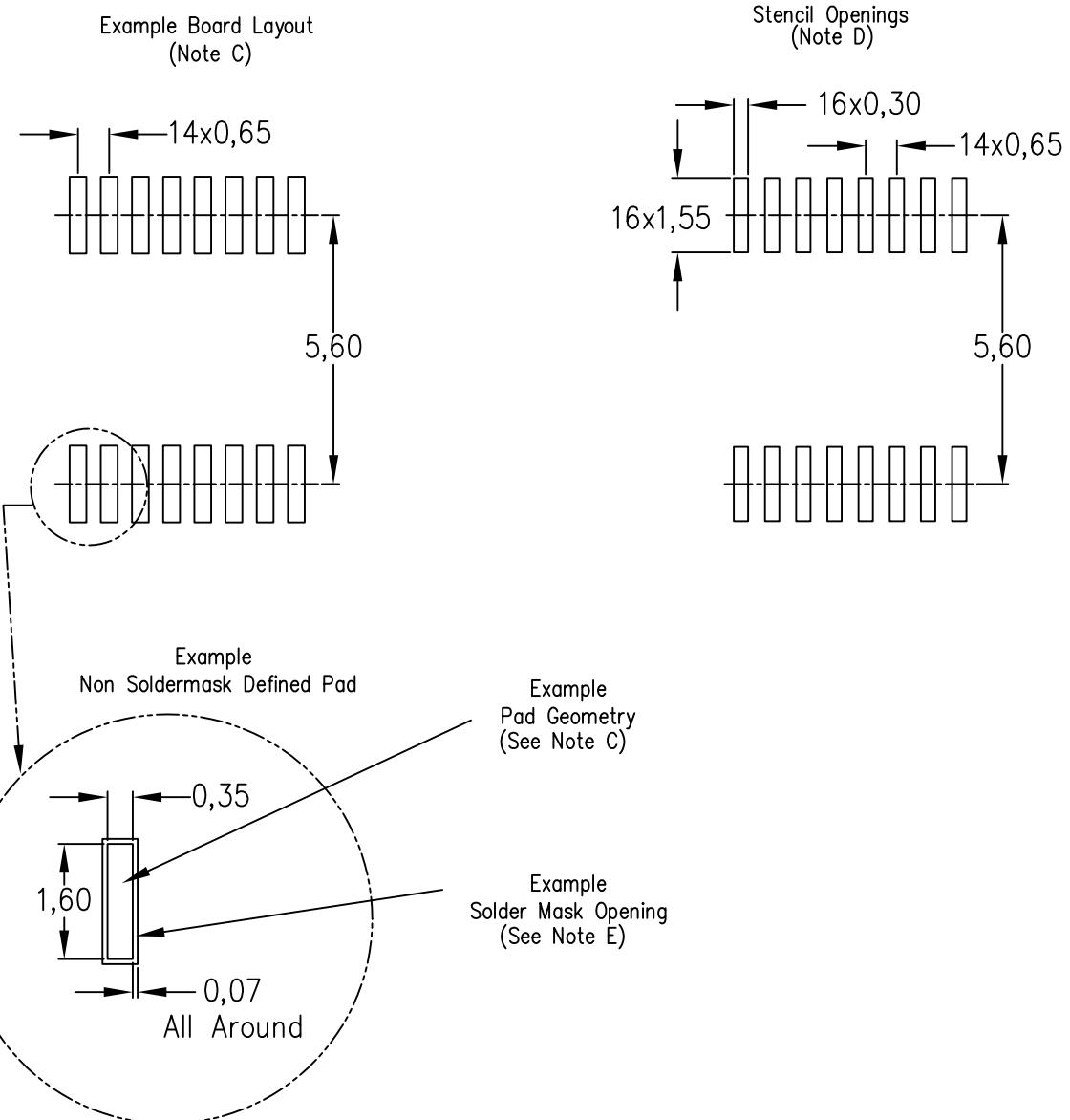
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

4040064-4/G 02/11

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity
	TI E2E Community
	e2e.ti.com