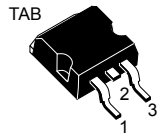
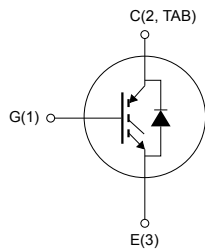


Trench gate field-stop, 650 V, 20 A, M series low-loss IGBT


D²PAK


NG1E3C2T



Features

- Maximum junction temperature: $T_J = 175\text{ }^{\circ}\text{C}$
- High short-circuit withstand time
- $V_{CE(sat)} = 1.55\text{ V (typ.) @ } I_C = 20\text{ A}$
- Tight parameters distribution
- Low thermal resistance
- Soft and very fast-recovery antiparallel diode

Applications

- Motor control
- UPS
- PFC
- General-purpose inverters

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the M series IGBTs, which represent an optimal balance between inverter system performance and efficiency where the low-loss and the short-circuit functionality is essential. Furthermore, the positive $V_{CE(sat)}$ temperature coefficient and the tight parameter distribution result in safer paralleling operation.

Product status link

[STGB20M65DF2](#)

Product summary

Order code	STGB20M65DF2
Marking	G20M65DF2
Package	D²PAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GE} = 0$)	650	V
I_C	Continuous collector current at $T_C = 25\text{ °C}$	40	A
	Continuous collector current at $T_C = 100\text{ °C}$	20	A
$I_{CP}^{(1)}$	Pulsed collector current	80	A
V_{GE}	Gate-emitter voltage	± 20	V
I_F	Continuous forward current at $T_C = 25\text{ °C}$	40	A
	Continuous forward current at $T_C = 100\text{ °C}$	20	A
$I_{FP}^{(1)}$	Pulsed forward current	80	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	166	W
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range	-55 to 175	°C

1. Pulse width limited by maximum junction temperature.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case IGBT	0.9	°C/W
R_{thJC}	Thermal resistance junction-case diode	2.08	°C/W
R_{thJA}	Thermal resistance junction-ambient	62.5	°C/W

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 3. Static characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	$V_{GE} = 0\text{ V}$, $I_C = 250\text{ }\mu\text{A}$	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}$, $I_C = 20\text{ A}$		1.55	2.0	V
		$V_{GE} = 15\text{ V}$, $I_C = 20\text{ A}$, $T_J = 125\text{ °C}$		1.95		
		$V_{GE} = 15\text{ V}$, $I_C = 20\text{ A}$, $T_J = 175\text{ °C}$		2.1		
V_F	Forward on-voltage	$I_F = 20\text{ A}$		1.85		V
		$I_F = 20\text{ A}$, $T_J = 125\text{ °C}$		1.65		
		$I_F = 20\text{ A}$, $T_J = 175\text{ °C}$		1.55		
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 500\text{ }\mu\text{A}$	5	6	7	V
I_{CES}	Collector cut-off current	$V_{GE} = 0\text{ V}$, $V_{CE} = 650\text{ V}$			25	μA
I_{GES}	Gate-emitter leakage current	$V_{CE} = 0\text{ V}$, $V_{GE} = \pm 20\text{ V}$			250	nA

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GE} = 0\text{ V}$	-	1688	-	pF
C_{oes}	Output capacitance		-	95	-	
C_{res}	Reverse transfer capacitance		-	35	-	
Q_g	Total gate charge	$V_{CC} = 520\text{ V}$, $I_C = 20\text{ A}$,	-	63	-	nC
Q_{ge}	Gate-emitter charge	$V_{GE} = 0\text{ to }15\text{ V}$	-	15	-	
Q_{gc}	Gate-collector charge	(see Figure 29. Gate charge test circuit)	-	26	-	

Table 5. IGBT switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CE} = 400\text{ V}$, $I_C = 20\text{ A}$, $V_{GE} = 15\text{ V}$, $R_G = 12\ \Omega$ (see Figure 28. Test circuit for inductive load switching)		26	-	ns
t_r	Current rise time			10.8	-	ns
$(di/dt)_{on}$	Turn-on current slope			1409	-	A/ μ s
$t_{d(off)}$	Turn-off delay time			108	-	ns
t_f	Current fall time			65	-	ns
$E_{on}^{(1)}$	Turn-on switching energy			0.14	-	mJ
$E_{off}^{(2)}$	Turn-off switching energy			0.56	-	mJ
E_{ts}	Total switching energy			0.7	-	mJ
$t_{d(on)}$	Turn-on delay time	$V_{CE} = 400\text{ V}$, $I_C = 20\text{ A}$, $V_{GE} = 15\text{ V}$, $R_G = 12\ \Omega$, $T_J = 175\text{ }^\circ\text{C}$ (see Figure 28. Test circuit for inductive load switching)		28.4	-	ns
t_r	Current rise time			11.2	-	ns
$(di/dt)_{on}$	Turn-on current slope			1393	-	A/ μ s
$t_{d(off)}$	Turn-off delay time			107	-	ns
t_f	Current fall time			145	-	ns
$E_{on}^{(1)}$	Turn-on switching energy			0.3	-	mJ
$E_{off}^{(2)}$	Turn-off switching energy			0.85	-	mJ
E_{ts}	Total switching energy			1.15	-	mJ
t_{sc}	Short-circuit withstand time	$V_{CC} = 400\text{ V}$, $V_{GE} = 13\text{ V}$, $T_{Jstart} = 150\text{ }^\circ\text{C}$	10		-	μ s
		$V_{CC} = 400\text{ V}$, $V_{GE} = 15\text{ V}$, $T_{Jstart} = 150\text{ }^\circ\text{C}$	6		-	

1. Including the reverse recovery of the diode.
2. Including the tail of the collector current.

Table 6. Diode switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	$I_F = 20\text{ A}$, $V_R = 400\text{ V}$, $V_{GE} = 15\text{ V}$, $di/dt = 1000\text{ A}/\mu\text{s}$ (see Figure 28. Test circuit for inductive load switching)	-	166		ns
Q_{rr}	Reverse recovery charge		-	690		nC
I_{rrm}	Reverse recovery current		-	13.2		A
dI_{rr}/dt	Peak rate of fall of reverse recovery current during t_b		-	769		A/ μ s
E_{rr}	Reverse recovery energy		-	81		μ J
t_{rr}	Reverse recovery time	$I_F = 20\text{ A}$, $V_R = 400\text{ V}$, $V_{GE} = 15\text{ V}$, $T_J = 175\text{ }^\circ\text{C}$, $di/dt = 1000\text{ A}/\mu\text{s}$ (see Figure 28. Test circuit for inductive load switching)	-	281		ns
Q_{rr}	Reverse recovery charge		-	2010		nC
I_{rrm}	Reverse recovery current		-	19.6		A
dI_{rr}/dt	Peak rate of fall of reverse recovery current during t_b		-	370		A/ μ s
E_{rr}	Reverse recovery energy		-	215		μ J

2.1 Electrical characteristics (curves)

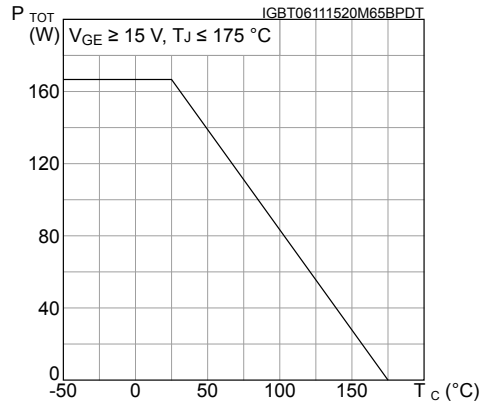
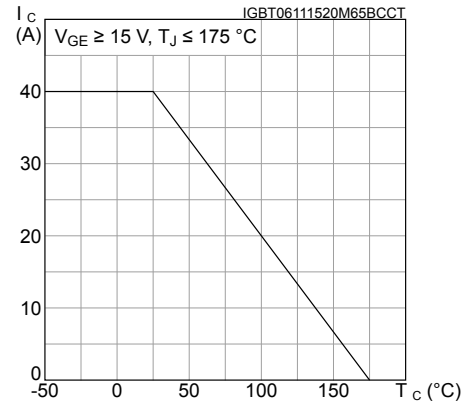
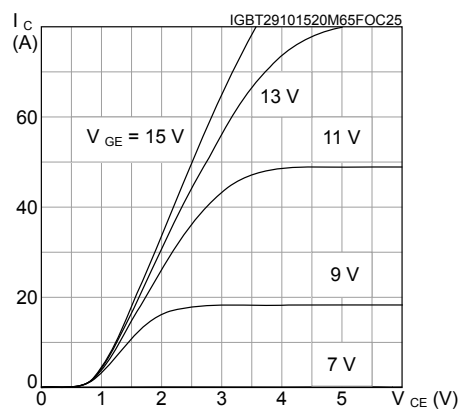
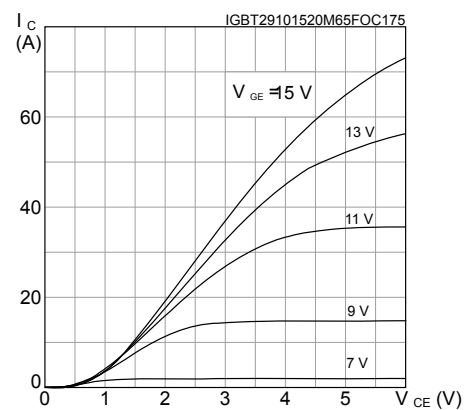
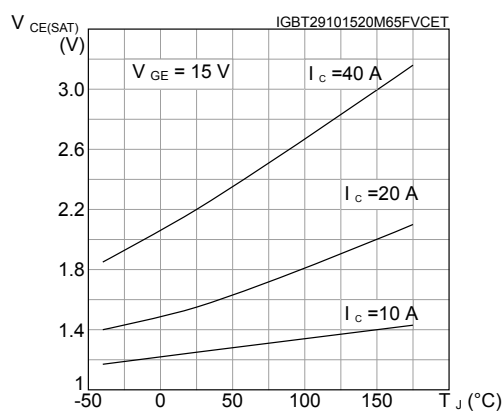
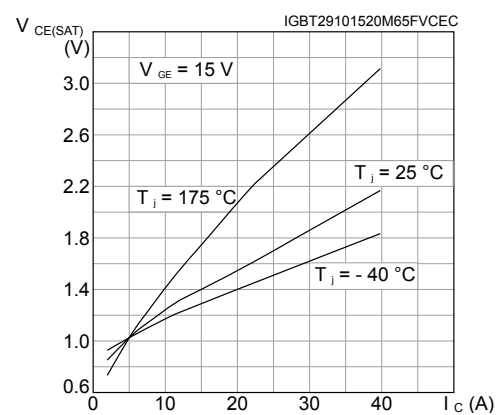
Figure 1. Power dissipation vs case temperature

Figure 2. Collector current vs case temperature

Figure 3. Output characteristics (T_J = 25 °C)

Figure 4. Output characteristics (T_J = 175 °C)

Figure 5. V_CE(sat) vs junction temperature

Figure 6. V_CE(sat) vs collector current


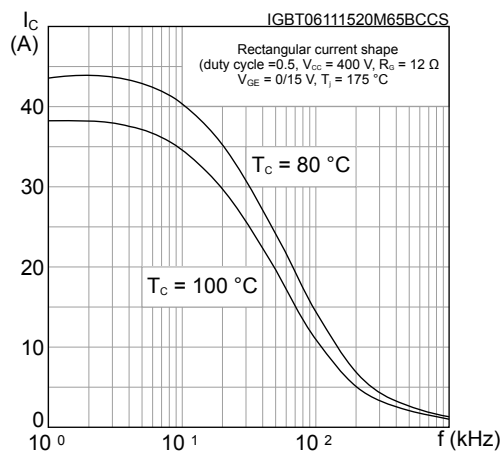
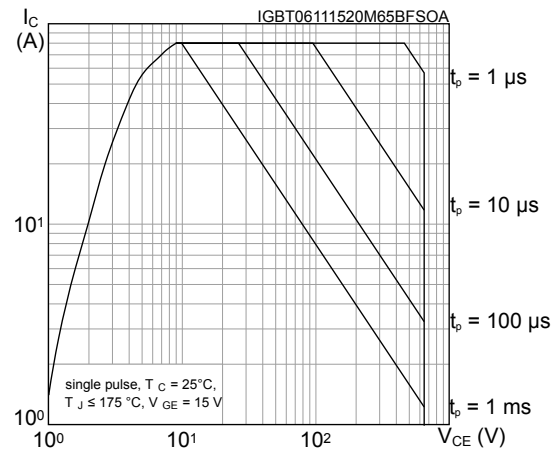
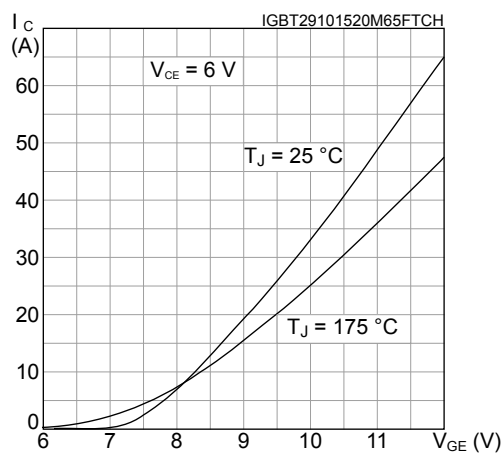
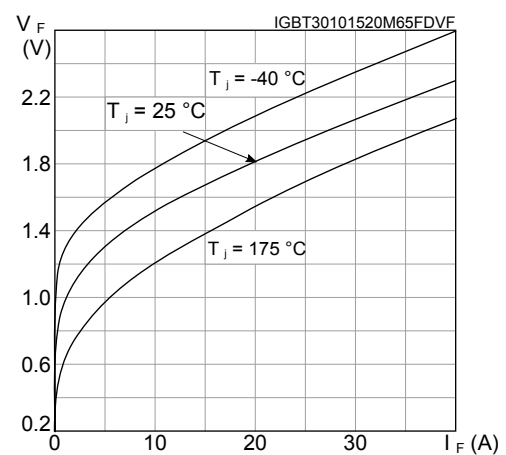
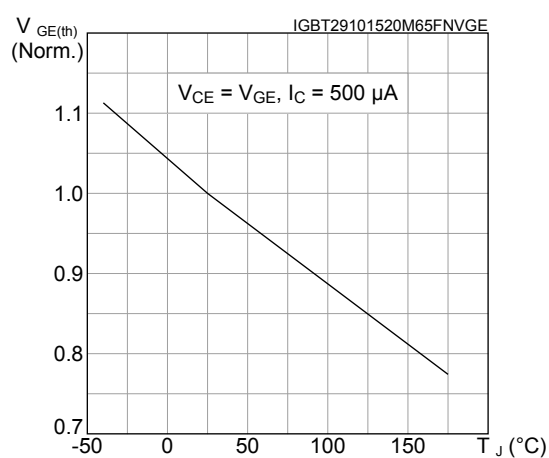
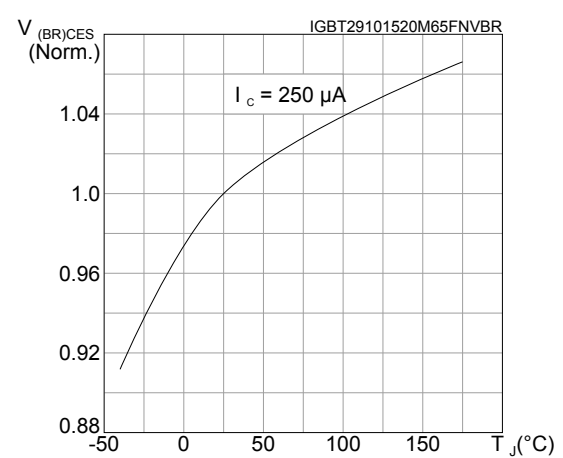
Figure 7. Collector current vs switching frequency

Figure 8. Forward bias safe operating area

Figure 9. Transfer characteristics

Figure 10. Diode V_F vs forward current

Figure 11. Normalized $V_{GE(th)}$ vs junction temperature

Figure 12. Normalized $V_{(BR)CES}$ vs junction temperature


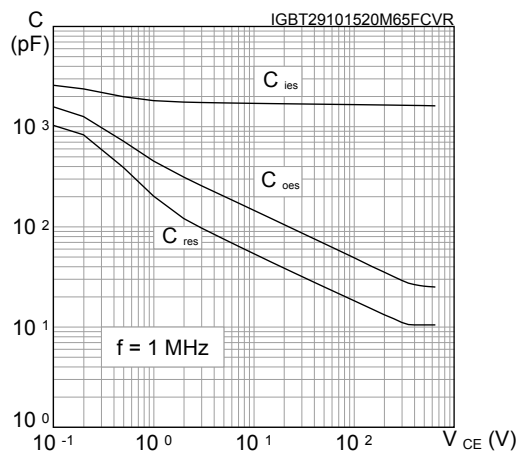
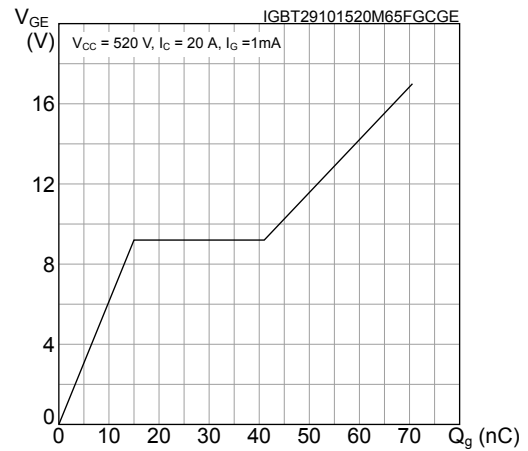
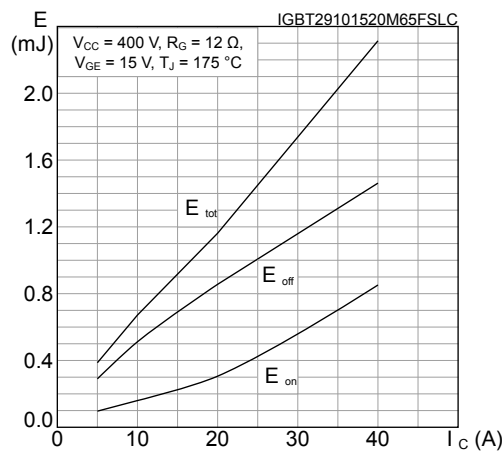
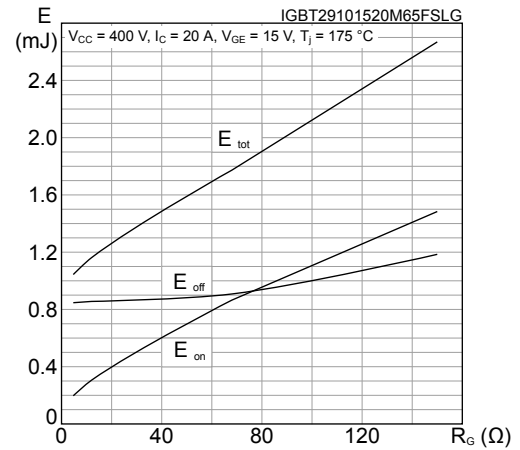
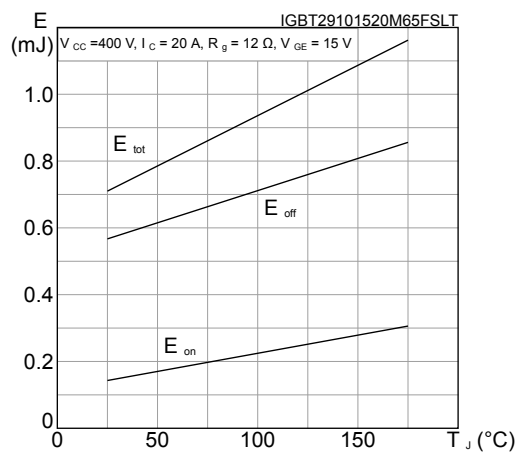
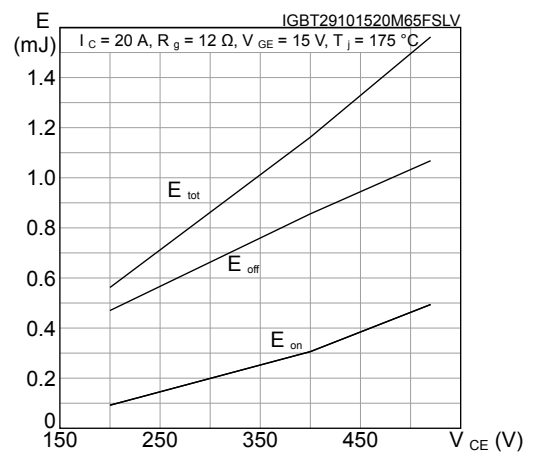
Figure 13. Capacitance variations

Figure 14. Gate charge vs gate-emitter voltage

Figure 15. Switching energy vs collector current

Figure 16. Switching energy vs gate resistance

Figure 17. Switching energy vs temperature

Figure 18. Switching energy vs collector emitter voltage


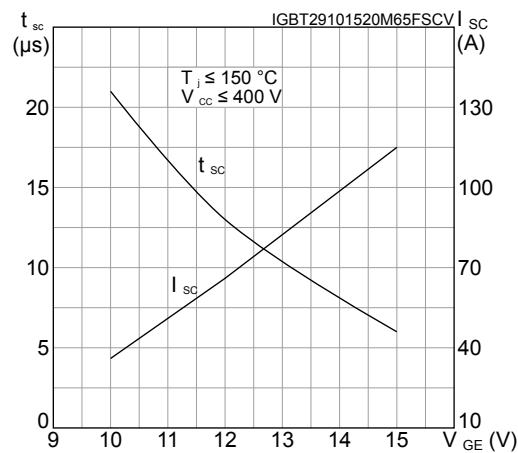
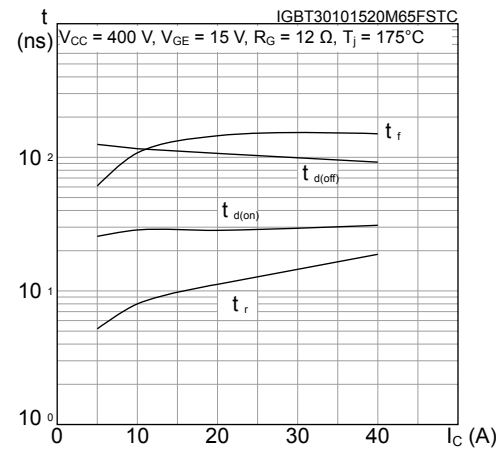
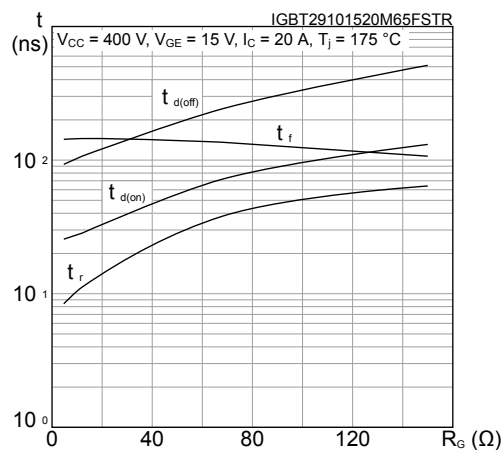
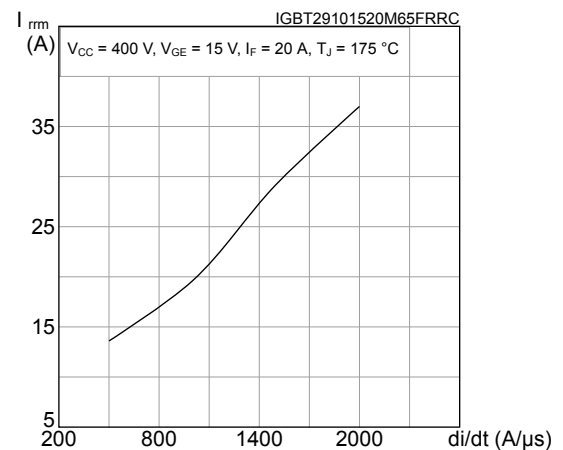
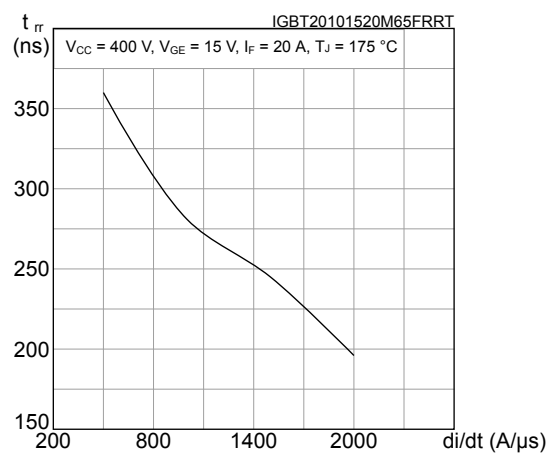
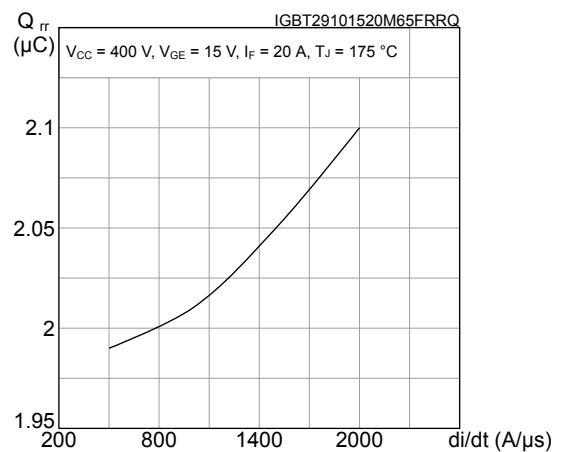
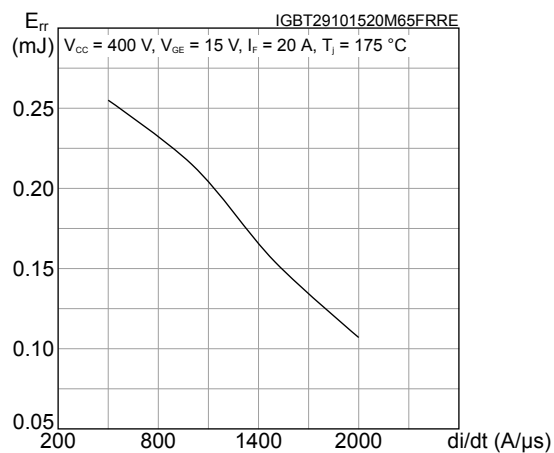
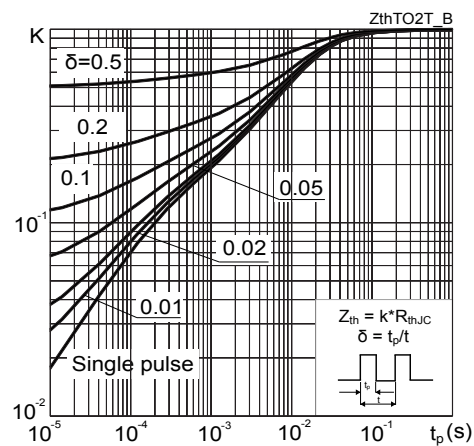
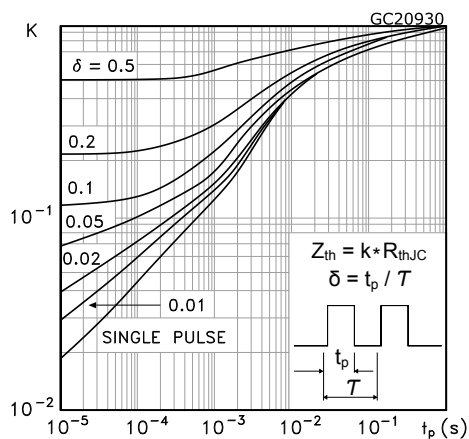
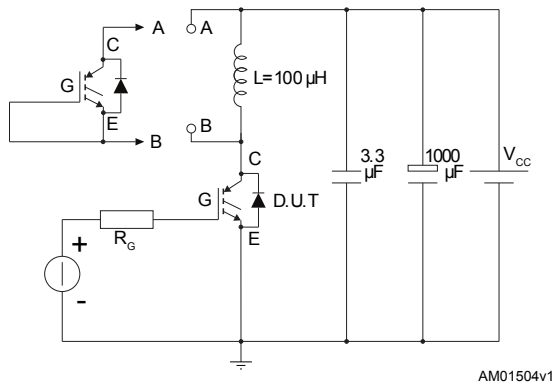
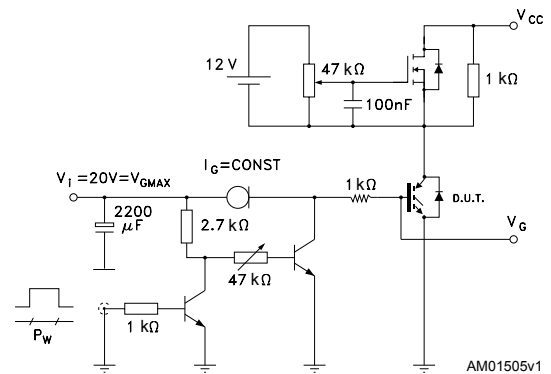
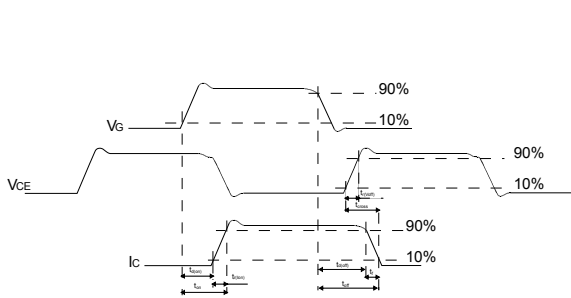
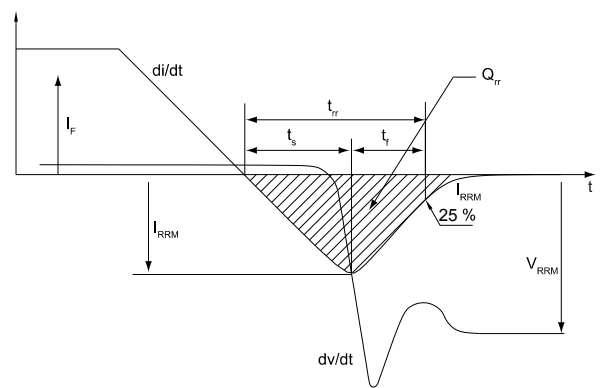
Figure 19. Short-circuit time and current vs V_{GE}

Figure 20. Switching times vs collector current

Figure 21. Switching times vs gate resistance

Figure 22. Reverse recovery current vs diode current slope

Figure 23. Reverse recovery time vs diode current slope

Figure 24. Reverse recovery charge vs diode current slope


Figure 25. Reverse recovery energy vs diode current slope

Figure 26. Thermal impedance for IGBT

Figure 27. Thermal impedance for diode


3 Test circuits

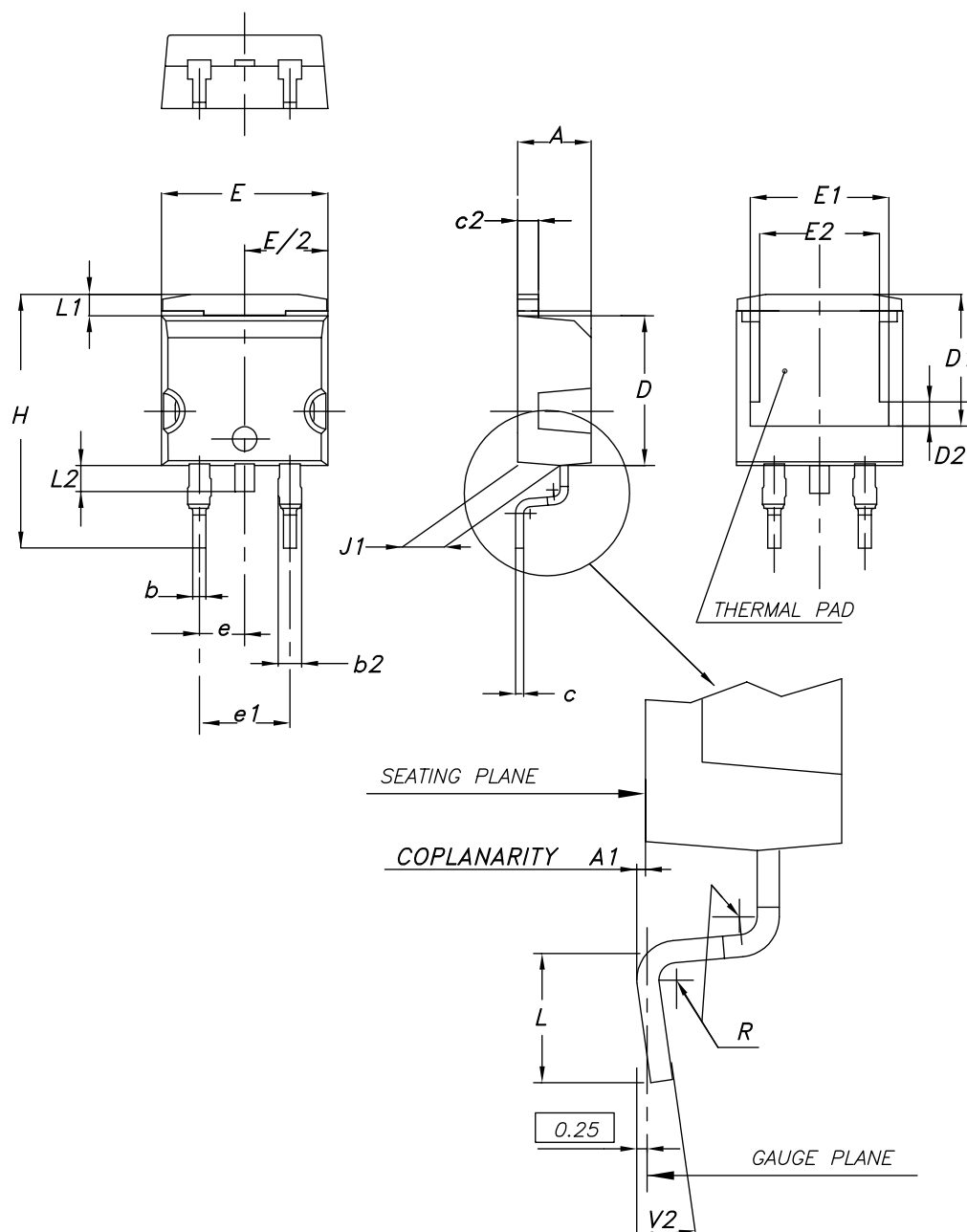
Figure 28. Test circuit for inductive load switching

Figure 29. Gate charge test circuit

Figure 30. Switching waveform

Figure 31. Diode reverse recovery waveform


4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 32. D²PAK (TO-263) type A2 package outline

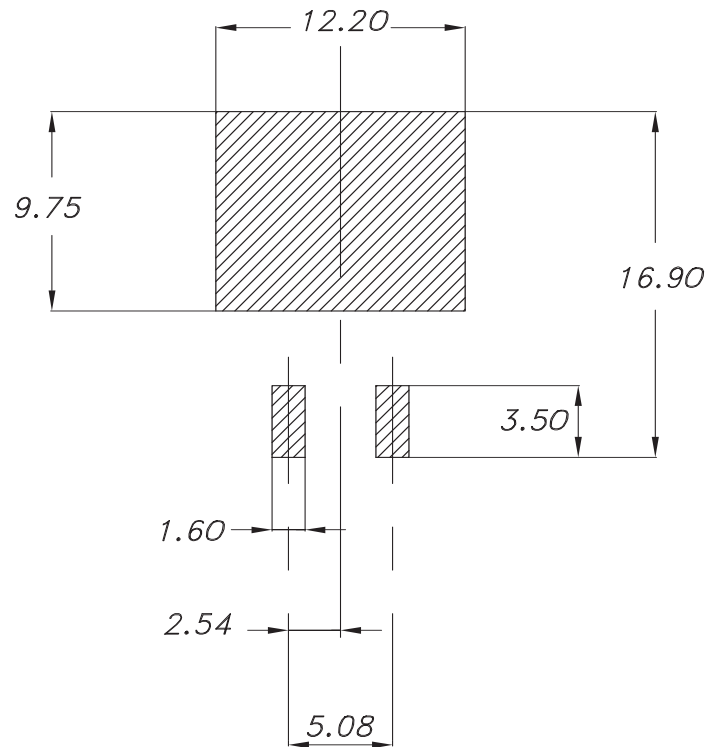


0079457_A2_27

Table 7. D²PAK (TO-263) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

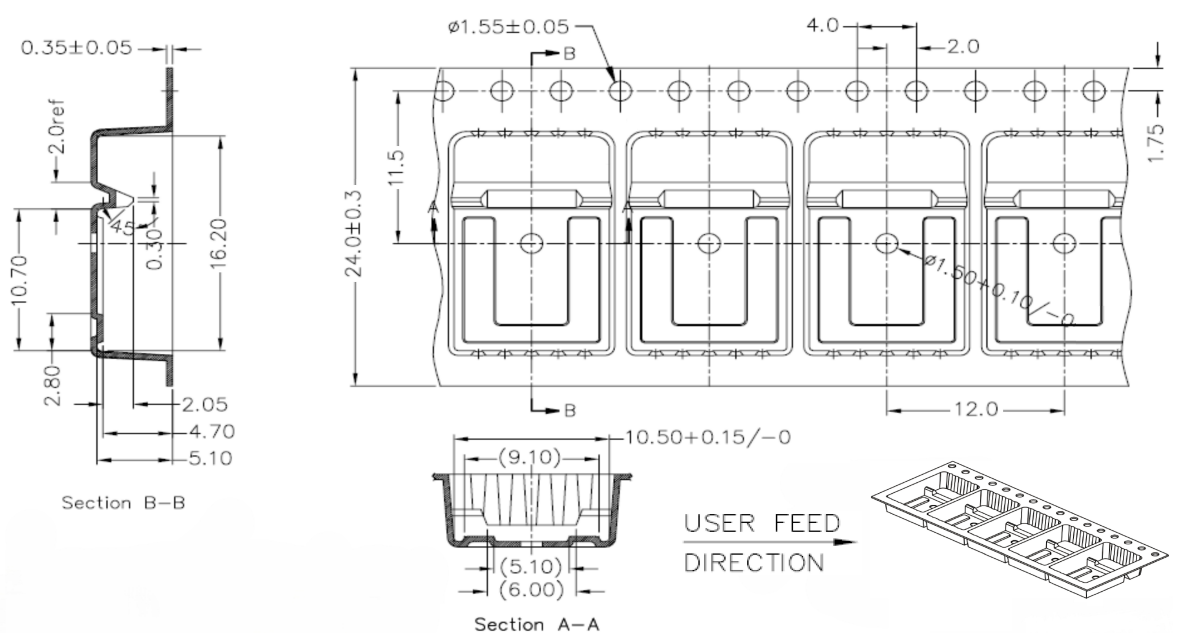
Figure 33. D²PAK (TO-263) recommended footprint (dimensions are in mm)



0079457_Rev27_footprint

4.2 D²PAK packing information

Figure 34. D²PAK tape drawing (dimensions are in mm)



DM01095771_1

Revision history

Table 8. Document revision history

Date	Revision	Changes
05-Nov-2015	1	First release.
14-Apr-2016	2	Updated <i>Figure 13: "Normalized $V(BR)_{CES}$ vs. junction temperature"</i> . Minor text changes.
08-Oct-2018	3	Updated <i>Table 3. Static characteristics</i> . Minor text changes
05-May-2025	4	Updated Section 4: Package information . Minor text changes.

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4.2	D ² PAK packing information	13
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