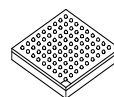


## MSC8157



FC-PBGA-783  
29 mm × 29 mm

### Six-Core Digital Signal Processor

- Six StarCore SC3850 DSP subsystems, each with an SC3850 DSP core, 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, unified 512 Kbyte L2 cache configurable as M2 memory in 64 Kbyte increments, memory management unit (MMU), extended programmable interrupt controller (EPIC), two general-purpose 32-bit timers, debug and profiling support, low-power Wait, Stop, and power-down processing modes, and ECC/EDC support.
- Chip-level arbitration and switching system (CLASS) that provides full fabric non-blocking arbitration between the cores and other initiators and the M2 memory, shared M3 memory, DDR SRAM controller, device configuration control and status registers, MAPLE-B, and other targets.
- 3072 Kbyte 128-bit wide M3 memory, 2048 Kbytes of which can be turned off to save power.
- 96 Kbyte boot ROM.
- Three input clocks (one global and two differential).
- Six PLLs (three global, two Serial RapidIO, one DDR PLLs).
- Second generation Multi-Accelerator Platform Engine for Baseband (MAPLE-B2) with a second generation programmable system interface (PSIF2); Turbo encoding and decoding; Viterbi decoding; FFT/iFFT and DFT/iDFT processing; downlink chip rate processing; CRC processing and insertion; equalization processing and matrix inversion; uplink batch and fast processing. Some MAPLE-B2 processors can be disabled when not required to reduce overall power consumption.
- One DDR controllers with up to a 667 MHz clock (1333 MHz data rate), 64/32 bit data bus, supporting up to a total 2 Gbyte in up to four banks (two per controller) and support for DDR3.
- DMA controller with 32 unidirectional channels supporting 16 memory-to-memory channels with up to 1024 buffer descriptors per channel, and programmable priority, buffer, and multiplexing configuration. It is optimized for DDR SDRAM.
- High-speed serial interface with a 10-lane SerDes PHY that supports two Serial RapidIO interfaces, one PCI Express interface, six CPRI lanes, and two SGMII interfaces (multiplexed). The Serial RapidIO interfaces support x1/x2/x4 operation up to 5 Gbaud with an enhanced messaging unit (eMSG) and two DMA units. The PCI Express controller supports 32- and 64-bit addressing, x1/x2/x4 link. The six CPRI controllers can support six lanes up to 6.144 Gbaud.
- QUICC Engine technology subsystem with dual RISC processors, 48 Kbyte multi-master RAM, 48 Kbyte instruction RAM, supporting two communication controllers for two Gigabit Ethernet interfaces (RGMII or SGMII), to offload scheduling tasks from the DSP cores, and an SPI.
- I/O Interrupt Concentrator consolidates all chip maskable interrupt and non-maskable interrupt sources and routes then to INT\_OUT/CP\_TX\_INT, NMI\_OUT/CP\_RX\_INT, and the cores.
- UART that permits full-duplex operation with a bit rate of up to 6.25 Mbps.
- Two general-purpose 32-bit timers for RTOS support per SC3850 core, four timer modules with four 16-bit fully programmable timers, two timer modules with four 32-bit fully programmable timers; and eight software watchdog timers (SWT).
- Eight programmable hardware semaphores.
- Up to 32 virtual interrupts and a virtual NMI asserted by simple write access.
- I<sup>2</sup>C interface.
- Up to 32 GPIO ports, sixteen of which can be configured as external interrupts.
- Boot interface options include Ethernet, Serial RapidIO interface, I<sup>2</sup>C, and SPI.
- Supports IEEE Std. 1149.6 JTAG interface
- Low power CMOS design, with low-power standby and power-down modes, and optimized power-management circuitry.
- 45 nm SOI CMOS technology.

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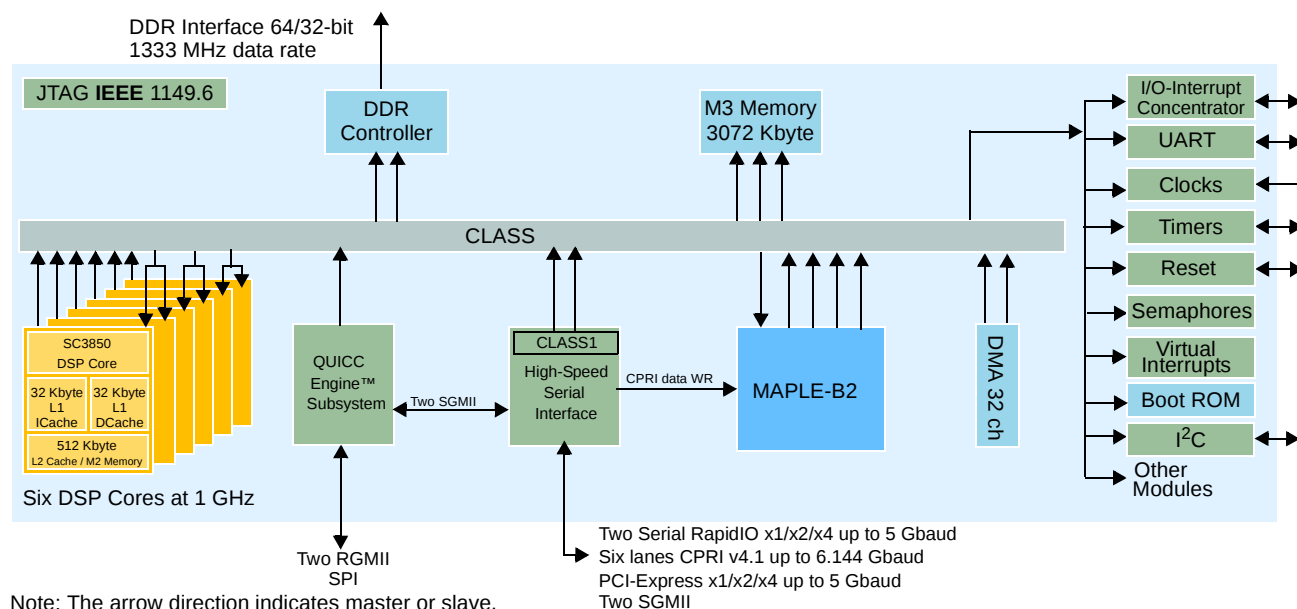


Figure 1. MSC8157 Block Diagram

# 1 Pin Assignment

This section includes a MSC8157 package ball grid array layout and table listing the signal allocation by ball location.

## 1.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in [Figure 2](#) with the ball location index numbers. Only the first multiplexed signal is shown. See [Table 1](#) for a complete signal list by ball location.

|    | 1     | 2     | 3     | 4     | 5     | 6         | 7       | 8       | 9       | 10      | 11      | 12     | 13    | 14        | 15                | 16        | 17        | 18           | 19          | 20         | 21          | 22            | 23      | 24            | 25        | 26           | 27           | 28      |             |             |   |
|----|-------|-------|-------|-------|-------|-----------|---------|---------|---------|---------|---------|--------|-------|-----------|-------------------|-----------|-----------|--------------|-------------|------------|-------------|---------------|---------|---------------|-----------|--------------|--------------|---------|-------------|-------------|---|
| A  |       | VSS   | MDQ57 | GVDD  | VSS   | MDQ63     | GVDD    | NC      | NC      | NC      | NC      | CLKOUT | EEO   | VSS       | MCLKIN (optional) | VSS       | CLKIN     | VSS          | GPI029      | GPI031     | GE1_TX_CTL  | GE1_GTX_CLK   | GE1_TD0 | GE1_TX_CLK    | GE1_TD2   | GE1_TD1      | GE1_TD3      | A       |             |             |   |
| B  | MDQ60 | MDQ59 | MDQ57 | MDQ57 | MDQ62 | MDQ58     | MDQ56   | NC      | VSS     | NC      | VSS     | NC     | VSS   | TDO       | TMS               | VSS       | VSS       | VSS          | VSS         | GE2_TX_CLK | VSS         | VSS           | VSS     | GPI025        | VSS       | GE_MDC       | VSS          | GPI018  | B           |             |   |
| C  | VSS   | GVDD  | MDQ61 | VSS   | GVDD  | MDM7      | VSS     | NC      | NC      | NC      | NC      | NC     | NC    | EE1       | NC                | DFT_TEST  | PORRESET  | VSS          | GPI015      | GE2_TD2    | GE2_GTX_CLK | GE2_TX_CTL    | GE2_TD1 | GE2_TD0       | GPI030    | GPI020       | GE_MDIQ      | GPI021  | C           |             |   |
| D  | MDQ49 | MDQ48 | MDQ56 | MDQ56 | MDQ50 | MDQ51     | MDQ52   | NC      | VSS     | NC      | VSS     | NC     | VSS   | NC        | NMI               | VSS       | HRESET_IN | VSS          | VSS         | GPI013     | NVDD        | GE2_TD3       | VSS     | GPI05         | NVDD      | GPI016       | VSS          | GPI010  | D           |             |   |
| E  | MDQ53 | VSS   | MDQ55 | GVDD  | VSS   | MDQ54     | GVDD    | VSS     | NC      | NC      | NC      | NC     | NC    | NC        | INT_OUT           | VSS       | HRESET    | TCK          | VSS         | NVDD       | GE2_RD3     | VSS           | VSS     | NVDD          | GPI027    | VSS          | GPI00        | GPI017  | GPI01       | E           |   |
| F  | MDQ40 | MDQ41 | MDQ55 | MDQ55 | MDQ43 | MDQ47     | MDM6    | VDD     | VSS     | VDD     | NC      | NC     | VSS   | NC        | NMI_OUT           | VSS       | TDI       | VSS          | GE2_RD2     | GE2_RX_CTL | GE2_RDO     | GE2_RX_CLK    | GE2_RD1 | GPI026        | GPI06     | GPI022       | GPI023       | GPI08   | F           |             |   |
| G  | VSS   | GVDD  | MDM5  | VSS   | GVDD  | MDQ46     | VDD     | VSS     | VDD     | VSS     | NC      | NC     | NC    | NC        | QVDD              | STOP_BS   | TRST      | VSS          | GPI028      | GE1_RD3    | GE1_RD2     | GE1_RX_CLK    | VSS     | GE1_RX_CTL    | NVDD      | GPI019       | VSS          | GPI011  | G           |             |   |
| H  | MDQ38 | MDQ54 | MDQ54 | MDQ44 | MDQ45 | MDQ42     | VSS     | VDD     | VSS     | VDD     | VSS     | VSS    | NC    | QVDD      | VSS               | VDD       | VSS       | VDD          | VSS         | NVDD       | VSS         | GE1_RDO       | NVDD    | GE1_RD1       | VSS       | GPI014       | NVDD         | GPI012  | H           |             |   |
| J  | MDQ37 | VSS   | MDQ35 | GVDD  | MDQ33 | MDQ36     | VDD     | VSS     | VDD     | VSS     | VDD     | VSS    | VDD   | VSS       | VDD               | VSS       | VDD       | VSS          | VDD         | VSS        | NVDD        | GPI024        | GPI09   | ROW_LSEL0     | ROW_LSEL3 | ROW_LSEL2    | RC21         | GPI03   | J           |             |   |
| K  | MCAS  | MC50  | MC51  | MDQ39 | MDQ32 | MDQ34     | VSS     | VDD     | VSS     | VDD     | VSS     | VDD    | VSS   | VDD       | VSS               | VDD       | VSS       | VDD          | VSS         | VDD        | VSS         | GPI04         | VSS     | ROW_LSEL1     | NVDD      | GPI07        | VSS          | GPI02   | K           |             |   |
| L  | VSS   | GVDD  | NC    | VSS   | GVDD  | MDM4      | VDD     | VSS     | VDD     | VSS     | VDD     | VSS    | VDD   | VSS       | VDD               | VSS       | VDD       | VSS          | VDD         | VSS        | NVDD        | NC            | NC      | VSS           | VSS       | VSS          | SXCVSS       | SXCVDD  | L           |             |   |
| M  | MCK0  | MCK0  | MA13  | MWE   | NC    | NC        | VSS     | VDD     | VSS     | VDD     | VSS     | VDD    | VSS   | VDD       | VSS               | VDD       | VSS       | VDD          | VSS         | VDD        | VSS         | VDD           | NC      | NC            | SD_A_TX   | SD_A_TX      | SXPVDD       | SXPVSS  | SD_A_RX     | SD_A_RX     | M |
| N  | MRA5  | VSS   | NC    | GVDD  | VSS   | MDT1      | CRPEVDD | VSS     | CRPEVDD | VSS     | CRPEVDD | VSS    | VDD   | VSS       | VDD               | VSS       | VDD       | VSS          | VDD         | VSS        | VDD         | VSS           | NC      | NC            | SXPVDD    | SXPVSS       | SD_B_TX      | SD_B_TX | SXCVSS      | SXCVDD      | N |
| P  | MCK2  | MA10  | NC    | MA4   | NC    | MDT0      | VSS     | CRPEVDD | VSS     | CRPEVDD | VSS     | VDD    | VSS   | VDD       | VSS               | VDD       | VSS       | VDD          | VSS         | VDD        | VSS         | VDD           | NC      | SD_IMP_CAL_RX | NC        | NC           | SXPVDD       | SXPVSS  | SD_B_RX     | SD_B_RX     | P |
| R  | MCK2  | GVDD  | MA0   | VSS   | GVDD  | MBA0      | GVDD    | VSS     | VDD     | VSS     | CRPEVDD | VSS    | VDD   | VSS       | VDD               | VSS       | VDD       | VSS          | VDD         | VSS        | VDD         | VSS           | NC      | NC            | NC        | NC           | SD_C_TX      | SD_C_TX | SXCVSS      | SXCVDD      | R |
| T  | VSS   | VSS   | MCK1  | MA1   | MA3   | MAPAR_OUT | VSS     | GVDD    | VSS     | VDD     | VSS     | VDD    | VSS   | VDD       | VSS               | VDD       | VSS       | VDD          | VSS         | VDD        | VSS         | VDD           | NC      | NC            | NC        | NC           | SXPVDD       | SXPVSS  | SD_C_RX     | SD_C_RX     | T |
| U  | MAVDD | VSS   | MCK1  | GVDD  | VSS   | MBA1      | GVDD    | VSS     | VDD     | VSS     | VDD     | VSS    | VDD   | VSS       | VDD               | VSS       | VDD       | VSS          | VDD         | VSS        | VDD         | VSS           | NC      | NC            | NC        | NC           | SD_D_TX      | SD_D_TX | SXCVSS      | SXCVDD      | U |
| V  | MVREF | VSS   | MA8   | MA2   | MA6   | MCKE1     | VSS     | GVDD    | VSS     | VDD     | VSS     | VDD    | VSS   | VDD       | VSS               | VDD       | VSS       | VDD          | VSS         | VDD        | VSS         | VDD           | NC      | NC            | NC        | NC           | NC           | NC      | SD_D_RX     | SD_D_RX     | V |
| W  | VSS   | VSS   | MA5   | VSS   | GVDD  | MMDIC1    | GVDD    | VSS     | VDD     | VSS     | M3VDD   | VSS    | M3VDD | VSS       | M3VDD             | VSS       | CPRIVDD   | VSS          | VDD         | VSS        | VDD         | VSS           | NC      | NC            | NC        | SD_PLL1_AVDD | SD_PLL1_AGND | NC      | SXCVSS      | SXCVDD      | W |
| Y  | MA11  | MA9   | MA12  | MA7   | NC    | MMDIC0    | VSS     | GVDD    | VSS     | VDD     | VSS     | M3VDD  | VSS   | M3VDD     | VSS               | CPRIVDD   | VSS       | CPRIVDD      | VSS         | CPRIVDD    | VSS         | VDD           | NC      | NC            | NC        | NC           | NC           | NC      | SD_REF_CLK1 | SD_REF_CLK1 | Y |
| AA | MDQ58 | VSS   | MA14  | GVDD  | VSS   | MA15      | MCKE0   | VSS     | GVDD    | VSS     | M3VDD   | VSS    | M3VDD | VSS       | CPRIVDD           | VSS       | CPRIVDD   | VSS          | CPRIVDD     | VSS        | NC          | SD_IMP_CAL_TX | NC      | NC            | NC        | SD_E_TX      | SD_E_TX      | SXCVSS  | SXCVDD      | AA          |   |
| AB | MDQ58 | MDM8  | MECC2 | MECC1 | NC    | MAPAR_IN  | MBA2    | MDQ2    | MDQ1    | MDQ0    | VSS     | M3VDD  | VSS   | M3VDD     | VSS               | CPRIVDD   | VSS       | CPRIVDD      | NC          | NC         | NC          | NC            | NC      | NC            | NC        | SXPVDD       | SXPVSS       | SD_E_RX | SD_E_RX     | AB          |   |
| AC | VSS   | GVDD  | MECC4 | VSS   | GVDD  | MDQ25     | VSS     | GVDD    | MDQ3    | VSS     | GVDD    | VSS    | M3VDD | VSS       | CPRIVDD           | VSS       | NC        | NC           | NC          | NC         | NC          | NC            | NC      | NC            | NC        | SD_F_TX      | SD_F_TX      | SXCVSS  | SXCVDD      | AC          |   |
| AD | MECC7 | MECC6 | MECC0 | MECC5 | MECC3 | MDQ24     | MDM0    | MDQ50   | MDQ50   | MDQ4    | MDQ6    | VSS    | VSS   | VSS       | VSS               | VSS       | NC        | SD_PLL2_AVDD | NC          | NC         | NC          | NC            | NC      | NC            | NC        | SXPVDD       | SXPVSS       | SD_F_RX | SD_F_RX     | AD          |   |
| AE | MDQ52 | VSS   | MDQ18 | GVDD  | VSS   | MDQ29     | GVDD    | VSS     | MDQ5    | GVDD    | VSS     | MDQ9   | VSS   | VSS       | VSS               | VSS       | NC        | SD_PLL2_AGND | NC          | SD_J_TX    | SXPVDD      | SD_I_TX       | SXPVDD  | NC            | SD_G_TX   | SD_G_TX      | SXCVSS       | SXCVDD  | AE          |             |   |
| AF | MDQ52 | MDQ17 | MDQ21 | MDQ16 | MDQ30 | MDQ27     | MDQ28   | MDQ7    | MDQ14   | MDQ11   | MDQ8    | MDQ10  | VSS   | VSS       | VSS               | VSS       | NC        | NC           | NC          | SD_J_TX    | SXPVSS      | SD_I_TX       | SXPVSS  | NC            | SXPVDD    | SXPVSS       | SD_G_RX      | SD_G_RX | AF          |             |   |
| AG | VSS   | GVDD  | MDQ22 | VSS   | GVDD  | MDQ26     | VSS     | GVDD    | MDQ13   | VSS     | GVDD    | MDQ12  | VSS   | VSS       | VSS               | VSS       | NC        | SXCVSS       | SD_REF_CLK2 | SXCVSS     | SD_J_RX     | SXCVSS        | SD_I_RX | SXCVSS        | SD_H_TX   | SD_H_TX      | SXCVSS       | SXCVDD  | AG          |             |   |
| AH | MDQ20 | MDQ19 | MDQ23 | MDM2  | MDQ53 | MDQ53     | MDM3    | MDQ31   | MDQ51   | MDQ51   | MDQ15   | MDM1   | VSS   | PLL0_AVDD | PLL1_AVDD         | PLL2_AVDD | NC        | SXCVDD       | SD_REF_CLK2 | SXCVDD     | SD_J_RX     | SXCVDD        | SD_I_RX | SXCVDD        | SXPVDD    | SXPVSS       | SD_H_RX      | SD_H_RX | AH          |             |   |
|    | 1     | 2     | 3     | 4     | 5     | 6         | 7       | 8       | 9       | 10      | 11      | 12     | 13    | 14        | 15                | 16        | 17        | 18           | 19          | 20         | 21          | 22            | 23      | 24            | 25        | 26           | 27           | 28      |             |             |   |

Figure 2. MSC8157 FC-PBGA Package, Top View

**Note:** See [Figure 32](#) as a reference for correct ball grid layout.

## 1.2 Signal Lists

**Table 1** presents the signal list sorted by ball number. **Table 2** presents the signal list by signal name. When designing a board, make sure that the power rail for each signal is appropriately considered. The specified power rail must be tied to the voltage level specified in this document if any of the related signal functions are used (active)

**Note:** The information in **Table 1** distinguishes among three concepts. First, the power pins are the balls of the device package used to supply specific power levels for different device subsystems (as opposed to signals). Second, the power rails are the electrical lines on the board that transfer power from the voltage regulators to the device. They are indicated here as the reference power rails for signal lines; therefore, the actual power inputs are listed as N/A with regard to the power rails. Third, symbols used in these tables are the names for the voltage levels (absolute, recommended, and so on) and not the power supplies themselves.

**Table 1. Signal List by Ball Number**

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| A2          | VSS                        | Ground                | N/A             |
| A3          | MDQ57                      | I/O                   | GVDD            |
| A4          | GVDD                       | Power                 | N/A             |
| A5          | VSS                        | Ground                | N/A             |
| A6          | MDQ63                      | I/O                   | GVDD            |
| A7          | GVDD                       | Power                 | N/A             |
| A8          | NC                         | Non-user              | N/A             |
| A9          | NC                         | Non-user              | N/A             |
| A10         | NC                         | Non-user              | N/A             |
| A11         | NC                         | Non-user              | N/A             |
| A12         | NC                         | Non-user              | N/A             |
| A13         | CLKOUT                     | O                     | QVDD            |
| A14         | EE0                        | I                     | QVDD            |
| A15         | VSS                        | Ground                | N/A             |
| A16         | MCLKIN (optional)          | I                     | QVDD            |
| A17         | VSS                        | Ground                | N/A             |
| A18         | CLKIN                      | I                     | QVDD            |
| A19         | VSS                        | Ground                | N/A             |
| A20         | GPIO29/UART_TXD/CP_LOS2    | I/O                   | NVDD            |
| A21         | GPIO31/I2C_SDA             | I/O                   | NVDD            |
| A22         | GE1_TX_CTL                 | O                     | NVDD            |
| A23         | GE1_GTX_CLK                | O                     | NVDD            |
| A24         | GE1_TD0                    | O                     | NVDD            |
| A25         | GE1_TX_CLK                 | I                     | NVDD            |
| A26         | GE1_TD2                    | O                     | NVDD            |
| A27         | GE1_TD1                    | O                     | NVDD            |
| A28         | GE1_TD3                    | O                     | NVDD            |
| B1          | MDQ60                      | I/O                   | GVDD            |
| B2          | MDQ59                      | I/O                   | GVDD            |
| B3          | MDQS7                      | I/O                   | GVDD            |
| B4          | MDQS7                      | I/O                   | GVDD            |
| B5          | MDQ62                      | I/O                   | GVDD            |
| B6          | MDQ58                      | I/O                   | GVDD            |
| B7          | MDQ56                      | I/O                   | GVDD            |
| B8          | NC                         | Non-user              | N/A             |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| B9          | VSS                        | Ground                | N/A             |
| B10         | NC                         | Non-user              | N/A             |
| B11         | VSS                        | Ground                | N/A             |
| B12         | NC                         | Non-user              | N/A             |
| B13         | VSS                        | Ground                | N/A             |
| B14         | TDO                        | O                     | QVDD            |
| B15         | TMS                        | I                     | QVDD            |
| B16         | VSS                        | Ground                | N/A             |
| B17         | VSS                        | Ground                | N/A             |
| B18         | VSS                        | Ground                | N/A             |
| B19         | VSS                        | Ground                | N/A             |
| B20         | GE2_TX_CLK                 | I                     | NVDD            |
| B21         | VSS                        | Ground                | N/A             |
| B22         | VSS                        | Non-user              | N/A             |
| B23         | VSS                        | Ground                | N/A             |
| B24         | GPIO25/TMR2/RCW_SRC1       | I/O                   | NVDD            |
| B25         | VSS                        | Ground                | N/A             |
| B26         | GE_MDC                     | O                     | NVDD            |
| B27         | VSS                        | Ground                | N/A             |
| B28         | GPIO18/SPI_MOSI/CP_LOS4    | I/O                   | NVDD            |
| C1          | VSS                        | Ground                | N/A             |
| C2          | GVDD                       | Power                 | N/A             |
| C3          | MDQ61                      | I/O                   | GVDD            |
| C4          | VSS                        | Ground                | N/A             |
| C5          | GVDD                       | Power                 | N/A             |
| C6          | MDM7                       | O                     | GVDD            |
| C7          | VSS                        | Ground                | N/A             |
| C8          | NC                         | Non-user              | N/A             |
| C9          | NC                         | Non-user              | N/A             |
| C10         | NC                         | Non-user              | N/A             |
| C11         | NC                         | Non-user              | N/A             |
| C12         | NC                         | Non-user              | N/A             |
| C13         | NC                         | Non-user              | N/A             |
| C14         | EE1                        | O                     | QVDD            |
| C15         | NC                         | Non-user              | N/A             |
| C16         | DFT_TEST                   | I                     | QVDD            |
| C17         | PORESET                    | I                     | QVDD            |
| C18         | VSS                        | Ground                | N/A             |
| C19         | GPIO15/DDN0/IRQ15/RC15     | I/O                   | NVDD            |
| C20         | GE2_TD2/CP_LOS3            | I/O                   | NVDD            |
| C21         | GE2_GTX_CLK/CP_LOS4        | I/O                   | NVDD            |
| C22         | GE2_TX_CTL                 | O                     | NVDD            |
| C23         | GE2_TD1                    | O                     | NVDD            |
| C24         | GE2_TD0                    | O                     | NVDD            |
| C25         | GPIO30/I2C_SCL             | I/O                   | NVDD            |
| C26         | GPIO20/SPI_SL/CP_LOS6      | I/O                   | NVDD            |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| C27         | GE_MDIO                    | I/O                   | NVDD            |
| C28         | GPIO21/TMR6                | I/O                   | NVDD            |
| D1          | MDQ49                      | I/O                   | GVDD            |
| D2          | MDQ48                      | I/O                   | GVDD            |
| D3          | MDQS6                      | I/O                   | GVDD            |
| D4          | MDQS6                      | I/O                   | GVDD            |
| D5          | MDQ50                      | I/O                   | GVDD            |
| D6          | MDQ51                      | I/O                   | GVDD            |
| D7          | MDQ52                      | I/O                   | GVDD            |
| D8          | NC                         | Non-user              | N/A             |
| D9          | VSS                        | Ground                | N/A             |
| D10         | NC                         | Non-user              | N/A             |
| D11         | VSS                        | Ground                | N/A             |
| D12         | NC                         | Non-user              | N/A             |
| D13         | VSS                        | Ground                | N/A             |
| D14         | NC                         | Non-user              | N/A             |
| D15         | NMI                        | I                     | QVDD            |
| D16         | VSS                        | Ground                | N/A             |
| D17         | HRESET_IN                  | I                     | QVDD            |
| D18         | VSS                        | Ground                | N/A             |
| D19         | VSS                        | Non-user              | N/A             |
| D20         | GPIO13/IRQ13/RC13          | I/O                   | NVDD            |
| D21         | NVDD                       | Power                 | N/A             |
| D22         | GE2_TD3/CP_LOS5            | I/O                   | NVDD            |
| D23         | VSS                        | Ground                | N/A             |
| D24         | GPIO5/IRQ5/RC5/CP_SYNC4    | I/O                   | NVDD            |
| D25         | NVDD                       | Power                 | N/A             |
| D26         | GPIO16/TMR5/RC16           | I/O                   | NVDD            |
| D27         | VSS'                       | Ground                | N/A             |
| D28         | GPIO10/IRQ10/RC10          | I/O                   | NVDD            |
| E1          | MDQ53                      | I/O                   | GVDD            |
| E2          | VSS                        | Ground                | N/A             |
| E3          | MDQ55                      | I/O                   | GVDD            |
| E4          | GVDD                       | Power                 | N/A             |
| E5          | VSS                        | Ground                | N/A             |
| E6          | MDQ54                      | I/O                   | GVDD            |
| E7          | GVDD                       | Power                 | N/A             |
| E8          | VSS                        | Ground                | N/A             |
| E9          | NC                         | Non-user              | N/A             |
| E10         | NC                         | Non-user              | N/A             |
| E11         | NC                         | Non-user              | N/A             |
| E12         | NC                         | Non-user              | N/A             |
| E13         | NC                         | Non-user              | N/A             |
| E14         | NC                         | Non-user              | N/A             |
| E15         | INT_OUT/CP_TX_INT          | O                     | QVDD            |
| E16         | HRESET                     | I/O                   | QVDD            |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| E17         | TCK                        | I                     | QVDD            |
| E18         | VSS                        | Ground                | N/A             |
| E19         | NVDD                       | Power                 | N/A             |
| E20         | GE2_RD3/CP_LOS2            | I                     | NVDD            |
| E21         | VSS                        | Ground                | N/A             |
| E22         | VSS                        | Non-user              | N/A             |
| E23         | NVDD                       | Power                 | N/A             |
| E24         | GPIO27/TMR4/RCW_SRC0       | I/O                   | NVDD            |
| E25         | VSS                        | Ground                | N/A             |
| E26         | GPIO0/IRQ0/RC0/CP_SYNC1    | I/O                   | NVDD            |
| E27         | GPIO17/SPI_SCK/CP_LOS3     | I/O                   | NVDD            |
| E28         | GPIO1/IRQ1/RC1/CP_SYNC2    | I/O                   | NVDD            |
| F1          | MDQ40                      | I/O                   | GVDD            |
| F2          | MDQ41                      | I/O                   | GVDD            |
| F3          | MDQS5                      | I/O                   | GVDD            |
| F4          | MDQS5                      | I/O                   | GVDD            |
| F5          | MDQ43                      | I/O                   | GVDD            |
| F6          | MDQ47                      | I/O                   | GVDD            |
| F7          | MDM6                       | O                     | GVDD            |
| F8          | VDD                        | Power                 | N/A             |
| F9          | VSS                        | Ground                | N/A             |
| F10         | VDD                        | Power                 | N/A             |
| F11         | NC                         | Non-user              | N/A             |
| F12         | NC                         | Non-user              | N/A             |
| F13         | VSS                        | Ground                | N/A             |
| F14         | NC                         | Non-user              | N/A             |
| F15         | NMI_OUT/CP_RX_INT          | O                     | QVDD            |
| F16         | VSS                        | Ground                | N/A             |
| F17         | TDI                        | I                     | QVDD            |
| F18         | VSS                        | Ground                | N/A             |
| F19         | GE2_RD2/CP_LOS1            | I                     | NVDD            |
| F20         | GE2_RX_CTL                 | I                     | NVDD            |
| F21         | GE2_RD0/CP_LOS6            | I                     | NVDD            |
| F22         | GE2_RX_CLK                 | I                     | NVDD            |
| F23         | GE2_RD1                    | I                     | NVDD            |
| F24         | GPIO26/TMR3                | I/O                   | NVDD            |
| F25         | GPIO6/IRQ6/RC6/CP_SYNC5    | I/O                   | NVDD            |
| F26         | GPIO22                     | I/O                   | NVDD            |
| F27         | GPIO23/TMR0/BOOT_SPI_SL    | I/O                   | NVDD            |
| F28         | GPIO8/IRQ8/RC8             | I/O                   | NVDD            |
| G1          | VSS                        | Ground                | N/A             |
| G2          | GVDD                       | Power                 | N/A             |
| G3          | MDM5                       | O                     | GVDD            |
| G4          | VSS                        | Ground                | N/A             |
| G5          | GVDD                       | Power                 | N/A             |
| G6          | MDQ46                      | I/O                   | GVDD            |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| G7          | VDD                        | Power                 | N/A             |
| G8          | VSS                        | Ground                | N/A             |
| G9          | VDD                        | Power                 | N/A             |
| G10         | VSS                        | Ground                | N/A             |
| G11         | NC                         | Non-user              | N/A             |
| G12         | NC                         | Non-user              | N/A             |
| G13         | NC                         | Non-user              | N/A             |
| G14         | NC                         | Non-user              | N/A             |
| G15         | QVDD                       | Power                 | N/A             |
| G16         | STOP_BS                    | I                     | QVDD            |
| G17         | TRST                       | I                     | QVDD            |
| G18         | VSS                        | Ground                | N/A             |
| G19         | GPIO28/UART_RXD/CP_LOS1    | I/O                   | NVDD            |
| G20         | GE1_RD3                    | I                     | NVDD            |
| G21         | GE1_RD2                    | I                     | NVDD            |
| G22         | GE1_RX_CLK                 | I                     | NVDD            |
| G23         | VSS                        | Ground                | N/A             |
| G24         | GE1_RX_CTL                 | I                     | NVDD            |
| G25         | NVDD                       | Power                 | N/A             |
| G26         | GPIO19/SPI_MISO/CP_LOS5    | I/O                   | NVDD            |
| G27         | VSS                        | Ground                | N/A             |
| G28         | GPIO11/IRQ11/RC11          | I/O                   | NVDD            |
| H1          | MDQ38                      | I/O                   | GVDD            |
| H2          | MDQS4                      | I/O                   | GVDD            |
| H3          | MDQS4                      | I/O                   | GVDD            |
| H4          | MDQ44                      | I/O                   | GVDD            |
| H5          | MDQ45                      | I/O                   | GVDD            |
| H6          | MDQ42                      | I/O                   | GVDD            |
| H7          | VSS                        | Ground                | N/A             |
| H8          | VDD                        | Power                 | N/A             |
| H9          | VSS                        | Ground                | N/A             |
| H10         | VDD                        | Power                 | N/A             |
| H11         | VSS                        | Ground                | N/A             |
| H12         | VSS                        | Non-user              | N/A             |
| H13         | NC                         | Non-user              | N/A             |
| H14         | QVDD                       | Power                 | N/A             |
| H15         | VSS                        | Ground                | N/A             |
| H16         | VDD                        | Power                 | N/A             |
| H17         | VSS                        | Ground                | N/A             |
| H18         | VDD                        | Power                 | N/A             |
| H19         | VSS                        | Ground                | N/A             |
| H20         | NVDD                       | Power                 | N/A             |
| H21         | VSS                        | Ground                | N/A             |
| H22         | GE1_RD0                    | I                     | NVDD            |
| H23         | NVDD                       | Power                 | N/A             |
| H24         | GE1_RD1                    | I                     | NVDD            |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup>                   | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------------------------|-----------------------|-----------------|
| H25         | VSS                                          | Ground                | N/A             |
| H26         | GPIO14/DRQ0/ $\overline{\text{IRQ14}}$ /RC14 | I/O                   | NVDD            |
| H27         | NVDD                                         | Power                 | N/A             |
| H28         | GPIO12/ $\overline{\text{IRQ12}}$ /RC12      | I/O                   | NVDD            |
| J1          | MDQ37                                        | I/O                   | GVDD            |
| J2          | VSS                                          | Ground                | N/A             |
| J3          | MDQ35                                        | I/O                   | GVDD            |
| J4          | GVDD                                         | Power                 | N/A             |
| J5          | MDQ33                                        | I/O                   | GVDD            |
| J6          | MDQ36                                        | I/O                   | GVDD            |
| J7          | VDD                                          | Power                 | N/A             |
| J8          | VSS                                          | Ground                | N/A             |
| J9          | VDD                                          | Power                 | N/A             |
| J10         | VSS                                          | Ground                | N/A             |
| J11         | VDD                                          | Power                 | N/A             |
| J12         | VSS                                          | Ground                | N/A             |
| J13         | VDD                                          | Power                 | N/A             |
| J14         | VSS                                          | Ground                | N/A             |
| J15         | VDD                                          | Power                 | N/A             |
| J16         | VSS                                          | Ground                | N/A             |
| J17         | VDD                                          | Power                 | N/A             |
| J18         | VSS                                          | Ground                | N/A             |
| J19         | VDD                                          | Power                 | N/A             |
| J20         | VSS                                          | Ground                | N/A             |
| J21         | NVDD                                         | Power                 | N/A             |
| J22         | GPIO24/TMR1/RCW_SRC2                         | I/O                   | NVDD            |
| J23         | GPIO9/ $\overline{\text{IRQ9}}$ /RC9         | I/O                   | NVDD            |
| J24         | RCW_LSEL0/RC17                               | I/O                   | NVDD            |
| J25         | RCW_LSEL3/RC20                               | I/O                   | NVDD            |
| J26         | RCW_LSEL2/RC19                               | I/O                   | NVDD            |
| J27         | RC21                                         | I                     | NVDD            |
| J28         | GPIO3/DRQ1/ $\overline{\text{IRQ3}}$ /RC3    | I/O                   | NVDD            |
| K1          | $\overline{\text{MCAS}}$                     | O                     | GVDD            |
| K2          | $\overline{\text{MCS0}}$                     | O                     | GVDD            |
| K3          | $\overline{\text{MCS1}}$                     | O                     | GVDD            |
| K4          | MDQ39                                        | I/O                   | GVDD            |
| K5          | MDQ32                                        | I/O                   | GVDD            |
| K6          | MDQ34                                        | I/O                   | GVDD            |
| K7          | VSS                                          | Ground                | N/A             |
| K8          | VDD                                          | Power                 | N/A             |
| K9          | VSS                                          | Ground                | N/A             |
| K10         | VDD                                          | Power                 | N/A             |
| K11         | VSS                                          | Ground                | N/A             |
| K12         | VDD                                          | Power                 | N/A             |
| K13         | VSS                                          | Ground                | N/A             |
| K14         | VDD                                          | Power                 | N/A             |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| K15         | VSS                        | Ground                | N/A             |
| K16         | VDD                        | Power                 | N/A             |
| K17         | VSS                        | Ground                | N/A             |
| K18         | VDD                        | Power                 | N/A             |
| K19         | VSS                        | Ground                | N/A             |
| K20         | VDD                        | Power                 | N/A             |
| K21         | VSS                        | Ground                | N/A             |
| K22         | GPIO4/DDN1/IRQ4/RC4        | I/O                   | NVDD            |
| K23         | VSS                        | Ground                | N/A             |
| K24         | RCW_LSEL1/RC18             | I/O                   | NVDD            |
| K25         | NVDD                       | Power                 | N/A             |
| K26         | GPIO7/IRQ7/RC7/CP_SYNC6    | I/O                   | NVDD            |
| K27         | VSS                        | Ground                | N/A             |
| K28         | GPIO2/IRQ2/RC2/CP_SYNC3    | I/O                   | NVDD            |
| L1          | VSS                        | Ground                | N/A             |
| L2          | GVDD                       | Power                 | N/A             |
| L3          | NC                         | Non-user              | N/A             |
| L4          | VSS                        | Ground                | N/A             |
| L5          | GVDD                       | Power                 | N/A             |
| L6          | MDM4                       | O                     | GVDD            |
| L7          | VDD                        | Power                 | N/A             |
| L8          | VSS                        | Ground                | N/A             |
| L9          | VDD                        | Power                 | N/A             |
| L10         | VSS                        | Ground                | N/A             |
| L11         | VDD                        | Power                 | N/A             |
| L12         | VSS                        | Ground                | N/A             |
| L13         | VDD                        | Power                 | N/A             |
| L14         | VSS                        | Ground                | N/A             |
| L15         | VDD                        | Power                 | N/A             |
| L16         | VSS                        | Ground                | N/A             |
| L17         | VDD                        | Power                 | N/A             |
| L18         | VSS                        | Ground                | N/A             |
| L19         | VDD                        | Power                 | N/A             |
| L20         | VSS                        | Ground                | N/A             |
| L21         | NVDD                       | Power                 | N/A             |
| L22         | NC                         | NC                    | N/A             |
| L23         | NC                         | NC                    | N/A             |
| L24         | VSS                        | Non-user              | N/A             |
| L25         | VSS                        | Non-user              | N/A             |
| L26         | VSS                        | Non-user              | N/A             |
| L27         | SXCVSS                     | Ground                | N/A             |
| L28         | SXCVDD                     | Power                 | N/A             |
| M1          | MCK0                       | O                     | GVDD            |
| M2          | MCK0                       | O                     | GVDD            |
| M3          | MA13                       | O                     | GVDD            |
| M4          | MWE                        | O                     | GVDD            |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| M5          | NC                         | Non-user              | N/A             |
| M6          | NC                         | Non-user              | N/A             |
| M7          | VSS                        | Ground                | N/A             |
| M8          | VDD                        | Power                 | N/A             |
| M9          | VSS                        | Ground                | N/A             |
| M10         | VDD                        | Power                 | N/A             |
| M11         | VSS                        | Ground                | N/A             |
| M12         | VDD                        | Power                 | N/A             |
| M13         | VSS                        | Ground                | N/A             |
| M14         | VDD                        | Power                 | N/A             |
| M15         | VSS                        | Ground                | N/A             |
| M16         | VDD                        | Power                 | N/A             |
| M17         | VSS                        | Ground                | N/A             |
| M18         | VDD                        | Power                 | N/A             |
| M19         | VSS                        | Ground                | N/A             |
| M20         | VDD                        | Power                 | N/A             |
| M21         | NC                         | NC                    | N/A             |
| M22         | NC                         | NC                    | N/A             |
| M23         | SD_A_TX                    | O                     | SXPVDD          |
| M24         | SD_A_TX                    | O                     | SXPVDD          |
| M25         | SXPVDD                     | Power                 | N/A             |
| M26         | SXPVSS                     | Ground                | N/A             |
| M27         | SD_A_RX                    | I                     | SXCVDD          |
| M28         | SD_A_RX                    | I                     | SXCVDD          |
| N1          | MRAS                       | O                     | GVDD            |
| N2          | VSS                        | Ground                | N/A             |
| N3          | NC                         | Non-user              | N/A             |
| N4          | GVDD                       | Power                 | N/A             |
| N5          | VSS                        | Ground                | N/A             |
| N6          | MODT1                      | O                     | GVDD            |
| N7          | CRPEVDD                    | Power                 | N/A             |
| N8          | VSS                        | Ground                | N/A             |
| N9          | CRPEVDD                    | Power                 | N/A             |
| N10         | VSS                        | Ground                | N/A             |
| N11         | CRPEVDD                    | Power                 | N/A             |
| N12         | VSS                        | Ground                | N/A             |
| N13         | VDD                        | Power                 | N/A             |
| N14         | VSS                        | Ground                | N/A             |
| N15         | VDD                        | Power                 | N/A             |
| N16         | VSS                        | Ground                | N/A             |
| N17         | VDD                        | Power                 | N/A             |
| N18         | VSS                        | Ground                | N/A             |
| N19         | VDD                        | Power                 | N/A             |
| N20         | VSS                        | Ground                | N/A             |
| N21         | NC                         | NC                    | N/A             |
| N22         | NC                         | NC                    | N/A             |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| N23         | SXPVDD                     | Power                 | N/A             |
| N24         | SXPVSS                     | Ground                | N/A             |
| N25         | SD_B_TX                    | O                     | SXPVDD          |
| N26         | SD_B_TX                    | O                     | SXPVDD          |
| N27         | SXCVSS                     | Ground                | N/A             |
| N28         | SXCVDD                     | Power                 | N/A             |
| P1          | MCK2                       | O                     | GVDD            |
| P2          | MA10                       | O                     | GVDD            |
| P3          | NC                         | Non-user              | N/A             |
| P4          | MA4                        | O                     | GVDD            |
| P5          | NC                         | Non-user              | N/A             |
| P6          | MODT0                      | O                     | GVDD            |
| P7          | VSS                        | Ground                | N/A             |
| P8          | CRPEVDD                    | Power                 | N/A             |
| P9          | VSS                        | Ground                | N/A             |
| P10         | CRPEVDD                    | Power                 | N/A             |
| P11         | VSS                        | Ground                | N/A             |
| P12         | VDD                        | Power                 | N/A             |
| P13         | VSS                        | Ground                | N/A             |
| P14         | VDD                        | Power                 | N/A             |
| P15         | VSS                        | Ground                | N/A             |
| P16         | VDD                        | Power                 | N/A             |
| P17         | VSS                        | Ground                | N/A             |
| P18         | VDD                        | Power                 | N/A             |
| P19         | VSS                        | Ground                | N/A             |
| P20         | VDD                        | Power                 | N/A             |
| P21         | NC                         | NC                    | N/A             |
| P22         | SD_IMP_CAL_RX              | I                     | SXCVDD          |
| P23         | NC                         | NC                    | N/A             |
| P24         | NC                         | NC                    | N/A             |
| P25         | SXPVDD                     | Power                 | N/A             |
| P26         | SXPVSS                     | Ground                | N/A             |
| P27         | SD_B_RX                    | I                     | SXCVDD          |
| P28         | SD_B_RX                    | I                     | SXCVDD          |
| R1          | MCK2                       | O                     | GVDD            |
| R2          | GVDD                       | Power                 | N/A             |
| R3          | MA0                        | O                     | GVDD            |
| R4          | VSS                        | Ground                | N/A             |
| R5          | GVDD                       | Power                 | N/A             |
| R6          | MBA0                       | O                     | GVDD            |
| R7          | GVDD                       | Power                 | N/A             |
| R8          | VSS                        | Ground                | N/A             |
| R9          | VDD                        | Power                 | N/A             |
| R10         | VSS                        | Ground                | N/A             |
| R11         | CRPEVDD                    | Power                 | N/A             |
| R12         | VSS                        | Ground                | N/A             |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| R13         | VDD                        | Power                 | N/A             |
| R14         | VSS                        | Ground                | N/A             |
| R15         | VDD                        | Power                 | N/A             |
| R16         | VSS                        | Ground                | N/A             |
| R17         | VDD                        | Power                 | N/A             |
| R18         | VSS                        | Ground                | N/A             |
| R19         | VDD                        | Power                 | N/A             |
| R20         | VSS                        | Ground                | N/A             |
| R21         | NC                         | NC                    | N/A             |
| R22         | NC                         | NC                    | N/A             |
| R23         | NC                         | NC                    | N/A             |
| R24         | NC                         | NC                    | N/A             |
| R25         | SD_C_TX                    | O                     | SXPVDD          |
| R26         | SD_C_TX                    | O                     | SXPVDD          |
| R27         | SXCVSS                     | Ground                | N/A             |
| R28         | SXCVDD                     | Power                 | N/A             |
| T1          | VSS                        | Ground                | N/A             |
| T2          | VSS                        | Ground                | N/A             |
| T3          | MCK1                       | O                     | GVDD            |
| T4          | MA1                        | O                     | GVDD            |
| T5          | MA3                        | O                     | GVDD            |
| T6          | MAPAR_OUT                  | O                     | GVDD            |
| T7          | VSS                        | Ground                | N/A             |
| T8          | GVDD                       | Power                 | N/A             |
| T9          | VSS                        | Ground                | N/A             |
| T10         | VDD                        | Power                 | N/A             |
| T11         | VSS                        | Ground                | N/A             |
| T12         | VDD                        | Power                 | N/A             |
| T13         | VSS                        | Ground                | N/A             |
| T14         | VDD                        | Power                 | N/A             |
| T15         | VSS                        | Ground                | N/A             |
| T16         | VDD                        | Power                 | N/A             |
| T17         | VSS                        | Ground                | N/A             |
| T18         | VDD                        | Power                 | N/A             |
| T19         | VSS                        | Ground                | N/A             |
| T20         | VDD                        | Power                 | N/A             |
| T21         | NC                         | NC                    | N/A             |
| T22         | NC                         | Non-user              | N/A             |
| T23         | NC                         | Non-user              | N/A             |
| T24         | NC                         | NC                    | N/A             |
| T25         | SXPVDD                     | Power                 | N/A             |
| T26         | SXPVSS                     | Ground                | N/A             |
| T27         | SD_C_RX                    | I                     | SXCVDD          |
| T28         | SD_C_RX                    | I                     | SXCVDD          |
| U1          | MAVDD                      | Power                 | N/A             |
| U2          | VSS                        | Ground                | N/A             |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| U3          | MCK1                       | O                     | GVDD            |
| U4          | GVDD                       | Power                 | N/A             |
| U5          | VSS                        | Ground                | N/A             |
| U6          | MBA1                       | O                     | GVDD            |
| U7          | GVDD                       | Power                 | N/A             |
| U8          | VSS                        | Ground                | N/A             |
| U9          | VDD                        | Power                 | N/A             |
| U10         | VSS                        | Ground                | N/A             |
| U11         | VDD                        | Power                 | N/A             |
| U12         | VSS                        | Ground                | N/A             |
| U13         | VDD                        | Power                 | N/A             |
| U14         | VSS                        | Ground                | N/A             |
| U15         | VDD                        | Power                 | N/A             |
| U16         | VSS                        | Ground                | N/A             |
| U17         | VDD                        | Power                 | N/A             |
| U18         | VSS                        | Ground                | N/A             |
| U19         | VDD                        | Power                 | N/A             |
| U20         | VSS                        | Ground                | N/A             |
| U21         | NC                         | NC                    | N/A             |
| U22         | NC                         | NC                    | N/A             |
| U23         | NC                         | NC                    | N/A             |
| U24         | NC                         | NC                    | N/A             |
| U25         | SD_D_TX                    | O                     | SXPVDD          |
| U26         | SD_D_TX                    | O                     | SXPVDD          |
| U27         | SXCVSS                     | Ground                | N/A             |
| U28         | SXCVDD                     | Power                 | N/A             |
| V1          | MVREF                      | Power                 | N/A             |
| V2          | VSS                        | Ground                | N/A             |
| V3          | MA8                        | O                     | GVDD            |
| V4          | MA2                        | O                     | GVDD            |
| V5          | MA6                        | O                     | GVDD            |
| V6          | MCKE1                      | O                     | GVDD            |
| V7          | VSS                        | Ground                | N/A             |
| V8          | GVDD                       | Power                 | N/A             |
| V9          | VSS                        | Ground                | N/A             |
| V10         | VDD                        | Power                 | N/A             |
| V11         | VSS                        | Ground                | N/A             |
| V12         | VDD                        | Power                 | N/A             |
| V13         | VSS                        | Ground                | N/A             |
| V14         | VDD                        | Power                 | N/A             |
| V15         | VSS                        | Ground                | N/A             |
| V16         | VDD                        | Power                 | N/A             |
| V17         | VSS                        | Ground                | N/A             |
| V18         | VDD                        | Power                 | N/A             |
| V19         | VSS                        | Ground                | N/A             |
| V20         | VDD                        | Power                 | N/A             |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| V21         | NC                         | NC                    | N/A             |
| V22         | NC                         | NC                    | N/A             |
| V23         | NC                         | NC                    | N/A             |
| V24         | NC                         | NC                    | N/A             |
| V25         | NC                         | NC                    | N/A             |
| V26         | NC                         | NC                    | N/A             |
| V27         | SD_D_RX                    | I                     | SXCVDD          |
| V28         | SD_D_RX                    | I                     | SXCVDD          |
| W1          | VSS                        | Ground                | N/A             |
| W2          | VSS                        | Ground                | N/A             |
| W3          | MA5                        | O                     | GVDD            |
| W4          | VSS                        | Ground                | N/A             |
| W5          | GVDD                       | Power                 | N/A             |
| W6          | MMDIC1                     | I/O                   | GVDD            |
| W7          | GVDD                       | Power                 | N/A             |
| W8          | VSS                        | Ground                | N/A             |
| W9          | VDD                        | Power                 | N/A             |
| W10         | VSS                        | Ground                | N/A             |
| W11         | M3VDD                      | Power                 | N/A             |
| W12         | VSS                        | Ground                | N/A             |
| W13         | M3VDD                      | Power                 | N/A             |
| W14         | VSS                        | Ground                | N/A             |
| W15         | M3VDD                      | Power                 | N/A             |
| W16         | VSS                        | Ground                | N/A             |
| W17         | CPRIVDD                    | Power                 | N/A             |
| W18         | VSS                        | Ground                | N/A             |
| W19         | VDD                        | Power                 | N/A             |
| W20         | VSS                        | Ground                | N/A             |
| W21         | NC                         | NC                    | N/A             |
| W22         | NC                         | NC                    | N/A             |
| W23         | NC                         | NC                    | N/A             |
| W24         | SD_PLL1_AVDD               | Power                 | N/A             |
| W25         | SD_PLL1_AGND               | Ground                | N/A             |
| W26         | NC                         | NC                    | N/A             |
| W27         | SXCVSS                     | Ground                | N/A             |
| W28         | SXCVDD                     | Power                 | N/A             |
| Y1          | MA11                       | O                     | GVDD            |
| Y2          | MA9                        | O                     | GVDD            |
| Y3          | MA12                       | O                     | GVDD            |
| Y4          | MA7                        | O                     | GVDD            |
| Y5          | NC                         | Non-user              | N/A             |
| Y6          | MMDIC0                     | I/O                   | GVDD            |
| Y7          | VSS                        | Ground                | N/A             |
| Y8          | GVDD                       | Power                 | N/A             |
| Y9          | VSS                        | Ground                | N/A             |
| Y10         | VDD                        | Power                 | N/A             |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| Y11         | VSS                        | Ground                | N/A             |
| Y12         | M3VDD                      | Power                 | N/A             |
| Y13         | VSS                        | Ground                | N/A             |
| Y14         | M3VDD                      | Power                 | N/A             |
| Y15         | VSS                        | Ground                | N/A             |
| Y16         | CPRIVDD                    | Power                 | N/A             |
| Y17         | VSS                        | Ground                | N/A             |
| Y18         | CPRIVDD                    | Power                 | N/A             |
| Y19         | VSS                        | Ground                | N/A             |
| Y20         | VDD                        | Power                 | N/A             |
| Y21         | NC                         | NC                    | N/A             |
| Y22         | NC                         | NC                    | N/A             |
| Y23         | NC                         | NC                    | N/A             |
| Y24         | NC                         | NC                    | N/A             |
| Y25         | NC                         | NC                    | N/A             |
| Y26         | NC                         | NC                    | N/A             |
| Y27         | SD_REF_CLK1                | I                     | SXCVDD          |
| Y28         | SD_REF_CLK1                | I                     | SXCVDD          |
| AA1         | MDQS8                      | I/O                   | GVDD            |
| AA2         | VSS                        | Ground                | N/A             |
| AA3         | MA14                       | O                     | GVDD            |
| AA4         | GVDD                       | Power                 | N/A             |
| AA5         | VSS                        | Ground                | N/A             |
| AA6         | MA15                       | O                     | GVDD            |
| AA7         | MCKE0                      | O                     | GVDD            |
| AA8         | VSS                        | Ground                | N/A             |
| AA9         | GVDD                       | Power                 | N/A             |
| AA10        | VSS                        | Ground                | N/A             |
| AA11        | M3VDD                      | Power                 | N/A             |
| AA12        | VSS                        | Ground                | N/A             |
| AA13        | M3VDD                      | Power                 | N/A             |
| AA14        | VSS                        | Ground                | N/A             |
| AA15        | CPRIVDD                    | Power                 | N/A             |
| AA16        | VSS                        | Ground                | N/A             |
| AA17        | CPRIVDD                    | Power                 | N/A             |
| AA18        | VSS                        | Ground                | N/A             |
| AA19        | CPRIVDD                    | Power                 | N/A             |
| AA20        | NC                         | NC                    | N/A             |
| AA21        | SD_IMP_CAL_TX              | I                     | SXPVDD          |
| AA22        | NC                         | NC                    | N/A             |
| AA23        | NC                         | NC                    | N/A             |
| AA24        | NC                         | NC                    | N/A             |
| AA25        | SD_E_TX                    | O                     | SXPVDD          |
| AA26        | SD_E_TX                    | O                     | SXPVDD          |
| AA27        | SXCVSS                     | Ground                | N/A             |
| AA28        | SXCVDD                     | Power                 | N/A             |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| AB1         | MDQS8                      | I/O                   | GVDD            |
| AB2         | MDM8                       | O                     | GVDD            |
| AB3         | MECC2                      | I/O                   | GVDD            |
| AB4         | MECC1                      | I/O                   | GVDD            |
| AB5         | NC                         | Non-user              | N/A             |
| AB6         | MAPAR_IN                   | I                     | GVDD            |
| AB7         | MBA2                       | O                     | GVDD            |
| AB8         | MDQ2                       | I/O                   | GVDD            |
| AB9         | MDQ1                       | I/O                   | GVDD            |
| AB10        | MDQ0                       | I/O                   | GVDD            |
| AB11        | VSS                        | Ground                | N/A             |
| AB12        | M3VDD                      | Power                 | N/A             |
| AB13        | VSS                        | Ground                | N/A             |
| AB14        | M3VDD                      | Power                 | N/A             |
| AB15        | VSS                        | Ground                | N/A             |
| AB16        | CPRIVDD                    | Power                 | N/A             |
| AB17        | VSS                        | Ground                | N/A             |
| AB18        | CPRIVDD                    | Power                 | N/A             |
| AB19        | NC                         | NC                    | N/A             |
| AB20        | NC                         | Non-user              | N/A             |
| AB21        | NC                         | NC                    | N/A             |
| AB22        | NC                         | NC                    | N/A             |
| AB23        | NC                         | NC                    | N/A             |
| AB24        | NC                         | NC                    | N/A             |
| AB25        | SXPVDD                     | Power                 | N/A             |
| AB26        | SXPVSS                     | Ground                | N/A             |
| AB27        | SD_E_RX                    | I                     | SXCVDD          |
| AB28        | SD_E_RX                    | I                     | SXCVDD          |
| AC1         | VSS                        | Ground                | N/A             |
| AC2         | GVDD                       | Power                 | N/A             |
| AC3         | MECC4                      | I/O                   | GVDD            |
| AC4         | VSS                        | Ground                | N/A             |
| AC5         | GVDD                       | Power                 | N/A             |
| AC6         | MDQ25                      | I/O                   | GVDD            |
| AC7         | VSS                        | Ground                | N/A             |
| AC8         | GVDD                       | Power                 | N/A             |
| AC9         | MDQ3                       | I/O                   | GVDD            |
| AC10        | VSS                        | Ground                | N/A             |
| AC11        | GVDD                       | Power                 | N/A             |
| AC12        | VSS                        | Ground                | N/A             |
| AC13        | M3VDD                      | Power                 | N/A             |
| AC14        | VSS                        | Ground                | N/A             |
| AC15        | CPRIVDD                    | Power                 | N/A             |
| AC16        | VSS                        | Ground                | N/A             |
| AC17        | NC                         | NC                    | N/A             |
| AC18        | NC                         | NC                    | N/A             |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| AC19        | NC                         | NC                    | N/A             |
| AC20        | NC                         | Non-user              | N/A             |
| AC21        | NC                         | NC                    | N/A             |
| AC22        | NC                         | NC                    | N/A             |
| AC23        | NC                         | NC                    | N/A             |
| AC24        | NC                         | NC                    | N/A             |
| AC25        | SD_F_TX                    | O                     | SXPVDD          |
| AC26        | SD_F_TX                    | O                     | SXPVDD          |
| AC27        | SXCVSS                     | Ground                | N/A             |
| AC28        | SXCVDD                     | Power                 | N/A             |
| AD1         | MECC7                      | I/O                   | GVDD            |
| AD2         | MECC6                      | I/O                   | GVDD            |
| AD3         | MECC0                      | I/O                   | GVDD            |
| AD4         | MECC5                      | I/O                   | GVDD            |
| AD5         | MECC3                      | I/O                   | GVDD            |
| AD6         | MDQ24                      | I/O                   | GVDD            |
| AD7         | MDM0                       | O                     | GVDD            |
| AD8         | MDQS0                      | I/O                   | GVDD            |
| AD9         | MDQS0                      | I/O                   | GVDD            |
| AD10        | MDQ4                       | I/O                   | GVDD            |
| AD11        | MDQ6                       | I/O                   | GVDD            |
| AD12        | VSS                        | Non-user              | N/A             |
| AD13        | VSS                        | Non-user              | N/A             |
| AD14        | VSS                        | Non-user              | N/A             |
| AD15        | VSS                        | Ground                | N/A             |
| AD16        | VSS                        | Ground                | N/A             |
| AD17        | NC                         | NC                    | N/A             |
| AD18        | SD_PLL2_AVDD               | Power                 | N/A             |
| AD19        | NC                         | NC                    | N/A             |
| AD20        | NC                         | NC                    | N/A             |
| AD21        | NC                         | NC                    | N/A             |
| AD22        | NC                         | NC                    | N/A             |
| AD23        | NC                         | NC                    | N/A             |
| AD24        | NC                         | NC                    | N/A             |
| AD25        | SXPVDD                     | Power                 | N/A             |
| AD26        | SXPVSS                     | Ground                | N/A             |
| AD27        | SD_F_RX                    | I                     | SXCVDD          |
| AD28        | SD_F_RX                    | I                     | SXCVDD          |
| AE1         | MDQS2                      | I/O                   | GVDD            |
| AE2         | VSS                        | Ground                | N/A             |
| AE3         | MDQ18                      | I/O                   | GVDD            |
| AE4         | GVDD                       | Power                 | N/A             |
| AE5         | VSS                        | Ground                | N/A             |
| AE6         | MDQ29                      | I/O                   | GVDD            |
| AE7         | GVDD                       | Power                 | N/A             |
| AE8         | VSS                        | Ground                | N/A             |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| AE9         | MDQ5                       | I/O                   | GVDD            |
| AE10        | GVDD                       | Power                 | N/A             |
| AE11        | VSS                        | Ground                | N/A             |
| AE12        | MDQ9                       | I/O                   | GVDD            |
| AE13        | VSS                        | Non-user              | N/A             |
| AE14        | VSS                        | Ground                | N/A             |
| AE15        | VSS                        | Ground                | N/A             |
| AE16        | VSS                        | Ground                | N/A             |
| AE17        | NC                         | NC                    | N/A             |
| AE18        | SD_PLL2_AGND               | Ground                | N/A             |
| AE19        | NC                         | NC                    | N/A             |
| AE20        | SD_J_TX                    | O                     | SXPVDD          |
| AE21        | SXPVDD                     | Power                 | N/A             |
| AE22        | SD_I_TX                    | O                     | SXPVDD          |
| AE23        | SXPVDD                     | Power                 | N/A             |
| AE24        | NC                         | NC                    | N/A             |
| AE25        | SD_G_TX                    | O                     | SXPVDD          |
| AE26        | SD_G_TX                    | O                     | SXPVDD          |
| AE27        | SXCVSS                     | Ground                | N/A             |
| AE28        | SXCVDD                     | Power                 | N/A             |
| AF1         | MDQS2                      | I/O                   | GVDD            |
| AF2         | MDQ17                      | I/O                   | GVDD            |
| AF3         | MDQ21                      | I/O                   | GVDD            |
| AF4         | MDQ16                      | I/O                   | GVDD            |
| AF5         | MDQ30                      | I/O                   | GVDD            |
| AF6         | MDQ27                      | I/O                   | GVDD            |
| AF7         | MDQ28                      | I/O                   | GVDD            |
| AF8         | MDQ7                       | I/O                   | GVDD            |
| AF9         | MDQ14                      | I/O                   | GVDD            |
| AF10        | MDQ11                      | I/O                   | GVDD            |
| AF11        | MDQ8                       | I/O                   | GVDD            |
| AF12        | MDQ10                      | I/O                   | GVDD            |
| AF13        | VSS                        | Non-user              | N/A             |
| AF14        | VSS                        | Ground                | N/A             |
| AF15        | VSS                        | Ground                | N/A             |
| AF16        | VSS                        | Ground                | N/A             |
| AF17        | NC                         | NC                    | N/A             |
| AF18        | NC                         | NC                    | N/A             |
| AF19        | NC                         | NC                    | N/A             |
| AF20        | SD_J_TX                    | O                     | SXPVDD          |
| AF21        | SXPVSS                     | Ground                | N/A             |
| AF22        | SD_I_TX                    | O                     | SXPVDD          |
| AF23        | SXPVSS                     | Ground                | N/A             |
| AF24        | NC                         | NC                    | N/A             |
| AF25        | SXPVDD                     | Power                 | N/A             |
| AF26        | SXPVSS                     | Ground                | N/A             |

Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| AF27        | SD_G_RX                    | I                     | SXCVDD          |
| AF28        | SD_G_RX                    | I                     | SXCVDD          |
| AG1         | VSS                        | Ground                | N/A             |
| AG2         | GVDD                       | Power                 | N/A             |
| AG3         | MDQ22                      | I/O                   | GVDD            |
| AG4         | VSS                        | Ground                | N/A             |
| AG5         | GVDD                       | Power                 | N/A             |
| AG6         | MDQ26                      | I/O                   | GVDD            |
| AG7         | VSS                        | Ground                | N/A             |
| AG8         | GVDD                       | Power                 | N/A             |
| AG9         | MDQ13                      | I/O                   | GVDD            |
| AG10        | VSS                        | Ground                | N/A             |
| AG11        | GVDD                       | Power                 | N/A             |
| AG12        | MDQ12                      | I/O                   | GVDD            |
| AG13        | VSS                        | Ground                | N/A             |
| AG14        | VSS                        | Ground                | N/A             |
| AG15        | VSS                        | Ground                | N/A             |
| AG16        | VSS                        | Ground                | N/A             |
| AG17        | NC                         | NC                    | N/A             |
| AG18        | SXCVSS                     | Ground                | N/A             |
| AG19        | SD_REF_CLK2                | I                     | SXCVDD          |
| AG20        | SXCVSS                     | Ground                | N/A             |
| AG21        | SD_J_RX                    | I                     | SXCVDD          |
| AG22        | SXCVSS                     | Ground                | N/A             |
| AG23        | SD_I_RX                    | I                     | SXCVDD          |
| AG24        | SXCVSS                     | Ground                | N/A             |
| AG25        | SD_H_TX                    | O                     | SXPVDD          |
| AG26        | SD_H_TX                    | O                     | SXPVDD          |
| AG27        | SXCVSS                     | Ground                | N/A             |
| AG28        | SXCVDD                     | Power                 | N/A             |
| AH1         | MDQ20                      | I/O                   | GVDD            |
| AH2         | MDQ19                      | I/O                   | GVDD            |
| AH3         | MDQ23                      | I/O                   | GVDD            |
| AH4         | MDM2                       | O                     | GVDD            |
| AH5         | MDQS3                      | I/O                   | GVDD            |
| AH6         | MDQS3                      | I/O                   | GVDD            |
| AH7         | MDM3                       | O                     | GVDD            |
| AH8         | MDQ31                      | I/O                   | GVDD            |
| AH9         | MDQS1                      | I/O                   | GVDD            |
| AH10        | MDQS1                      | I/O                   | GVDD            |
| AH11        | MDQ15                      | I/O                   | GVDD            |
| AH12        | MDM1                       | O                     | GVDD            |
| AH13        | VSS                        | Ground                | N/A             |
| AH14        | PLL0_AVDD                  | Power                 | N/A             |
| AH15        | PLL1_AVDD                  | Power                 | N/A             |
| AH16        | PLL2_AVDD                  | Power                 | N/A             |

Table 1. Signal List by Ball Number (continued)

| Ball Number                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-----------------------|-----------------|
| AH17                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | NC                         | NC                    | N/A             |
| AH18                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | SXCVDD                     | Power                 | N/A             |
| AH19                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | SD_REF_CLK2                | I                     | SXCVDD          |
| AH20                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | SXCVDD                     | Power                 | N/A             |
| AH21                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | SD_J_RX                    | I                     | SXCVDD          |
| AH22                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | SXCVDD                     | Power                 | N/A             |
| AH23                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | SD_I_RX                    | I                     | SXCVDD          |
| AH24                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | SXCVDD                     | Power                 | N/A             |
| AH25                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | SXPVDD                     | Power                 | N/A             |
| AH26                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | SXPVSS                     | Ground                | N/A             |
| AH27                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | SD_H_RX                    | I                     | SXCVDD          |
| AH28                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | SD_H_RX                    | I                     | SXCVDD          |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. Signal function during power-on reset is determined by the RCW source type. Selection of RapidIO, SGMII, CPRI, and PCI Express functionality during normal operation is configured by the RCW bit values. Selection of the GPIO function and other functions is done by GPIO register setup. For signals with GPIO functionality, the open-drain and internal 20 K<math>\Omega</math> pull-up resistor can be configured by GPIO register programming. For configuration details, see the <i>GPIO</i> chapter in the <i>MSC8157 Reference Manual</i>.</li> <li>2. NC signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS or SXCVSS), or pulled up (VDD).</li> <li>3. Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected; non-user = connect as specified under Signal Name.</li> <li>4. Connect power inputs to the power supplies via external filters. See the <i>MSC8157 Design Checklist</i> (AN4110) for details.</li> </ol> |                            |                       |                 |

Table 2. Signal List by Primary Signal Name

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| A18         | CLKIN                      | I                     | QVDD            |
| A13         | CLKOUT                     | O                     | QVDD            |
| AA15        | CPRIVDD                    | Power                 | N/A             |
| AA17        | CPRIVDD                    | Power                 | N/A             |
| AA19        | CPRIVDD                    | Power                 | N/A             |
| AB16        | CPRIVDD                    | Power                 | N/A             |
| AB18        | CPRIVDD                    | Power                 | N/A             |
| AC15        | CPRIVDD                    | Power                 | N/A             |
| W17         | CPRIVDD                    | Power                 | N/A             |
| Y16         | CPRIVDD                    | Power                 | N/A             |
| Y18         | CPRIVDD                    | Power                 | N/A             |
| N11         | CRPEVDD                    | Power                 | N/A             |
| N7          | CRPEVDD                    | Power                 | N/A             |
| N9          | CRPEVDD                    | Power                 | N/A             |
| P10         | CRPEVDD                    | Power                 | N/A             |
| P8          | CRPEVDD                    | Power                 | N/A             |
| R11         | CRPEVDD                    | Power                 | N/A             |
| C16         | DFT_TEST                   | I                     | QVDD            |
| A14         | EE0                        | I                     | QVDD            |
| C14         | EE1                        | O                     | QVDD            |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| B26         | GE_MDC                     | O                     | NVDD            |
| C27         | GE_MDIO                    | I/O                   | NVDD            |
| A23         | GE1_GTX_CLK                | O                     | NVDD            |
| H22         | GE1_RD0                    | I                     | NVDD            |
| H24         | GE1_RD1                    | I                     | NVDD            |
| G21         | GE1_RD2                    | I                     | NVDD            |
| G20         | GE1_RD3                    | I                     | NVDD            |
| G22         | GE1_RX_CLK                 | I                     | NVDD            |
| G24         | GE1_RX_CTL                 | I                     | NVDD            |
| A24         | GE1_TD0                    | O                     | NVDD            |
| A27         | GE1_TD1                    | O                     | NVDD            |
| A26         | GE1_TD2                    | O                     | NVDD            |
| A28         | GE1_TD3                    | O                     | NVDD            |
| A25         | GE1_TX_CLK                 | I                     | NVDD            |
| A22         | GE1_TX_CTL                 | O                     | NVDD            |
| C21         | GE2_GTX_CLK/CP_LOS4        | I/O                   | NVDD            |
| F21         | GE2_RD0/CP_LOS6            | I                     | NVDD            |
| F23         | GE2_RD1                    | I                     | NVDD            |
| F19         | GE2_RD2/CP_LOS1            | I                     | NVDD            |
| E20         | GE2_RD3/CP_LOS2            | I                     | NVDD            |
| F22         | GE2_RX_CLK                 | I                     | NVDD            |
| F20         | GE2_RX_CTL                 | I                     | NVDD            |
| C24         | GE2_TD0                    | O                     | NVDD            |
| C23         | GE2_TD1                    | O                     | NVDD            |
| C20         | GE2_TD2/CP_LOS3            | I/O                   | NVDD            |
| D22         | GE2_TD3/CP_LOS5            | I/O                   | NVDD            |
| B20         | GE2_TX_CLK                 | I                     | NVDD            |
| C22         | GE2_TX_CTL                 | O                     | NVDD            |
| E26         | GPIO0/IRQ0/RC0/CP_SYNC1    | I/O                   | NVDD            |
| E28         | GPIO1/IRQ1/RC1/CP_SYNC2    | I/O                   | NVDD            |
| D28         | GPIO10/IRQ10/RC10          | I/O                   | NVDD            |
| G28         | GPIO11/IRQ11/RC11          | I/O                   | NVDD            |
| H28         | GPIO12/IRQ12/RC12          | I/O                   | NVDD            |
| D20         | GPIO13/IRQ13/RC13          | I/O                   | NVDD            |
| H26         | GPIO14/DRQ0/IRQ14/RC14     | I/O                   | NVDD            |
| C19         | GPIO15/DDN0/IRQ15/RC15     | I/O                   | NVDD            |
| D26         | GPIO16/TMR5/RC16           | I/O                   | NVDD            |
| E27         | GPIO17/SPI_SCK/CP_LOS3     | I/O                   | NVDD            |
| B28         | GPIO18/SPI_MOSI/CP_LOS4    | I/O                   | NVDD            |
| G26         | GPIO19/SPI_MISO/CP_LOS5    | I/O                   | NVDD            |
| K28         | GPIO2/IRQ2/RC2/CP_SYNC3    | I/O                   | NVDD            |
| C26         | GPIO20/SPI_SL/CP_LOS6      | I/O                   | NVDD            |
| C28         | GPIO21/TMR6                | I/O                   | NVDD            |
| F26         | GPIO22                     | I/O                   | NVDD            |
| F27         | GPIO23/TMR0/BOOT_SPI_SL    | I/O                   | NVDD            |
| J22         | GPIO24/TMR1/RCW_SRC2       | I/O                   | NVDD            |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| B24         | GPIO25/TMR2/RCW_SRC1       | I/O                   | NVDD            |
| F24         | GPIO26/TMR3                | I/O                   | NVDD            |
| E24         | GPIO27/TMR4/RCW_SRC0       | I/O                   | NVDD            |
| G19         | GPIO28/UART_RXD/CP_LOS1    | I/O                   | NVDD            |
| A20         | GPIO29/UART_TXD/CP_LOS2    | I/O                   | NVDD            |
| J28         | GPIO3/DRQ1/IRQ3/RC3        | I/O                   | NVDD            |
| C25         | GPIO30/I2C_SCL             | I/O                   | NVDD            |
| A21         | GPIO31/I2C_SDA             | I/O                   | NVDD            |
| K22         | GPIO4/DDN1/IRQ4/RC4        | I/O                   | NVDD            |
| D24         | GPIO5/IRQ5/RC5/CP_SYNC4    | I/O                   | NVDD            |
| F25         | GPIO6/IRQ6/RC6/CP_SYNC5    | I/O                   | NVDD            |
| K26         | GPIO7/IRQ7/RC7/CP_SYNC6    | I/O                   | NVDD            |
| F28         | GPIO8/IRQ8/RC8             | I/O                   | NVDD            |
| J23         | GPIO9/IRQ9/RC9             | I/O                   | NVDD            |
| A4          | GVDD                       | Power                 | N/A             |
| A7          | GVDD                       | Power                 | N/A             |
| AA4         | GVDD                       | Power                 | N/A             |
| AA9         | GVDD                       | Power                 | N/A             |
| AC11        | GVDD                       | Power                 | N/A             |
| AC2         | GVDD                       | Power                 | N/A             |
| AC5         | GVDD                       | Power                 | N/A             |
| AC8         | GVDD                       | Power                 | N/A             |
| AE10        | GVDD                       | Power                 | N/A             |
| AE4         | GVDD                       | Power                 | N/A             |
| AE7         | GVDD                       | Power                 | N/A             |
| AG11        | GVDD                       | Power                 | N/A             |
| AG2         | GVDD                       | Power                 | N/A             |
| AG5         | GVDD                       | Power                 | N/A             |
| AG8         | GVDD                       | Power                 | N/A             |
| C2          | GVDD                       | Power                 | N/A             |
| C5          | GVDD                       | Power                 | N/A             |
| E4          | GVDD                       | Power                 | N/A             |
| E7          | GVDD                       | Power                 | N/A             |
| G2          | GVDD                       | Power                 | N/A             |
| G5          | GVDD                       | Power                 | N/A             |
| J4          | GVDD                       | Power                 | N/A             |
| L2          | GVDD                       | Power                 | N/A             |
| L5          | GVDD                       | Power                 | N/A             |
| N4          | GVDD                       | Power                 | N/A             |
| R2          | GVDD                       | Power                 | N/A             |
| R5          | GVDD                       | Power                 | N/A             |
| R7          | GVDD                       | Power                 | N/A             |
| T8          | GVDD                       | Power                 | N/A             |
| U4          | GVDD                       | Power                 | N/A             |
| U7          | GVDD                       | Power                 | N/A             |
| V8          | GVDD                       | Power                 | N/A             |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| W5          | GVDD                       | Power                 | N/A             |
| W7          | GVDD                       | Power                 | N/A             |
| Y8          | GVDD                       | Power                 | N/A             |
| E16         | HRESET                     | I/O                   | QVDD            |
| D17         | HRESET_IN                  | I                     | QVDD            |
| E15         | INT_OUT/CP_TX_INT          | O                     | QVDD            |
| AA11        | M3VDD                      | Power                 | N/A             |
| AA13        | M3VDD                      | Power                 | N/A             |
| AB12        | M3VDD                      | Power                 | N/A             |
| AB14        | M3VDD                      | Power                 | N/A             |
| AC13        | M3VDD                      | Power                 | N/A             |
| W11         | M3VDD                      | Power                 | N/A             |
| W13         | M3VDD                      | Power                 | N/A             |
| W15         | M3VDD                      | Power                 | N/A             |
| Y12         | M3VDD                      | Power                 | N/A             |
| Y14         | M3VDD                      | Power                 | N/A             |
| R3          | MA0                        | O                     | GVDD            |
| T4          | MA1                        | O                     | GVDD            |
| P2          | MA10                       | O                     | GVDD            |
| Y1          | MA11                       | O                     | GVDD            |
| Y3          | MA12                       | O                     | GVDD            |
| M3          | MA13                       | O                     | GVDD            |
| AA3         | MA14                       | O                     | GVDD            |
| AA6         | MA15                       | O                     | GVDD            |
| V4          | MA2                        | O                     | GVDD            |
| T5          | MA3                        | O                     | GVDD            |
| P4          | MA4                        | O                     | GVDD            |
| W3          | MA5                        | O                     | GVDD            |
| V5          | MA6                        | O                     | GVDD            |
| Y4          | MA7                        | O                     | GVDD            |
| V3          | MA8                        | O                     | GVDD            |
| Y2          | MA9                        | O                     | GVDD            |
| AB6         | MAPAR_IN                   | I                     | GVDD            |
| T6          | MAPAR_OUT                  | O                     | GVDD            |
| U1          | MAVDD                      | Power                 | N/A             |
| R6          | MBA0                       | O                     | GVDD            |
| U6          | MBA1                       | O                     | GVDD            |
| AB7         | MBA2                       | O                     | GVDD            |
| K1          | MCAS                       | O                     | GVDD            |
| M1          | MCK0                       | O                     | GVDD            |
| M2          | MCK0                       | O                     | GVDD            |
| T3          | MCK1                       | O                     | GVDD            |
| U3          | MCK1                       | O                     | GVDD            |
| P1          | MCK2                       | O                     | GVDD            |
| R1          | MCK2                       | O                     | GVDD            |
| AA7         | MCKE0                      | O                     | GVDD            |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| V6          | MCKE1                      | O                     | GVDD            |
| A16         | MCLKIN (optional)          | I                     | QVDD            |
| K2          | MCS0                       | O                     | GVDD            |
| K3          | MCS1                       | O                     | GVDD            |
| AD7         | MDM0                       | O                     | GVDD            |
| AH12        | MDM1                       | O                     | GVDD            |
| AH4         | MDM2                       | O                     | GVDD            |
| AH7         | MDM3                       | O                     | GVDD            |
| L6          | MDM4                       | O                     | GVDD            |
| G3          | MDM5                       | O                     | GVDD            |
| F7          | MDM6                       | O                     | GVDD            |
| C6          | MDM7                       | O                     | GVDD            |
| AB2         | MDM8                       | O                     | GVDD            |
| AB10        | MDQ0                       | I/O                   | GVDD            |
| AB9         | MDQ1                       | I/O                   | GVDD            |
| AF12        | MDQ10                      | I/O                   | GVDD            |
| AF10        | MDQ11                      | I/O                   | GVDD            |
| AG12        | MDQ12                      | I/O                   | GVDD            |
| AG9         | MDQ13                      | I/O                   | GVDD            |
| AF9         | MDQ14                      | I/O                   | GVDD            |
| AH11        | MDQ15                      | I/O                   | GVDD            |
| AF4         | MDQ16                      | I/O                   | GVDD            |
| AF2         | MDQ17                      | I/O                   | GVDD            |
| AE3         | MDQ18                      | I/O                   | GVDD            |
| AH2         | MDQ19                      | I/O                   | GVDD            |
| AB8         | MDQ2                       | I/O                   | GVDD            |
| AH1         | MDQ20                      | I/O                   | GVDD            |
| AF3         | MDQ21                      | I/O                   | GVDD            |
| AG3         | MDQ22                      | I/O                   | GVDD            |
| AH3         | MDQ23                      | I/O                   | GVDD            |
| AD6         | MDQ24                      | I/O                   | GVDD            |
| AC6         | MDQ25                      | I/O                   | GVDD            |
| AG6         | MDQ26                      | I/O                   | GVDD            |
| AF6         | MDQ27                      | I/O                   | GVDD            |
| AF7         | MDQ28                      | I/O                   | GVDD            |
| AE6         | MDQ29                      | I/O                   | GVDD            |
| AC9         | MDQ3                       | I/O                   | GVDD            |
| AF5         | MDQ30                      | I/O                   | GVDD            |
| AH8         | MDQ31                      | I/O                   | GVDD            |
| K5          | MDQ32                      | I/O                   | GVDD            |
| J5          | MDQ33                      | I/O                   | GVDD            |
| K6          | MDQ34                      | I/O                   | GVDD            |
| J3          | MDQ35                      | I/O                   | GVDD            |
| J6          | MDQ36                      | I/O                   | GVDD            |
| J1          | MDQ37                      | I/O                   | GVDD            |
| H1          | MDQ38                      | I/O                   | GVDD            |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| K4          | MDQ39                      | I/O                   | GVDD            |
| AD10        | MDQ4                       | I/O                   | GVDD            |
| F1          | MDQ40                      | I/O                   | GVDD            |
| F2          | MDQ41                      | I/O                   | GVDD            |
| H6          | MDQ42                      | I/O                   | GVDD            |
| F5          | MDQ43                      | I/O                   | GVDD            |
| H4          | MDQ44                      | I/O                   | GVDD            |
| H5          | MDQ45                      | I/O                   | GVDD            |
| G6          | MDQ46                      | I/O                   | GVDD            |
| F6          | MDQ47                      | I/O                   | GVDD            |
| D2          | MDQ48                      | I/O                   | GVDD            |
| D1          | MDQ49                      | I/O                   | GVDD            |
| AE9         | MDQ5                       | I/O                   | GVDD            |
| D5          | MDQ50                      | I/O                   | GVDD            |
| D6          | MDQ51                      | I/O                   | GVDD            |
| D7          | MDQ52                      | I/O                   | GVDD            |
| E1          | MDQ53                      | I/O                   | GVDD            |
| E6          | MDQ54                      | I/O                   | GVDD            |
| E3          | MDQ55                      | I/O                   | GVDD            |
| B7          | MDQ56                      | I/O                   | GVDD            |
| A3          | MDQ57                      | I/O                   | GVDD            |
| B6          | MDQ58                      | I/O                   | GVDD            |
| B2          | MDQ59                      | I/O                   | GVDD            |
| AD11        | MDQ6                       | I/O                   | GVDD            |
| B1          | MDQ60                      | I/O                   | GVDD            |
| C3          | MDQ61                      | I/O                   | GVDD            |
| B5          | MDQ62                      | I/O                   | GVDD            |
| A6          | MDQ63                      | I/O                   | GVDD            |
| AF8         | MDQ7                       | I/O                   | GVDD            |
| AF11        | MDQ8                       | I/O                   | GVDD            |
| AE12        | MDQ9                       | I/O                   | GVDD            |
| AD8         | MDQS0                      | I/O                   | GVDD            |
| AD9         | MDQS0                      | I/O                   | GVDD            |
| AH10        | MDQS1                      | I/O                   | GVDD            |
| AH9         | MDQS1                      | I/O                   | GVDD            |
| AE1         | MDQS2                      | I/O                   | GVDD            |
| AF1         | MDQS2                      | I/O                   | GVDD            |
| AH5         | MDQS3                      | I/O                   | GVDD            |
| AH6         | MDQS3                      | I/O                   | GVDD            |
| H2          | MDQS4                      | I/O                   | GVDD            |
| H3          | MDQS4                      | I/O                   | GVDD            |
| F3          | MDQS5                      | I/O                   | GVDD            |
| F4          | MDQS5                      | I/O                   | GVDD            |
| D3          | MDQS6                      | I/O                   | GVDD            |
| D4          | MDQS6                      | I/O                   | GVDD            |
| B3          | MDQS7                      | I/O                   | GVDD            |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| B4          | MDQS7                      | I/O                   | GVDD            |
| AA1         | MDQS8                      | I/O                   | GVDD            |
| AB1         | $\overline{\text{MDQS8}}$  | I/O                   | GVDD            |
| AD3         | MECC0                      | I/O                   | GVDD            |
| AB4         | MECC1                      | I/O                   | GVDD            |
| AB3         | MECC2                      | I/O                   | GVDD            |
| AD5         | MECC3                      | I/O                   | GVDD            |
| AC3         | MECC4                      | I/O                   | GVDD            |
| AD4         | MECC5                      | I/O                   | GVDD            |
| AD2         | MECC6                      | I/O                   | GVDD            |
| AD1         | MECC7                      | I/O                   | GVDD            |
| Y6          | MMDIC0                     | I/O                   | GVDD            |
| W6          | MMDIC1                     | I/O                   | GVDD            |
| P6          | MODT0                      | O                     | GVDD            |
| N6          | MODT1                      | O                     | GVDD            |
| N1          | $\overline{\text{MRAS}}$   | O                     | GVDD            |
| V1          | MVREF                      | Power                 | N/A             |
| M4          | $\overline{\text{MWE}}$    | O                     | GVDD            |
| A10         | NC                         | Non-user              | N/A             |
| A11         | NC                         | Non-user              | N/A             |
| A12         | NC                         | Non-user              | N/A             |
| A8          | NC                         | Non-user              | N/A             |
| A9          | NC                         | Non-user              | N/A             |
| AA20        | NC                         | NC                    | N/A             |
| AA22        | NC                         | NC                    | N/A             |
| AA23        | NC                         | NC                    | N/A             |
| AA24        | NC                         | NC                    | N/A             |
| AB19        | NC                         | NC                    | N/A             |
| AB20        | NC                         | Non-user              | N/A             |
| AB21        | NC                         | NC                    | N/A             |
| AB22        | NC                         | NC                    | N/A             |
| AB23        | NC                         | NC                    | N/A             |
| AB24        | NC                         | NC                    | N/A             |
| AB5         | NC                         | Non-user              | N/A             |
| AC17        | NC                         | NC                    | N/A             |
| AC18        | NC                         | NC                    | N/A             |
| AC19        | NC                         | NC                    | N/A             |
| AC20        | NC                         | Non-user              | N/A             |
| AC21        | NC                         | NC                    | N/A             |
| AC22        | NC                         | NC                    | N/A             |
| AC23        | NC                         | NC                    | N/A             |
| AC24        | NC                         | NC                    | N/A             |
| AD17        | NC                         | NC                    | N/A             |
| AD19        | NC                         | NC                    | N/A             |
| AD20        | NC                         | NC                    | N/A             |
| AD21        | NC                         | NC                    | N/A             |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| AD22        | NC                         | NC                    | N/A             |
| AD23        | NC                         | NC                    | N/A             |
| AD24        | NC                         | NC                    | N/A             |
| AE17        | NC                         | NC                    | N/A             |
| AE19        | NC                         | NC                    | N/A             |
| AE24        | NC                         | NC                    | N/A             |
| AF17        | NC                         | NC                    | N/A             |
| AF18        | NC                         | NC                    | N/A             |
| AF19        | NC                         | NC                    | N/A             |
| AF24        | NC                         | NC                    | N/A             |
| AG17        | NC                         | NC                    | N/A             |
| AH17        | NC                         | NC                    | N/A             |
| B10         | NC                         | Non-user              | N/A             |
| B12         | NC                         | Non-user              | N/A             |
| B8          | NC                         | Non-user              | N/A             |
| C10         | NC                         | Non-user              | N/A             |
| C11         | NC                         | Non-user              | N/A             |
| C12         | NC                         | Non-user              | N/A             |
| C13         | NC                         | Non-user              | N/A             |
| C15         | NC                         | Non-user              | N/A             |
| C8          | NC                         | Non-user              | N/A             |
| C9          | NC                         | Non-user              | N/A             |
| D10         | NC                         | Non-user              | N/A             |
| D12         | NC                         | Non-user              | N/A             |
| D14         | NC                         | Non-user              | N/A             |
| D8          | NC                         | Non-user              | N/A             |
| E10         | NC                         | Non-user              | N/A             |
| E11         | NC                         | Non-user              | N/A             |
| E12         | NC                         | Non-user              | N/A             |
| E13         | NC                         | Non-user              | N/A             |
| E14         | NC                         | Non-user              | N/A             |
| E9          | NC                         | Non-user              | N/A             |
| F11         | NC                         | Non-user              | N/A             |
| F12         | NC                         | Non-user              | N/A             |
| F14         | NC                         | Non-user              | N/A             |
| G11         | NC                         | Non-user              | N/A             |
| G12         | NC                         | Non-user              | N/A             |
| G13         | NC                         | Non-user              | N/A             |
| G14         | NC                         | Non-user              | N/A             |
| H13         | NC                         | Non-user              | N/A             |
| L22         | NC                         | NC                    | N/A             |
| L23         | NC                         | NC                    | N/A             |
| L3          | NC                         | Non-user              | N/A             |
| M21         | NC                         | NC                    | N/A             |
| M22         | NC                         | NC                    | N/A             |
| M5          | NC                         | Non-user              | N/A             |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup>               | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|------------------------------------------|-----------------------|-----------------|
| M6          | NC                                       | Non-user              | N/A             |
| N21         | NC                                       | NC                    | N/A             |
| N22         | NC                                       | NC                    | N/A             |
| N3          | NC                                       | Non-user              | N/A             |
| P21         | NC                                       | NC                    | N/A             |
| P23         | NC                                       | NC                    | N/A             |
| P24         | NC                                       | NC                    | N/A             |
| P3          | NC                                       | Non-user              | N/A             |
| P5          | NC                                       | Non-user              | N/A             |
| R21         | NC                                       | NC                    | N/A             |
| R22         | NC                                       | NC                    | N/A             |
| R23         | NC                                       | NC                    | N/A             |
| R24         | NC                                       | NC                    | N/A             |
| T21         | NC                                       | NC                    | N/A             |
| T22         | NC                                       | Non-user              | N/A             |
| T23         | NC                                       | Non-user              | N/A             |
| T24         | NC                                       | NC                    | N/A             |
| U21         | NC                                       | NC                    | N/A             |
| U22         | NC                                       | NC                    | N/A             |
| U23         | NC                                       | NC                    | N/A             |
| U24         | NC                                       | NC                    | N/A             |
| V21         | NC                                       | NC                    | N/A             |
| V22         | NC                                       | NC                    | N/A             |
| V23         | NC                                       | NC                    | N/A             |
| V24         | NC                                       | NC                    | N/A             |
| V25         | NC                                       | NC                    | N/A             |
| V26         | NC                                       | NC                    | N/A             |
| W21         | NC                                       | NC                    | N/A             |
| W22         | NC                                       | NC                    | N/A             |
| W23         | NC                                       | NC                    | N/A             |
| W26         | NC                                       | NC                    | N/A             |
| Y21         | NC                                       | NC                    | N/A             |
| Y22         | NC                                       | NC                    | N/A             |
| Y23         | NC                                       | NC                    | N/A             |
| Y24         | NC                                       | NC                    | N/A             |
| Y25         | NC                                       | NC                    | N/A             |
| Y26         | NC                                       | NC                    | N/A             |
| Y5          | NC                                       | Non-user              | N/A             |
| D15         | $\overline{\text{NMI}}$                  | I                     | QVDD            |
| F15         | $\overline{\text{NMI\_OUT/CP\_RX\_INT}}$ | O                     | QVDD            |
| D21         | NVDD                                     | Power                 | N/A             |
| D25         | NVDD                                     | Power                 | N/A             |
| E19         | NVDD                                     | Power                 | N/A             |
| E23         | NVDD                                     | Power                 | N/A             |
| G25         | NVDD                                     | Power                 | N/A             |
| H20         | NVDD                                     | Power                 | N/A             |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup>          | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|-------------------------------------|-----------------------|-----------------|
| H23         | NVDD                                | Power                 | N/A             |
| H27         | NVDD                                | Power                 | N/A             |
| J21         | NVDD                                | Power                 | N/A             |
| K25         | NVDD                                | Power                 | N/A             |
| L21         | NVDD                                | Power                 | N/A             |
| AH14        | PLL0_AVDD                           | Power                 | N/A             |
| AH15        | PLL1_AVDD                           | Power                 | N/A             |
| AH16        | PLL2_AVDD                           | Power                 | N/A             |
| C17         | $\overline{\text{PORESET}}$         | I                     | QVDD            |
| G15         | QVDD                                | Power                 | N/A             |
| H14         | QVDD                                | Power                 | N/A             |
| J27         | RC21                                | I                     | NVDD            |
| J24         | $\overline{\text{RCW\_LSEL0/RC17}}$ | I/O                   | NVDD            |
| K24         | $\overline{\text{RCW\_LSEL1/RC18}}$ | I/O                   | NVDD            |
| J26         | $\overline{\text{RCW\_LSEL2/RC19}}$ | I/O                   | NVDD            |
| J25         | $\overline{\text{RCW\_LSEL3/RC20}}$ | I/O                   | NVDD            |
| M27         | $\overline{\text{SD\_A\_RX}}$       | I                     | SXCVDD          |
| M28         | SD_A_RX                             | I                     | SXCVDD          |
| M23         | SD_A_TX                             | O                     | SXPVDD          |
| M24         | $\overline{\text{SD\_A\_TX}}$       | O                     | SXPVDD          |
| P27         | $\overline{\text{SD\_B\_RX}}$       | I                     | SXCVDD          |
| P28         | SD_B_RX                             | I                     | SXCVDD          |
| N25         | SD_B_TX                             | O                     | SXPVDD          |
| N26         | $\overline{\text{SD\_B\_TX}}$       | O                     | SXPVDD          |
| T27         | $\overline{\text{SD\_C\_RX}}$       | I                     | SXCVDD          |
| T28         | SD_C_RX                             | I                     | SXCVDD          |
| R25         | SD_C_TX                             | O                     | SXPVDD          |
| R26         | $\overline{\text{SD\_C\_TX}}$       | O                     | SXPVDD          |
| V27         | $\overline{\text{SD\_D\_RX}}$       | I                     | SXCVDD          |
| V28         | SD_D_RX                             | I                     | SXCVDD          |
| U25         | SD_D_TX                             | O                     | SXPVDD          |
| U26         | $\overline{\text{SD\_D\_TX}}$       | O                     | SXPVDD          |
| AB27        | $\overline{\text{SD\_E\_RX}}$       | I                     | SXCVDD          |
| AB28        | SD_E_RX                             | I                     | SXCVDD          |
| AA25        | SD_E_TX                             | O                     | SXPVDD          |
| AA26        | $\overline{\text{SD\_E\_TX}}$       | O                     | SXPVDD          |
| AD27        | $\overline{\text{SD\_F\_RX}}$       | I                     | SXCVDD          |
| AD28        | SD_F_RX                             | I                     | SXCVDD          |
| AC25        | SD_F_TX                             | O                     | SXPVDD          |
| AC26        | $\overline{\text{SD\_F\_TX}}$       | O                     | SXPVDD          |
| AF27        | $\overline{\text{SD\_G\_RX}}$       | I                     | SXCVDD          |
| AF28        | SD_G_RX                             | I                     | SXCVDD          |
| AE25        | SD_G_TX                             | O                     | SXPVDD          |
| AE26        | $\overline{\text{SD\_G\_TX}}$       | O                     | SXPVDD          |
| AH27        | $\overline{\text{SD\_H\_RX}}$       | I                     | SXCVDD          |
| AH28        | SD_H_RX                             | I                     | SXCVDD          |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup>        | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|-----------------------------------|-----------------------|-----------------|
| AG25        | SD_H_TX                           | O                     | SXPVDD          |
| AG26        | $\overline{\text{SD\_H\_TX}}$     | O                     | SXPVDD          |
| AG23        | $\overline{\text{SD\_I\_RX}}$     | I                     | SXCVDD          |
| AH23        | SD_I_RX                           | I                     | SXCVDD          |
| AE22        | SD_I_TX                           | O                     | SXPVDD          |
| AF22        | $\overline{\text{SD\_I\_TX}}$     | O                     | SXPVDD          |
| P22         | SD_IMP_CAL_RX                     | I                     | SXCVDD          |
| AA21        | SD_IMP_CAL_TX                     | I                     | SXPVDD          |
| AG21        | $\overline{\text{SD\_J\_RX}}$     | I                     | SXCVDD          |
| AH21        | SD_J_RX                           | I                     | SXCVDD          |
| AE20        | SD_J_TX                           | O                     | SXPVDD          |
| AF20        | $\overline{\text{SD\_J\_TX}}$     | O                     | SXPVDD          |
| W25         | SD_PLL1_AGND                      | Ground                | N/A             |
| W24         | SD_PLL1_AVDD                      | Power                 | N/A             |
| AE18        | SD_PLL2_AGND                      | Ground                | N/A             |
| AD18        | SD_PLL2_AVDD                      | Power                 | N/A             |
| Y27         | SD_REF_CLK1                       | I                     | SXCVDD          |
| Y28         | $\overline{\text{SD\_REF\_CLK1}}$ | I                     | SXCVDD          |
| AG19        | $\overline{\text{SD\_REF\_CLK2}}$ | I                     | SXCVDD          |
| AH19        | SD_REF_CLK2                       | I                     | SXCVDD          |
| G16         | STOP_BS                           | I                     | QVDD            |
| AA28        | SXCVDD                            | Power                 | N/A             |
| AC28        | SXCVDD                            | Power                 | N/A             |
| AE28        | SXCVDD                            | Power                 | N/A             |
| AG28        | SXCVDD                            | Power                 | N/A             |
| AH18        | SXCVDD                            | Power                 | N/A             |
| AH20        | SXCVDD                            | Power                 | N/A             |
| AH22        | SXCVDD                            | Power                 | N/A             |
| AH24        | SXCVDD                            | Power                 | N/A             |
| L28         | SXCVDD                            | Power                 | N/A             |
| N28         | SXCVDD                            | Power                 | N/A             |
| R28         | SXCVDD                            | Power                 | N/A             |
| U28         | SXCVDD                            | Power                 | N/A             |
| W28         | SXCVDD                            | Power                 | N/A             |
| AA27        | SXCVSS                            | Ground                | N/A             |
| AC27        | SXCVSS                            | Ground                | N/A             |
| AE27        | SXCVSS                            | Ground                | N/A             |
| AG18        | SXCVSS                            | Ground                | N/A             |
| AG20        | SXCVSS                            | Ground                | N/A             |
| AG22        | SXCVSS                            | Ground                | N/A             |
| AG24        | SXCVSS                            | Ground                | N/A             |
| AG27        | SXCVSS                            | Ground                | N/A             |
| L27         | SXCVSS                            | Ground                | N/A             |
| N27         | SXCVSS                            | Ground                | N/A             |
| R27         | SXCVSS                            | Ground                | N/A             |
| U27         | SXCVSS                            | Ground                | N/A             |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| W27         | SXCVSS                     | Ground                | N/A             |
| AB25        | SXPVDD                     | Power                 | N/A             |
| AD25        | SXPVDD                     | Power                 | N/A             |
| AE21        | SXPVDD                     | Power                 | N/A             |
| AE23        | SXPVDD                     | Power                 | N/A             |
| AF25        | SXPVDD                     | Power                 | N/A             |
| AH25        | SXPVDD                     | Power                 | N/A             |
| M25         | SXPVDD                     | Power                 | N/A             |
| N23         | SXPVDD                     | Power                 | N/A             |
| P25         | SXPVDD                     | Power                 | N/A             |
| T25         | SXPVDD                     | Power                 | N/A             |
| AB26        | SXPVSS                     | Ground                | N/A             |
| AD26        | SXPVSS                     | Ground                | N/A             |
| AF21        | SXPVSS                     | Ground                | N/A             |
| AF23        | SXPVSS                     | Ground                | N/A             |
| AF26        | SXPVSS                     | Ground                | N/A             |
| AH26        | SXPVSS                     | Ground                | N/A             |
| M26         | SXPVSS                     | Ground                | N/A             |
| N24         | SXPVSS                     | Ground                | N/A             |
| P26         | SXPVSS                     | Ground                | N/A             |
| T26         | SXPVSS                     | Ground                | N/A             |
| E17         | TCK                        | I                     | QVDD            |
| F17         | TDI                        | I                     | QVDD            |
| B14         | TDO                        | O                     | QVDD            |
| B15         | TMS                        | I                     | QVDD            |
| G17         | $\overline{\text{TRST}}$   | I                     | QVDD            |
| F10         | VDD                        | Power                 | N/A             |
| F8          | VDD                        | Power                 | N/A             |
| G7          | VDD                        | Power                 | N/A             |
| G9          | VDD                        | Power                 | N/A             |
| H10         | VDD                        | Power                 | N/A             |
| H16         | VDD                        | Power                 | N/A             |
| H18         | VDD                        | Power                 | N/A             |
| H8          | VDD                        | Power                 | N/A             |
| J11         | VDD                        | Power                 | N/A             |
| J13         | VDD                        | Power                 | N/A             |
| J15         | VDD                        | Power                 | N/A             |
| J17         | VDD                        | Power                 | N/A             |
| J19         | VDD                        | Power                 | N/A             |
| J7          | VDD                        | Power                 | N/A             |
| J9          | VDD                        | Power                 | N/A             |
| K10         | VDD                        | Power                 | N/A             |
| K12         | VDD                        | Power                 | N/A             |
| K14         | VDD                        | Power                 | N/A             |
| K16         | VDD                        | Power                 | N/A             |
| K18         | VDD                        | Power                 | N/A             |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| K20         | VDD                        | Power                 | N/A             |
| K8          | VDD                        | Power                 | N/A             |
| L11         | VDD                        | Power                 | N/A             |
| L13         | VDD                        | Power                 | N/A             |
| L15         | VDD                        | Power                 | N/A             |
| L17         | VDD                        | Power                 | N/A             |
| L19         | VDD                        | Power                 | N/A             |
| L7          | VDD                        | Power                 | N/A             |
| L9          | VDD                        | Power                 | N/A             |
| M10         | VDD                        | Power                 | N/A             |
| M12         | VDD                        | Power                 | N/A             |
| M14         | VDD                        | Power                 | N/A             |
| M16         | VDD                        | Power                 | N/A             |
| M18         | VDD                        | Power                 | N/A             |
| M20         | VDD                        | Power                 | N/A             |
| M8          | VDD                        | Power                 | N/A             |
| N13         | VDD                        | Power                 | N/A             |
| N15         | VDD                        | Power                 | N/A             |
| N17         | VDD                        | Power                 | N/A             |
| N19         | VDD                        | Power                 | N/A             |
| P12         | VDD                        | Power                 | N/A             |
| P14         | VDD                        | Power                 | N/A             |
| P16         | VDD                        | Power                 | N/A             |
| P18         | VDD                        | Power                 | N/A             |
| P20         | VDD                        | Power                 | N/A             |
| R13         | VDD                        | Power                 | N/A             |
| R15         | VDD                        | Power                 | N/A             |
| R17         | VDD                        | Power                 | N/A             |
| R19         | VDD                        | Power                 | N/A             |
| R9          | VDD                        | Power                 | N/A             |
| T10         | VDD                        | Power                 | N/A             |
| T12         | VDD                        | Power                 | N/A             |
| T14         | VDD                        | Power                 | N/A             |
| T16         | VDD                        | Power                 | N/A             |
| T18         | VDD                        | Power                 | N/A             |
| T20         | VDD                        | Power                 | N/A             |
| U11         | VDD                        | Power                 | N/A             |
| U13         | VDD                        | Power                 | N/A             |
| U15         | VDD                        | Power                 | N/A             |
| U17         | VDD                        | Power                 | N/A             |
| U19         | VDD                        | Power                 | N/A             |
| U9          | VDD                        | Power                 | N/A             |
| V10         | VDD                        | Power                 | N/A             |
| V12         | VDD                        | Power                 | N/A             |
| V14         | VDD                        | Power                 | N/A             |
| V16         | VDD                        | Power                 | N/A             |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| V18         | VDD                        | Power                 | N/A             |
| V20         | VDD                        | Power                 | N/A             |
| W19         | VDD                        | Power                 | N/A             |
| W9          | VDD                        | Power                 | N/A             |
| Y10         | VDD                        | Power                 | N/A             |
| Y20         | VDD                        | Power                 | N/A             |
| A15         | VSS                        | Ground                | N/A             |
| A17         | VSS                        | Ground                | N/A             |
| A19         | VSS                        | Ground                | N/A             |
| A2          | VSS                        | Ground                | N/A             |
| A5          | VSS                        | Ground                | N/A             |
| AA10        | VSS                        | Ground                | N/A             |
| AA12        | VSS                        | Ground                | N/A             |
| AA14        | VSS                        | Ground                | N/A             |
| AA16        | VSS                        | Ground                | N/A             |
| AA18        | VSS                        | Ground                | N/A             |
| AA2         | VSS                        | Ground                | N/A             |
| AA5         | VSS                        | Ground                | N/A             |
| AA8         | VSS                        | Ground                | N/A             |
| AB11        | VSS                        | Ground                | N/A             |
| AB13        | VSS                        | Ground                | N/A             |
| AB15        | VSS                        | Ground                | N/A             |
| AB17        | VSS                        | Ground                | N/A             |
| AC1         | VSS                        | Ground                | N/A             |
| AC10        | VSS                        | Ground                | N/A             |
| AC12        | VSS                        | Ground                | N/A             |
| AC14        | VSS                        | Ground                | N/A             |
| AC16        | VSS                        | Ground                | N/A             |
| AC4         | VSS                        | Ground                | N/A             |
| AC7         | VSS                        | Ground                | N/A             |
| AD12        | VSS                        | Non-user              | N/A             |
| AD13        | VSS                        | Non-user              | N/A             |
| AD14        | VSS                        | Non-user              | N/A             |
| AD15        | VSS                        | Ground                | N/A             |
| AD16        | VSS                        | Ground                | N/A             |
| AE11        | VSS                        | Ground                | N/A             |
| AE13        | VSS                        | Non-user              | N/A             |
| AE14        | VSS                        | Ground                | N/A             |
| AE15        | VSS                        | Ground                | N/A             |
| AE16        | VSS                        | Ground                | N/A             |
| AE2         | VSS                        | Ground                | N/A             |
| AE5         | VSS                        | Ground                | N/A             |
| AE8         | VSS                        | Ground                | N/A             |
| AF13        | VSS                        | Non-user              | N/A             |
| AF14        | VSS                        | Ground                | N/A             |
| AF15        | VSS                        | Ground                | N/A             |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| AF16        | VSS                        | Ground                | N/A             |
| AG1         | VSS                        | Ground                | N/A             |
| AG10        | VSS                        | Ground                | N/A             |
| AG13        | VSS                        | Ground                | N/A             |
| AG14        | VSS                        | Ground                | N/A             |
| AG15        | VSS                        | Ground                | N/A             |
| AG16        | VSS                        | Ground                | N/A             |
| AG4         | VSS                        | Ground                | N/A             |
| AG7         | VSS                        | Ground                | N/A             |
| AH13        | VSS                        | Ground                | N/A             |
| B11         | VSS                        | Ground                | N/A             |
| B13         | VSS                        | Ground                | N/A             |
| B16         | VSS                        | Ground                | N/A             |
| B17         | VSS                        | Ground                | N/A             |
| B18         | VSS                        | Ground                | N/A             |
| B19         | VSS                        | Ground                | N/A             |
| B21         | VSS                        | Ground                | N/A             |
| B22         | VSS                        | Non-user              | N/A             |
| B23         | VSS                        | Ground                | N/A             |
| B25         | VSS                        | Ground                | N/A             |
| B27         | VSS                        | Ground                | N/A             |
| B9          | VSS                        | Ground                | N/A             |
| C1          | VSS                        | Ground                | N/A             |
| C18         | VSS                        | Ground                | N/A             |
| C4          | VSS                        | Ground                | N/A             |
| C7          | VSS                        | Ground                | N/A             |
| D11         | VSS                        | Ground                | N/A             |
| D13         | VSS                        | Ground                | N/A             |
| D16         | VSS                        | Ground                | N/A             |
| D18         | VSS                        | Ground                | N/A             |
| D19         | VSS                        | Non-user              | N/A             |
| D23         | VSS                        | Ground                | N/A             |
| D9          | VSS                        | Ground                | N/A             |
| E18         | VSS                        | Ground                | N/A             |
| E2          | VSS                        | Ground                | N/A             |
| E21         | VSS                        | Ground                | N/A             |
| E22         | VSS                        | Non-user              | N/A             |
| E25         | VSS                        | Ground                | N/A             |
| E5          | VSS                        | Ground                | N/A             |
| E8          | VSS                        | Ground                | N/A             |
| F13         | VSS                        | Ground                | N/A             |
| F16         | VSS                        | Ground                | N/A             |
| F18         | VSS                        | Ground                | N/A             |
| F9          | VSS                        | Ground                | N/A             |
| G1          | VSS                        | Ground                | N/A             |
| G10         | VSS                        | Ground                | N/A             |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| G18         | VSS                        | Ground                | N/A             |
| G23         | VSS                        | Ground                | N/A             |
| G27         | VSS                        | Ground                | N/A             |
| G4          | VSS                        | Ground                | N/A             |
| G8          | VSS                        | Ground                | N/A             |
| H11         | VSS                        | Ground                | N/A             |
| H12         | VSS                        | Non-user              | N/A             |
| H15         | VSS                        | Ground                | N/A             |
| H17         | VSS                        | Ground                | N/A             |
| H19         | VSS                        | Ground                | N/A             |
| H21         | VSS                        | Ground                | N/A             |
| H25         | VSS                        | Ground                | N/A             |
| H7          | VSS                        | Ground                | N/A             |
| H9          | VSS                        | Ground                | N/A             |
| J10         | VSS                        | Ground                | N/A             |
| J12         | VSS                        | Ground                | N/A             |
| J14         | VSS                        | Ground                | N/A             |
| J16         | VSS                        | Ground                | N/A             |
| J18         | VSS                        | Ground                | N/A             |
| J2          | VSS                        | Ground                | N/A             |
| J20         | VSS                        | Ground                | N/A             |
| J8          | VSS                        | Ground                | N/A             |
| K11         | VSS                        | Ground                | N/A             |
| K13         | VSS                        | Ground                | N/A             |
| K15         | VSS                        | Ground                | N/A             |
| K17         | VSS                        | Ground                | N/A             |
| K19         | VSS                        | Ground                | N/A             |
| K21         | VSS                        | Ground                | N/A             |
| K23         | VSS                        | Ground                | N/A             |
| K27         | VSS                        | Ground                | N/A             |
| K7          | VSS                        | Ground                | N/A             |
| K9          | VSS                        | Ground                | N/A             |
| L1          | VSS                        | Ground                | N/A             |
| L10         | VSS                        | Ground                | N/A             |
| L12         | VSS                        | Ground                | N/A             |
| L14         | VSS                        | Ground                | N/A             |
| L16         | VSS                        | Ground                | N/A             |
| L18         | VSS                        | Ground                | N/A             |
| L20         | VSS                        | Ground                | N/A             |
| L24         | VSS                        | Non-user              | N/A             |
| L25         | VSS                        | Non-user              | N/A             |
| L26         | VSS                        | Non-user              | N/A             |
| L4          | VSS                        | Ground                | N/A             |
| L8          | VSS                        | Ground                | N/A             |
| M11         | VSS                        | Ground                | N/A             |
| M13         | VSS                        | Ground                | N/A             |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|-------------|----------------------------|-----------------------|-----------------|
| M15         | VSS                        | Ground                | N/A             |
| M17         | VSS                        | Ground                | N/A             |
| M19         | VSS                        | Ground                | N/A             |
| M7          | VSS                        | Ground                | N/A             |
| M9          | VSS                        | Ground                | N/A             |
| N10         | VSS                        | Ground                | N/A             |
| N12         | VSS                        | Ground                | N/A             |
| N14         | VSS                        | Ground                | N/A             |
| N16         | VSS                        | Ground                | N/A             |
| N18         | VSS                        | Ground                | N/A             |
| N2          | VSS                        | Ground                | N/A             |
| N20         | VSS                        | Ground                | N/A             |
| N5          | VSS                        | Ground                | N/A             |
| N8          | VSS                        | Ground                | N/A             |
| P11         | VSS                        | Ground                | N/A             |
| P13         | VSS                        | Ground                | N/A             |
| P15         | VSS                        | Ground                | N/A             |
| P17         | VSS                        | Ground                | N/A             |
| P19         | VSS                        | Ground                | N/A             |
| P7          | VSS                        | Ground                | N/A             |
| P9          | VSS                        | Ground                | N/A             |
| R10         | VSS                        | Ground                | N/A             |
| R12         | VSS                        | Ground                | N/A             |
| R14         | VSS                        | Ground                | N/A             |
| R16         | VSS                        | Ground                | N/A             |
| R18         | VSS                        | Ground                | N/A             |
| R20         | VSS                        | Ground                | N/A             |
| R4          | VSS                        | Ground                | N/A             |
| R8          | VSS                        | Ground                | N/A             |
| T1          | VSS                        | Ground                | N/A             |
| T11         | VSS                        | Ground                | N/A             |
| T13         | VSS                        | Ground                | N/A             |
| T15         | VSS                        | Ground                | N/A             |
| T17         | VSS                        | Ground                | N/A             |
| T19         | VSS                        | Ground                | N/A             |
| T2          | VSS                        | Ground                | N/A             |
| T7          | VSS                        | Ground                | N/A             |
| T9          | VSS                        | Ground                | N/A             |
| U10         | VSS                        | Ground                | N/A             |
| U12         | VSS                        | Ground                | N/A             |
| U14         | VSS                        | Ground                | N/A             |
| U16         | VSS                        | Ground                | N/A             |
| U18         | VSS                        | Ground                | N/A             |
| U2          | VSS                        | Ground                | N/A             |
| U20         | VSS                        | Ground                | N/A             |
| U5          | VSS                        | Ground                | N/A             |

Table 2. Signal List by Primary Signal Name (continued)

| Ball Number                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Signal Name <sup>1,2</sup> | Pin Type <sup>3</sup> | Power Rail Name |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-----------------------|-----------------|
| U8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSS                        | Ground                | N/A             |
| V11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| V13                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| V15                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| V17                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| V19                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| V2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSS                        | Ground                | N/A             |
| V7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSS                        | Ground                | N/A             |
| V9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSS                        | Ground                | N/A             |
| W1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSS                        | Ground                | N/A             |
| W10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| W12                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| W14                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| W16                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| W18                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| W2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSS                        | Ground                | N/A             |
| W20                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| W4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSS                        | Ground                | N/A             |
| W8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSS                        | Ground                | N/A             |
| Y11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| Y13                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| Y15                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| Y17                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| Y19                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS                        | Ground                | N/A             |
| Y7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSS                        | Ground                | N/A             |
| Y9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSS                        | Ground                | N/A             |
| D27                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSS'                       | Ground                | N/A             |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. Signal function during power-on reset is determined by the RCW source type. Selection of RapidIO, SGMII, CPRI, and PCI Express functionality during normal operation is configured by the RCW bit values. Selection of the GPIO function and other functions is done by GPIO register setup. For signals with GPIO functionality, the open-drain and internal 20 K<math>\Omega</math> pull-up resistor can be configured by GPIO register programming. For configuration details, see the <i>GPIO</i> chapter in the <i>MSC8157 Reference Manual</i>.</li> <li>2. NC signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS or SXC VSS), or pulled up (VDD).</li> <li>3. Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected; non-user = connect as specified under Signal Name.</li> <li>4. Connect power inputs to the power supplies via external filters. See the <i>MSC8157 Design Checklist</i> (AN4110) for details.</li> </ol> |                            |                       |                 |

## 2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8157 Reference Manual*.

### 2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 3 describes the maximum electrical ratings for the MSC8157.

**Table 3. Absolute Maximum Ratings**

| Rating                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Power Rail Name | Symbol         | Value                           | Unit |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------------|---------------------------------|------|
| Core supply voltage<br>• Cores 0–5                                                                                                                                                                                                                                                                                                                                                                                                                                             | VDD             | $V_{DD}$       | –0.3 to 1.1                     | V    |
| PLL supply voltage <sup>3</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                | PLL0_AVDD       | $V_{DDPLL0}$   | –0.3 to 1.1                     | V    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | PLL1_AVDD       | $V_{DDPLL1}$   | –0.3 to 1.1                     | V    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | PLL2_AVDD       | $V_{DDPLL2}$   | –0.3 to 1.1                     | V    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | MAVDD           | $V_{DDPLL M}$  | –0.3 to 1.1                     | V    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | SD_PLL1_AVDD    | $V_{DDPLL}$    | –0.3 to 1.1                     | V    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | SD_PLL2_AVDD    | $V_{DDPLL}$    | –0.3 to 1.1                     | V    |
| CRPE supply voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                            | CRPEVDD         | $V_{DDCRPE}$   | –0.3 to 1.1                     | V    |
| CPRI supply voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                            | CPRIVDD         | $V_{DDCPRI}$   | –0.3 to 1.1                     | V    |
| M3 memory supply voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                       | M3VDD           | $V_{DDM3}$     | –0.3 to 1.1                     | V    |
| DDR memory supply voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                      | GVDD            | $V_{DDDDR}$    | –0.3 to 1.65                    | V    |
| DDR reference voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                          | MVREF           | $MV_{REF}$     | –0.3 to $0.51 \times V_{DDDDR}$ | V    |
| Input DDR voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                 | $V_{INDDR}$    | –0.3 to $V_{DDDDR} + 0.3$       | V    |
| I/O voltage excluding DDR and RapidIO lines                                                                                                                                                                                                                                                                                                                                                                                                                                    | NVDD, QVDD      | $V_{DDIO}$     | –0.3 to 2.625                   | V    |
| Input I/O voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                 | $V_{INIO}$     | –0.3 to $V_{DDIO} + 0.3$        | V    |
| SerDes pad voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                             | SXPVDD          | $V_{DSDXP}$    | –0.3 to 1.65                    | V    |
| SerDes core voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                            | SXCVDD          | $V_{DSDXC}$    | –0.3 to 1.21                    | V    |
| SerDes PLL voltage <sup>3</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                |                 | $V_{DDRIOPLL}$ | –0.3 to 1.21                    | V    |
| Input SerDes I/O voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                 | $V_{INRIO}$    | –0.3 to $V_{DSDXC} + 0.3$       | V    |
| Operating temperature                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                 | $T_J$          | –40 to 105                      | °C   |
| Storage temperature range                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                 | $T_{STG}$      | –55 to +150                     | °C   |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>Functional operating conditions are given in Table 4.</li> <li>Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.</li> <li>PLL supply voltage is specified at input of the filter and not at pin of the MSC8157 (see the MSC8157 Design Checklist (AN4110))</li> </ol> |                 |                |                                 |      |

## 2.2 Recommended Operating Conditions

Table 4 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

**Table 4. Recommended Operating Conditions**

| Rating                                                                                                                                                                                                                                                                                                                                 | Supply                                                                       | Min                             | Nominal                        | Max                             | Unit           |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|---------------------------------|--------------------------------|---------------------------------|----------------|
| Core supply voltage <sup>1</sup>                                                                                                                                                                                                                                                                                                       | VDD                                                                          | 0.97                            | 1.0                            | 1.05                            | V              |
| PLL supply voltage <sup>1,3</sup>                                                                                                                                                                                                                                                                                                      | PLL0_AVDD<br>PLL1_AVDD<br>PLL2_AVDD<br>MAVDD<br>SD_PLL1_AVDD<br>SD_PLL2_AVDD | 0.97                            | 1.0                            | 1.05                            | V              |
| CRPE supply voltage <sup>1</sup>                                                                                                                                                                                                                                                                                                       | CRPEVDD                                                                      | 0.97                            | 1.0                            | 1.05                            | V              |
| CPRI supply voltage <sup>1</sup>                                                                                                                                                                                                                                                                                                       | CPRIVDD                                                                      | 0.97                            | 1.0                            | 1.05                            | V              |
| Switchable M3 memory supply voltage <sup>1</sup>                                                                                                                                                                                                                                                                                       | M3VDD                                                                        | 0.97                            | 1.0                            | 1.05                            | V              |
| DDR memory supply voltage                                                                                                                                                                                                                                                                                                              | GVDD                                                                         | 1.425                           | 1.5                            | 1.575                           | V              |
| DDR reference voltage                                                                                                                                                                                                                                                                                                                  | MVREF                                                                        | $0.49 \times \text{GVDD (nom)}$ | $0.5 \times \text{GVDD (nom)}$ | $0.51 \times \text{GVDD (nom)}$ | V              |
| RGMII Ethernet and GPIO supply voltage <sup>2</sup>                                                                                                                                                                                                                                                                                    | NVDD                                                                         | 2.375                           | 2.5                            | 2.625                           | V              |
| Input/output clocks, reset signal, and JTAG supply voltage <sup>2</sup>                                                                                                                                                                                                                                                                | QVDD                                                                         | 2.375                           | 2.5                            | 2.625                           | V              |
| SerDes pad supply voltage                                                                                                                                                                                                                                                                                                              | SXPVDD                                                                       | 1.425                           | 1.5                            | 1.575                           | V              |
| SerDes core supply voltage <sup>1</sup>                                                                                                                                                                                                                                                                                                | SXCVDD                                                                       | 0.97                            | 1.0                            | 1.05                            | V              |
| Operating temperature range:<br>• Standard<br>• Extended                                                                                                                                                                                                                                                                               | T <sub>J</sub><br>T <sub>A</sub><br>T <sub>J</sub>                           | 0<br>-40<br>—                   |                                | 105<br>—<br>105                 | °C<br>°C<br>°C |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. Designates supplies that use the same 1.0 V nominal voltage level.</li> <li>2. Designates supplies that use the same 2.5 V nominal voltage level.</li> <li>3. PLL supply voltage is specified at the input of the filter and not at the MSC8157 pin for the supply.</li> </ol> |                                                                              |                                 |                                |                                 |                |

## 2.3 Thermal Characteristics

Table 5 describes thermal characteristics of the MSC8157 for the FC-PBGA packages.

Table 5. Thermal Characteristics for the MSC8157

| Characteristic                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Symbol           | FC-PBGA<br>29 × 29 mm <sup>2</sup> |                               | Unit |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|------------------------------------|-------------------------------|------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                  | Natural<br>Convection              | 200 ft/min<br>(1 m/s) airflow |      |
| Junction-to-ambient <sup>1, 2</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | R <sub>θJA</sub> | 18                                 | 12                            | °C/W |
| Junction-to-ambient, four-layer board <sup>1, 2</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | R <sub>θJA</sub> | 13                                 | 9                             | °C/W |
| Junction-to-board (bottom) <sup>3</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | R <sub>θJB</sub> | 4                                  |                               | °C/W |
| Junction-to-case <sup>4</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | R <sub>θJC</sub> | 0.4                                |                               | °C/W |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.</li> <li>2. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for the specified package.</li> <li>3. Junction-to-board thermal resistance determined per JEDEC JESD 51-8. Thermal test board meets JEDEC specification for the specified package.</li> <li>4. Junction-to-case at the top of the package determined using MIL-STD-883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer</li> </ol> |                  |                                    |                               |      |

## 2.4 CLKIN/MCLKIN Requirements

Table 6 summarizes the required characteristics for the CLKIN/MCLKIN signal.

Table 6. CLKIN/MCLKIN Requirements

| Parameter/Condition <sup>1</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Symbol           | Min | Typ | Max  | Unit | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|-----|-----|------|------|-------|
| CLKIN/MCLKIN duty cycle                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | —                | 40  | —   | 60   | %    | 2     |
| CLKIN/MCLKIN slew rate                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | —                | 1   | —   | 4    | V/ns | 3     |
| CLKIN/MCLKIN peak period jitter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | —                | —   | —   | ±150 | ps   | —     |
| CLKIN/MCLKIN jitter phase noise at -56 dBc                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | —                | —   | —   | 500  | KHz  | 4     |
| AC input swing limits                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | ΔV <sub>AC</sub> | 1.5 | —   | —    | V    | —     |
| Input capacitance                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | C <sub>IN</sub>  | —   | —   | 15   | pf   | 5     |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. For clock frequencies, see the <i>Clock</i> chapter in the <i>MSC8157 Reference Manual</i>.</li> <li>2. Measured at the rising edge and/or the falling edge at V<sub>DDIO</sub>/2.</li> <li>3. Slew rate as measured from ±20% to 80% of voltage swing at clock input.</li> <li>4. Phase noise is calculated as FFT of TIE jitter.</li> <li>5. The specified capacitance is not an external requirement. It represents the internal capacitance specification.</li> </ol> |                  |     |     |      |      |       |

## 2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8157.

### 2.5.1 DDR SDRAM Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8157. Table 7 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

**Note:** At recommended operating conditions (see Table 4) with GVDD = 1.5 V.

Table 7. DDR3 SDRAM Interface DC Electrical Characteristics

| Parameter/Condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Symbol     | Min                     | Max                     | Unit    | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-------------------------|-------------------------|---------|-------|
| I/O reference voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | $MV_{REF}$ | $0.49 \times V_{DDDDR}$ | $0.51 \times V_{DDDDR}$ | V       | 2,3,4 |
| Input high voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | $V_{IH}$   | $MV_{REF} + 0.100$      | $V_{DDDDR}$             | V       | 5     |
| Input low voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | $V_{IL}$   | GND                     | $MV_{REF} - 0.100$      | V       | 5     |
| Output high current ( $V_{OUT} = 0.7125$ V)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | $I_{OH}$   | —                       | –25.9                   | mA      | 6, 7  |
| Output low current ( $V_{OUT} = 0.7125$ V)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | $I_{OL}$   | 25.9                    | —                       | mA      | 6, 7  |
| I/O leakage current                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | $I_{OZ}$   | –50                     | 50                      | $\mu$ A | 8     |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. <math>V_{DDDDR}</math> is expected to be within 50 mV of the DRAM <math>V_{DD}</math> at all times. The DRAM and memory controller can use the same or different sources.</li> <li>2. <math>MV_{REF}</math> is expected to be equal to <math>0.5 \times V_{DDDDR}</math> and to track <math>V_{DDDDR}</math> DC variations as measured at the receiver. Peak-to-peak noise on <math>MV_{REF}</math> may not exceed 1% of the <math>V_{DDDDR}</math> DC value (that is, 15 mV).</li> <li>3. <math>V_{TT}</math> is not applied directly to the device. It is the supply to which the far end signal termination is made and is expected to be equal to <math>MV_{REF}</math> with a minimum value of <math>MV_{REF} - 0.04</math> and a maximum value of <math>MV_{REF} + 0.04</math> V. <math>V_{TT}</math> should track variations in the DC-level of <math>MV_{REF}</math>.</li> <li>4. The voltage regulator for <math>MV_{REF}</math> must meet the specifications stated in Table 9.</li> <li>5. Input capacitance load for DQ, DQS, and DQS signals are available in the IBIS models.</li> <li>6. <math>I_{OH}</math> and <math>I_{OL}</math> are measured at <math>V_{DDDDR} = 1.425</math> V.</li> <li>7. Refer to the IBIS model for the complete output IV curve characteristics.</li> <li>8. Output leakage is measured with all outputs are disabled, <math>0 \text{ V} \leq V_{OUT} \leq V_{DDDDR}</math>.</li> </ol> |            |                         |                         |         |       |

Table 8 provides the DDR controller interface capacitance for DDR3 memory.

**Note:** At recommended operating conditions (see Table 4) with  $V_{DDDDR} = 1.5$  V.

Table 8. DDR3 SDRAM Capacitance

| Parameter                                                      | Symbol    | Min | Max | Unit |
|----------------------------------------------------------------|-----------|-----|-----|------|
| I/O capacitance: DQ, DQS, $\overline{DQS}$                     | $C_{IO}$  | 6   | 8   | pF   |
| Delta I/O capacitance: DQ, DQS, $\overline{DQS}$               | $C_{DIO}$ | —   | 0.5 | pF   |
| <b>Note:</b> Guaranteed by FAB process and micro-construction. |           |     |     |      |

Table 9 lists the current draw characteristics for  $MV_{REF}$ .

**Note:** Values when used at recommended operating conditions (see Table 4).

Table 9. Current Draw Characteristics for  $MV_{REF}$ 

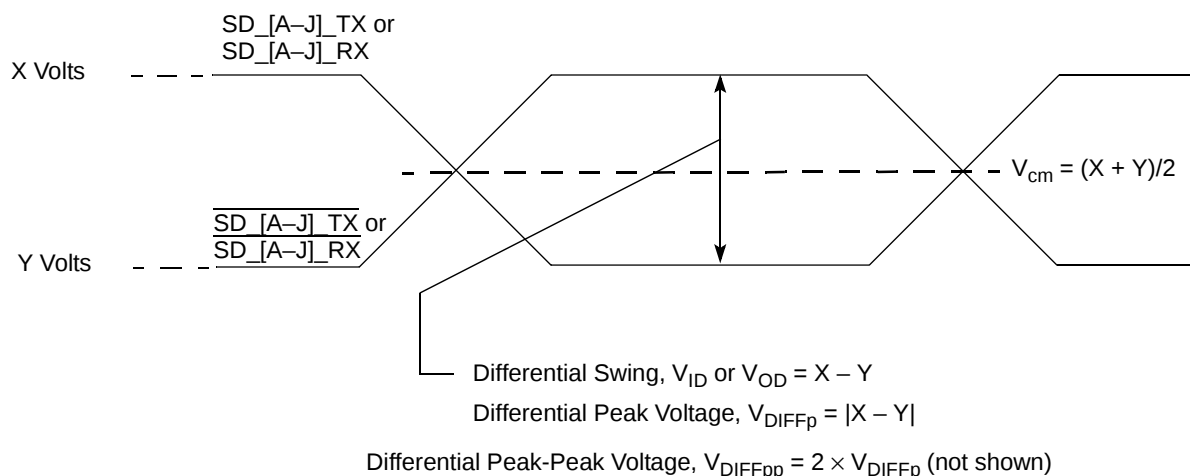
| Parameter / Condition       | Symbol       | Min | Max  | Unit    |
|-----------------------------|--------------|-----|------|---------|
| Current draw for $MV_{REF}$ | $I_{MVREFn}$ | —   | 1250 | $\mu$ A |

## 2.5.2 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The MSC8157 features an HSSI that includes one 10-channel SerDes port (lanes A through J) used for high-speed serial interface applications (PCI Express, Serial RapidIO interfaces, CPRI, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 2.6.2, “HSSI AC Timing Specifications.”

### 2.5.2.1 Signal Term Definitions

The SerDes interface uses differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 3 shows how the signals are defined. Figure 3 shows the waveform for either a transmitter output ( $\overline{\text{SD}}_{[A-J]}_{\text{TX}}$  and  $\overline{\text{SD}}_{[A-J]}_{\text{TX}}$ ) or a receiver input ( $\overline{\text{SD}}_{[A-J]}_{\text{RX}}$  and  $\overline{\text{SD}}_{[A-J]}_{\text{RX}}$ ). Each signal swings between X volts and Y volts where  $X > Y$ .



**Figure 3. Differential Voltage Definitions for Transmitter/Receiver**

Using this waveform, the definitions are listed in Table 10. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

**Table 10. Differential Signal Definitions**

| Term                                                                                    | Definition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Single-Ended Swing</b>                                                               | The transmitter output signals and the receiver input signals $\overline{\text{SD}}_{[A-J]}_{\text{TX}}$ , $\overline{\text{SD}}_{[A-J]}_{\text{TX}}$ , $\overline{\text{SD}}_{[A-J]}_{\text{RX}}$ and $\overline{\text{SD}}_{[A-J]}_{\text{RX}}$ each have a peak-to-peak swing of $X - Y$ volts. This is also referred to as each signal wire's single-ended swing.                                                                                                                                                                                                                                |
| <b>Differential Output Voltage, <math>V_{OD}</math> (or Differential Output Swing):</b> | The differential output voltage (or swing) of the transmitter, $V_{OD}$ , is defined as the difference of the two complimentary output voltages: $V_{\overline{\text{SD}}_{[A-J]}_{\text{TX}}} - V_{\overline{\text{SD}}_{[A-J]}_{\text{TX}}}$ . The $V_{OD}$ value can be either positive or negative.                                                                                                                                                                                                                                                                                              |
| <b>Differential Input Voltage, <math>V_{ID}</math> (or Differential Input Swing)</b>    | The differential input voltage (or swing) of the receiver, $V_{ID}$ , is defined as the difference of the two complimentary input voltages: $V_{\overline{\text{SD}}_{[A-J]}_{\text{RX}}} - V_{\overline{\text{SD}}_{[A-J]}_{\text{RX}}}$ . The $V_{ID}$ value can be either positive or negative.                                                                                                                                                                                                                                                                                                   |
| <b>Differential Peak Voltage, <math>V_{DIFFp}</math></b>                                | The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} =  X - Y $ volts.                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <b>Differential Peak-to-Peak, <math>V_{DIFFp-p}</math></b>                              | Since the differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times  (A - B) $ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times  V_{OD} $ . |

Table 10. Differential Signal Definitions (continued)

| Term                                                   | Definition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Differential Waveform</b>                           | The differential waveform is constructed by subtracting the inverting signal ( $\overline{\text{SD\_}[A-J]_{\text{TX}}}$ , for example) from the non-inverting signal ( $\text{SD\_}[A-J]_{\text{TX}}$ , for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to <a href="#">Figure 3</a> as an example for differential waveform.                                                                                                                                                                                                    |
| <b>Common Mode Voltage, <math>V_{\text{cm}}</math></b> | The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{\text{cm\_out}} = (V_{\text{SD\_}[A-J]_{\text{TX}}} + V_{\overline{\text{SD\_}[A-J]_{\text{TX}}}}) / 2 = (A + B) / 2$ , which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions. |

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and  $\overline{\text{TD}}$ . If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or  $\overline{\text{TD}}$ ) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output differential swing ( $V_{\text{OD}}$ ) has the same amplitude as each signal single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words,  $V_{\text{OD}}$  is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage ( $V_{\text{DIFFp}}$ ) is 500 mV. The peak-to-peak differential voltage ( $V_{\text{DIFFp-p}}$ ) is 1000 mV p-p.

### 2.5.2.2 SerDes Reference Clock Receiver Characteristics

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are  $\text{SD\_REF\_CLK1}/\overline{\text{SD\_REF\_CLK1}}$  or  $\text{SD\_REF\_CLK2}/\overline{\text{SD\_REF\_CLK2}}$ . [Figure 4](#) shows a receiver reference diagram of the SerDes reference clocks.

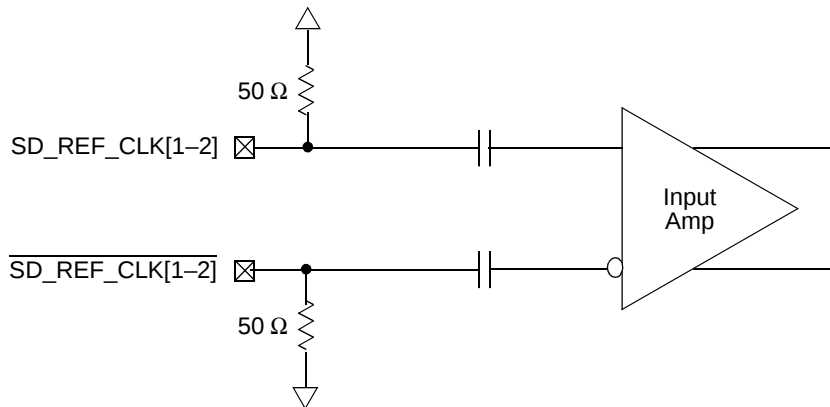


Figure 4. Receiver of SerDes Reference Clocks

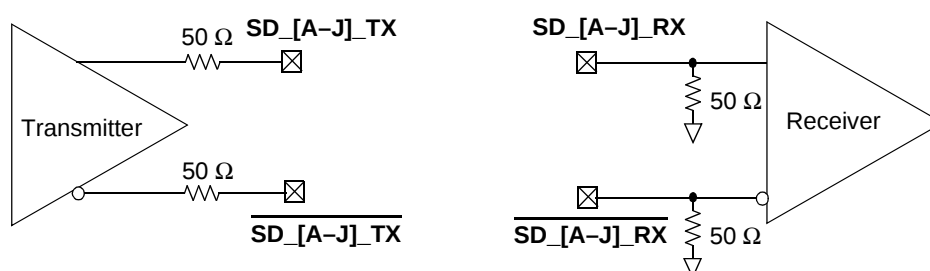
The characteristics of the clock signals are as follows:

- The supply voltage requirements for  $V_{\text{DSSXC}}$  are as specified in [Table 4](#).
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The  $\text{SD\_REF\_CLK}[1-2]$  and  $\overline{\text{SD\_REF\_CLK}}[1-2]$  are internally AC-coupled differential inputs as shown in [Figure 4](#). Each differential clock input ( $\text{SD\_REF\_CLK}[1-2]$  or  $\overline{\text{SD\_REF\_CLK}}[1-2]$ ) has on-chip 50- $\Omega$  termination to  $\text{SXC}_{\text{VSS}}$  followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.

- When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
- This current limitation sets the maximum common mode input voltage to be less than 0.4 V ( $0.4 \text{ V} / 50 = 8 \text{ mA}$ ) while the minimum common mode input level is 0.1 V above  $\text{GND}_{\text{SXC}}$ . For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
- If the device driving the  $\text{SD\_REF\_CLK}[1-2]$  and  $\overline{\text{SD\_REF\_CLK}}[1-2]$  inputs cannot drive  $50 \Omega$  to  $\text{GND}_{\text{SXC}}$  DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled externally.
- The input amplitude requirement is described in detail in the following sections.

### 2.5.2.3 SerDes Transmitter and Receiver Reference Circuits

Figure 5 shows the reference circuits for SerDes data lane transmitter and receiver.



**Note:** The [A–J] indicates the specific SerDes lane. Each lane can be assigned to a specific protocol by the RCW assignments at reset (see **Chapter 5, Reset** in the reference manual for details). External AC coupling capacitors are required for all protocols for all lanes.

**Figure 5. SerDes Transmitter and Receiver Reference Circuits**

### 2.5.2.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver beyond that allowed by the specification. To offset a portion of these effects, equalization can be used. The following is a list of the most commonly used equalization techniques:

- Pre-emphasis on the transmitter.
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization.
- The use of active circuits in the receiver, often referred to as adaptive equalization.

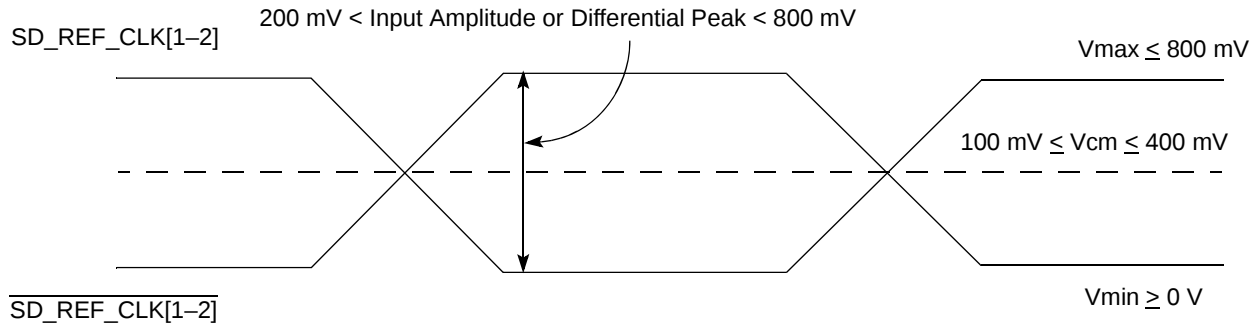
## 2.5.3 DC-Level Requirements for SerDes Interfaces

The following subsections define the DC-level requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, the CPRI data lines, and the SGMII data lines.

### 2.5.3.1 DC-Level Requirements for SerDes Reference Clocks

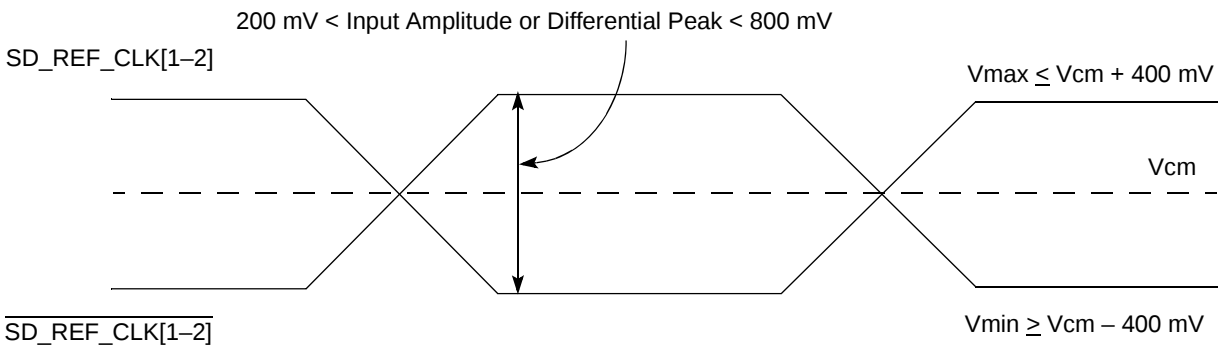
The DC-level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. [Figure 6](#) shows the SerDes reference clock input requirement for DC-coupled connection scheme.



**Figure 6. Differential Reference Clock Input DC Requirements (External DC-Coupled)**

- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC-level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to  $\text{GND}_{\text{SXC}}$ . Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage  $\text{GND}_{\text{SXC}}$ . [Figure 7](#) shows the SerDes reference clock input requirement for AC-coupled connection scheme.



**Figure 7. Differential Reference Clock Input DC Requirements (External AC-Coupled)**

- **Single-Ended Mode**
  - The reference clock can also be single-ended. The  $\text{SD\_REF\_CLK}[1-2]$  input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from  $V_{\text{MIN}}$  to  $V_{\text{MAX}}$ ) with  $\text{SD\_REF\_CLK}[1-2]$  either left unconnected or tied to ground.
  - The  $\text{SD\_REF\_CLK}[1-2]$  input average voltage must be between 200 and 400 mV. [Figure 8](#) shows the SerDes reference clock input requirement for single-ended signaling mode.

- To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD\_REF\_CLK[1–2]) through the same source impedance as the clock input (SD\_REF\_CLK[1–2]) in use.

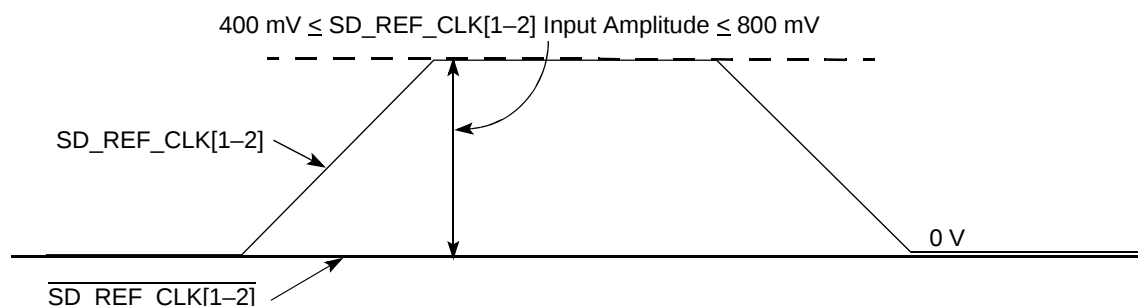


Figure 8. Single-Ended Reference Clock Input DC Requirements

### 2.5.3.2 DC-Level Requirements for PCI Express Configurations

The DC-level requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8157 supports a 2.5 Gbps and a 5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 2.0*. The transmitter specifications for 2.5 Gbps are defined in Table 11 and the receiver specifications are defined in Table 12. For 5 Gbps, the transmitter specifications are defined in Table 13 and the receiver specifications are defined in Table 14.

**Note:** Specifications are valid at the recommended operating conditions listed in Table 4.

Table 11. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output DC Specifications

| Parameter                                         | Symbol                   | Min | Nom  | Max  | Units    | Condition                                                                                                                                                                                                                                             |
|---------------------------------------------------|--------------------------|-----|------|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Differential peak-to-peak output voltage swing    | $V_{\text{TX-DIFFP-P}}$  | 800 | 1000 | 1200 | mV       | $V_{\text{TX-DIFFP-P}} = 2 \times  V_{\text{TX-D+}} - V_{\text{TX-D-}} $ . Measured at the package pins with a test load of 50 $\Omega$ to GND on each pin.                                                                                           |
| De-emphasized differential output voltage (ratio) | $V_{\text{TX-DE-RATIO}}$ | 3.0 | 3.5  | 4.0  | dB       | Ratio of the $V_{\text{TX-DIFFP-P}}$ of the second and following bits after a transition divided by the $V_{\text{TX-DIFFP-P}}$ of the first bit after a transition. Measured at the package pins with a test load of 50 $\Omega$ to GND on each pin. |
| DC differential Tx impedance                      | $Z_{\text{TX-DIFF-DC}}$  | 80  | 100  | 120  | $\Omega$ | Tx DC differential mode low Impedance                                                                                                                                                                                                                 |
| DC single-ended TX impedance                      | $Z_{\text{TX-DC}}$       | 40  | 50   | 60   | $\Omega$ | Required Tx D+ as well as D– DC Impedance during all states                                                                                                                                                                                           |

Table 12. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

| Parameter                               | Symbol                           | Min | Nom  | Max  | Units      | Notes |
|-----------------------------------------|----------------------------------|-----|------|------|------------|-------|
| Differential input peak-to-peak voltage | $V_{\text{RX-DIFFP-P}}$          | 120 | 1000 | 1200 | mV         | 1     |
| DC differential Input Impedance         | $Z_{\text{RX-DIFF-DC}}$          | 80  | 100  | 120  | $\Omega$   | 2     |
| DC input impedance                      | $Z_{\text{RX-DC}}$               | 40  | 50   | 60   | $\Omega$   | 3     |
| Powered down DC input impedance         | $Z_{\text{RX-HIGH-IMP-DC}}$      | 50  | —    | —    | K $\Omega$ | 4     |
| Electrical idle detect threshold        | $V_{\text{RX-IDLE-DET-DIFFP-P}}$ | 65  | —    | 175  | mV         | 5     |

Table 12. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications (continued)

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Symbol | Min | Nom | Max | Units | Notes |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|-----|-----|-------|-------|
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. <math>V_{RX-DIFFp-p} = 2 \times  V_{RX-D+} - V_{RX-D-} </math> Measured at the package pins with a test load of 50 <math>\Omega</math> to GND on each pin.</li> <li>2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.</li> <li>3. Required Rx D+ as well as D– DC Impedance (50 <math>\pm</math>20% tolerance). Measured at the package pins with a test load of 50 <math>\Omega</math> to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.</li> <li>4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.</li> <li>5. <math>V_{RX-IDLE-DET-DIFFp-p} = 2 \times  V_{RX-D+} - V_{RX-D-} </math>. Measured at the package pins of the receiver</li> </ol> |        |     |     |     |       |       |

Table 13. PCI Express (5 Gbps) Differential Transmitter (Tx) Output DC Specifications

| Parameter                                                | Symbol                  | Min | Nom  | Max  | Units    | Condition                                                                                                                                                                                                                               |
|----------------------------------------------------------|-------------------------|-----|------|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Differential peak-to-peak output voltage swing           | $V_{TX-DIFFp-p}$        | 800 | 1000 | 1200 | mV       | $V_{TX-DIFFp-p} = 2 \times  V_{TX-D+} - V_{TX-D-} $ . Measured at the package pins with a test load of 50 $\Omega$ to GND on each pin.                                                                                                  |
| Low power differential peak-to-peak output voltage swing | $V_{TX-DIFFp-p\_low}$   | 400 | 500  | 1200 | mV       | $V_{TX-DIFFp-p} = 2 \times  V_{TX-D+} - V_{TX-D-} $ . Measured at the package pins with a test load of 50 $\Omega$ to GND on each pin.                                                                                                  |
| De-emphasized differential output voltage (ratio)        | $V_{TX-DE-RATIO-3.5dB}$ | 3.0 | 3.5  | 4.0  | dB       | Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 $\Omega$ to GND on each pin. |
| De-emphasized differential output voltage (ratio)        | $V_{TX-DE-RATIO-6.0dB}$ | 5.5 | 6.0  | 6.5  | dB       | Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 $\Omega$ to GND on each pin. |
| DC differential Tx impedance                             | $Z_{TX-DIFF-DC}$        | 80  | 100  | 120  | $\Omega$ | Tx DC differential mode low impedance                                                                                                                                                                                                   |
| Transmitter DC impedance                                 | $Z_{TX-DC}$             | 40  | 50   | 60   | $\Omega$ | Required Tx D+ as well as D– DC impedance during all states                                                                                                                                                                             |

Table 14. PCI Express (5 Gbps) Differential Receiver (Rx) Input DC Specifications

| Parameter                               | Symbol                    | Min | Nom  | Max  | Units      | Notes |
|-----------------------------------------|---------------------------|-----|------|------|------------|-------|
| Differential input peak-to-peak voltage | $V_{RX-DIFFp-p}$          | 120 | 1000 | 1200 | mV         | 1     |
| DC differential Input Impedance         | $Z_{RX-DIFF-DC}$          | 80  | 100  | 120  | $\Omega$   | 2     |
| DC input impedance                      | $Z_{RX-DC}$               | 40  | 50   | 60   | $\Omega$   | 3     |
| Powered down DC input impedance         | $Z_{RX-HIGH-IMP-DC}$      | 50  | —    | —    | K $\Omega$ | 4     |
| Electrical idle detect threshold        | $V_{RX-IDLE-DET-DIFFp-p}$ | 65  | —    | 175  | mV         | 5     |

Table 14. PCI Express (5 Gbps) Differential Receiver (Rx) Input DC Specifications (continued)

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Symbol | Min | Nom | Max | Units | Notes |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|-----|-----|-------|-------|
| <b>Notes:</b> <ol style="list-style-type: none"> <li><math>V_{RX-DIFFp-p} = 2 \times  V_{RX-D+} - V_{RX-D-} </math> Measured at the package pins with a test load of 50 <math>\Omega</math> to GND on each pin.</li> <li>Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.</li> <li>Required Rx D+ as well as D– DC Impedance (50 <math>\pm</math>20% tolerance). Measured at the package pins with a test load of 50 <math>\Omega</math> to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.</li> <li>Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.</li> <li><math>V_{RX-IDLE-DET-DIFFp-p} = 2 \times  V_{RX-D+} - V_{RX-D-} </math>. Measured at the package pins of the receiver</li> </ol> |        |     |     |     |       |       |

### 2.5.3.3 DC Level Requirements for Serial RapidIO Configurations

**Note:** Specifications are valid at the recommended operating conditions listed in Table 4.

Table 15. Serial RapidIO Transmitter DC Specifications for Transfer Rates  $\leq$  3.125 Gbaud

| Parameter                                                                                | Symbol       | Min   | Nom | Max  | Units    | Condition                       |
|------------------------------------------------------------------------------------------|--------------|-------|-----|------|----------|---------------------------------|
| Output voltage                                                                           | $V_O$        | –0.40 | —   | 2.30 | V        |                                 |
| Long run differential output voltage                                                     | $V_{DIFFPP}$ | 800   | —   | 1600 | mVp-p    | L[A–J]TECR0[AMP_RED] = 0b000000 |
| Short run differential output voltage                                                    | $V_{DIFFPP}$ | 500   | —   | 1000 | mVp-p    | L[A–J]TECR0[AMP_RED] = 0b001000 |
| DC differential TX impedance                                                             | ZTX-DIFF-DC  | 80    | 100 | 120  | $\Omega$ |                                 |
| <b>Note:</b> Voltage relative to COMMON of either signal comprising a differential pair. |              |       |     |      |          |                                 |

Table 16. Serial RapidIO Receiver DC Specifications for Transfer Rates  $\leq$  3.125 Gbaud

| Parameter                                                                                                                                                                                       | Symbol      | Min | Nom | Max  | Units    |  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-----|-----|------|----------|--|
| Differential input voltage                                                                                                                                                                      | $V_{IN}$    | 200 | —   | 1600 | mVp-p    |  |
| DC differential RX impedance                                                                                                                                                                    | ZRX-DIFF-DC | 80  | 100 | 120  | $\Omega$ |  |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>Voltage relative to COMMON of either signal comprising a differential pair.</li> <li>Specifications are for Long and Short Run.</li> </ol> |             |     |     |      |          |  |

Table 17. Serial RapidIO Transmitter DC Specifications for Short Run at 5 Gbaud

| Parameter                                                                 | Symbol  | Min | Nom | Max | Units    | Condition                                            |
|---------------------------------------------------------------------------|---------|-----|-----|-----|----------|------------------------------------------------------|
| Output differential voltage<br>(into floating load Rload = 100 $\Omega$ ) | T_Vdiff | 400 | —   | 750 | mV       | Amplitude setting<br>L[A–J]TECR0[AMP_RED] = 0b001101 |
| Differential resistance                                                   | T_Rd    | 80  | 100 | 120 | $\Omega$ |                                                      |

Table 18. Serial RapidIO Receiver DC Specifications for Short Run at 5 Gbaud

| Parameter                  | Symbol  | Min | Nom | Max  | Units    |  |
|----------------------------|---------|-----|-----|------|----------|--|
| Input differential voltage | R_Vdiff | 125 | —   | 1200 | mV       |  |
| Differential resistance    | R_Rdin  | 80  |     | 120  | $\Omega$ |  |

Table 19. Serial RapidIO Transmitter DC Specifications for Long Run at 5 Gbaud

| Parameter                                                                 | Symbol  | Min | Nom | Max  | Units | Conditions                                                                          |
|---------------------------------------------------------------------------|---------|-----|-----|------|-------|-------------------------------------------------------------------------------------|
| Output differential voltage<br>(into floating load Rload = 100 $\Omega$ ) | T_Vdiff | 800 | —   | 1200 | mV    | Amplitude setting<br>L[A–J]TECR0[AMP_RED] = 0b000000<br>(with de-emphasis disabled) |

Table 19. Serial RapidIO Transmitter DC Specifications for Long Run at 5 Gbaud (continued)

| Parameter                                 | Symbol                      | Min | Nom | Max | Units    | Conditions                                                                                                                                                          |
|-------------------------------------------|-----------------------------|-----|-----|-----|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| De-emphasized differential output voltage | $T_{V_{TX-DE-RATIO-3.5dB}}$ | 3   | 3.5 | 4   | dB       | <ul style="list-style-type: none"> <li><math>p(n)_{(y)}_{tx\_eq\_type}[1:0] = 01</math></li> <li><math>p(n)_{(y)}_{tx\_ratio\_post1q}[3:0] = 1110</math></li> </ul> |
| Tx De-emphasized level                    | $T_{V_{TX-DE-RATIO-6.0dB}}$ | 5.5 | 6   | 6.5 | dB       | <ul style="list-style-type: none"> <li><math>p(n)_{(y)}_{tx\_eq\_type}[1:0] = 01</math></li> <li><math>p(n)_{(y)}_{tx\_ratio\_post1q}[3:0] = 1100</math></li> </ul> |
| Differential resistance                   | $T_{Rd}$                    | 80  | 100 | 120 | $\Omega$ |                                                                                                                                                                     |

Table 20. Serial RapidIO Receiver DC Specifications for Long Run at 5 Gbaud

| Parameter                  | Symbol      | Min | Nom | Max  | Units    | Condition                                                                                                                                                                       |
|----------------------------|-------------|-----|-----|------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Input differential voltage | $R_{Vdiff}$ | N/A | —   | 1200 | mV       | It is assumed that for the $R_{Vdiff}$ min specification, that the eye can be closed at the receiver after passing the signal through a CEI/SRIO Level II LR compliant channel. |
| Differential resistance    | $R_{Rdin}$  | 80  | —   | 120  | $\Omega$ |                                                                                                                                                                                 |

### 2.5.3.4 DC-Level Requirements for CPRI Configurations

This section provide various DC-level requirements for CPRI Configurations.

**Note:** Specifications are valid at the recommended operating conditions listed in [Table 4](#).

Table 21. CPRI Transmitter DC Specifications (LV: 1.2288, 2.4576 and 3.072 Gbps)

| Parameter                   | Symbol       | Min   | Nom | Max  | Units    | Condition                                                                   |
|-----------------------------|--------------|-------|-----|------|----------|-----------------------------------------------------------------------------|
| Output voltage              | $V_O$        | -0.40 | —   | 2.30 | V        | Voltage relative to COMMON of either signal comprising a differential pair. |
| Differential output voltage | $V_{DIFFPP}$ | 800   | —   | 1600 | mVp-p    | $L[A-J]TECR0[AMP\_RED] = 0b000000$ .                                        |
| Differential resistance     | $T_{Rd}$     | 80    | 100 | 120  | $\Omega$ |                                                                             |

**Note:** LV is XAUI-based.

Table 22. CPRI Transmitter DC Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

| Parameter                                                                 | Symbol      | Min | Nom | Max  | Units    | Condition                          |
|---------------------------------------------------------------------------|-------------|-----|-----|------|----------|------------------------------------|
| Output differential voltage (into floating load $R_{load} = 100 \Omega$ ) | $T_{Vdiff}$ | 800 | —   | 1200 | mV       | $L[A-J]TECR0[AMP\_RED] = 0x000000$ |
| Differential resistance                                                   | $T_{Rd}$    | 80  | 100 | 120  | $\Omega$ |                                    |

**Note:** LV-II is CEI-6G-LR-based.

Table 23. CPRI Receiver DC Specifications (LV: 1.2288, 2.4576 and 3.072 Gbps)

| Parameter                  | Symbol     | Min | Nom | Max  | Units    | Condition             |
|----------------------------|------------|-----|-----|------|----------|-----------------------|
| Differential input voltage | $V_{IN}$   | 200 | —   | 1600 | mVp-p    | Measured at receiver. |
| Difference resistance      | $R_{Rdin}$ | 80  | —   | 120  | $\Omega$ |                       |

**Note:** LV is XAUI-based.

Table 24. CPRI Receiver DC Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

| Parameter                  | Symbol      | Min | Nom | Max  | Units | Condition                                                                                                                                                                       |
|----------------------------|-------------|-----|-----|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Input differential voltage | $R_{Vdiff}$ | N/A | —   | 1200 | mV    | It is assumed that for the $R_{Vdiff}$ min specification, that the eye can be closed at the receiver after passing the signal through a CEI/CPRI Level II LR compliant channel. |

Table 24. CPRI Receiver DC Specifications (continued)(LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

| Parameter                              | Symbol | Min | Nom | Max | Units    | Condition |
|----------------------------------------|--------|-----|-----|-----|----------|-----------|
| Differential resistance                | R_Rdin | 80  | —   | 120 | $\Omega$ |           |
| <b>Note:</b> LV-II is CEI-6G-LR-based. |        |     |     |     |          |           |

### 2.5.3.5 DC-Level Requirements for SGMII Configurations

**Note:** Specifications are valid at the recommended operating conditions listed in Table 4.

Table 25 describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics.

Table 25. SGMII DC Transmitter Electrical Characteristics

| Parameter                   | Symbol     | Min                      | Nom | Max                      | Unit | Conditions                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----------------------------|------------|--------------------------|-----|--------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Output differential voltage | $ V_{OD} $ | $0.64 \times \text{Nom}$ | 500 | $1.45 \times \text{Nom}$ | mV   | <ol style="list-style-type: none"> <li>The <math> V_{OD} </math> value shown in the Typ column is based on the condition of <math>XV_{DD\_SRDS2-Typ}=1.0</math> V, no common mode offset variation (<math>V_{OS}=500</math>mV), SerDes transmitter is terminated with 100-<math>\Omega</math> differential load between SD_TXn and SD_TXn.</li> <li>Amplitude setting:<br/>[A-J]TECR0[AMD_RED] = 0b000000</li> </ol> |
| Output differential voltage | $ V_{OD} $ | $0.64 \times \text{Nom}$ | 459 | $1.45 \times \text{Nom}$ | mV   | <ol style="list-style-type: none"> <li>The <math> V_{OD} </math> value shown in the Typ column is based on the condition of <math>XV_{DD\_SRDS2-Typ}=1.0</math>V, no common mode offset variation (<math>V_{OS}=500</math>mV), SerDes transmitter is terminated with 100-<math>\Omega</math> differential load between SD_TXn and SD_TXn.</li> <li>Amplitude setting:<br/>[A-J]TECR0[AMD_RED] = 0b000010</li> </ol>  |
| Output differential voltage | $ V_{OD} $ | $0.64 \times \text{Nom}$ | 417 | $1.45 \times \text{Nom}$ | mV   | <ol style="list-style-type: none"> <li>The <math> V_{OD} </math> value shown in the Typ column is based on the condition of <math>XV_{DD\_SRDS2-Typ}=1.0</math>V, no common mode offset variation (<math>V_{OS}=500</math>mV), SerDes transmitter is terminated with 100-<math>\Omega</math> differential load between SD_TXn and SD_TXn.</li> <li>Amplitude setting:<br/>[A-J]TECR0[AMD_RED] = 0b000101</li> </ol>  |
| Output differential voltage | $ V_{OD} $ | $0.64 \times \text{Nom}$ | 376 | $1.45 \times \text{Nom}$ | mV   | <ol style="list-style-type: none"> <li>The <math> V_{OD} </math> value shown in the Typ column is based on the condition of <math>XV_{DD\_SRDS2-Typ}=1.0</math>V, no common mode offset variation (<math>V_{OS}=500</math>mV), SerDes transmitter is terminated with 100-<math>\Omega</math> differential load between SD_TXn and SD_TXn.</li> <li>Amplitude setting:<br/>[A-J]TECR0[AMD_RED] = 0b001000</li> </ol>  |
| Output differential voltage | $ V_{OD} $ | $0.64 \times \text{Nom}$ | 333 | $1.45 \times \text{Nom}$ | mV   | <ol style="list-style-type: none"> <li>The <math> V_{OD} </math> value shown in the Typ column is based on the condition of <math>XV_{DD\_SRDS2-Typ}=1.0</math>V, no common mode offset variation (<math>V_{OS}=500</math>mV), SerDes transmitter is terminated with 100-<math>\Omega</math> differential load between SD_TXn and SD_TXn.</li> <li>Amplitude setting:<br/>[A-J]TECR0[AMD_RED] = 0b001100</li> </ol>  |

Table 25. SGMII DC Transmitter Electrical Characteristics (continued)

| Parameter                       | Symbol     | Min                      | Nom | Max                               | Unit     | Conditions                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------------------|------------|--------------------------|-----|-----------------------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Output differential voltage     | $ V_{OD} $ | $0.64 \times \text{Nom}$ | 292 | $1.45 \times \text{Nom}$          | mV       | <ol style="list-style-type: none"> <li>The <math> V_{OD} </math> value shown in the Typ column is based on the condition of <math>XV_{DD\_SRDS2-Typ}=1.0V</math>, no common mode offset variation (<math>V_{OS}=500mV</math>), SerDes transmitter is terminated with 100-<math>\Omega</math> differential load between SD_TXn and SD_TXn.</li> <li>Amplitude setting:<br/>[A-J]TECR0[AMD_RED] = 0b001111</li> </ol> |
| Output differential voltage     | $ V_{OD} $ | $0.64 \times \text{Nom}$ | 250 | $1.45 \times \text{Nom}$          | mV       | <ol style="list-style-type: none"> <li>The <math> V_{OD} </math> value shown in the Typ column is based on the condition of <math>XV_{DD\_SRDS2-Typ}=1.0V</math>, no common mode offset variation (<math>V_{OS}=500mV</math>), SerDes transmitter is terminated with 100-<math>\Omega</math> differential load between SD_TXn and SD_TXn.</li> <li>Amplitude setting:<br/>[A-J]TECR0[AMD_RED] = 0b010011</li> </ol> |
| Output impedance (single-ended) | $R_O$      | 40                       | 50  | 60                                | $\Omega$ | —                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Output high voltage             | $V_{OH}$   | —                        | —   | $1.5 \times  V_{OD, \text{max}} $ | mV       | —                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Output low voltage              | $V_{OL}$   | $ V_{OD} , \text{min}/2$ | —   | —                                 | mV       | —                                                                                                                                                                                                                                                                                                                                                                                                                   |

Table 26 describes the SGMII SerDes receiver AC-coupled DC electrical characteristics.

Table 26. SGMII DC Receiver Electrical Characteristics<sup>1,2</sup>

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Symbol            | Min | Nom | Max  | Unit     | Condition                      |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-----|-----|------|----------|--------------------------------|
| Input differential voltage <sup>3</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | $V_{RX\_DIFFp-p}$ | 100 | —   | 1200 | mV       | L[A-J]GCR1[RECTL_SIGD] = 0b001 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                   | 175 | —   | 1200 | mV       | L[A-J]GCR1[RECTL_SIGD] = 0b100 |
| Loss of signal threshold <sup>4</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | VLOS              | 30  | —   | 100  | mV       | L[A-J]GCR1[RECTL_SIGD] = 0b001 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                   | 65  | —   | 175  | mV       | L[A-J]GCR1[RECTL_SIGD] = 0b100 |
| Receiver differential input impedance                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | $Z_{RX\_DIFF}$    | 80  | —   | 120  | $\Omega$ | —                              |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>The supply voltage is 1.0 V.</li> <li>Input must be externally AC-coupled.</li> <li><math>V_{RX\_DIFFp-p}</math> is also referred to as peak-to-peak input differential voltage.</li> <li>The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in the PCI Express interface. Refer to the PCI Express Differential Receiver (RX) Input Specifications section of the <i>PCI Express Specification</i> document for details.</li> </ol> |                   |     |     |      |          |                                |

## 2.5.4 RGMII and Other Interface DC Electrical Characteristics

Table 27 describes the DC electrical characteristics for the following interfaces:

- RGMII Ethernet
- SPI
- GPIO
- UART
- TIMER
- EE
- I<sup>2</sup>C
- Interrupts ( $\overline{\text{IRQn}}$ ,  $\overline{\text{NMI\_OUT/CP\_RX\_INT}}$ ,  $\overline{\text{INT\_OUT/CP\_TX\_INT}}$ )
- Clock and resets ( $\overline{\text{CLKIN/MCLKIN}}$ ,  $\overline{\text{PORESET}}$ ,  $\overline{\text{HRESET}}$ ,  $\overline{\text{HRESET\_IN}}$ )
- DMA External Request
- JTAG signals

**Table 27. 2.5 V I/O DC Electrical Characteristics**

| Characteristic                                                                                                                                                                                                                                                                                                                              | Symbol    | Min                | Max              | Unit          | Notes |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------------------|------------------|---------------|-------|
| Input high voltage                                                                                                                                                                                                                                                                                                                          | $V_{IH}$  | 1.7                | —                | V             | 1     |
| Input low voltage                                                                                                                                                                                                                                                                                                                           | $V_{IL}$  | —                  | 0.7              | V             | 1     |
| Input high current ( $V_{IN} = V_{DDIO}$ )                                                                                                                                                                                                                                                                                                  | $I_{INH}$ | —                  | 30               | $\mu\text{A}$ | 2     |
| Input low current ( $V_{IN} = \text{GND}$ )                                                                                                                                                                                                                                                                                                 | $I_{INL}$ | −30                | —                | $\mu\text{A}$ | 2     |
| Output high voltage ( $V_{DDIO} = \text{min}$ , $I_{OH} = -1.0 \text{ mA}$ )                                                                                                                                                                                                                                                                | $V_{OH}$  | 2.0                | $V_{DDIO} + 0.3$ | V             | 1     |
| Output low voltage ( $V_{DDIO} = \text{min}$ , $I_{OL} = 1.0 \text{ mA}$ )                                                                                                                                                                                                                                                                  | $V_{OL}$  | $\text{GND} - 0.3$ | 0.40             | V             | 1     |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. The min <math>V_{IL}</math> and max <math>V_{IH}</math> values are based on the respective min and max <math>V_{IN}</math> values listed in Table 4.</li> <li>2. The symbol <math>V_{IN}</math> represents the input voltage of the supply. It is referenced in Table 4.</li> </ol> |           |                    |                  |               |       |

## 2.6 AC Timing Characteristics

This section describes the AC timing characteristics for the MSC8157.

### 2.6.1 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

#### 2.6.1.1 DDR SDRAM Input AC Timing Specifications

Table 28 provides the input AC timing specifications for the DDR SDRAM when  $V_{DDDDR}$  (typ) = 1.5 V.

**Table 28. DDR3 SDRAM Input AC Timing Specifications for 1.5 V Interface**

| Parameter                                                                            | Symbol     | Min                                      | Max                                      | Unit |
|--------------------------------------------------------------------------------------|------------|------------------------------------------|------------------------------------------|------|
| AC input low voltage<br>• > 1200 MHz data rate<br>• ≤ 1200 MHz data rate             | $V_{ILAC}$ | —                                        | $MV_{REF} - 0.150$<br>$MV_{REF} - 0.175$ | V    |
| AC input high voltage<br>• > 1200 MHz data rate<br>• ≤ 1200 MHz data rate            | $V_{IHAC}$ | $MV_{REF} + 0.150$<br>$MV_{REF} + 0.175$ | —                                        | V    |
| <b>Note:</b> At recommended operating conditions with $V_{DDDDR}$ of $1.5 \pm 5\%$ . |            |                                          |                                          |      |

Table 29 provides the input AC timing specifications for the DDR SDRAM interface.

**Table 29. DDR SDRAM Input AC Timing Specifications**

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Symbol       | Min                                  | Max                             | Unit                       | Notes   |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------------------------------|---------------------------------|----------------------------|---------|
| Controller Skew for MDQS—MDQ/MECC<br>• 1333 MHz data rate<br>• 1200 MHz data rate<br>• 1066 MHz data rate<br>• 800 MHz data rate<br>• 667 MHz data rate                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | $t_{CISKEW}$ | –125<br>–142<br>–170<br>–200<br>–240 | 125<br>142<br>170<br>200<br>240 | ps<br>ps<br>ps<br>ps<br>ps | 1, 2, 4 |
| Tolerated Skew for MDQS—MDQ/MECC<br>• 1333 MHz data rate<br>• 1200 MHz data rate<br>• 1066 MHz data rate<br>• 800 MHz data rate<br>• 667 MHz data rate                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | $t_{DISKEW}$ | –250<br>–275<br>–300<br>–425<br>–510 | 250<br>275<br>300<br>425<br>510 | ps<br>ps<br>ps<br>ps<br>ps | 2, 3    |
| <b>Notes:</b> <ol style="list-style-type: none"> <li><math>t_{CISKEW}</math> represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.</li> <li>At recommended operating conditions with <math>V_{DDDDR}</math> (1.5 V) <math>\pm 5\%</math></li> <li>The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called <math>t_{DISKEW}</math>. This can be determined by the following equation: <math>t_{DISKEW} = \pm(T \div 4 - \text{abs}(t_{CISKEW}))</math> where T is the clock period and <math>\text{abs}(t_{CISKEW})</math> is the absolute value of <math>t_{CISKEW}</math>.</li> <li>The <math>t_{CISKEW}</math> test coverage is derived from the <math>t_{DISKEW}</math> parameters.</li> </ol> |              |                                      |                                 |                            |         |

Figure 9 shows the DDR3 SDRAM interface input timing diagram.

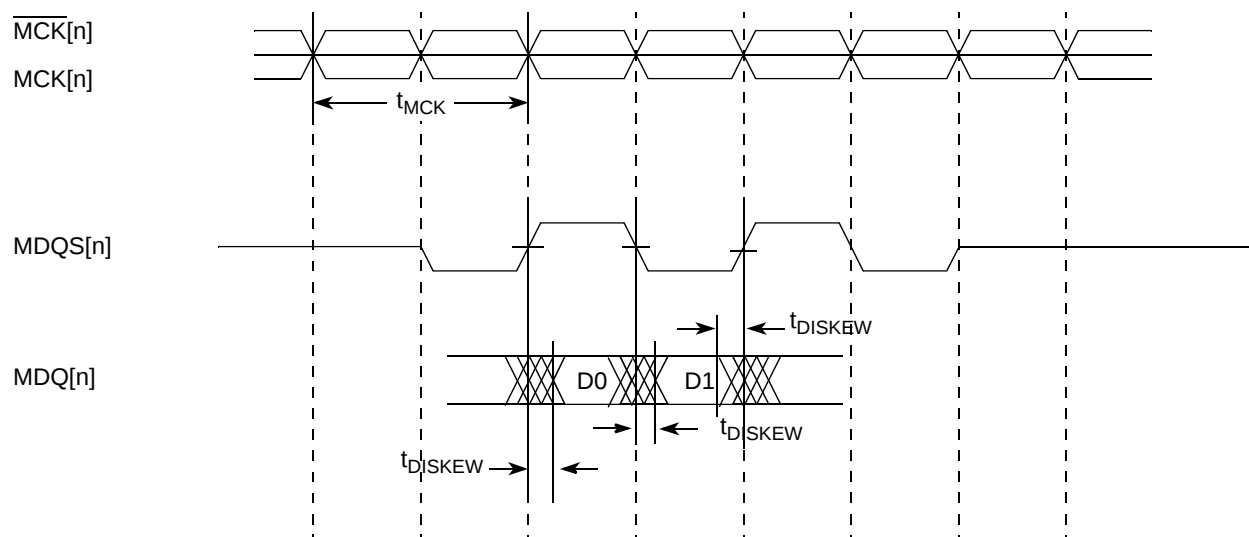


Figure 9. DDR3 SDRAM Interface Input Timing Diagram

## 2.6.1.2 DDR SDRAM Output AC Timing Specifications

Table 30 provides the output AC timing specifications for the DDR SDRAM interface.

Table 30. DDR SDRAM Output AC Timing Specifications

| Parameter                                 | Symbol <sup>1</sup> | Min                                      | Max                   | Unit                       | Notes |
|-------------------------------------------|---------------------|------------------------------------------|-----------------------|----------------------------|-------|
| MCK[n] cycle time                         | $t_{MCK}$           | 1.5                                      | 3                     | ns                         | 2     |
| ADDR/CMD output setup with respect to MCK | $t_{DDKHAS}$        | 0.606<br>0.675<br>0.744<br>0.917<br>1.10 | —<br>—<br>—<br>—<br>— | ns<br>ns<br>ns<br>ns<br>ns | 3     |
| ADDR/CMD output hold with respect to MCK  | $t_{DDKHAX}$        | 0.606<br>0.675<br>0.744<br>0.917<br>1.10 | —<br>—<br>—<br>—<br>— | ns<br>ns<br>ns<br>ns<br>ns | 3     |
| MCSn output setup with respect to MCK     | $t_{DDKHCS}$        | 0.606<br>0.675<br>0.744<br>0.917<br>1.10 | —<br>—<br>—<br>—<br>— | ns<br>ns<br>ns<br>ns<br>ns | 3     |
| MCSn output hold with respect to MCK      | $t_{DDKHCSX}$       | 0.606<br>0.675<br>0.744<br>0.917<br>1.10 | —<br>—<br>—<br>—<br>— | ns<br>ns<br>ns<br>ns<br>ns | 3     |
| MCK to MDQS Skew                          | $t_{DDKMHM}$        | −0.245<br>−0.375<br>−0.6                 | 0.245<br>0.375<br>0.6 | ns<br>ns<br>ns             | 4     |

Table 30. DDR SDRAM Output AC Timing Specifications (continued)

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Symbol <sup>1</sup>            | Min                             | Max                   | Unit                       | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|---------------------------------|-----------------------|----------------------------|-------|
| MDQ/MECC/MDM output setup with respect to MDQS <ul style="list-style-type: none"> <li>1333 MHz data rate</li> <li>1200 MHz data rate</li> <li>1066 MHz data rate</li> <li>800 MHz data rate</li> <li>667 MHz data rate</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | $t_{DDKHDS}$ ,<br>$t_{DDKLDS}$ | 250<br>275<br>300<br>375<br>450 | —<br>—<br>—<br>—<br>— | ps<br>ps<br>ps<br>ps<br>ps | 5, 6  |
| MDQ/MECC/MDM output hold with respect to MDQS <ul style="list-style-type: none"> <li>1333 MHz data rate</li> <li>1200 MHz data rate</li> <li>1066 MHz data rate</li> <li>800 MHz data rate</li> <li>667 MHz data rate</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | $t_{DDKHDX}$ ,<br>$t_{DDKLDX}$ | 250<br>275<br>300<br>375<br>450 | —<br>—<br>—<br>—<br>— | ps<br>ps<br>ps<br>ps<br>ps | 5     |
| MDQS preamble                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | $t_{DDKHMP}$                   | $0.9 \times t_{MCK}$            | —                     | ns                         | —     |
| MDQS postamble                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | $t_{DDKHME}$                   | $0.4 \times t_{MCK}$            | $0.6 \times t_{MCK}$  | ns                         | —     |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>The symbols used for timing specifications follow the pattern of <math>t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}</math> for inputs and <math>t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}</math> for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, <math>t_{DDKHAS}</math> symbolizes DDR timing (DD) for the time <math>t_{MCK}</math> memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, <math>t_{DDKLDS}</math> symbolizes DDR timing (DD) for the time <math>t_{MCK}</math> memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.</li> <li>All MCK/MCK referenced measurements are made from the crossing of the two signals.</li> <li>ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, <math>\overline{MCS}</math>, and MDQ/MECC/MDM/MDQS.</li> <li>Note that <math>t_{DDKHMH}</math> follows the symbol conventions described in note 1. For example, <math>t_{DDKHMH}</math> describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). <math>t_{DDKHMH}</math> can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the <i>MSC8157 Reference Manual</i> for a description and understanding of the timing modifications enabled by use of these bits.</li> <li>Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MSC8157.</li> <li>At recommended operating conditions with <math>V_{DDDDR}</math> (1.5 V) <math>\pm</math> 5%.</li> </ol> |                                |                                 |                       |                            |       |

**Note:** For the ADDR/CMD setup and hold specifications in Table 30, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Figure 10 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement ( $t_{DDKHMH}$ ).

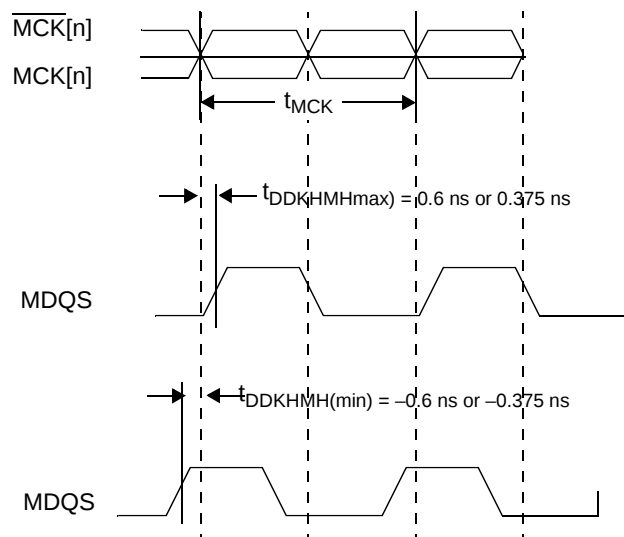


Figure 10. MCK to MDQS Timing

Figure 11 shows the DDR SDRAM output timing diagram.

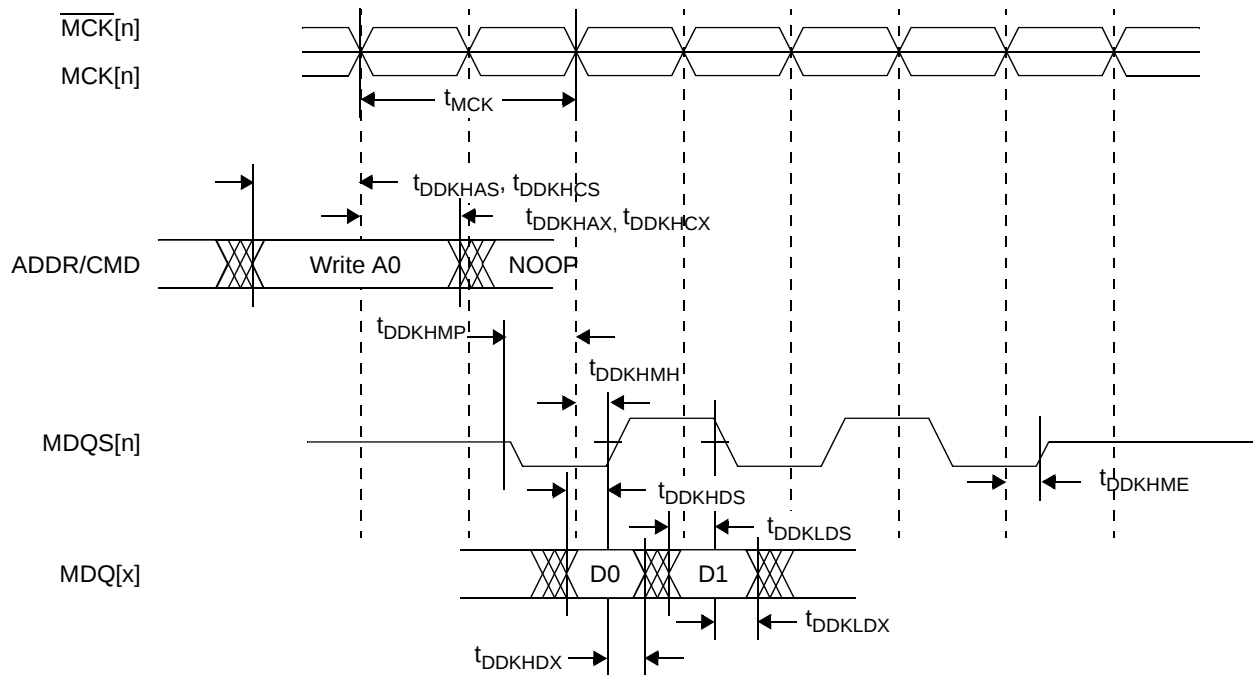


Figure 11. DDR SDRAM Output Timing

Figure 12 provides the AC test load for the DDR3 controller bus.

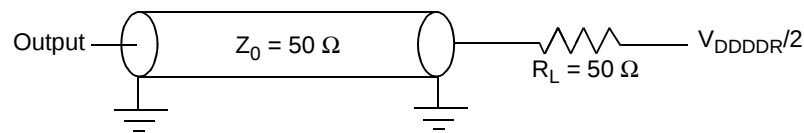


Figure 12. DDR3 Controller Bus AC Test Load

### 2.6.1.3 DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR3 SDRAM controller interface. Figure 13 shows the differential timing specification.

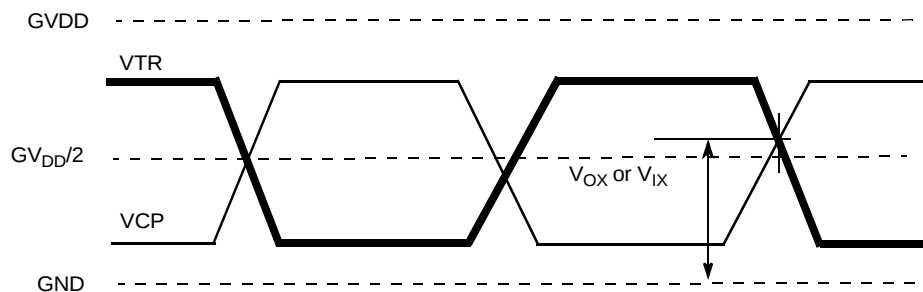


Figure 13. DDR3 SDRAM Differential Timing Specifications

**Note:** VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as  $\overline{\text{MCK}}$  or  $\overline{\text{MDQS}}$ ).

Table 31 provides the DDR3 differential specifications for the differential signals MDQS/ $\overline{\text{MDQS}}$  and MCK/ $\overline{\text{MCK}}$ .

Table 31. DDR3 SDRAM Differential Electrical Characteristics

| Parameter                                                           | Symbol     | Min                            | Max                            | Unit |
|---------------------------------------------------------------------|------------|--------------------------------|--------------------------------|------|
| Input AC differential cross-point voltage                           | $V_{IXAC}$ | $0.5 \times V_{DDDDR} - 0.150$ | $0.5 \times V_{DDDDR} + 0.150$ | V    |
| Output AC differential cross-point voltage                          | $V_{OXAC}$ | $0.5 \times V_{DDDDR} - 0.115$ | $0.5 \times V_{DDDDR} + 0.115$ | V    |
| <b>Note:</b> I/O drivers are calibrated before making measurements. |            |                                |                                |      |

## 2.6.2 HSSI AC Timing Specifications

The following subsections define the AC timing requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

### 2.6.2.1 AC Requirements for SerDes Reference Clock

Table 32 lists AC requirements for the SerDes reference clocks.

**Note:** Specifications are valid at the recommended operating conditions listed in Table 4.

Table 32. SD\_REF\_CLK[1–2] and  $\overline{\text{SD\_REF\_CLK}}$ [1–2] Input Clock Requirements

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Symbol                | Min          | Nom                     | Max        | Units      | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|--------------|-------------------------|------------|------------|-------|
| SD_REF_CLK[1–2]/ $\overline{\text{SD\_REF\_CLK}}$ [1–2] frequency range                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | $t_{CLK\_REF}$        | —            | 100/125<br>CPRI: 122.88 | —          | MHz        | 1     |
| SD_REF_CLK[1–2]/ $\overline{\text{SD\_REF\_CLK}}$ [1–2] clock frequency tolerance<br>• Serial RapidIO, CPRI, SGMII<br>• PCI Express interface                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | $t_{CLK\_TOL}$        | –100<br>–300 | —<br>—                  | 100<br>300 | ppm<br>ppm | —     |
| SD_REF_CLK[1–2]/ $\overline{\text{SD\_REF\_CLK}}$ [1–2] reference clock duty cycle                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | $t_{CLK\_DUTY}$       | 40           | 50                      | 60         | %          | 4     |
| SD_REF_CLK[1–2]/ $\overline{\text{SD\_REF\_CLK}}$ [1–2]max deterministic peak-peak jitter at $10^{-6}$ BER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | $t_{CLK\_DJ}$         | —            | —                       | 42         | ps         | —     |
| SD_REF_CLK[1–2]/ $\overline{\text{SD\_REF\_CLK}}$ [1–2] total reference clock jitter at $10^{-6}$ BER (peak-to-peak jitter at ref_clk input)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | $t_{CLK\_TJ}$         | —            | —                       | 86         | ps         | 2     |
| SD_REF_CLK/SD_REF_CLK rising/falling edge rate                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | $t_{CLKRR}/t_{CLKFR}$ | 1            | —                       | 4          | V/ns       | 3     |
| Differential input high voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | $V_{IH}$              | 200          | —                       | —          | mV         | 4     |
| Differential input low voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | $V_{IL}$              | —            | —                       | –200       | mV         | 4     |
| Rising edge rate (SD_REF_CLKn to falling edge rate)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Rise-Fall             | —            | —                       | 20         | %          | 5, 6  |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>Only 100, 122.88, and 125 MHz have been tested. CPRI uses 122.88 MHz. The other interfaces use 100 or 125 MHz. Other values will not work correctly with the rest of the system.</li> <li>Limits are from PCI Express CEM Rev 2.0.</li> <li>Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLKn minus <math>\overline{\text{SD\_REF\_CLK}}</math>n). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 14.</li> <li>Measurement taken from differential waveform.</li> <li>Measurement taken from single-ended waveform.</li> <li>Matching applies to rising edge for SD_REF_CLKn and falling edge rate for <math>\overline{\text{SD\_REF\_CLK}}</math>n. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLKn rising meets <math>\overline{\text{SD\_REF\_CLK}}</math>n falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rising edge rate of SD_REF_CLKn should be compared to the falling edge rate of <math>\overline{\text{SD\_REF\_CLK}}</math>n; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 15.</li> <li>REF_CLK jitter must be less than 0.05 UI when measured against a Golden PLL reference. The Golden PLL must have a maximum baud rate bandwidth greater than 1667, with a maximum 20 dB/dec rolloff down to a baud rate of 16.67 with no peaking around the corner frequency.</li> </ol> |                       |              |                         |            |            |       |

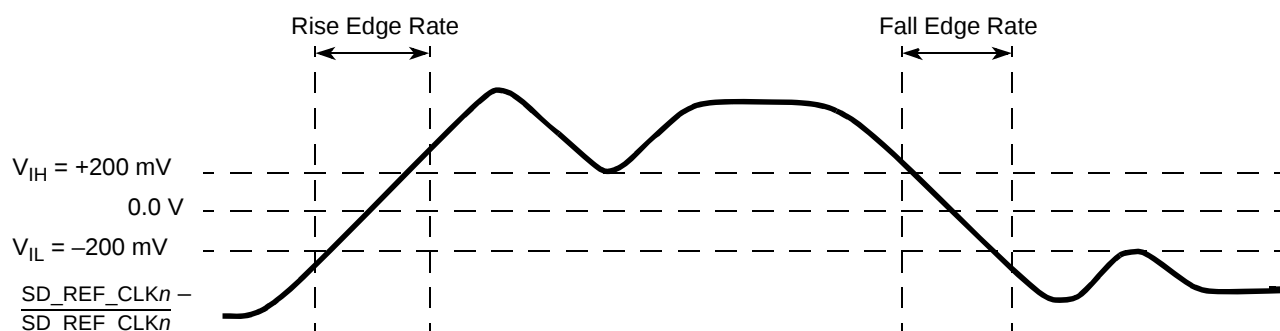


Figure 14. Differential Measurement Points for Rise and Fall Time

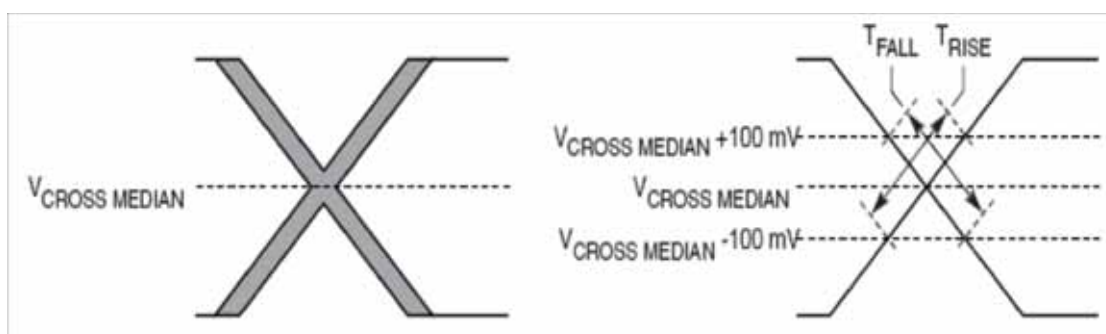


Figure 15. Single-Ended Measurement Points for Rise and Fall Time Matching

### 2.6.2.2 Spread Spectrum Clock

SD\_REF\_CLK[1–2] and  $\overline{\text{SD\_REF\_CLK}}[1–2]$  were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 KHz rate is allowed), assuming both ends have the same reference clock and the industry protocol supports it. For better results, use a source without significant unintended modulation.

### 2.6.2.3 PCI Express AC Physical Layer Specifications

The AC requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8157 supports a 2.5 Gbps or a 5.0 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 2.0*. The 2.5 Gbps transmitter specifications are defined in Table 33 and the receiver specifications are defined in Table 34. The 5.0 Gbps transmitter specifications are defined in Table 35 and the receiver specifications are defined in Table 36. The parameters are specified at the component pins. the AC timing specifications do not include REF\_CLK jitter.

**Note:** Specifications are valid at the recommended operating conditions listed in Table 4.

Table 33. PCI Express 2.0 (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications

| Parameter     | Symbol              | Min    | Nom    | Max    | Units | Comments                                                                                                                                                                                                                                    |
|---------------|---------------------|--------|--------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Unit interval | UI                  | 399.88 | 400.00 | 400.12 | ps    | Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.                                                                                                                             |
| Tx eye width  | $T_{\text{TX-EYE}}$ | 0.75   | —      | —      | UI    | The maximum transmitter jitter can be derived as $T_{\text{TX-MAX-JITTER}} = 1 - T_{\text{TX-EYE}} = 0.25$ UI. This does not include spread spectrum or REF_CLK jitter. It includes device random jitter at $10^{-12}$ . See notes 2 and 3. |

Table 33. PCI Express 2.0 (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications (continued)

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Symbol                            | Min | Nom | Max   | Units | Comments                                                                                                                                                                                                                                                                                                                                                            |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|-----|-----|-------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Time between the jitter median and maximum deviation from the median.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | —   | —   | 0.125 | UI    | Jitter is defined as the measurement variation of the crossing points ( $V_{TX-DIFFP-P} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2 and 3. |
| AC coupling capacitor                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | $C_{TX}$                          | 75  | —   | 200   | nF    | All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.                                                                                                                                                                                                                   |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. No test load is necessarily associated with this value.</li> <li>2. Specified at the measurement point into a timing and voltage test load as shown in Figure 16 and measured over any 250 consecutive Tx UIs.</li> <li>3. A <math>T_{TX-EYE} = 0.75</math> UI provides for a total sum of deterministic and random jitter budget of <math>T_{TX-NAX-JITTER} = 0.25</math> UI for the transmitter collected over any 250 consecutive Tx UIs. The <math>T_{TX-EYE-MEDIAN-to-MAX-JITTER}</math> median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.</li> <li>4. The DSP device SerDes transmitter does not have a built-in <math>C_{TX}</math>. An external AC coupling capacitor is required.</li> </ol> |                                   |     |     |       |       |                                                                                                                                                                                                                                                                                                                                                                     |

Table 34. PCI Express 2.0 (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Symbol                            | Min    | Nom    | Max    | Units | Comments                                                                                                                                                                                                                                                                                                                                                                |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|--------|--------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Unit Interval                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | UI                                | 399.88 | 400.00 | 400.12 | ps    | Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.                                                                                                                                                                                                                                                         |
| Minimum receiver eye width                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | $T_{RX-EYE}$                      | 0.4    | —      | —      | UI    | The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See notes 2 and 3.                                                                                                                                                                                         |
| Maximum time between the jitter median and maximum deviation from the median.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | —      | —      | 0.3    | UI    | Jitter is defined as the measurement variation of the crossing points ( $V_{RX-DIFFP-P} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2, 3, and 4. |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. No test load is necessarily associated with this value.</li> <li>2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 16 should be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.</li> <li>3. A <math>T_{RX-EYE} = 0.40</math> UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The <math>T_{RX-EYE-MEDIAN-to-MAX-JITTER}</math> specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.</li> <li>4. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.</li> </ol> |                                   |        |        |        |       |                                                                                                                                                                                                                                                                                                                                                                         |

Table 35. PCI Express 2.0 (5.0 Gbps) Differential Transmitter (Tx) Output AC Specifications

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Symbol            | Min    | Nom    | Max    | Units | Comments                                                                                                                                          |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|--------|--------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| Unit Interval                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | UI                | 199.94 | 200.00 | 200.06 | ps    | Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.                                   |
| Minimum Tx eye width                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | $T_{TX-EYE}$      | 0.75   | —      | —      | UI    | The maximum Transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See notes 2 and 3.                              |
| Tx RMS deterministic jitter > 1.5 MHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | $T_{TX-HF-DJ-DD}$ | —      | —      | 0.15   | ps    | —                                                                                                                                                 |
| Tx RMS deterministic jitter < 1.5 MHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | $T_{TX-LF-RMS}$   | —      | 3.0    | —      | ps    | Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps                                                                                        |
| AC coupling capacitor                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | $C_{TX}$          | 75     | —      | 200    | nF    | All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4. |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. No test load is necessarily associated with this value.</li> <li>2. Specified at the measurement point into a timing and voltage test load as shown in Figure 16 and measured over any 250 consecutive Tx UIs.</li> <li>3. A <math>T_{TX-EYE} = 0.75</math> UI provides for a total sum of deterministic and random jitter budget of <math>T_{TX-MAX-JITTER} = 0.25</math> UI for the Transmitter collected over any 250 consecutive Tx UIs. The <math>T_{TX-EYE-MEDIAN-to-MAX-JITTER}</math> median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.</li> <li>4. The DSP device SerDes transmitter does not have a built-in <math>C_{TX}</math>. An external AC coupling capacitor is required.</li> </ol> |                   |        |        |        |       |                                                                                                                                                   |

Table 36. PCI Express 2.0 (5.0 Gbps) Differential Receiver (Rx) Input AC Specifications

| Parameter                                                                    | Symbol            | Min    | Nom    | Max    | Units | Conditions                                                                                                      |
|------------------------------------------------------------------------------|-------------------|--------|--------|--------|-------|-----------------------------------------------------------------------------------------------------------------|
| Unit Interval                                                                | UI                | 199.40 | 200.00 | 200.06 | ps    | Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1. |
| Max Rx inherent timing error                                                 | $T_{RX-TJ-CC}$    | —      | —      | 0.4    | UI    | The maximum inherent total timing error for common REF_CLK Rx architecture                                      |
| Maximum time between the jitter median and maximum deviation from the median | $T_{RX-TJ-DC}$    | —      | —      | 0.34   | UI    | Max Rx inherent total timing error                                                                              |
| Max Rx inherent deterministic timing error                                   | $T_{RX-DJ-DD-CC}$ | —      | —      | 0.30   | UI    | The maximum inherent deterministic timing error for common REF_CLK Rx architecture                              |
| Max Rx inherent deterministic timing error                                   | $T_{RX-DJ-DD-DC}$ | —      | —      | 0.24   | UI    | The maximum inherent deterministic timing error for common REF_CLK Rx architecture                              |
| <b>Note:</b> No test load is necessarily associated with this value.         |                   |        |        |        |       |                                                                                                                 |

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in Figure 16.

**Note:** The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

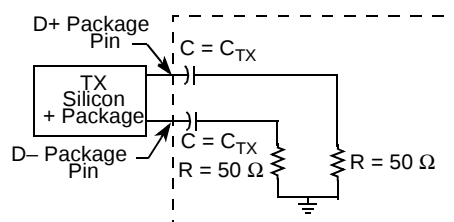


Figure 16. Test Measurement Load

## 2.6.2.4 Serial RapidIO AC Timing Specifications

**Note:** Specifications are valid at the recommended operating conditions listed in [Table 4](#).

[Table 37](#) defines the transmitter AC specifications for the Serial RapidIO interface at frequencies up to 3.125 Gbaud. The AC timing specifications do not include REF\_CLK jitter.

**Table 37. Serial RapidIO Transmitter AC Timing Specifications Up to 3.125 Gbaud**

| Characteristic             | Symbol | Min          | Nom | Max          | Unit   |
|----------------------------|--------|--------------|-----|--------------|--------|
| Deterministic Jitter       | $J_D$  | —            | —   | 0.17         | UI p-p |
| Total Jitter               | $J_T$  | —            | —   | 0.35         | UI p-p |
| Unit Interval: 1.25 Gbaud  | UI     | 800 – 100ppm | 800 | 800 + 100ppm | ps     |
| Unit Interval: 2.5 Gbaud   | UI     | 400 – 100ppm | 400 | 400 + 100ppm | ps     |
| Unit Interval: 3.125 Gbaud | UI     | 320 – 100ppm | 320 | 320 + 100ppm | ps     |

[Table 38](#) defines the Receiver AC specifications for the Serial RapidIO interface at frequencies up to 3.125 Gbaud. The AC timing specifications do not include REF\_CLK jitter.

**Table 38. Serial RapidIO Receiver AC Timing Specifications Up to 3.125 Gbaud**

| Characteristic                                                                                                                                                                                                                                                                                                                                                                                                                             | Symbol   | Min          | Nom | Max          | Unit   | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|--------------|-----|--------------|--------|-------|
| Deterministic Jitter Tolerance                                                                                                                                                                                                                                                                                                                                                                                                             | $J_D$    | —            | —   | 0.37         | UI p-p | 1     |
| Combined Deterministic and Random Jitter Tolerance                                                                                                                                                                                                                                                                                                                                                                                         | $J_{DR}$ | —            | —   | 0.55         | UI p-p | 1     |
| Total Jitter Tolerance                                                                                                                                                                                                                                                                                                                                                                                                                     | $J_T$    | —            | —   | 0.65         | UI p-p | 1, 2  |
| Bit Error Rate                                                                                                                                                                                                                                                                                                                                                                                                                             | BER      | —            | —   | $10^{-12}$   | —      | —     |
| Unit Interval: 1.25 Gbaud                                                                                                                                                                                                                                                                                                                                                                                                                  | UI       | 800 – 100ppm | 800 | 800 + 100ppm | ps     | —     |
| Unit Interval: 2.5 Gbaud                                                                                                                                                                                                                                                                                                                                                                                                                   | UI       | 400 – 100ppm | 400 | 400 + 100ppm | ps     | —     |
| Unit Interval: 3.125 Gbaud                                                                                                                                                                                                                                                                                                                                                                                                                 | UI       | 320 – 100ppm | 320 | 320 + 100ppm | ps     | —     |
| <b>Notes:</b> 1. Measured at receiver.<br>2. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of <a href="#">Figure 17</a> . The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects. |          |              |     |              |        |       |

[Table 39](#) defines the short run transmitter AC specifications for the Serial RapidIO interface at 5 Gbaud. The AC timing specifications do not include REF\_CLK jitter.

**Table 39. Serial RapidIO Short Run Transmitter AC Timing Specifications at 5.0 Gbaud**

| Characteristic                       | Symbol     | Min            | Nom   | Max            | Unit   |
|--------------------------------------|------------|----------------|-------|----------------|--------|
| Uncorrelated High Probability Jitter | $T_{UHPJ}$ | —              | —     | 0.15           | UI p-p |
| Total Jitter                         | $T_{TJ}$   | —              | —     | 0.30           | UI p-p |
| Baud Rate                            | UI         | 5.000 – 100ppm | 5.000 | 5.000 + 100ppm | Gbaud  |

[Table 40](#) defines the short run Receiver AC specifications for the Serial RapidIO interface at 5 Gbaud. The AC timing specifications do not include REF\_CLK jitter.

**Table 40. Serial RapidIO Short Run Receiver AC Timing Specifications at 5 Gbaud**

| Characteristic                               | Symbol       | Min            | Nom   | Max            | Unit  |
|----------------------------------------------|--------------|----------------|-------|----------------|-------|
| Rx Baud Rate                                 | R_Baud       | 5.000 – 100ppm | 5.000 | 5.000 + 100ppm | Gbaud |
| Uncorrelated Bounded High Probability Jitter | $R_{UBHPJ}$  | —              | —     | 0.15           | UIp-p |
| Correlated Bounded High Probability Jitter   | $R_{CBHPJ}$  | —              | —     | 0.3            | UIp-p |
| Bounded High Probability Jitter              | $R_{BHPJ}$   | —              | —     | 0.45           | UIp-p |
| Sinusoidal Jitter maximum                    | $R_{SJ-max}$ | —              | —     | 5              | UIp-p |
| Sinusoidal Jitter, High Frequency            | $R_{SJ-hf}$  | —              | —     | 0.05           | UIp-p |

**Table 40. Serial RapidIO Short Run Receiver AC Timing Specifications at 5 Gbaud (continued)**

| Characteristic                                                                                                                                                                                                                                                                | Symbol | Min | Nom | Max | Unit  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|-----|-----|-------|
| Total jitter (without sinusoidal jitter)                                                                                                                                                                                                                                      | R_Tj   | —   | —   | 0.6 | UIp-p |
| <b>Note:</b> The AC specifications do not include REF_CLK jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region in <a href="#">Figure 18</a> . The ISI jitter (R_CBHPJ) and amplitude have to be correlated, for example, by a PCB trace. |        |     |     |     |       |

[Table 41](#) defines the Transmitter AC specifications for long run Serial RapidIO interfaces using a transfer rate of 5 Gbps. The AC timing specifications do not include REF\_CLK jitter.

**Table 41. Serial RapidIO Transmitter Long Run AC Timing for Transfer Rate of 5 Gbps**

| Characteristic                       | Symbol | Min             | Nom   | Max             | Unit   | Conditions                 |
|--------------------------------------|--------|-----------------|-------|-----------------|--------|----------------------------|
| Tx Baud Rate                         | T_Baud | 5.000 – 100 ppm | 5.000 | 5.000 + 100 ppm | Gbps   | ± 100 ppm                  |
| Uncorrelated high probability jitter | T_UHPJ |                 |       | 0.15            | UI p-p | With de-emphasis disabled. |
| Total Jitter                         | T_TJ   | —               | —     | 0.30            | UI p-p | With de-emphasis disabled. |

[Table 42](#) defines the Receiver AC specifications for long run Serial RapidIO interfaces using a transfer rate of 5 Gbps. The AC timing specifications do not include REF\_CLK jitter.

**Table 42. Serial RapidIO Receiver Long Run AC Timing for Transfer Rate of 5 Gbps**

| Characteristic                                                                                                                                                                                                                                                                                             | Symbol   | Min             | Nom   | Max             | Unit   | Condition                           |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-----------------|-------|-----------------|--------|-------------------------------------|
| Rx Baud Rate                                                                                                                                                                                                                                                                                               | R_Baud   | 5.000 – 100 ppm | 5.000 | 5.000 + 100 ppm | Gbps   |                                     |
| Gaussian                                                                                                                                                                                                                                                                                                   | R_GJ     |                 |       | 0.275           | UI p-p | Informative jitter budget @Rx input |
| Uncorrelated bounded high probability jitter ( $D_j$ )                                                                                                                                                                                                                                                     | R_UBHPJ  |                 |       | 0.15            | UI p-p | Informative jitter budget @Rx input |
| Correlated bounded high probability jitter (ISI)                                                                                                                                                                                                                                                           | R_CBHPJ  |                 |       | 0.525           | UI p-p | Informative jitter budget @Rx input |
| Bounded high probability jitter ( $D_j$ + ISI)                                                                                                                                                                                                                                                             | R_BHPJ   |                 |       | 0.675           | UI p-p | Informative jitter budget @Rx input |
| Sinusoidal jitter, maximum                                                                                                                                                                                                                                                                                 | R_SJ-max |                 |       | 5               | UI p-p | Informative jitter budget @Rx input |
| Sinusoidal jitter, high frequency                                                                                                                                                                                                                                                                          | R_SJ-hf  |                 |       | 0.05            | UI p-p | Informative jitter budget @Rx input |
| Total Jitter (does not include sinusoidal jitter).                                                                                                                                                                                                                                                         | R_TJ     |                 |       | 0.95            | UI p-p | Informative jitter budget @Rx input |
| <b>Note:</b> The AC specifications do not include REF_CLK jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of <a href="#">Figure 18</a> . The ISI jitter (R_CBHPJ) and amplitude have to be correlated, for example, by a PC trace. |          |                 |       |                 |        |                                     |

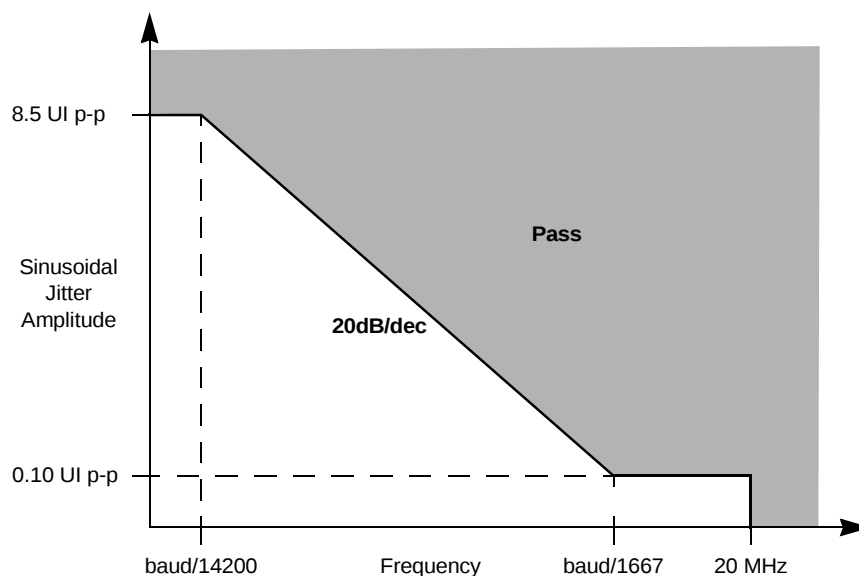


Figure 17. Single Frequency Sinusoidal Jitter Limits for Data Rates for 3.125 Gbps and below

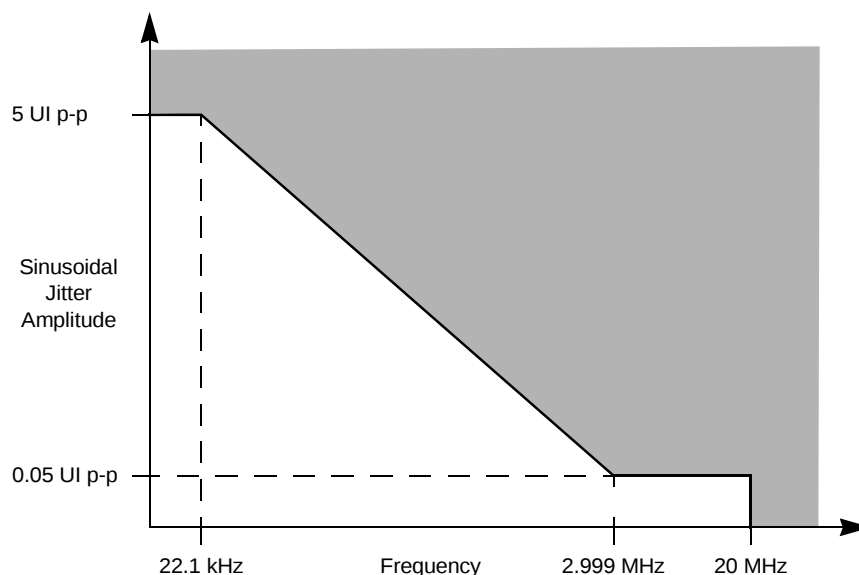


Figure 18. Single Frequency Sinusoidal Jitter Limits for Data Rate 5.0 Gbps

### 2.6.2.5 CPRI AC Timing Specifications

**Note:** Specifications are valid at the recommended operating conditions listed in [Table 4](#).

[Table 43](#) defines the transmitter AC specifications for the CPRI LV lanes. The AC timing specifications do not include REF\_CLK jitter.

Table 43. CPRI Transmitter AC Timing Specifications (LV-I: 1.2288, 2.4576, and 3.072 Gbps)

| Characteristic              | Symbol | Min               | Nom      | Max               | Unit   |
|-----------------------------|--------|-------------------|----------|-------------------|--------|
| Deterministic Jitter        | JD     | —                 | —        | 0.17              | UI p-p |
| Total Jitter                | JT     | —                 | —        | 0.35              | UI p-p |
| Unit Interval: 1.2288 GBaud | UI     | 1/1228.8 – 100ppm | 1/1228.8 | 1/1228.8 + 100ppm | μs     |

**Table 43. CPRI Transmitter AC Timing Specifications (LV-I: 1.2288, 2.4576, and 3.072 Gbps) (continued)**

| Characteristic              | Symbol | Min               | Nom      | Max               | Unit |
|-----------------------------|--------|-------------------|----------|-------------------|------|
| Unit Interval: 2.4576 GBaud | UI     | 1/2457.6 – 100ppm | 1/2457.6 | 1/2457.6 + 100ppm | μs   |
| Unit Interval: 3.072 GBaud  | UI     | 1/3072.0 – 100ppm | 1/3072.0 | 1/3072.0 + 100ppm | μs   |

Table 44 defines the transmitter AC specifications for the CPRI LV-II lanes. The AC timing specifications do not include REF\_CLK jitter.

**Table 44. CPRI Transmitter AC Timing Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)**

| Characteristic                       | Symbol | Min               | Nom      | Max               | Unit   |
|--------------------------------------|--------|-------------------|----------|-------------------|--------|
| Uncorrelated High Probability Jitter | T_UHPJ | —                 | —        | 0.15              | UI p-p |
| Total Jitter                         | T_TJ   | —                 | —        | 0.30              | UI p-p |
| Unit Interval: 1.2288 GBaud          | UI     | 1/1228.8 – 100ppm | 1/1228.8 | 1/1228.8 + 100ppm | μs     |
| Unit Interval: 2.4576 GBaud          | UI     | 1/2457.6 – 100ppm | 1/2457.6 | 1/2457.6 + 100ppm | μs     |
| Unit Interval: 3.072 GBaud           | UI     | 1/3072.0 – 100ppm | 1/3072.0 | 1/3072.0 + 100ppm | μs     |
| Unit Interval: 4.9152 GBaud          | UI     | 1/4915.2 – 100ppm | 1/4915.2 | 1/4915.2 + 100ppm | μs     |
| Unit Interval: 6.144 GBaud           | UI     | 1/6144.0 – 100ppm | 1/6144.0 | 1/6144.0 + 100ppm | μs     |

Table 45 defines the Receiver AC specifications for CPRI LV. The AC timing specifications do not include REF\_CLK jitter.

**Table 45. CPRI Receiver AC Timing Specifications (LV-I: 1.2288, 2.4576, and 3.072 Gbps)**

| Characteristic                                     | Symbol | Min               | Nom      | Max               | Unit   |
|----------------------------------------------------|--------|-------------------|----------|-------------------|--------|
| Deterministic jitter tolerance                     | JD     | —                 | —        | 0.37              | UI p-p |
| Combined deterministic and random jitter tolerance | JDR    | —                 | —        | 0.55              | UI p-p |
| Total Jitter tolerance                             | JT     | —                 | —        | 0.65              | UI p-p |
| Unit Interval: 1.2288 GBaud                        | UI     | 1/1228.8 – 100ppm | 1/1228.8 | 1/1228.8 + 100ppm | ps     |
| Unit Interval: 2.4576 GBaud                        | UI     | 1/2457.6 – 100ppm | 1/2457.6 | 1/2457.6 + 100ppm | ps     |
| Unit Interval: 3.072 GBaud                         | UI     | 1/3072.0 – 100ppm | 1/3072.0 | 1/3072.0 + 100ppm | ps     |
| Bit error ratio                                    | BER    | —                 | —        | 10 <sup>-12</sup> | —      |

Table 46 defines the Receiver AC specifications for CPRI LV-II. The AC timing specifications do not include REF\_CLK jitter.

**Table 46. CPRI Receiver AC Timing Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)**

| Characteristic                                                                                                                                                                                                                                                                            | Symbol   | Min               | Nom      | Max               | Unit   |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------------------|----------|-------------------|--------|
| Gaussian                                                                                                                                                                                                                                                                                  | R_GJ     | —                 | —        | 0.275             | UI p-p |
| Uncorrelated bounded high probability jitter                                                                                                                                                                                                                                              | R_UBHPJ  | —                 | —        | 0.150             | UI p-p |
| Correlated bounded high probability jitter                                                                                                                                                                                                                                                | R_CBHPJ  | —                 | —        | 0.525             | UI p-p |
| Bounded high probability jitter                                                                                                                                                                                                                                                           | R_BHPJ   | —                 | —        | 0.675             | UI p-p |
| Sinusoidal jitter, maximum                                                                                                                                                                                                                                                                | R_SJ-max | —                 | —        | 5.000             | UI p-p |
| Sinusoidal jitter, high frequency                                                                                                                                                                                                                                                         | R_SJ-hf  | —                 | —        | 0.050             | UI p-p |
| Total Jitter (does not include sinusoidal jitter).                                                                                                                                                                                                                                        | R_TJ     | —                 | —        | 0.950             | UI p-p |
| Unit Interval: 1.2288 GBaud                                                                                                                                                                                                                                                               | UI       | 1/1228.8 – 100ppm | 1/1228.8 | 1/1228.8 + 100ppm | μs     |
| Unit Interval: 2.4576 GBaud                                                                                                                                                                                                                                                               | UI       | 1/2457.6 – 100ppm | 1/2457.6 | 1/2457.6 + 100ppm | μs     |
| Unit Interval: 3.072 GBaud                                                                                                                                                                                                                                                                | UI       | 1/3072.0 – 100ppm | 1/3072.0 | 1/3072.0 + 100ppm | μs     |
| Unit Interval: 4.9152 GBaud                                                                                                                                                                                                                                                               | UI       | 1/4915.2 – 100ppm | 1/4915.2 | 1/4915.2 + 100ppm | μs     |
| Unit Interval: 6.144 GBaud                                                                                                                                                                                                                                                                | UI       | 1/6144.0 – 100ppm | 1/6144.0 | 1/6144.0 + 100ppm | μs     |
| <b>Note:</b> The AC specifications do not include REF_CLK jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 18. The ISI jitter (R_CBHPJ) and amplitude have to be correlated, for example, by a PC trace. |          |                   |          |                   |        |

**Note:** The intended application is a point-to-point interface up to two connectors. The maximum allowed total loss (channel + interconnects + other loss) is 20.4 dB @ 6.144 Gbps.

## 2.6.2.6 SGMII AC Timing Specifications

**Note:** Specifications are valid at the recommended operating conditions listed in Table 4.

Transmitter and receiver AC characteristics are measured at the transmitter outputs ( $\overline{\text{SD}}_{\text{[A-J]}}\text{TX}$  and  $\overline{\text{SD}}_{\text{[A-J]}}\text{TX}$ ) or at the receiver inputs ( $\text{SD}_{\text{[A-J]}}\text{RX}$  and  $\text{SD}_{\text{[A-J]}}\text{RX}$ ) as depicted in Figure 19, respectively.

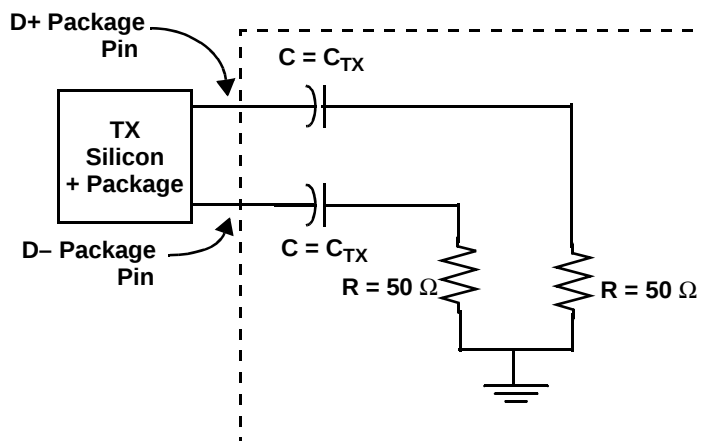


Figure 19. SGMII AC Test/Measurement Load

Table 47 provides the SGMII transmit AC timing specifications. The AC timing specifications do not include REF\_CLK jitter.

Table 47. SGMII Transmit AC Timing Specifications

| Parameter             | Symbol | Min          | Nom | Max          | Unit   | Condition                           |
|-----------------------|--------|--------------|-----|--------------|--------|-------------------------------------|
| Unit interval         | UI     | 800 – 100ppm | 800 | 800 + 100ppm | pS     | ± 100ppm                            |
| Deterministic jitter  | JD     | —            | —   | 0.17         | UI p-p | —                                   |
| Total jitter          | JT     | —            | —   | 0.35         | UI p-p | —                                   |
| AC coupling capacitor | CTX    | 75           | —   | 200          | nF     | All transmitters must be AC-coupled |

**Note:** The AC specifications do not include REF\_CLK jitter.

Table 48 provides the SGMII receiver AC timing specifications. The AC timing specifications do not include REF\_CLK jitter.

Table 48. SGMII Receive AC Timing Specifications

| Parameter                                          | Symbol | Min          | Nom | Max          | Unit   | Condition             |
|----------------------------------------------------|--------|--------------|-----|--------------|--------|-----------------------|
| Unit interval                                      | UI     | 800 – 100ppm | 800 | 800 + 100ppm | pS     | ± 100ppm              |
| Deterministic jitter tolerance                     | JD     | —            | —   | 0.37         | UI p-p | Measured at receiver. |
| Combined deterministic and random jitter tolerance | JDR    | —            | —   | 0.55         | UI p-p | Measured at receiver  |
| Total jitter tolerance                             | JT     | —            | —   | 0.65         | UI p-p | Measured at receiver  |
| Bit error ratio                                    | BER    | —            | —   | $10^{-12}$   | —      | —                     |

**Note:** The AC specifications do not include REF\_CLK jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region shown in Figure 20 or Figure 21.

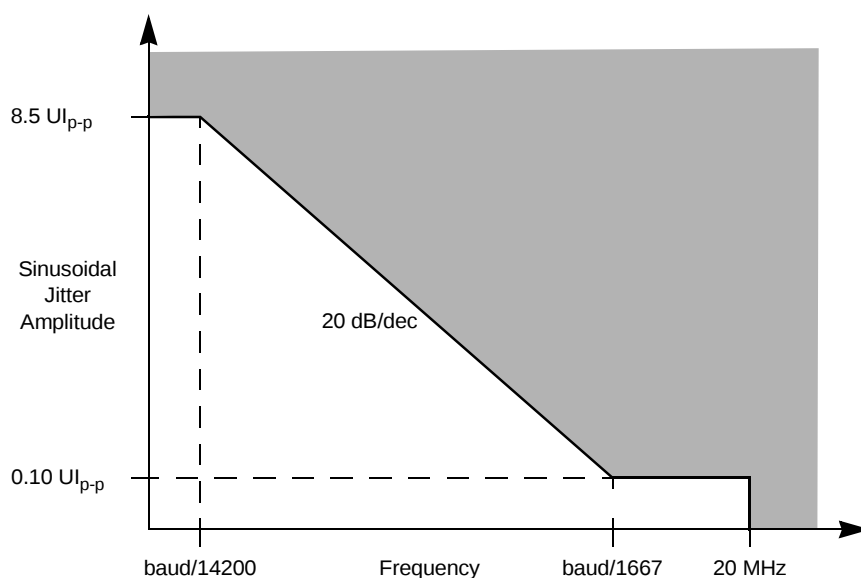


Figure 20. Single Frequency Sinusoidal Jitter Limits for Baud Rate for <3.125 Gbps

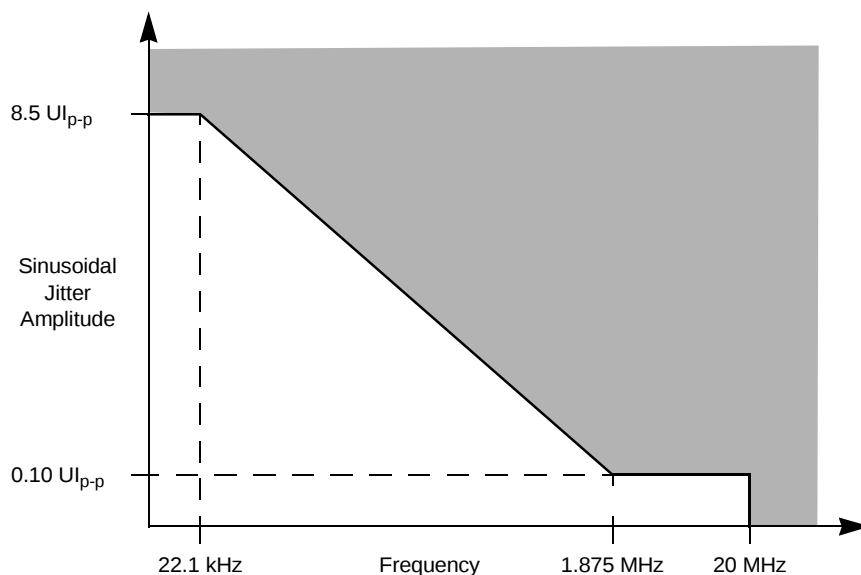


Figure 21. Single Frequency Sinusoidal Jitter Limits for Baud Rate for 3.125 Gbps

### 2.6.3 Timers and Timers\_32b AC Timing Specifications

Table 49 lists the timer input AC timing specifications.

Table 49. Timers Input AC Timing Specifications

| Characteristics                                                                                                                                                                                                                                                                                                                                                                                                                                  | Symbol      | Minimum | Unit | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|---------|------|-------|
| Timers inputs—minimum pulse width                                                                                                                                                                                                                                                                                                                                                                                                                | $T_{TIWID}$ | 8       | ns   | 1, 2  |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately.</li> <li>2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least <math>t_{TIWID}</math> ns to ensure proper operation.</li> </ol> |             |         |      |       |

**Note:** For recommended operating conditions, see Table 4.

Figure 22 shows the AC test load for the timers.

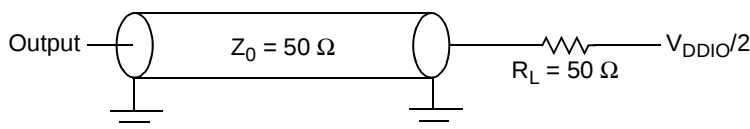


Figure 22. Timer AC Test Load

## 2.6.4 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are three general configuration registers used to configure the timing: GCR4, UCC1\_DELAY\_HR, and UCC3\_DELAY\_HR. These registers configure the programmable delay units (PDU) that should be programmed differently for each Interface to meet timing requirements. For additional information, see the *MSC8157 Reference Manual*.

### 2.6.4.1 Management Interface Timing

Table 50. Ethernet Controller Management Interface Timing

| Characteristics                          | Symbol       | Min | Max | Unit |
|------------------------------------------|--------------|-----|-----|------|
| GE_MDC frequency                         | $f_{MDC}$    | —   | 2.5 | MHz  |
| GE_MDC period                            | $t_{MDC}$    | 400 | —   | ns   |
| GE_MDC clock pulse width high            | $t_{MDC\_H}$ | 160 | —   | ns   |
| GE_MDC clock pulse width low             | $t_{MDC\_L}$ | 160 | —   | ns   |
| GE_MDC to GE_MDIO delay                  | $t_{MDKHDX}$ | 10  | 70  | ns   |
| GE_MDIO to GE_MDC rising edge setup time | $t_{MDDVKH}$ | 20  | —   | ns   |
| GE_MDC rising edge to GE_MDIO hold time  | $t_{MDDXKH}$ | 0   | —   | ns   |

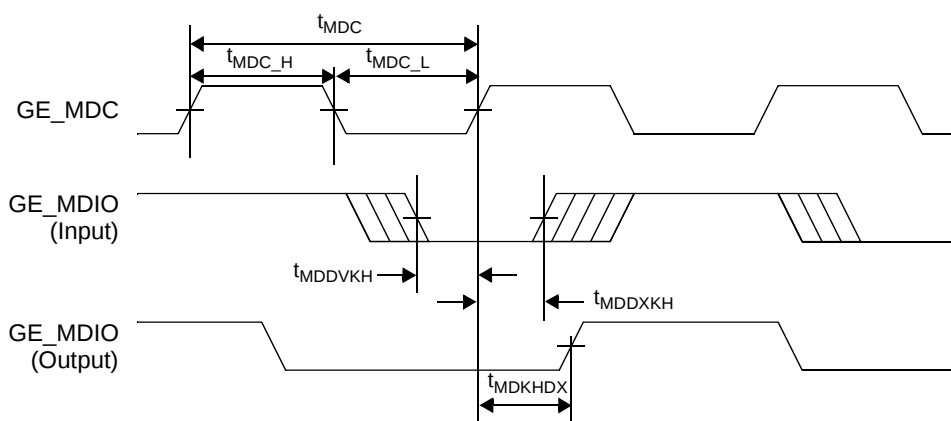


Figure 23. MII Management Interface Timing

### 2.6.4.2 RGMII AC Timing Specifications

Table 51 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

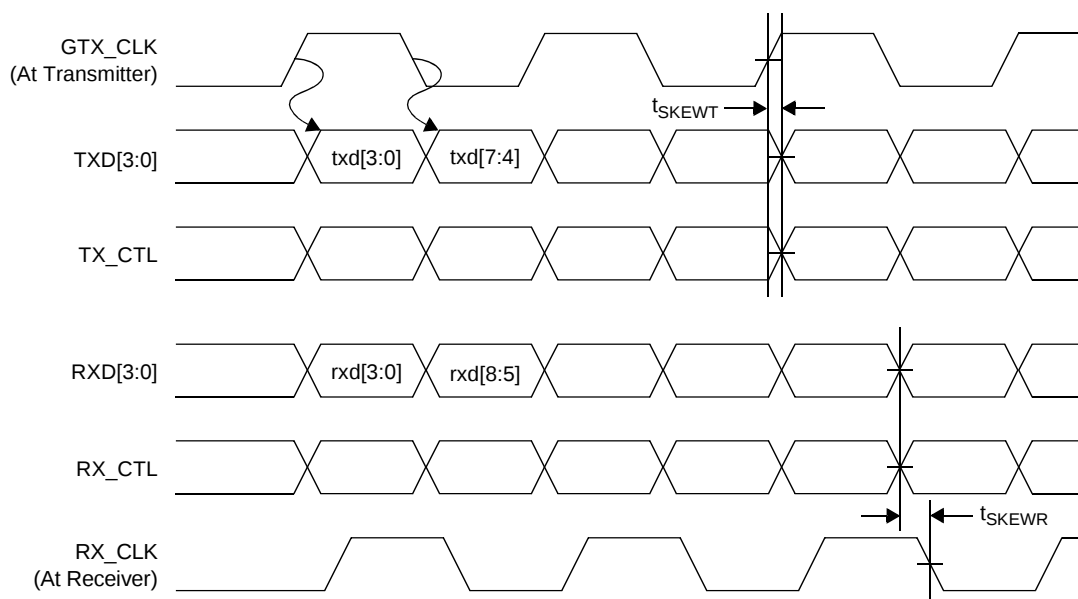
Table 51. RGMII at 1 Gbps with On-Board Delay<sup>2</sup> AC Timing Specifications<sup>1</sup>

| Parameter/Condition                                     | Symbol      | Min  | Typ | Max | Unit |
|---------------------------------------------------------|-------------|------|-----|-----|------|
| Data to clock output skew (at transmitter) <sup>3</sup> | $t_{SKEWT}$ | -0.5 | —   | 0.5 | ns   |
| Data to clock input skew (at receiver) <sup>3</sup>     | $t_{SKEWR}$ | 1    | —   | 2.6 | ns   |

**Table 51. RGMII at 1 Gbps with On-Board Delay<sup>2</sup> AC Timing Specifications<sup>1</sup> (continued)**

| Parameter/Condition                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Symbol | Min | Typ | Max | Unit |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|-----|-----|------|
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. At recommended operating conditions with <math>V_{DDIO}</math> of 2.5 V <math>\pm</math> 5%.</li> <li>2. Program GCR4 as 0x00000000, UCC1_DELAY_HR as 0x00000000, and UCC3_DELAY_HR as 0x00000000.</li> <li>3. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.</li> </ol> |        |     |     |     |      |

Figure 24 shows the RGMII AC timing and multiplexing diagrams.

**Figure 24. RGMII AC Timing and Multiplexing**

## 2.6.5 SPI Timing

Table 52 lists the SPI input and output AC timing specifications.

**Table 52. SPI AC Timing Specifications**

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Symbol <sup>1</sup> | Min | Max | Unit | Note |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-----|-----|------|------|
| SPI outputs valid—Master mode (internal clock) delay                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | $t_{NIKHOV}$        | —   | 6   | ns   | 2    |
| SPI outputs hold—Master mode (internal clock) delay                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | $t_{NIKHOX}$        | 0.5 | —   | ns   | 2    |
| SPI outputs valid—Slave mode (external clock) delay                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | $t_{NEKHOV}$        | —   | 12  | ns   | 2    |
| SPI outputs hold—Slave mode (external clock) delay                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | $t_{NEKHOX}$        | 2   | —   | ns   | 2    |
| SPI inputs—Master mode (internal clock) input setup time                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | $t_{NIIVKH}$        | 12  | —   | ns   | —    |
| SPI inputs—Master mode (internal clock) input hold time                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | $t_{NIIXKH}$        | 0   | —   | ns   | —    |
| SPI inputs—Slave mode (external clock) input setup time                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | $t_{NEIVKH}$        | 4   | —   | ns   | —    |
| SPI inputs—Slave mode (external clock) input hold time                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | $t_{NEIXKH}$        | 2   | —   | ns   | —    |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. The symbols used for timing specifications follow the pattern of <math>t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}</math> (reference)(state) for inputs and <math>t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}</math> for outputs. For example, <math>t_{NIKHOX}</math> symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).</li> <li>2. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.</li> </ol> |                     |     |     |      |      |

Figure 25 provides the AC test load for the SPI.

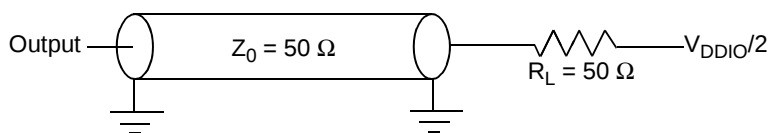
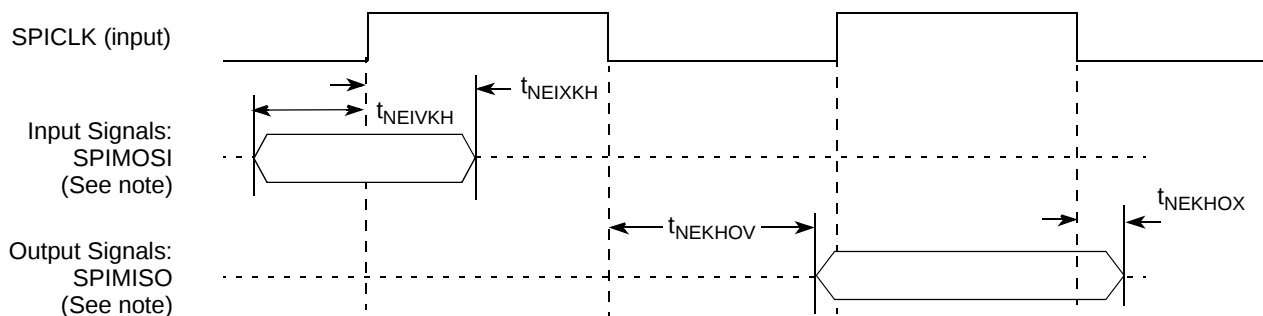


Figure 25. SPI AC Test Load

Figure 26 and Figure 27 represent the AC timings from Table 52. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

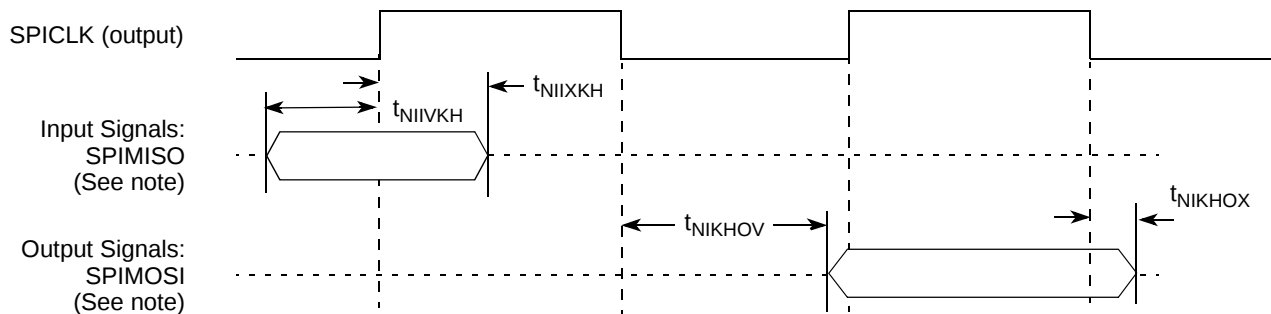
Figure 26 shows the SPI timings in slave mode (external clock).



**Note:** measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 26. SPI AC Timing in Slave Mode (External Clock)

Figure 27 shows the SPI timings in master mode (internal clock).



**Note:** measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 27. SPI AC Timing in Master Mode (Internal Clock)

## 2.6.6 Asynchronous Signal Timing

Table 53 lists the asynchronous signal timing specifications.

**Table 53. Signal Timing**

| Characteristics                                                                                | Symbol    | Type         | Min                    |
|------------------------------------------------------------------------------------------------|-----------|--------------|------------------------|
| Input                                                                                          | $t_{IN}$  | Asynchronous | One CLKIN/MCLKIN cycle |
| Output                                                                                         | $t_{OUT}$ | Asynchronous | Application dependent  |
| <b>Note:</b> Input value relevant for EE0, $\overline{IRQ}[15-0]$ , and $\overline{NMI}$ only. |           |              |                        |

The following interfaces use the specified asynchronous signals:

- *GPIO*. Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

**Note:** When used as a general purpose input (GPI), the input signal should be driven until it is acknowledged by the MSC8157 device, that is, when the expected input value is read from the GPIO data register.

- *EE port*. Signals EE0, EE1.
- *Boot function*. Signal STOP\_BS.
- *I<sup>2</sup>C interface*. Signals I2C\_SCL and I2C\_SDA.
- *Interrupt inputs*. Signals  $\overline{IRQ}[15-0]$  and  $\overline{NMI}$ .
- *Interrupt outputs*. Signals  $\overline{INT\_OUT/CP\_TX\_INT}$  and  $\overline{NMI\_OUT/CP\_RX\_INT}$  (minimum pulse width is 32 ns).

## 2.6.7 JTAG Signals

Table 54. JTAG Timing

| Characteristics                                     | Symbol       | All frequencies |      | Unit |
|-----------------------------------------------------|--------------|-----------------|------|------|
|                                                     |              | Min             | Max  |      |
| TCK cycle time                                      | $t_{TCKX}$   | 36.0            | —    | ns   |
| TCK clock high phase measured at $V_M = V_{DDIO}/2$ | $t_{TCKH}$   | 15.0            | —    | ns   |
| Boundary scan input data setup time                 | $t_{BSVKH}$  | 0.0             | —    | ns   |
| Boundary scan input data hold time                  | $t_{BSXKH}$  | 15.0            | —    | ns   |
| TCK fall to output data valid                       | $t_{TCKHOV}$ | —               | 20.0 | ns   |
| TCK fall to output high impedance                   | $t_{TCKHOZ}$ | —               | 24.0 | ns   |
| TMS, TDI data setup time                            | $t_{TDIVKH}$ | 5.0             | —    | ns   |
| TMS, TDI data hold time                             | $t_{TDIXKH}$ | 5.0             | —    | ns   |
| TCK fall to TDO data valid                          | $t_{TDOHOV}$ | —               | 10.0 | ns   |
| TCK fall to TDO high impedance                      | $t_{TDOHOZ}$ | —               | 12.0 | ns   |
| TRST assert time                                    | $t_{TRST}$   | 100.0           | —    | ns   |

**Note:** All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.

Figure 28 shows the Test Clock Input Timing Diagram

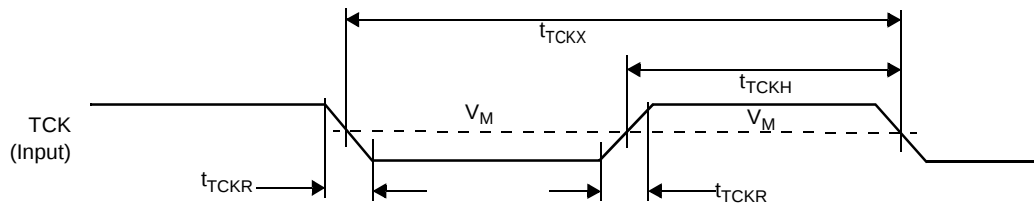


Figure 28. Test Clock Input Timing

Figure 29 shows the boundary scan (JTAG) timing diagram.

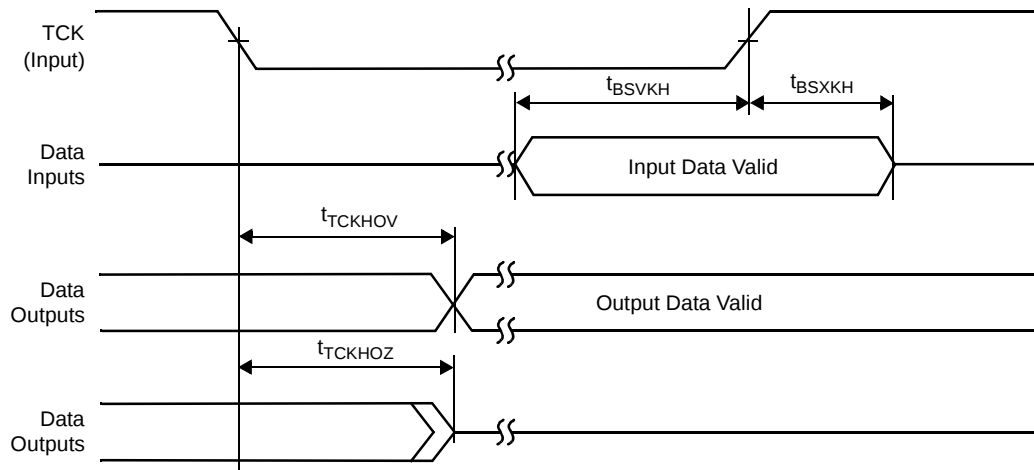


Figure 29. Boundary Scan (JTAG) Timing

Figure 30 shows the test access port timing diagram

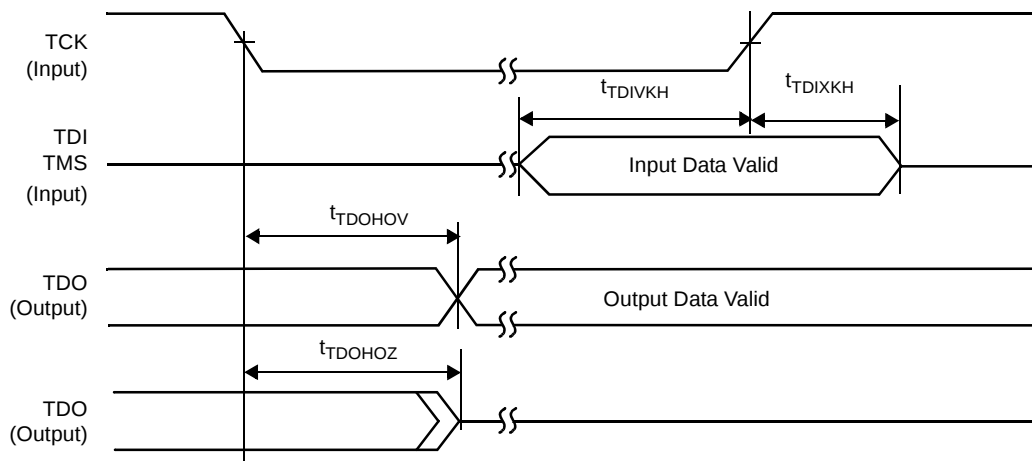


Figure 30. Test Access Port Timing

Figure 31 shows the  $\overline{\text{TRST}}$  timing diagram.



Figure 31.  $\overline{\text{TRST}}$  Timing

## 3 Hardware Design Considerations

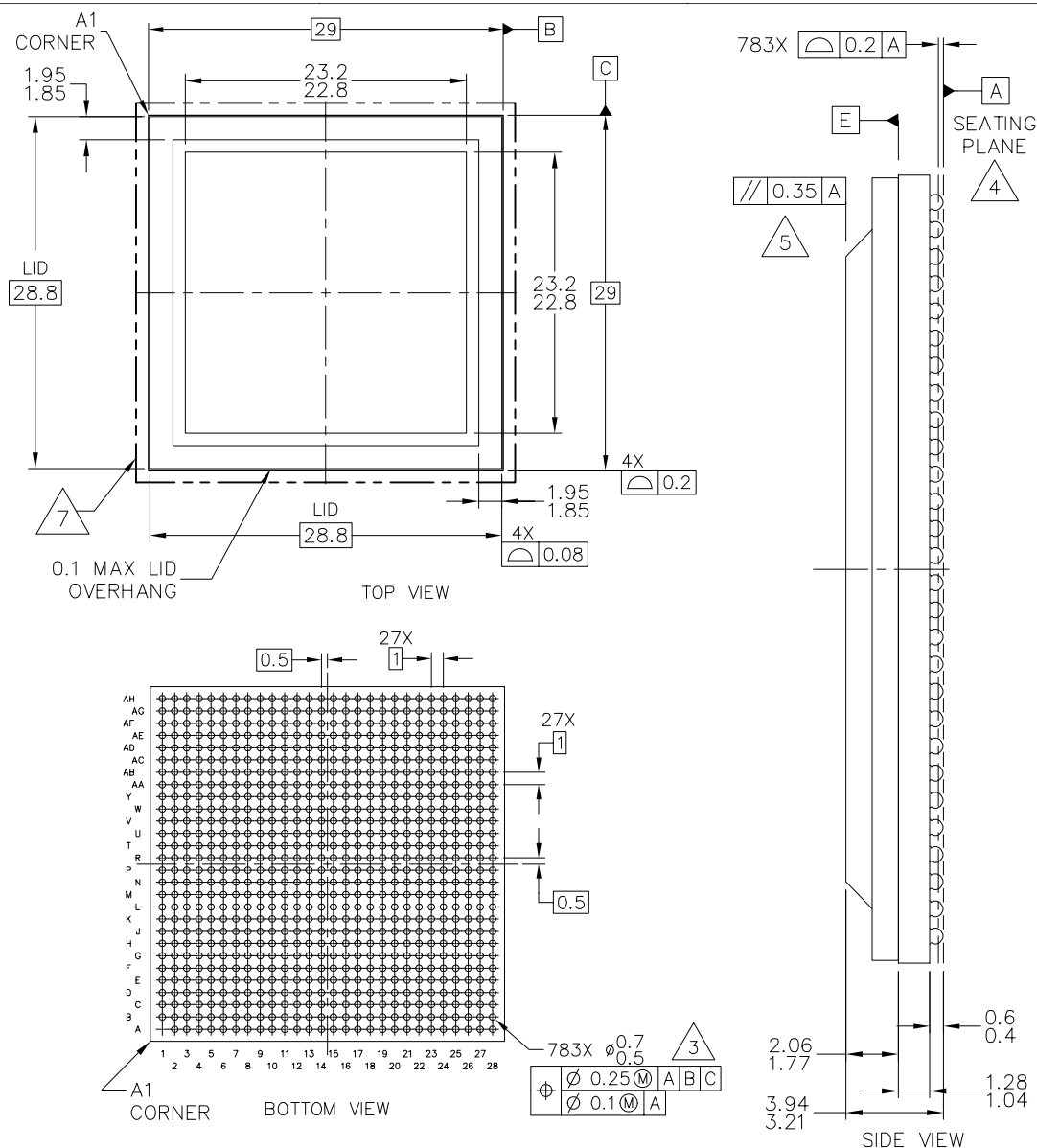
For detailed information about how to design this device into an application, see the *MSC8157 Design Checklist* (AN4110).

## 4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

| Part    | Package Type                                | Spheres   | Core Voltage | Operating Temperature | Core Frequency (MHz) | Power Dissipation | Order Number    |
|---------|---------------------------------------------|-----------|--------------|-----------------------|----------------------|-------------------|-----------------|
| MSC8157 | Flip Chip Plastic Ball Grid Array (FC-PBGA) | Lead-free | 1.0 V        | 0° C to 105°C         | 1000                 | Nominal           | MSC8157SVT1000A |
|         |                                             |           |              | 0° C to 105°C         | 1000                 | Low               | MSC8157LVT1000A |
|         |                                             |           |              | -40° to 105°C         | 1000                 | Nominal           | MSC8157TVT1000A |

## 5 Package Information



### NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURE PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
7. 29.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y.

**Figure 32. MSC8157 Mechanical Information, 783-ball FC-PBGA Package**

## 6 Product Documentation

Following is a general list of supporting documentation:

- *MSC8157 Technical Data Sheet* (MSC8157). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8157 device.
- *MSC8157 Reference Manual* (MSC8157RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8157 device.
- *QUICC Engine Block Reference Manual with Protocol Interworking* (QEIWRM). Provides detailed information regarding the QUICC Engine technology including functional description, registers, and programming information.
- *SC3850 DSP Core Reference Manual*. Covers the SC3850 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8156SC3850 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

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