Ultra Low Power 10/100 Ethernet Transceiver with Auto_MDIX

DESCRIPTION

The AC101L is a single channel, low power, 10/100BASE-TX/FX Transceiver. The AC101L has an integrated voltage regulator to allow operation from a single 3.3V or 2.5V supply source. The device contains a full-duplex 10BASE-T/100BASE-TX/100BASE-FX Fast Ethernet transceiver, which performs all of the physical layer interface functions.

The AC101L is a highly integrated solution combining a encoder/decoder, link monitor, auto-negotiation selection, parallel detection, adaptive equalization, clock/data recovery, base line wander correction, multi mode transmitter, scrambler/descrambler, Far End Fault (FEF), and auto MDI/MDIX circuitry. It is fully compliant with the IEEE802.3 and 802.3u standards.

FEATURES

- 3.3V tolerant and 2.5V capable
- Integrated voltage regulator to allow operation from a single 3.3V or 2.5V supply source
- 10/100 TX/FX
- Full-Duplex or Half-Duplex
- FEFI on 100FX
- 48-pin TQFP
- Industrial Temp (-40°C to +85°C)
- .25 µm CMOS
- Fully compliant with IEEE 802.3 / 802.3u
- MII/RMII Interface
- Baseline Wander Compensation
- Multi-Function LED outputs
- Cable length indicator
- HP auto-MDI/MDIX
- Eight programmable interrupts
- Diagnostic registers

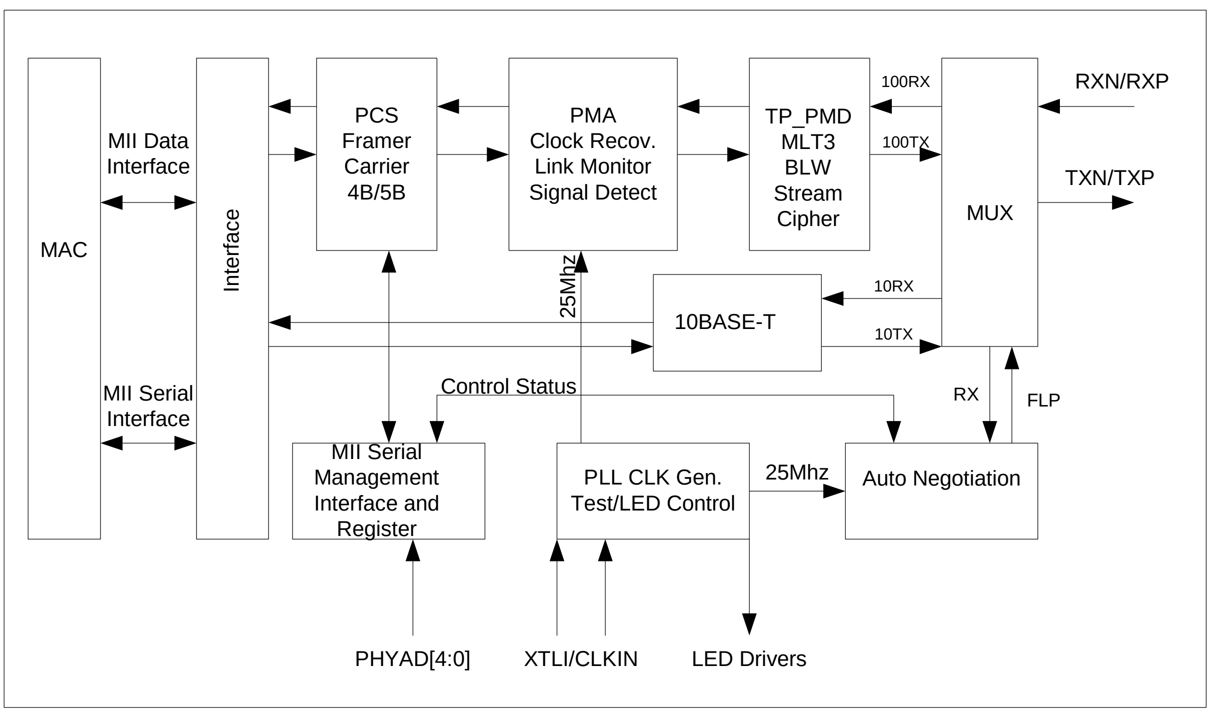

Figure 1: AC101L Functional Block Diagram

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Revision History

Revision #	*Date*	*Change Description*
AC101L-DS00-R	01/02/02	Initial release.
AC101L-DS01-R	02/20/02	Second release. Updated figure 12 and figure 13.

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Section 1: Functional Description

The AC101L is a single-chip, Fast Ethernet transceiver. It performs all of the physical layer interface functions for 100BASE-TX full- or half-duplex on CAT 5 twisted-pair cable, and 10BASE-T full- or half-duplex on CAT 3 cable. It can be configure for 100BASE-FX full- or half-duplex transmission over fiber optic cable when pair with an external fiber optic line driver and receiver.

The chip performs 4B5B, MLT3, NRZI, Encoder/Decoder, Link monitor, auto-negotiation selection, adaptive equalization, clock/data recovery, base line wander correction, multi mode transmitter, scrambler/descrambler, Far End Fault (FEF), and auto-MDI/MDIX. It can be connected to a MAC switch controller through the MII on one side, and connects directly to the media on the other side through a transformer for Twisted Pair (TP) mode, or fiber optic module for FX mode. It is fully compliant with the IEEE 802.3 and 803.3u standards.

Encoder/Decoder

In 100BASE-TX and 100BASE-FX modes, the AC101L transmits and receives data stream on twisted pair or fiber optic cable. When the MII transmit enable is asserted, nibble wide (4 bit) data from transmit data pins is encoded into 5-bit code groups and inserted into transmit data stream. The 4B5B encoding is shown in Section 6: “4B/5B Code-Group” on page 28. The transmit packet is encapsulated by replacing the first 2 nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of packet. When the MII transmit error input is asserted during a packet, the error code group (H) is sent in place of the corresponding data code group. The transmitter sends repeatedly the idle code group between packets.

In 100BASE-TX mode, the encode data stream is scrambled by a stream cipher block and then serialized and encoded into an MLT3 signal level. A multi mode transmit DAC (digital to analog converter) is used to drive the MLT3 data onto twisted pair cable. Following are baseline wander correction, adaptive equalization and clock/data recovery in 100BASE-TX mode, the receive data stream is converted from MLT3 to serial NRZ data. The NRZ data is descrambled by the stream cipher block and then deserialized and aligned into 5-bit code groups.

In 100BASE-FX mode, the scrambling function is bypassed and the data is NRZII encoded. The multi mode transmit DAC drives differential Positive ECL (PECL) levels to an external fiber optic transmitter. Baseline wander correction, adaptive equalization, stream cipher descrambling functions are bypass and NRZI decoding is used instead of MLT3.

The 5-bit code groups are decoded into 4 bit data nibbles. The start of stream delimiter is replaced with preamble nibbles and the end of stream delimiter and idle codes are replaced with all zeros. The decoded data is driven onto the MII receive data pins. When an invalid code group or bad SSD is detected in the data stream, the AC101L asserts the MII RXER signal.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multi mode transmit DAC performs pre-equalization for 100 meters of CAT 3 cable.

Link Monitor

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. The signal levels are qualified using squelch detect circuits. When no signal or certain valid signal is detected on the receive pair for a minimum period of time, the link monitor enter the link pass state and the transmit and receive functions are enabled.

In 100BASE-FX mode, the external fiber-optic receiver performs the signal energy detection function and communicates this information directly to the SD signal (PIN 28).

In 10BASE-T mode, a link pulse detection circuit constantly monitors the RXP/RXN pins for the present of valid link pulses.

CARRIER SENSE (CRS)/RXDV

Carrier sense is asserted asynchronously on the CRS pins as soon as activity is detected on the receive data stream. RXDV is asserted as soon as a valid SSD (Start-of-Stream Delimiter) is detected. Carrier sense and RXDV are de-asserted synchronously upon detection of a valid end of stream delimiter or two consecutive idle code groups in the receive data stream. However, if the carrier sense is asserted and a valid SSD is not detected immediately, RXER is asserted instead of RXDV.

In 10BASE-T mode, CRS is asserted asynchronously when the valid preamble and data activity is detected on the RXIP and RXIN pins.

In the half-duplex mode, the CRS is activated during data transmit. In the full-duplex mode, the CRS is activated during data receiving only.

COLLISION DETECTION

In half-duplex mode, collision detect is asserted on the COL pin whenever carrier sense is asserted and transmission is in progress.

AUTO-NEGOTIATION

Auto-negotiation selection is on 100BASE-Twisted pair PHY only, it is not operating in 100BASE-Fiber PHY.

In 100BASE-TX mode, auto-negotiation can be enabled or disabled by hardware or software control. When auto-negotiation function is enable, the 100BASE-TX PHY automatically chooses its mode of operation by advertising its abilities and comparing them with those received from it’s link partner. 100BASE-TX PHY can be configured to advertise 100BASE-TX full-duplex or 100BASE-TX half-duplex.

The default auto-negotiation mode is configured via reset read value of ANEN/LED3 signal (pin 23) and SPD100/LED1.

0.13	Speed select	The default value is: SPD100
0.12	ANEN Enable	1 = Enable Auto-negotiation. 0 = Disable Auto-negotiation.
0.8	Duplex	The default value is: !ANEN && DUPLEX
4.8/1.14	100BASE-TX Full-Duplex	The default value of this bit is: SPD100 && DUPLEX
4.7/1.13	100BASE-TX	The default value is: SPD100 && (ANEN || !DUPLEX)
4.6/1.12	10BASE-T Full-Duplex	The default value of this bit is: DUPLEX && (ANEN || !SPD100)
4.5/1.11	10BASE-T	The default value is: ANEN || (!SPD100 && !DUPLEX)

PARALLEL DETECTION

Because there are many devices in the field that do not support the ANEN process, but must still be communicated with, it is necessary to detect and link through the Parallel Detection process. The parallel detection circuit is enabled in the absence of FLPs. The circuit is able to detect:

- Normal Link Pulse (NLP)
- 10BASE-T receive data
- 100BASE-TX idle

The mode of operation gets configured based on the technology of the incoming signal. If any of the above is detected, the device automatically configures to match the detected operating speed in the half-duplex mode. This ability allows the device to communicate with the legacy 10BASE-T and 100BASE-TX systems, while maintaining the flexibility of auto-negotiation.

ANALOG ADAPTIVE EQUALIZER

The analog adaptive equalizer removes Inter Symbol Interference (ISI) created by the transmission channel media.

The PHY is designed to accommodate a maximum of 140 meters of UTP CAT 5 cable. An AT&T 1061 CAT 5 cable of this length typically has an attenuation of 31 dB at 100 MHz. A typical attenuation of 100-meter cable is 21 dB. The worst case cable attenuation is around 24-26 dB as defined by TP-PMD specification. The amplitude and phase distortion from the cable causes ISI which makes clock and data recovery difficult. The adaptive equalizer is designed to closely match the inverse transfer function of the twisted-pair cable. The equalizer has the ability to changes its equalizer frequency response according to the cable length. The equalizer will tune itself automatically for any cable, compensating for the amplitude and phase distortion introduced by the cable.

CLOCK RECOVERY

The equalized MLT-3 signal passes through the slicer circuit, and gets converted to NRZI format. The PHY uses a proprietary mixed-signal Phase Locked Loop (PLL) to extract clock information from the incoming NRZI data. The extracted clock is used to re-time the data stream and set the data boundaries. The transmit clock is locked to the 25 MHz clock input while the receive clock is locked to the incoming data streams. When initial lock is achieved, the PLL switches to the data stream, extracts the 125 MHz clock, and uses it for the bit framing for the recovered data. The recovered 125 MHz clock is also used to generate the 25 MHz RX_CLK signal. The PLL requires no external components for its operation and has high noise immunity and low jitter. It provides fast phase alignment and locks to data in one transition. Its data/clock acquisition time, after power-on, is less than 60 transitions. The PLL can maintain lock on run-lengths of up to 60 data bits in the absence of signal transitions. When no valid data is present, (i.e., when the SD is de-asserted) the PLL will switch and lock on to TX_CLK. This provides a continuously running RX_CLK. At the PCS interface, the 5-bit data RXD[4:0] is synchronized to the 25 MHz RX_CLK.

BASELINE WANDER CORRECTION

A 100BASE-TX data stream is not always DC balanced because the receive signal must pass through a transformer, the DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The 100BASE-TX PHY automatically compensates for baseline wander by removing the DC offset from the input signal, and thereby significantly reduces the chance of a receive symbol error.

The baseline wander circuit is not required in 100BASE-FX PHY.

Multi Mode Transmitter

The multi-mode transmitter transmits MLT3 coded symbols in 100BASE-TX mode, and NRZI coded symbols in 100BASE-FX mode. It utilizes a current drive output, which is well balanced and produces very low noise transmit signals. PECL voltage levels are produced with resistive terminations in 100BASE-FX mode.

The serialized data bypasses the scrambler and 4B/5B encoder in FX mode. The output data is NRZI PECL signals. The PECL level signals are used to drive the Fiber-transmitter.

Stream Cipher Scrambler/Descrambler

In 100BASE-TX mode, the transmit data stream is scramble to reduce radiated emissions on the twisted pair cable. The data is scrambled by exclusive ORing the NRZ signal with the output of an 11-bit wide Linear Feedback Shift Register (LFSR), which produces a 2047 bit non repeating sequence. The scrambler reduces peak emission by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detect the state of transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle code group.

The receiver does not attempt to decode the data stream unless the de-scrambler is locked. When locked, the descrambler is continuously monitor the data stream to make sure that it has not lost synchronization.

The receive data stream is expected to contain inter-packet idle periods. If the descrambler does not detect enough idle code within 724 µs, it becomes unlocked and the receive decoder is disable. The descrambler is always forced into the unlock state when a link failure condition is detected.

Stream cipher descrambler is not used in the 100BASE-FX mode.

FEF (Far End Fault)

Auto-negotiation provides the mechanism to inform the link partner that a remote fault has occurred. However, auto-negotiation is disabled in the 100BASE-FX applications. An alternative in-band signaling function (FEFI) is used to signal a remote fault condition.

FEFI is a stream of 84 consecutive ones followed by one logic zero. This pattern is repeated three times.

A FEFI will signal under three conditions:

- When no activity is received from the link partner,
- When the clock recovery circuit detects a signal error or PLL lock error,
- When management entity sets the transmit Far-End-Fault bit.

The FEFI mechanism is enabled by default in the 100BASE-FX mode, and is disabled in 100BASE-TX or 10BASE-T modes. The register setting can be changed by software after reset.

TRANSMIT DRIVER

In 100BASE-TX mode, the PHY transmit function converts synchronous 4-bit data nibbles from the MII to a pair of 125 Mbps differential serial data streams. The serial data is transmitted over network twisted-pair cables via an isolation transformer. Data conversion includes 4B/5B encoding, scrambling, parallel to serial, NRZ to NRZI, and MLT-3 encoding. The entire operation is synchronous to 25 MHz and 125 MHz clock. Both clocks are generated by an on-chip PLL clock synthesizer that is locked on to an external 25 MHz clock source.

In 100BASE-FX, the transmit driver does not perform filtering, it utilizes a current drive output that is well balanced and produces a low noise PECL signal. PECL voltage levels are produced with resistive terminations.

In 10BASE-T mode, if the MII interface is used, Parallel to Serial logic is used to convert the 4-bit data into the serial stream through the output wave shaping driver. The wave shaper reduces any EMI emission by filtering out the harmonics, therefore eliminating the need for an external filter.

HP-AUTO MDI/MDIX

This feature will be able to detect the required cable connection type straight through or crossed over and make correction automatically.

MAC INTERFACE

MII

The Media Independent Interface (MII) is an 18-wire MAC/PHY interface described in 802.3u. The purpose of the interface is to allow MAC layer devices to attach to a variety of physical layer devices through a common interface. MII operates at either 100 Mbps or 10 Mbps, dependent on the speed of the physical layer. With clocks running at either 25 MHz or 2.5 MHz, 4-bit data is clocked between the MAC and PHY, synchronously with Enable and Error signals.

At the time of PLL lock on an incoming signal from the wire interface, the PHY will generate RX_CLK at either 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

On receipt of valid data from the wire interface, RXDV goes active signaling the MAC that valid data will be presented on the RXD[3:0] pins at the speed of the RX_CLK.

On transmission of data from the MAC, TXEN is presented to the PHY indicating the presence of valid data on TXD[3:0]. TXD[3:0] are sampled by the PHY synchronous to TX_CLK during the time that TXEN is valid.

RMII

The Reduced Media Independent Interface (RMII) is used to connect the PHY with the MAC. The PHY and MAC obtain their clock from a common 50 MHz source, such as a clock oscillator. This clock is shared by all ports within the PHY for transmitting and receiving data on two individual 2-bit data buses. CRS and RXDV are muxed together to indicate to the MAC when there is valid data on the receive bus. In 100M mode RXD[1:0] is sampled on every cycle of REFCLK. In 10M mode RXD[1:0] is sampled on every 10^{th} cycle of REFCLK. RXER is generated by the PHY to indicate a receive error to the MAC. TXEN is generated by the MAC to indicate to the PHY when there is valid data on the transmit bus. In 100M mode the PHY will read 2 bits from TXD[1:0] for each cycle of REFCLK. In 10M mode the PHY will read 2 bits of data from TXD[1:0] every 10^{th} cycle of REFCLK.

SMI

The PHYs internal registers are accessible only through the MII 2-wire Serial Management Interface (SMI). MDC is a clock input to the PHY, which is used to latch in or out data and instructions for the PHY. The clock can run at any speed from DC to 25 MHz. MDIO is a bidirectional connection used to write instructions to, write data to, or read data from the PHY. Each data bit is latched either in or out on the rising edge of MDC. MDC is not required to maintain any speed or duty cycle, provided no half cycle is less than 20 ns, and that data is presented synchronous to MDC.

MDC/MDIO are a common signal pair to all PHYs on a design. Therefore, each PHY needs to have its own unique physical address. The physical address of the PHY is set using the pins defined as PHYAD[4:0]. These input signals are strapped externally and sampled as reset is negated. At idle, the PHY is responsible to pull MDIO line to a high state. Therefore, a 1.5K Ohms resistor is required to connect MDIO line to VCC.

PHYSICAL LAYER INTERFACES

Twisted Pair (TP) interface with Auto-MDI/MDIX selection, or Fiber Interface with PECL signaling are the two supported interfaces.

The selection of these two interfaces is performed at reset time by the SD/FXEN signal (pin 28). Pull pin 28 LOW to enable the TP interface, or connect pin 28 to the Fiber module to enable FX interface.

Section 2: Pin Descriptions

Many of the pin have multiple functions. The multi-function pins will be designated by bolding of the pin number. The separate descriptions of these pins will be listed in the proper sections. Designers must assure that they have identified all modes of operation prior to final design.

Signal Types:

- B = Bidirection pin
- P = Power pin
- G = Ground pin
- AI = Analog Input pin
- AO = Analog Output pin
- D = Digital Pull Down pin
- U = Digital Pull Up pin
- # = Active low

All Digital pins are Bidirectional pins.

Table 1: Pinout and Signal Definitions

PIN #	*PIN Name*	*Type*	*Description*
1	VCC	P	+2.5V Power supply.
2	GND	G	Ground
2	GND	G	Ground
3	RXDV/CRSDV	B_D	RXDV (active HIGH output): Receive data valid is output signal in MII mode. RXDV actives HIGH to indicate that the receive frame is in progress, and that data stream present on the RXD output pins is valid. CRSDV (active HIGH output): Carrier Sense/Data Valid is output signal in RMII mode. The CRSDV pin is asserted high when media is non idle.
4	RMII_mode/ RX_CLK	B_D	RMII_mode (Reset read input): pull HIGH to configure the chip into RMII mode. Default is in MII mode. RX_CLK (Out put): Receive clock in MII mode. RX_CLK is 25 MHz out put in 100BASE and 2.5 MHz output in 10BASE. This clock is recovered from the incoming data on the cable inputs.
5	ISOLATE/RXER	B_D	ISOLATE (Reset Read Input): Pull HIGH to isolate the PHY from MII. The MII output pins are high impedance. The MII input pins still respond to data. This allows multiple PHY to be attached to the same MII interface. RXER (active HIGH output): asserted to indicate that invalid symbol or bad SSD is detected in both RMII and MII mode.
6	GND	G	Ground
7	VCC	P	+2.5V Power supply.
8	TXER	B_D	TXER (active HIGH input): Transmit error in MII interface. When TXER is asserted for one or more TX_CLK periods while TXEN is also asserted, the PHY shall emit one or more symbols that are not part of the valid data or delimiter set somewhere in the frame being transmitted. The relative position of the error within the frame need not be preserved.
9	TX_CLK	B_D	TX_CLK (Output): Transmit clock signal of MII mode. TX_CLK is 25MHz output in 100BASE and 2.5MHz in 10BASE. This clock is a continuously driven output, generated from XI (Crystal input) pin.

Table 1: Pinout and Signal Definitions (Cont.)

PIN #	PIN Name	Type	Description
10	TXEN	B_D	TXEN (active HIGH input): Transmit Enable signal in RMII and MII interface. TXEN is asserted by the MAC to indicate that valid data is present on TXD[3:0].
11	TXD0	B_D	TXD0: transmit data input for MII and RMII interface.
12	TXD1	B_D	TXD1: transmit data input for MII and RMII interface.
13	TXD2	B_D	TXD2: transmit data input for MII interface.
14	TXD3	B_D	TXD3: transmit data input for MII interface.
15	COL	B_D	COL (active HIGH output): is Collision detects signal in MII interface. In half-duplex mode, COL active high output to indicate that a collision has occurred. In full-duplex mode, COL remains low.
16	REPEATER/ CRS	B_D	REPEATER (Reset Read Input): Active High to put the chip in Repeater mode. CRS (active HIGH output): Carrier sense signal in the MII interface. CRS is asserted when twisted pair media is non idle and de-asserted when idle or a valid end of stream delimiter is detected.
17	GND	G	Ground
18	VCC	P	+2.5V Power supply.
19	PHYAD0/INTR	B_U	PHYAD0 (Reset Read Input): Pull High or Low to set the PHY Address bit 0 for MII/RMII management function. INTR (Output): interrupt output enable. The active value will be the invert of its reset read value.
20	BURNIN#/ LED0	B_U	BURNIN# (Reset Read Input): Active LOW to put the chip in Burn-in Test mode. LED0 (Output): Low active, the default behavior is ON when the chip is in link-up condition, BLINK when the chip detects transmits or receive activity.
21	SPD100/LED1	B_U	SPD100 (Reset Read Input): If ANEN is Low, SPD100 will set the TP port speed in Reg. 0 If ANEN is High, SPD100 will be used to set 100Mb Half, and 100Mb Full bits in Register 4. LED1 (Output): Low active, the default behavior is ON when the chip is at 100Mbps, OFF when the chip is at 10 Mbps.
22	DUPLEX/LED2	B_U	DUPLEX (Reset Read Input): If ANEN is Low, DUPLEX will set the TP port in Full Duplex mode in Reg. 0 If ANEN is High, DUPLEX will be used to set 10Mb FDX, and 100Mb FDX bits in Register 4. LED2 (Output): Low active, the default behavior is ON when the chip is at Full duplex, OFF when the chip is at half-duplex.
23	ANEN/LED3	B_U	ANEN (Reset Read Input): Auto-negotiation Enable for Twisted Pair Port. Pull high to enable Auto-negotiation. Pull low to disable Auto-negotiation. LED3 (Output): Low active, the default behavior is BLINK when the chip detect collision in half-duplex.
24	PDOWN#	B_U	PDOWN# (input): Power down input. Pull low will put both TP and Fiber port into power down mode. This is a regular input. NOT a reset read signal.
25	VCC	P	+2.5V Power supply.
26	RXN	A	Receive – for TP port in MDI mode. Transmit – for TP port in MDIX mode.

Table 1: Pinout and Signal Definitions (Cont.)

PIN #	PIN Name	Type	Description
27	RXP	A	Receive + for TP port in MDI mode. Transmit + for TP port in MDIX mode.
28	SD/FXEN	AI	SD/FXEN (Analog input): Pull LOW to enable TP mode. Connect to fiber module to Enable FX mode, also served as Signal Detect input.
29	GND	G	Ground
30	GND	G	Ground
31	RBIAD	A	Bias resister connection. Connect to a 10K 1% resister to GND.
32	VCCPLL	P	+2.5V supply for Analog Bias, PLL modules.
33	GND	G	Ground
34	TXN	A	Transmit – in MDI mode. Receive – in MDIX mode.
35	TXP	A	Transmit + in MDI mode. Receive + in MDIX mode.
36	VCC25OUT	P	+2.5 VCC out from the on chip regulator.
37	GND	G	Ground
38	GND	G	Ground
39	XO	A	XTAL output.
40	XI	A	XTAL input. In RMII mode it is defined as CLK_REF=50 MHz clock input. In MII Mode: XI and XO is designed to connect to a 25 MHz., 50 PPM XTAL or 25MHz OSC.
41	VCC33IN	P	3.3 V Power supply input.
42	RST#	I_U	Reset input. Low active.
43	MDIO	B_U	MDIO (Input/ Output): Management Data I/O. This serial input/output pin is used to read from and write to MII register. The data value on the MDIO pin is valid and latched on the rising edge of MDC. This pin requires a 1K Ohm resistor pull-up.
44	MDC	I_D	MDC (Input): Management Data Clock. The MDC clock input must be provided to allow MII management function. This pin has SCHMTT trigger input.
45	PHYAD1/ RXD3	B_D	PHYAD1 (Reset Read Input): Pull High or Low to set the PHY Address bit 1 for MII/RMII management function. RXD3: Receive data output signal in MII interface.
46	PHYAD2/ RXD2	B_D	PHYAD2 (Reset Read Input): Pull High or Low to set the PHY Address bit 2 for MII/RMII management function. RXD2: Receive data output signal in MII interface.
47	PHYAD3/ RXD1	B_D	PHYAD3 (Reset Read Input): Pull High or Low to set the PHY Address bit 3 for MII/RMII management function. RXD1: Receive data output signal in MII/RMII interface.
48	PHYAD4/ RXD0	B_D	PHYAD4 (Reset Read Input): Pull High or Low to set the PHY Address bit 4 for MII/RMII management function. RXD0: Receive data output signal in MII/RMII interface.

Section 3: Pin Diagram

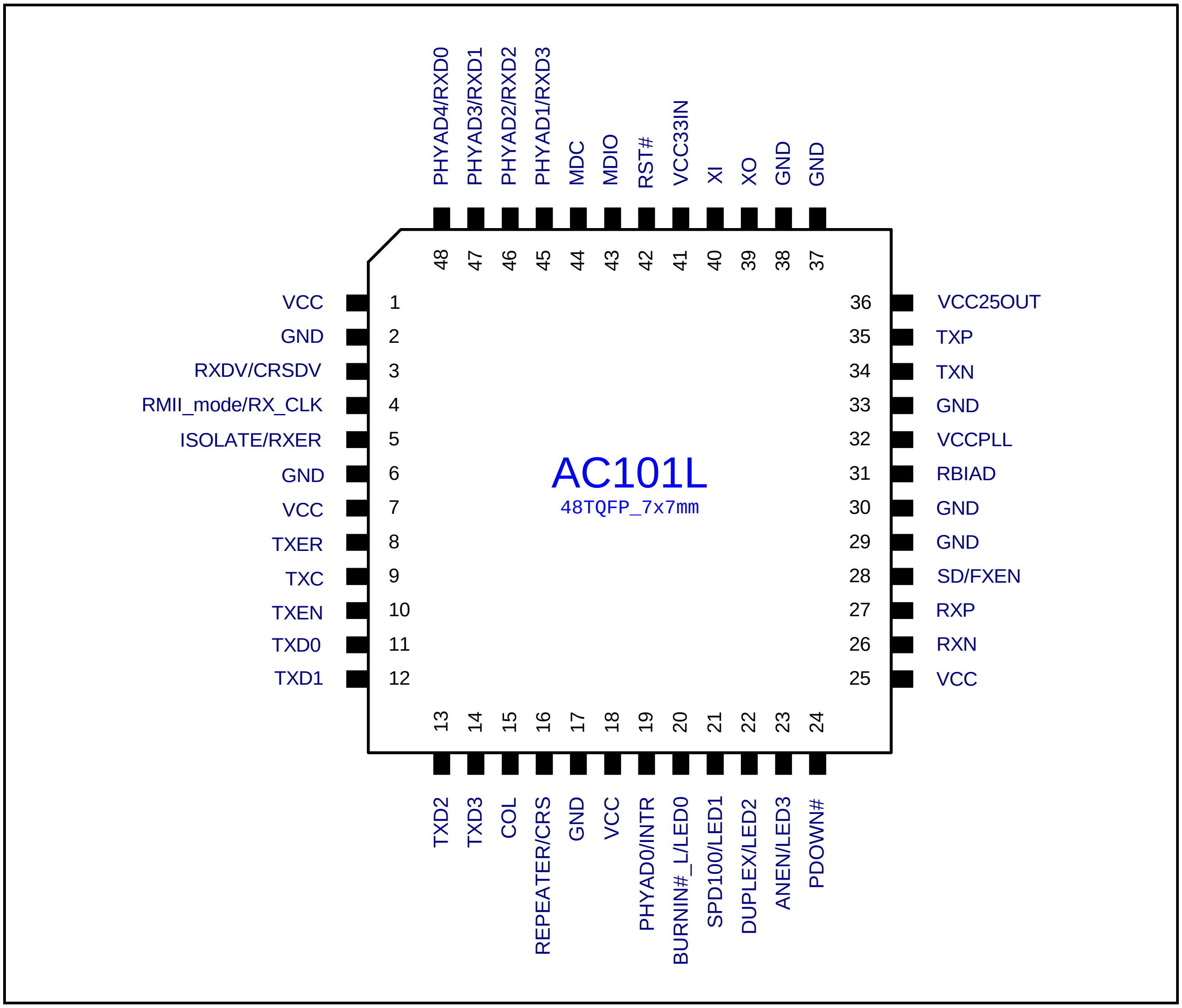


Figure 2: AC101L Pinout Diagram

Section 4: Operational Description

RESET

The PHY can be reset in three ways:

- During initial power on.
- Hardware Reset: (See “Pin Descriptions” on page 7).
- Software Reset: (See “Register Description” on page 14).

POWER SOURCE

The chip provide on board 3.3V +/- 5% input to 2.5V +/- 5% output regulator, with the capability to drive 150 mA current. The 2.5V will supply the PHY operation, include the LEDs. It is recommended to limit the LED current below 10 mA per LED.

The 2.5V power shall be decoupled to provide the digital, and analog pins on the chip.

POWER SAVING MODE

The power consumption of the device is significantly reduced due to its built-in power management features. Separate power supply lines are used to power the 10BASE-T circuitry and the 100BASE-TX circuitry. Therefore, the two circuits can be turned-on and turned-off independently. When the PHY is set to operate in 100BASE-TX mode, the 10BASE-T circuitry is powered down.

The following power management features are supported:

- **Power Down Mode**: (See pin and register descriptions). During power down mode, the device is still able to interface through the management interface.
- **Energy Detect/Power Saving Mode**: Energy detect mode turns off the power to select internal circuitry when there is no live network connected. Energy Detect (ED) circuit is always turned on to monitor if there is a signal energy present on the media. The management circuitry is also powered on and ready to respond to any management transaction. The transmit circuit still send out link pulses with minimum power consumption. If a valid signal is received from the media, the device will power up and resume normal transmit/receive operation.
- **Valid Data Detection Mode**: This can be achieved by writing to the Receive Clock Register Control Bit. During this mode, if there is no data other than idles coming in, the receive clock (RX_CLK) will turn off. This could save the power of the attached media access controller. RX_CLK will resume operation one clock period prior to the assertion of RXDV. The receive clock will again shut off 64 clock cycles after RXDV gets deasserted.

CLOCK SOURCE

The clock source for this chip is from XI pin.

In MII mode, it can connect to a 25 MHz 50 ppm OSC or a 25 MHz 50 ppm Xtal (crystal).

When operate in RMII mode, this pin shall be connected to 50 MHz, 50 ppm clock reference. The internal circuit will determine the operation mode upon reset read of RX_CLK/RMII_SEL signal, and decide weather to divide done this clock to provide 25 MHz internal clock reference.

Isolate Mode

When AC101L is put into isolate mode, all MII inputs (TXD[3:0}, TXEN, TXER) are ignore, and all MII outputs (TX_CLK, COL, CRS, RX_CLK, RXDV, RXER, RXD[3:0] are set to high impedance. Only the MII management pins (MDC, MDIO) operate normally. Pull HIGH pin 4 at reset or write 1 to bit 10 register 0 to put the chip into isolate mode.

Loop Back Mode

Local loop back is provided for testing purpose. It can be enabled by writing a one to Reg. 0 bit 14.

The local loop back routes transmitted data through the transmit path back to the receiving path's clock and data recovery module. The loop back data are presented to the PCS in 5 bits symbol format. This loop back is used to check the operation of the 5-bit symbol decoder and the phase locked loop circuitry. In local loop back, the SD output is forced to logic one and TXOP/N outputs are tristated.

Interrupt Mode

The INTR pin on the PHY will be asserted whenever one of eight selectable interrupt events occur. Assertion state is high or low programmable through the INTR_LEVL register bit. The selection is made by setting the appropriate bit in the upper half of the Interrupt Control/Status register. When the INTR bit goes active, the MAC interface is required to read the Interrupt Control/Status register to determine which event caused the interrupt. The Status bits are read only and clear on read. When INTR is not asserted, the pin is held in a high impedance state.

LED Operation

LED Interface

The LED interface is fully configurable through register setting. The connection of LED (source/sink current) depends on the default setting.

The default LED mode is:

LED0	LED1	LED2	LED3
Link/Act	Speed	Duplex	COL

LED Configuration Section

However, the LEDs are fully configurable to other operation modes. Each LED has two 16-bit registers to define its operation. See “Common Registers” on page 24 and Table 2: “LED [3:0] Event Table,” on page 13 to configure the LEDs to work with other operation mode other than default mode:

LED [3:0] Event Table

LED [3:0] are configurable. The following events are defined for AC101L operation:

Table 2: LED [3:0] Event Table

LED [3:0]	*Bit#*	*Description*
	7	Duplex
	6	Collision
	5	Speed 100
	4	Speed 10
	3	Transmit Activity
	2	Transmit/Receive Activity
	1	Receive Activity
	0	Link

Section 5: Register Description

The first seven registers of the MII register set are defined by the MII specification. In addition to these required registers are several Altima Communications Inc. specific registers. There are reserved registers and/or bits that are for Altima internal use only. The following standard registers are supported. (**Register numbers are in Decimal format, the values are in Hex format**):

Note **When writing to registers it is recommended that a read/modify/write operation be performed, as unintended bits may get set to unwanted states. This applies to all registers, including those with reserved bits.**

Legend:

- RW = Read and Write Access
- SC = Self Clearing
- LL = Latch Low Until cleared by Reading
- RO = Read Only
- RC = Cleared on Read
- LH = Latch High Until Cleared by Reading

TP PHY Register Summary

Table 3: TP PHY Register Summary

Register	*Description*	*Default*
Registers 0-7		
0	Control Register	3000
1	Status Register	7849
2	PHY Identifier 1 Register	0022
3	PHY Identifier 2 Register	5521
4	Auto-Negotiation Advertisement Register	01E1
5	Auto-Negotiation Link Partner Ability Register	0001
6	Auto-Negotiation Expansion Register	0004
7	Next Page Advertisement Register	2001
Registers 8-31		
8-15	Reserved	XXXX
16	BT and Interrupt Level Control Register	03C0
17	Interrupt Control/Status Register	0000
18,19	Reserved	XXXX
20	Cable measurement capability Register	XXXX
21	Receive Error Counter Register	0304
22-31	Reserved	XXXX

REGISTER 0: CONTROL REGISTER

Table 4: Register 0: Control Register

Reg.bit	Name	Description	Mode	Default
0.15	Reset	1 = PHY reset. This bit is self-clearing.	RW/SC	0
0.14	Loop back	1 = Enable loop back mode. This will loop back TXD to RXD and ignore all the activity on the cable media. 0 = Normal operation.	RW	0
0.13	Speed Select	1 = 100 Mbps 0 = 10 Mbps The default value is: SPD100	RW	Set by SPD100
0.12	ANEN Enable	1 = Enable Auto-Negotiate process (overrides 0.13 and 0.8) 0 = Disable Auto-Negotiate process. Mode selection is controlled via bit 0.8, 0.13 The default value is: ANEN	RW	Set by ANEN
0.11	Power Down	1 = Power down. All blocks except for SMI will be turned off. Setting PDOWN# pin (24) to LOW will achieve the same result. 0 = Normal operation.	RW	0
0.10	Isolate	1 = Electrically isolate the PHY from MII. PHY is still able to response to SMI. 0 = Normal operation.	RW	0
0.9	Restart ANEN	1 = Restart Auto-Negotiation process. 0 = Normal operation.	RW/SC	0
0.8	Duplex Mode	1 = Full duplex. 0 = Half duplex. The default value is: !ANEN && DUPLEX	RW	See Description
0.7	Collision Test	1 = Enable collision test, which issues the COL signal in response to the assertion of TXEN signal. Collision test is disabled if PCSBP pin is high. Collision test is enabled regardless of the duplex mode. 0 = Disable COL test.	RW	0
0.[6:0]	Reserved		RW	0000000

Register 1: Status Register

Table 5: Register 1: Status Register

Reg.bit	*Name*	*Description*	*Mode*	*Default*
1.15	100BASE-T4	Permanently tied to zero indicates no 100BASE-T4 capability.	RO	0
1.14	100BASE-TX Full-Duplex	1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable. The default value is: SPD100 && DUPLEX	RO	See Description
1.13	100BASE-TX Half-Duplex	1 = 100BASE-TX half-duplex capable. 0 = Not TX half-duplex capable. The default value is: SPD100 && (ANEN || !DUPLEX).	RO	See Description
1.12	10BASE-T Full-Duplex	1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable. The default value is: DUPLEX && (ANEN || !SPD100)	RO	See Description
1.11	10BASE-T Half-Duplex	1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable. The default value is: ANEN || (!SPD100 && !DUPLEX)	RO	See Description
1.[10:7]	Reserved		RO	0000
1.6	MF Preamble Suppression	The PHY is able to perform management transaction without MDIO preamble. The management interface needs minimum of 32 bits of preamble after reset.	RO	1
1.5	ANEN Complete	1 = Auto-Negotiate process completed. Reg. 4, 5, 6 are valid after this bit is set. 0 = Auto-negotiate process not completed.	RO	0
1.4	Remote Fault	1 = Remote fault condition detected. 0 = No remote fault. This bit will remain set until it is cleared by reading register 1.	RO/LH	0
1.3	ANEN Ability	1 = Able to perform Auto-Negotiation function, default value determined by ANEN pin. 0 = Unable to perform Auto-Negotiation function.	RO	Set by ANEN
1.2	Link Status	1 = Link is established. If link fails, this bit will be cleared and remain at 0 until register is read again. 0 = Link has gone down.	RO/LL	0
1.1	Jabber Detect	1 = Jabber condition detect. 0 = No Jabber condition detected.	RO/LH	0
1.0	Extended Capability	1 = Extended register capable. This bit is tied permanently to one.	RO	1

REGISTER 2: PHY IDENTIFIER 1 REGISTER

Table 6: Register 2: PHY Identifier 1 Register

Reg.bit	*Name*	*Description*	*Mode*	*Default*
2.[15:0]	OUI*	Composed of the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0022(H)

* = Based on an OUI is 0010A9 (Hex)

REGISTER 3: PHY IDENTIFIER 2 REGISTER

Table 7: Register 3: PHY Identifier 2 Register

Reg.bit	*Name*	*Description*	*Mode*	*Default*
3.[15:10]	OUI	Assigned to the 19th through 24th bits of the OUI.	RO	010101
3.[9:4]	Model Number	Six bit manufacturer’s model number.	RO	010010
3.[3:0]	Revision Number	Four-bit manufacturer’s revision number.	RO	0001

* = Based on an OUI of 0010A9 (Hex)

Register 4: Auto-Negotiation Advertisement Register

Table 8: Register 4: Auto-Negotiation Advertisement Register

Reg.bit	Name	Description	Mode	Default
4.15	Next Page	1 = Next Page enabled. 0 = Next Page disabled.	RW	0
4.14	Acknowledge	This bit will be set internally after receiving 3 consecutive and consistent FLP bursts.	RO	0
4.[13:11]	Reserved			
4.10	FDFC	Full-Duplex Flow Control. 1 = Advertise that the DTE(MAC) has implemented both the optional MAC control sub layer and the pause function as specified in clause 31 and annex 31B of 802.3u. 0 = MAC does not support flow control.		
4.9	100BASE-T4	Technology not supported. This bit always 0.	RO	0
4.8	100BASE-TX Full-Duplex	1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable. The default value is: SPD100 && DUPLEX	RW	See Description
4.7	100BASE-TX	1 = 100BASE-TX half-duplex capable. 0 = Not TX half-duplex capable. The default value is: SPD100 && (ANEN || !DUPLEX)	RW	See Description
4.6	10BASE-T Full Duplex	1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable. The default value is: DUPLEX && (ANEN || !SPD100)	RW	See Description
4.5	10BASE-T	1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable. The default value is: ANEN || (!SPD100 && !DUPLEX)	RW	See Description
4.[4:0]	Selector Field	Protocol Selection [00001] = IEEE 802.3.	RO	00001

Register 5: Auto-Negotiation Link Partner Ability Register/Link Partner Next Page Message

Table 9: Register 5: Auto-Negotiation Link Partner Ability Register/Link Partner Next Page Message

Reg.bit	*Name*	*Description*	*Mode*	*Default*
5.15	Next Page	1 = Link partner desires Next Page transfer. 0 = Link partner does not desire Next Page transfer.	RO	0
5.14	Acknowledge	1 = Link Partner acknowledges reception of FLP words. 0 = Not acknowledged by Link Partner.	RO	0
5.[13:10]	Reserved			
5.9	100BASE-T4	1 = 100BASE-T4 supported by Link Partner. 0 = 100BASE-T4 not supported by Link Partner.	RO	0
5.8	100BASE-TX Full Duplex	1 = 100BASE-TX full-duplex supported by Link Partner. 0 = 100BASE-TX full-duplex not supported by Link Partner.	RO	0
5.7	100BASE-TX	1 = 100BASE-TX half-duplex supported by Link Partner. 0 = 100BASE-TX half-duplex not supported by Link Partner.	RO	0
5.6	10BASE-T Full Duplex	1 = 10 Mbps full-duplex supported by Link Partner. 0 = 10 Mbps full-duplex not supported by Link Partner.	RO	0
5.5	10BASE-T	1 = 10 Mbps half-duplex supported by Link Partner. 0 = 10 Mbps half-duplex not supported by Link Partner.	RO	0
5.[4:0]	Selector Field	Protocol Selection [00001] = IEEE 802.3.	RO	00001

*When this register is used as Next Page Message, the bit definition is the same as Register 7.

Register 6: Auto-Negotiation Expansion Register

Table 10: Register 6: Auto-Negotiation Expansion Register

Reg.bit	*Name*	*Description*	*Mode*	*Default*
6.[15:5]	Reserved		RO	0
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection logic, this fault is due to more than one technology detecting concurrent link up condition. This bit can only be cleared by reading Register 6, using the management interface. 0 = No fault detected by parallel detection logic.	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner supports next page function. 0 = Link partner does not support next page function.	RO	0
6.2	Next Page Able	Next page is supported.	RO	1
6.1	Page Received	This bit is set when a new link code word has been received into the Auto-Negotiation Link Partner Ability Register. This bit is cleared upon a read of this register.	RC	0
6.0	Link Partner ANEN-Able	1 = Link partner is Auto-Negotiation capable. 0 = Link partner is not Auto-Negotiation capable.	RO	0

REGISTER 7: AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER

Table 11: Register 7: Auto-Negotiation Next Page Transmit Register

Reg.bit	*Name*	*Description*	*Mode*	*Default*
7.15	NP	1 = Another Next Page desired. 0 = No other Next Page Transfer desired.	RW	0
7.14	Reserved		RO	0
7.13	MP	1 = Message page. 0 = Unformatted page.	RW	1
7.12	ACK2	1 = Will comply with message. 0 = Can not comply with message.	RW	0
7.11	TOG_TX	1 = Previous value of transmitted link code word equals to 0. 0 = Previous value of transmitted link code word equals to 1.	RW	0
17.[10:0]	CODE	Message/Unformatted Code Field.	RW	001

REGISTER 16: BT AND INTERRUPT LEVEL CONTROL REGISTER

Table 12: Register 16: BT and Interrupt Level Control Register

Reg.bit	*Name*	*Description*	*Mode*	*Default*
16.15	Repeater	1 = Repeater mode, full- duplex will be inactive, and CRS only responses to receive activity. SQE test function is disabled.	RW	Set by Repeater
16.14	INTR_LEVL	1 = INTR pin will be active high. 0 = INTR pin will be active low.	RW	0
16.13	TXJAM	1 = Force CIM to send JAM pattern. 0 = Normal operation.	RW	0
16.12	CIM Disable	1 = Disable Carrier Integrity Monitor. 0 = Enable Carrier Integrity Monitor.	RW	1
16.11	SQE Test Inhibit	1 = Disable 10BASE-T SQE testing. 0 = Enable 10BASE-T SQE testing, which will generate a COL pulse following the completion of a packet transmission.	RW	0
16.[10:6]	Reserved		RO	0
16.5	Auto Polarity Disable	1 = Disable Auto Polarity detection/correction. 0 = Enable Auto Polarity detection/correction.	RW	0
16.4	Reverse Polarity	1 = Reverse Polarity when Reg. 16.5 = 0. 0 = Normal Polarity when Reg. 16.5 = 0. If Reg. 16.5 is set to 1, writing a one to this bit will reverse the polarity of the transmitter.	RW	0
16.[3:0]	Reserved		RO	0

REGISTER 17: INTERRUPT CONTROL/STATUS REGISTER

Table 13: Register 17: Interrupt Control/Status Register

Reg.bit	Name	Description	Mode	Default
17.15	Jabber_IE	Jabber Interrupt Enable.	RW	0
17.14	RXER_IE	Receive Error Interrupt Enable.	RW	0
17.13	Page_Rx_IE	Page Received Interrupt Enable.	RW	0
17.12	PD_Fault_IE	Parallel Detection Fault Interrupt Enable.	RW	0
17.11	LP_Ack_IE	Link Partner Acknowledge Interrupt Enable.	RW	0
17.10	Link_Status_ Change_IE	Link Status Change Interrupt Enable.	RW	0
17.9	R_Fault_IE	Remote Fault Interrupt Enable.	RW	0
17.8	ANEN_Comp_IE	Auto-Negotiation Complete Interrupt Enable.	RW	0
17.7	Jabber_Int	This bit is set when a jabber event is detected.	RC	0
17.6	RXER_Int	This bit is set when RXER transitions high.	RC	0
17.5	Page_Rx_Int	This bit is set when a new page is received during ANEN.	RC	0
17.4	PD_Fault_Int	This bit is set when parallel detect fault is detected.	RC	0
17.3	LP_Ack_Int	This bit is set when the FLP with acknowledge bit set is received.	RC	0
17.2	Link_Not_OK Int	This bit is set when link status switches from OK status to Non-OK status (Fail or Ready).	RC	0
17.1	R_Fault_Int	This bit is set when remote fault is detected.	RC	0
17.0	ANEN _Comp Int	This bit is set when ANEN is complete.	RC	0

REGISTER 18: DIAGNOSTIC REGISTER

Table 14: Register 18: Diagnostic Register

Reg. bit	Name	Description	Mode	Default
18.[15]	Reserved	Reserved	RW	0
18.[14]	Reserved	Reserved	RW	0
18.[13]	Force link pass 10BT	1 = Enable Force link pass 10BT. 0 = Disable Force link pass 10BT.	RW	0
18.[12]	Force link pass 100TX	1 = Force link pass 100TX. 0 = Disable Force link pass 100TX.	RW	0
18.11	Reserved	Reserved	RO	0
18.10	Reserved	Reserved	RO	0
18.9	Reserved	Reserved	RO	0
18.8	Reserved	Reserved	RO/RC	0
18.[7:0]	Reserved	Reserved	RO	0

Register 19: Power/Loopback Register

Table 15: Register 19: Power/Loopback Register

Reg. bit	Name	Description	Mode	Default
19.[14:7]	Reserved	Reserved	RW	00
19.6	Reserved	Reserved	RW	0
19.5	Disable watch dog timer for decipher	1 = Disable watch dog timer. 0 = Enable advanced power saving mode.	RW	0
19.4	Low Power Mode disable	0 = Enable advanced power saving mode. 1 = Disable advanced power saving mode.	RW	0
19.3	Reserved	Reserved	RW	0
19. 2	Reserved	Reserved	RW	0
19.1	NLP Link Integrity Test	1 = In Auto-Negotiation test mode, send NLP instead of FLP in order to test NLP receive integrity. 0 = Sending FLP in Auto-Negotiation test mode.	RW	0
19.0	Jabber disable	1 = Disable jabber.	RW	0

Register 20: Cable Measurement Capability Register

Table 16: Register 20: Cable Measurement Capability Register

Reg.bit	Name	Description	Mode	Default
20.15	Reserved	Reserved	RW	1
20.14	Reserved	1 = On; 0 = Off	RW	1
20.[13:9]	Reserved	Reserved	RO	0
[a]20.8	Adaptation disable	1 = Disable Adaptation. 0 = Enable Adaptation.	RW	0
20.[7:4]	Cable measurement capability	These bits can be used as cable length indicator. The bits are incremented from 0000 to 1111, with an increment of approximately 10 meters. The equivalent is 0 to 32 dB with an increment of 2 dB @ 100 MHz. The value is a read back from the equalizer, and the measured value is not absolute.	RW	X
20.[3:0]	Reserved	Reserved	RO	X

a. If you want to set the value of 20.[7:4], you must turn on 20.8 and turn off 20.14. Or this PHY will reject to receive packets.

Register 21: Receive Error Counter

Table 17: Register 21: Receive Error Counter

Reg.bit	Name	Description	Mode	Default
21.[15:0]	RXER Counter	Count Receive Error Events.	RO	0

REGISTER 22: POWER MANAGEMENT REGISTER

Table 18: Register 22: Power Management Register

Reg.bit	*Name*	*Description*	*Mode*	*Default*
22.[15:14]	Reserved		RO	00
22.13	PD_PLL	1 = Power down PLL circuit.	RO	X
22.12	PD_EQUAL	1 = Power down equalizer circuit.	RO	X
22.11	PD_BT_RCVR	1 = Power down 10BASE-T receiver.	RO	X
22.10	PD_LP	1 = Power down link pulse receiver.	RO	X
22.9	PD_EN_DET	1 = Power down energy detect circuit.	RO	X
22.8	PD_FX	1 = Power down FX circuit.	RO	X
22.[7:6]	Reserved		RW	00
22.5	MSK_PLL	0 = Force power up PLL circuit.	RW	X
22.4	MSK_EQUAL	0 = Force power up equalizer circuit.	RW	X
22.3	MSK_BT_RCVR	0 = Force power up 10BASE-T receiver.	RW	X
22.2	MSK_LP	0 = Force power up link pulse receiver.	RW	X
22.1	MSK_EN_DET	0 = Force power up energy detect circuit.	RW	X
22.0	MSK_FX	0 = Force power up FX circuit.	RW	X

REGISTER 23: OPERATION MODE REGISTER

Table 19: Register 23: Operation Mode Register

Reg.bit	*Name*	*Description*	*Mode*	*Default*
23.[15:14]	Reserved			
23.13	Clk_rclk_save	1 = Set rclk save mode. Rclk will be shut off after 64 cycles of each packet.		0
23.12	Reserved			
23.11	Scramble disable	1 = Disable scrambler. 0 = Enable scrambler.	RW	0
23.10	Reserved		RW	0
23.9	Pcsbp	1 = Enable PCS bypass mode. 0 = Disable PCS.	RW	0
23:8	Reserved		RW	0
23.[7:6]	Reserved			
23.5	Reserved		RO	0
23.[4:0]	Reserved		RO	XXXXX

Register 24: CRC for Recent Received Packet

Table 20: Register 24: CRC for Recent Received Packet

Reg.bit	Name	Description	Mode	Default
24.[15:0]	CRC16	CRC16 value displayed. For system level test purpose.	RC	0000H

Common Registers

The following registers are mapped to Reg28-31 on the TP PHY. Reg28.[15:12] is used as page select. There are multiple pages of Reg29-31, depends of the value of Reg. 28[15:12]

Common Register 0 (Map to Reg. 28) Mode Control Register

Table 21: Common Register 0 (Map to Reg. 28) Mode Control Register

Reg. Bit	Name	Description	Mode	Default
a.28.[15:12]	Page Selection	Select Multiple Common Register Pages.	RW	0000
a.28.[11:7]	Reserved	Reserved	RO	0000
a.28.6	MII_enable	1 = Enable MII Interface.	RO	0
a.28.5	Reserved	Reserved	RO	0
a.28.4	RMII_enable	1 = Put the chip in Reduce MII mode.	RO	1
a.28.3	Reserved	Reserved		
a.28.2	Act select	Act Event Select. 0 = Receive activity. 1 = TX or RX activity.	RW	1
a.28.1	Reserved		RO	0
a.28.0	Reserved		RW	0

Common Register 1: (Map to Reg. 29, Page 0 a28.[15:12]=0000) Test Mode Register

Table 22: Common Register 1: (Map to Reg. 29, Page 0 a28.[15:12]=0000) Test Mode Register

Reg.bit	Name	Description	Mode	Default
A0.29.15	Reduce_mcount	Reduce millisecond counter to 256 micro second.	RO	0
A0.29.[14:10]	Reserved		RO	00100
A0.29.[9:8]	Reserved		RW	00
A0.29.[7:4]	Test Mode	0000 = Normal operation.	RW	0000
A0.29.3	Burn In	1 = Enable burn in test mode. 0 = Normal operation.	RW	0
A0.29.2	Output Disable	1 = Disable all digital output. 0 = Normal operation.	RW	0
A0.29.1	Reserved	0 = Normal operation.	RW	0
A0.29.0	Reduce Timer	1 = Reduce timer for auto-neg testing. 0 = Normal operation.	RW	0

Common Register 4: (Map to Reg. 29, Page 1 a28.[15:12]=0001) LED Blink Rate

Table 23: Common Register 4: (Map to Reg. 29, Page 1 a28.[15:12]=0001) LED Blink Rate

Reg.bit	Name	Description	Mode	Default
A1.29.[15:8]	Reserved		RO	00000000
A1.29.[7:0]	Blink Rate	Set LED blink rate. The blink rate is this number * 16 ms. Default is 256 ms.	RW	00010000

Common Register 5: (Map to Reg. 30, Page 1 a.28.[15:12]=0001) LED0 Setting1 Register

Default operation for LED0 is ON when Link; BLINK when Activity.

Table 24: Common Register 5: (Map to Reg. 30, Page 1 a.28.[15:12]=0001) LED0 Setting1 Register

Reg.bit	Name	Description	Mode	Default
A1.30.[15:13]	Reserved		RW	0000
A1.30.12	Force LED On	Force LED0 on.	RW	0
A1.30.[11:9]	Reserved		RW	000
A1.30.8	Force LED Off	Force LED0 off.	RW	0
A1.30.[7:0]	Msk Blink	Blink Mask. When the bits are set to one, corresponding event will cause the led to blink.	RW	00000100

Common Register 6: (Map to Reg. 31, Page 1 a.28.[15:12]=0001) LED0 Setting2 Register

Table 25: Common Register 6: (Map to Reg. 31, Page 1 a.28.[15:12]=0001) LED0 Setting2 Register

Reg.bit	Name	Description	Mode	Default
A1.31. [15:8]	Msk On	On Mask. When the bits are set to one, corresponding event will cause the led to turn on.	RW	00000001
A1.31. [7:0]	Msk Off	Off Mask. When the bits are set to one, corresponding event will cause the led to turn off.	RW	00000000

Common Register 7: (Map to Reg. 29, Page 2 a.28.[15:12]=0010) LED1 Setting1 Register

Table 26: Common Register 7: (Map to Reg. 29, Page 2 a.28.[15:12]=0010) LED1 Setting1 Register

Reg.bit	Name	Description	Mode	Default
A2.29.[15:13]	Reserved		RO	000
A2.29.12	Force LED On	Force LED1 on.	RW	0
A2.29.[11:9]	Reserved		RO	000
A2.29.8	Force LED Off	Force LED1 off.	RW	0
A2.29.[7:0]	Msk Blink	Blink Mask. When the bits are set to one, corresponding event will cause the led to blink.	RW	00000000

Common Register 8: (Map to Reg. 30, Page 2 a.28.[15:12]=0010) LED1 Setting2 Register

Default Operation for LED1 is ON when 100 Mbps.

Table 27: Common Register 8: (Map to Reg. 30, Page 2 a.28.[15:12]=0010) LED1 Setting2 Register

Reg.bit	Name	Description	Mode	Default
A2.30.[15:8]	Msk On	On Mask. When the bits are set to one, corresponding event will cause the led to turn on.	RW	00100000
A2.30.[7:0]	Msk Off	Off Mask. When the bits are set to one, corresponding event will cause the led to turn off.	RW	00000000

Common Register 9: (Map to Reg. 31, Page 2 a.28.[15:12]=0010) LED2 Setting1 Register

Table 28: Common Register 9: (Map to Reg. 31, Page 2 a.28.[15:12]=0010) LED2 Setting1 Register

Reg.bit	Name	Description	Mode	Default
A2.31.[15:13]	Reserved		RO	000
A2.31.12	Force LED On	Force LED2 On.	RW	0

Table 28: Common Register 9: (Map to Reg. 31, Page 2 a.28.[15:12]=0010) LED2 Setting1 Register (Cont.)

Reg.bit	Name	Description	Mode	Default
A2.31.[11:9]	Reserved		RO	000
A2.31.8	Force LED Off	Force LED2 Off.	RW	0
A2.31.[7:0]	Msk Blink	Blink Mask. When the bits are set to one, corresponding event will cause the led to blink.	RW	00000000

Common Register 10: (Map to Reg. 29, Page 3 a.28.[15:12]=0011) LED2 Setting2 Register

Default Operation for LED2 is ON when Duplex.

Table 29: Common Register 10: (Map to Reg. 29, Page 3 a.28.[15:12]=0011) LED2 Setting2 Register

Reg.bit	Name	Description	Mode	Default
A3.29.[15:8]	Msk On	On Mask. When the bits are set to one, corresponding event will cause the led to turn on.	RW	10000000
A3.29.[7:0]	Msk Off	Off Mask. When the bits are set to one, corresponding event will cause the led to turn off.	RW	00000000

Common Register 11: (Map to Reg. 30, Page 3 a.28[.15:12]=0011) LED3 Setting1 Register

Default Operation for LED3 is BLINK when COL.

Table 30: Common Register 11: (Map to Reg. 30, Page 3 a.28[.15:12]=0011) LED3 Setting1 Register

Reg.bit	Name	Description	Mode	Default
A3.30.[15:13]	Reserved		RO	000
A3.30.12	Force LED On	Force LED3 On.	RW	0
A3.30.[11:9]	Reserved		RO	000
A3.30.8	Force LED Off	Force LED3 Off.	RW	0
A3.30.[7:0]	Msk Blink	Blink Mask. When the bits are set to one, corresponding event will cause the led to blink.	RW	0100000

Common Register 12: (Map to Reg. 31, Page 3 a.28.[15:12]=0011) LED3 Setting2 Register

Table 31: Common Register 12: (Map to Reg. 31, Page 3 a.28.[15:12]=0011) LED3 Setting2 Register

Reg.bit	Name	Description	Mode	Default
A3.31.[15:8]	Msk On	On Mask. When the bits are set to one, corresponding event will cause the led to turn on.	RW	00000000
A3.31.[7:0]	Msk Off	Off Mask. When the bits are set to one, corresponding event will cause the led to turn off.	RW	00000000

Section 6: 4B/5B Code-Group

Table 32: 4B/5B Code-Group Table

Symbol Name	*4B CODE*	*5B CODE*	*Description*
0	0000	11110	Data 0
1	0001	01001	Data 1
2	0010	10100	Data 2
3	0011	10101	Data 3
4	0100	01010	Data 4
5	0101	01011	Data 5
6	0110	01110	Data 6
7	0111	01111	Data 7
8	1000	10010	Data 8
9	1001	10011	Data 9
A	1010	10110	Data A
B	1011	10111	Data B
C	1100	11010	Data C
D	1101	11011	Data D
E	1110	11100	Data E
F	1111	11101	Data F
Idle and Control Codes			
I	0000	11111	Idle
J	0101	11000	Start of stream delimiter, part 1 of 2; always use in pair with K symbol.
K	0101	10001	Start of stream delimiter, part 2 of 2; always use in pair with J symbol.
T	Undefined	01101	End of stream delimiter, part 1 of 2; always use in pair with R symbol.
R	Undefined	00111	End of stream delimiter, part 2 of 2; always use in pair with T symbol.
Invalid Code			
H	Undefined	00100	Transmit Error; used to send HALT code-group
V	Undefined	00000	Invalid code
V	Undefined	00001	Invalid code
V	Undefined	00010	Invalid code
V	Undefined	00011	Invalid code
V	Undefined	00101	Invalid code
V	Undefined	00110	Invalid code
V	Undefined	01000	Invalid code
V	Undefined	01100	Invalid code
V	Undefined	10000	Invalid code
V	Undefined	11001	Invalid code

Section 7: SMI Read/Write Sequence

Table 33: SMI Read/Write Sequence

SMI Read/Write Sequence								
	Pream (32 bits)	Start (2 bits)	OpCode (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	TurnAround (2 bits)	Data (16 bits)	Idle
Read	1…1	01	10	AAAAA	RRRRR	Z0	D…D	Z
Write	1…1	01	01	AAAAA	RRRRR	10	D…D	Z

Section 8: Timing and AC Characteristics

CLOCK TIMING

Table 34: Clock Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Units*
XTAL input Cycle Time	CK_CYCLE	-	40	-	ns
XTAL input High/Low Time	CK_HI CK_LO	-	20	-	ns
XTAL input Rise/Fall Time	CK_EDGE	-	-	4	ns
REF_CLK Cycle Time (RMII)	-	-	20	-	ns
REF_CLK High/Low Time (RMII)	-	-	10	13	ns
REF_CLK Rise/Fall Time (RMII)	-	-	-	2	ns

RESET TIMING

Table 35: Reset Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Units*
Reset Pulse Length Low Period with stable XTAL input	RESET_LEN	1	-	-	µs
Activity after end of Hardware Reset	RESET_WAIT	1	-	-	µs
Reset Rise / Fall Time	RESET_WAIT	-	5	10	ns

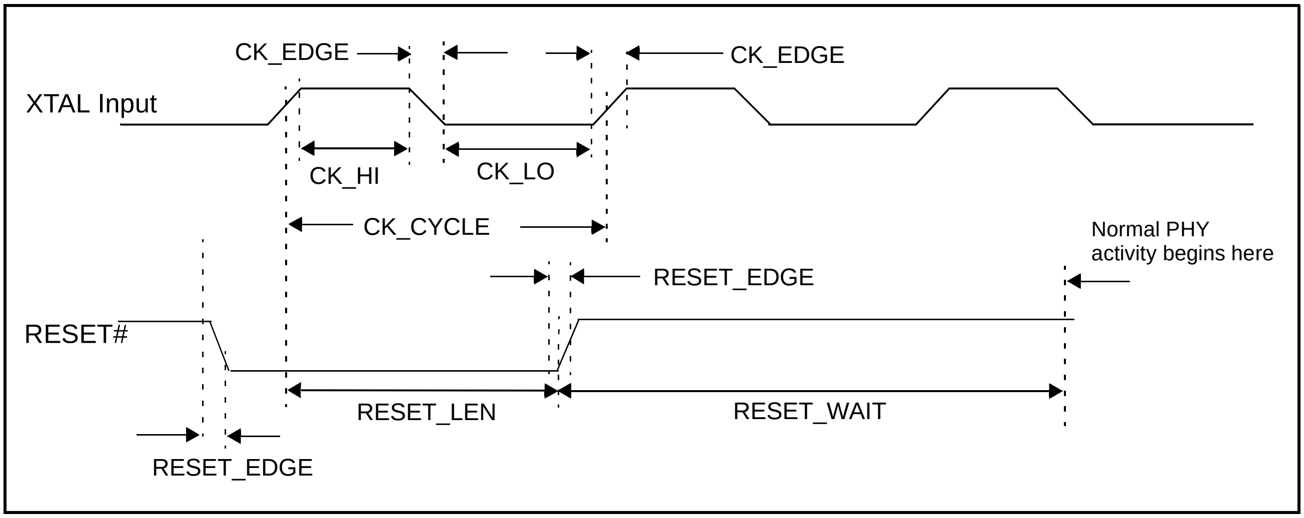


Figure 3: Reset Timing

Management Data Interface Timing

Table 36: Management Interface Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Units*
MDC Cycle Time	MDC_CYCLE	40	-	-	ns
MDC High/Low	-	20	-	-	ns
MDC Rise/Fall Time	MDC_RISE MDC_FALL	-	-	10	ns
MDIO input Setup Time to MDC rising	MDIO_SETUP	10	-	-	ns
MDIO input Hold Time from MDC rising	MDIO_HOLD	10	-	-	ns
MDIO output Delay from MDC rising	MDIO_DELAY	0	-	30	ns

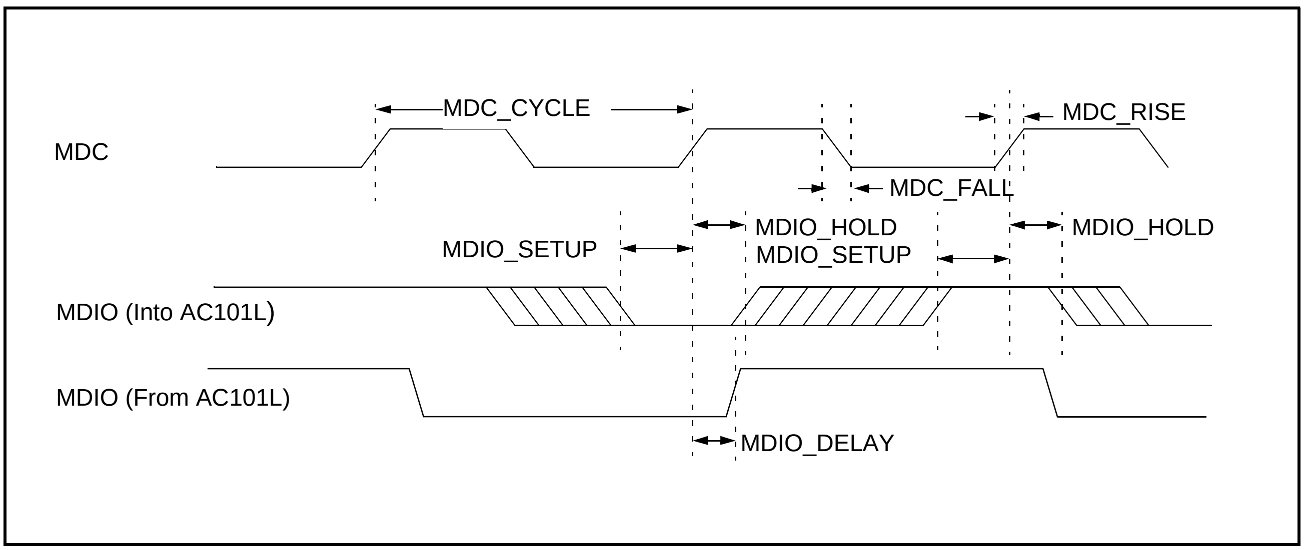


Figure 4: Management Interface Timing

100BASE-TX/FX MII TRANSMIT SYSTEM TIMING

Table 37: 100BASE-X MII Transmit System Timing

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
TX_CLK period	tCK	-	39.998	40.000	40.002	ns
TX_CLK High period	tCKH	-	18.000	20.000	22.000	ns
TX_CLK Low period	tCKL	-	18.000	20.000	22.000	ns
TXEN to /J/	tTJ	-	-	40	180	ns
TXEN sampled to CRS	tCSA	RPTR is logic low	-	40	180	ns
TXEN sampled to COL	tCLA	RPTR is logic low	-	40	180	ns
!TXEN to /T/	tTT	-	-	40	180	ns
!TXEN sampled to !CRS	tCSD	RPTR is logic low	-	40	180	ns
!TXEN sampled to !COL	tCLD	RPTR is logic low	-	40	180	ns
TX Propagation Delay	tTJ	From TXD[3:0] to TXOP/N(FXTP/N)	-	40	180	ns
TXD[3:0], TXEN, TXER Setup	tTXS	From rising edge of TX_CLK	10	-	-	ns
TXD[3:0], TXEN, TXER Hold	tTXH	From rising edge of TX_CLK	0	-	-	ns

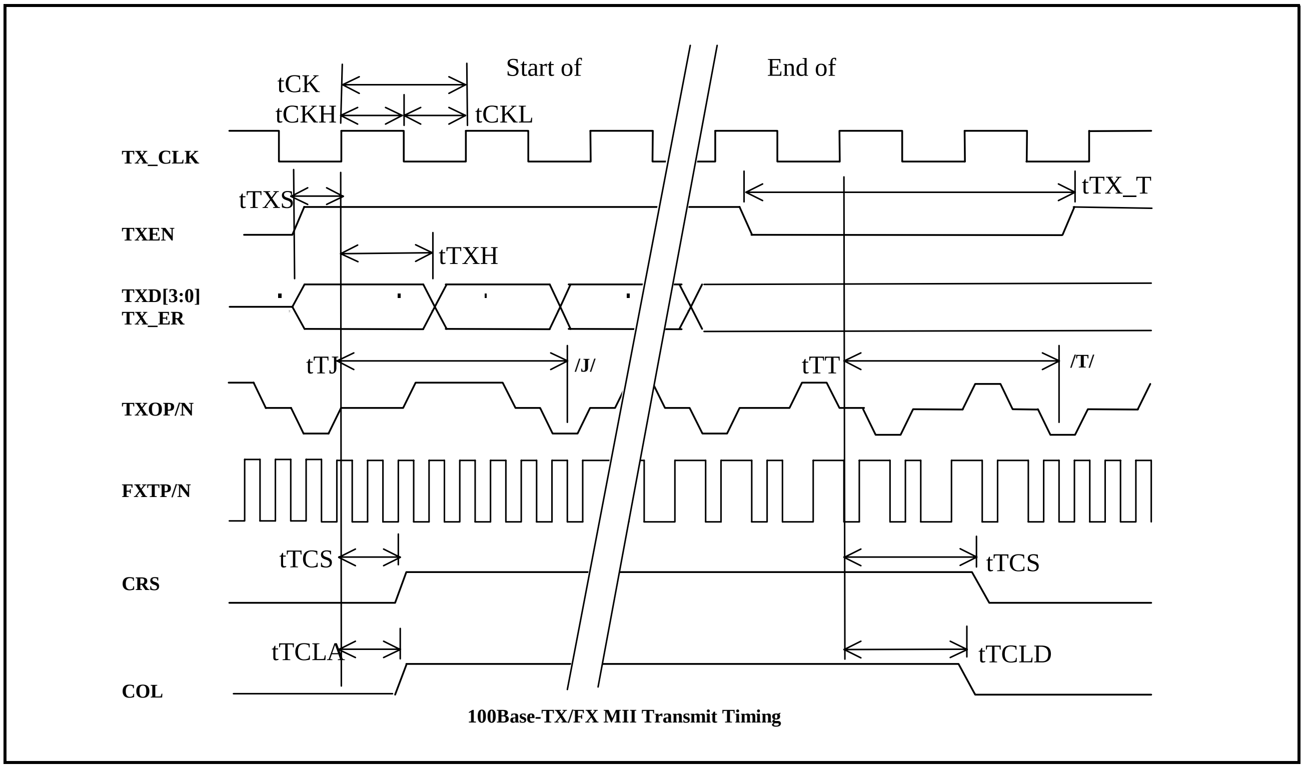


Figure 5: 100BASE-T MII Transmit Timing

100BASE-TX/FX MII Receive System Timing

Table 38: 100BASE-TX/FX MII Receive System Timing

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
RX_CLK period	tCK	-	39.998	40.000	40.002	ns
RX_CLK High period	tCKH	-	18.000	20.000	22.000	ns
RX_CLK Low period	tCKL	-	18.000	20.000	22.000	ns
/J/K to RXDV assert	tRDVA	-	-	40	180	ns
/J/K to CRS assert	tRCSA	-	-	40	180	ns
/J/K to COL assert	tRCLA	RPTR is logic low	-	40	180	ns
/T/R to !RXDV	tRDVD	RPTR is logic low	-	40	180	ns
/T/R to !CRS	tRCSD	RPTR is logic low	-	40	180	ns
/T/R to !COL	tRCLD	RPTR is logic low	-	40	180	ns
RX Propagation Delay	tRDVA	From RXIP/N(FXRP/N) to RXD[3:0]	-	40	180	ns
RXD[3:0], RXDV, RXER Setup	tRXS	From rising edge of RX_CLK	10	-	-	ns
RXD[3:0], RXDV, RXER Hold	tRXH	From rising edge of RX_CLK	10	-	-	ns

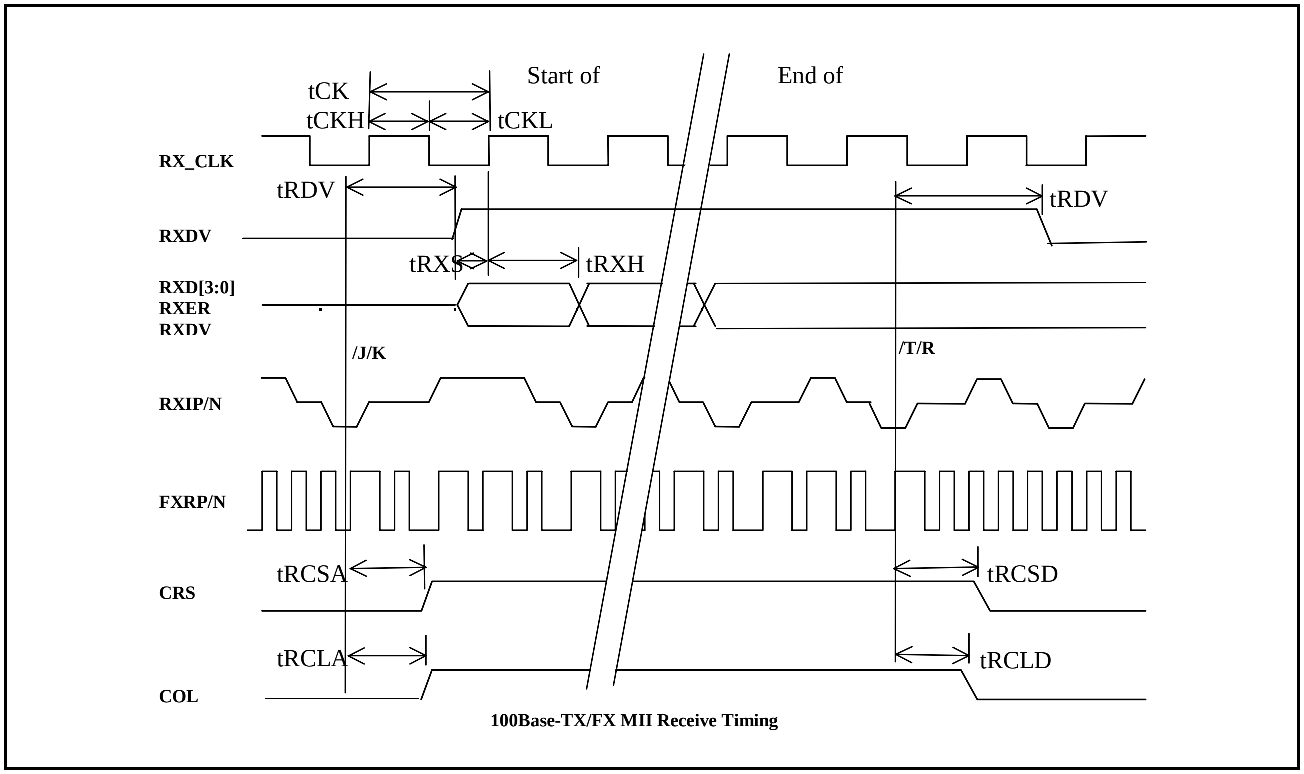


Figure 6: 100BASE-T MII Receive Timing

10BASE-T MII Transmit System Timing

Table 39: 10BASE-T MII Transmit System Timing

Parameter	***SYM***	***Conditions***	***Min***	***Typ***	***Max***	***Units***
TX_CLK period	tCK	-	399.98	400.00	400.02	ns
TX_CLK High period	tCKH	-	180.00	200.00	220.00	ns
TX_CLK Low period	tCKL	-	180.00	200.00	220.00	ns
TXEN to SOP	tTJ	-	240	-	360	ns
TXEN sampled to CRS	tTCSA	RPTR is logic low	-	-	130	ns
TXEN sampled to COL	tTCLA	RPTR is logic low	-	-	300	ns
!TXEN to EOP	tTJ	-	240	-	360	ns
!TXEN sampled to !CRS	tTCSD	RPTR is logic low	-	-	130	ns
!TXEN sampled to !COL	tTCLD	RPTR is logic low	-	-	300	ns
TX Propagation Delay	tTJ	From TXD[3:0] to TXOP/N	240	-	360	ns
TXD[3:0], TXEN, TXER Setup	tTXS	From rising edge of TX_CLK	10	-	-	ns
TXD[3:0], TXEN, TXER Hold	tTXH	From rising edge of TX_CLK	0	-	-	ns

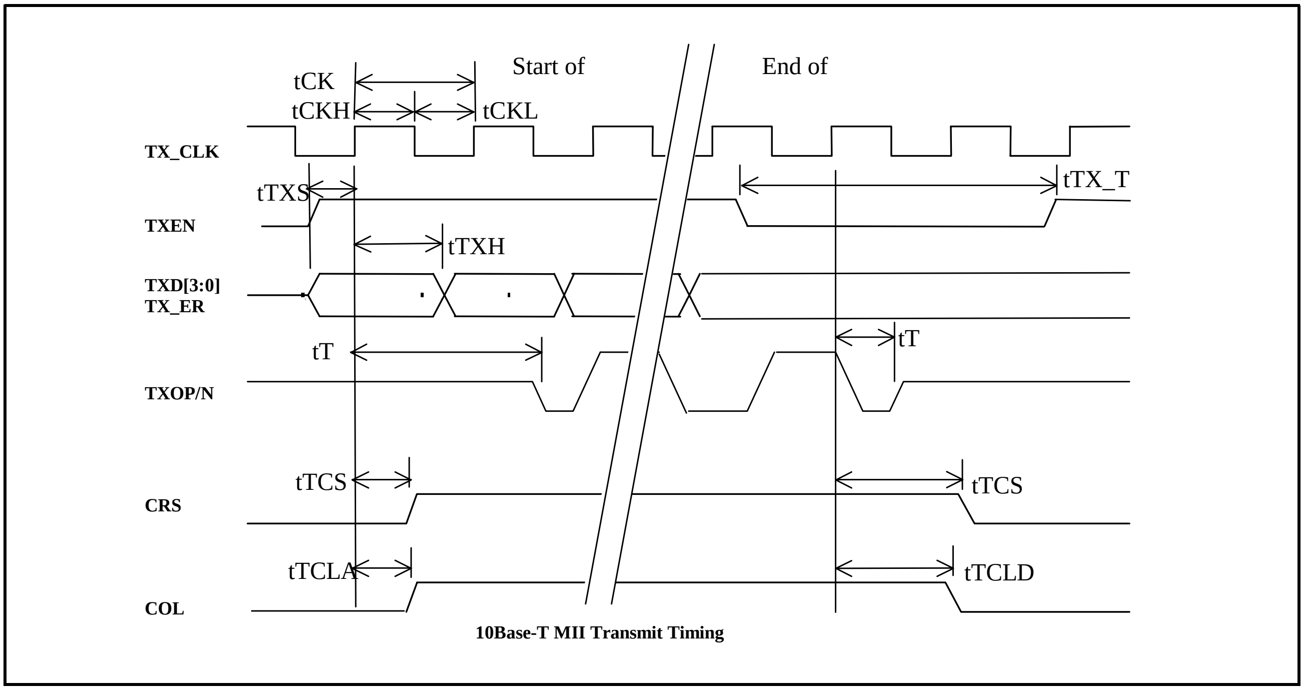


Figure 7: 10BASE-T Transmit Timing

10BASE-T MII RECEIVE SYSTEM TIMING

Table 40: 10BASE-T MII Receive System Timing

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
RX_CLK period	tCK	-	399.98	400.00	400.02	ns
RX_CLK High period	tCKH	-	180.00	200.00	220.00	ns
RX_CLK Low period	tCKL	-	180.00	200.00	220.00	ns
CRS to RXDV	tRDVA	-	100	100	100	ns
SOP to CRS	tRCSA	-	80	-	150	ns
SOP to COL	tRCLA	RPTR is logic low	80	-	150	ns
EOP to !RXDV	tRDVD	RPTR is logic low	120	-	140	ns
EOP to !CRS	tRCSD	RPTR is logic low	130	-	190	ns
EOP to !COL	tRCLD	RPTR is logic low	125	-	185	ns
RX Propagation Delay	tRDVA	From RXIP/N to RXD[3:0]	180	-	250	ns
RXD[3:0], RXDV, RXER Setup	tRXS	From rising edge of RX_CLK	16	-	-	ns
RXD[3:0], RXDV, RXER Hold	tRXH	From rising edge of RX_CLK	12	-	-	ns

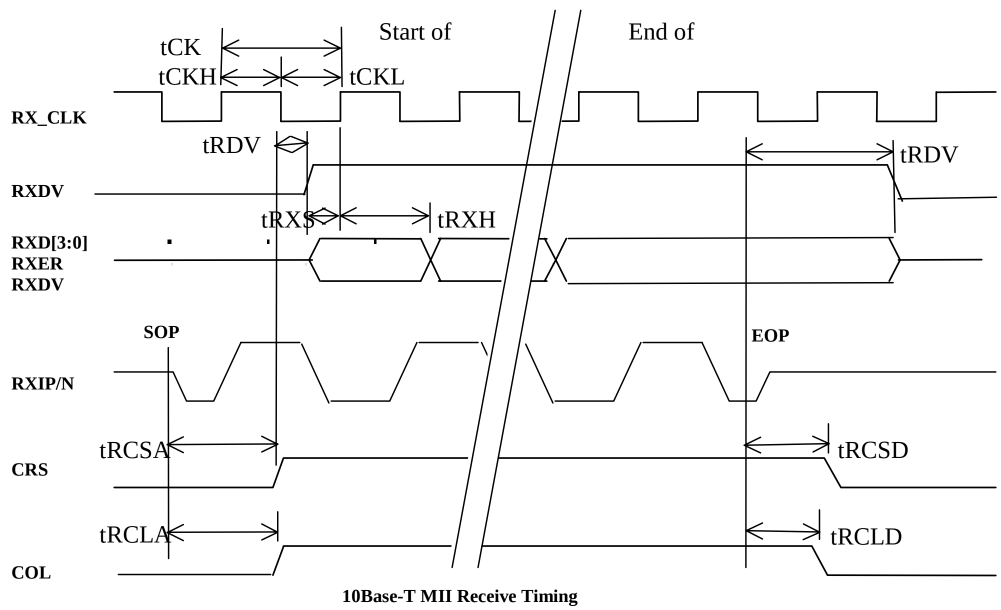
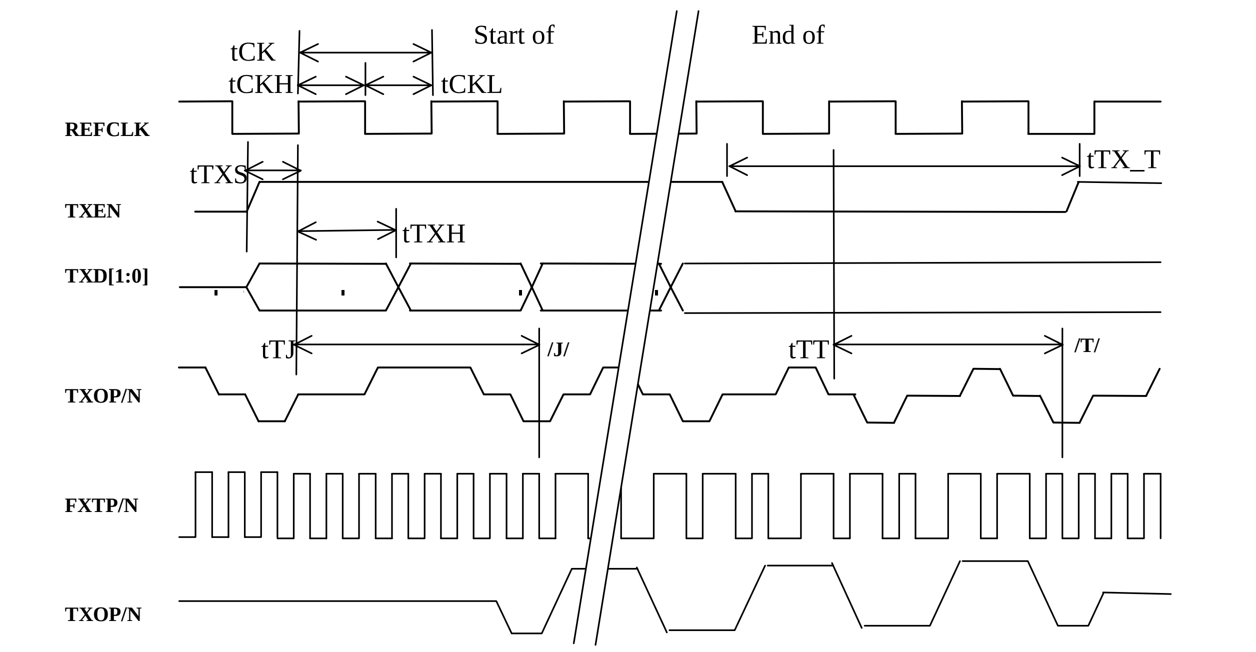


Figure 8: 10BASE-T Receive Timing

RMII TRANSMIT TIMING

Table 41: RMII Transmit Timing

Parameter	Symbol	Conditions	Min	Typ	Max	Units
REFCLK period	tCK	-	19.999	20.000	20.001	ns
REFCLK High period	tCKH	-	9.000	10.000	11.000	ns
REFCLK Low period	tCKL	-	9.000	10.000	11.000	ns
TX Propagation Delay	tTJ	From TXD[1:0] to TXOP/N(FXTP/N)	60	-	100	ns
TXD[1:0], TXEN Setup	tTXS	From rising edge of REFCLK	4	-	-	ns
TXD[1:0], TXEN Hold	tTXH	From rising edge of REFCLK	0	-	2	ns



100Base-TX/FX & 10Base -T RMII Transmit Timing

Figure 9: RMII Transmit Timing

RMII Receive Timing

Table 42: RMII Receive Timing

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
REFCLK period	tCK	-	19.999	20.000	20.001	ns
REFCLK High period	tCKH	-	9.000	10.000	11.000	ns
REFCLK Low period	tCKL	-	9.000	10.000	11.000	ns
RX Propagation Delay	tRDVA	From RXIP/N(FXRP/N) to RXD[1:0]	-	40	180	ns
RXD[1:0], CRS_DV, RXER Setup	tRXS	From rising edge of REFCLK	4	-	-	ns
RXD[1:0], CRS_DV, RXER Hold	tRXH	From rising edge of REFCLK	5	-	-	ns

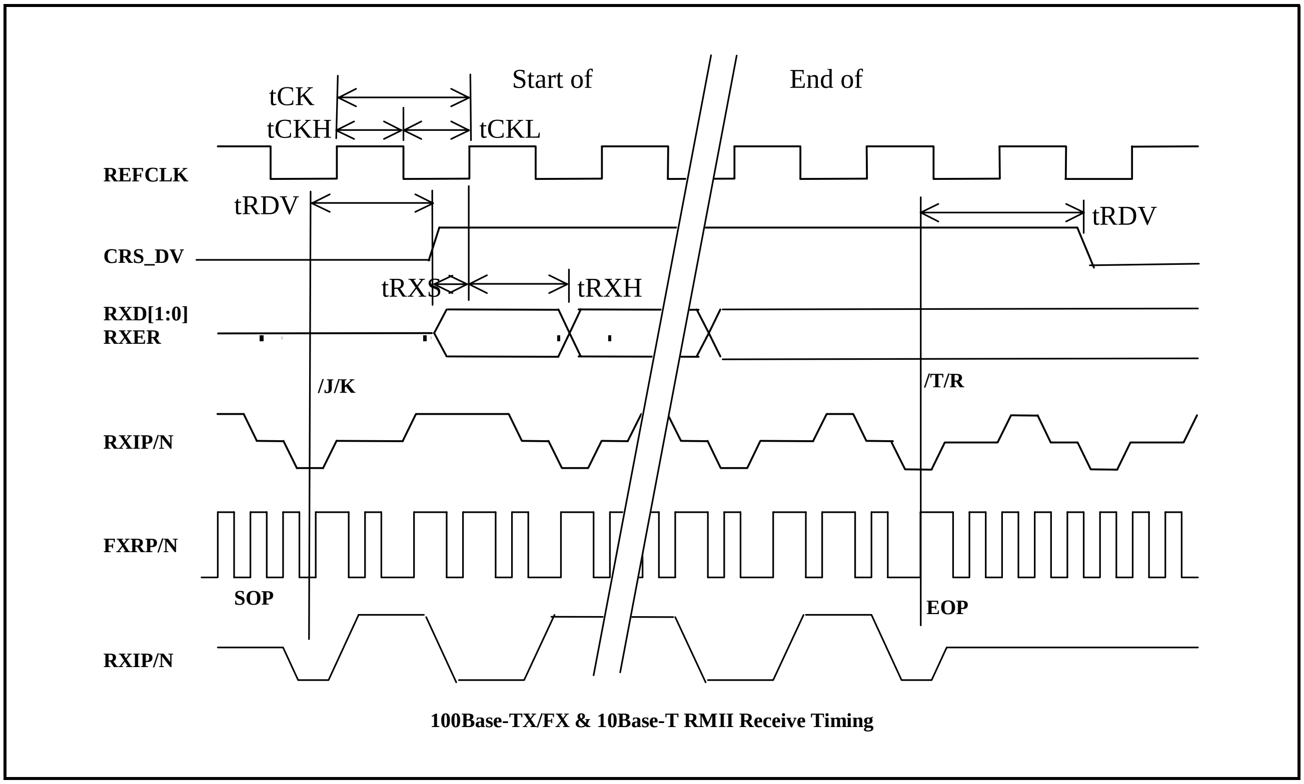


Figure 10: RMII Receive Timing

COPPER APPLICATION TERMINATION

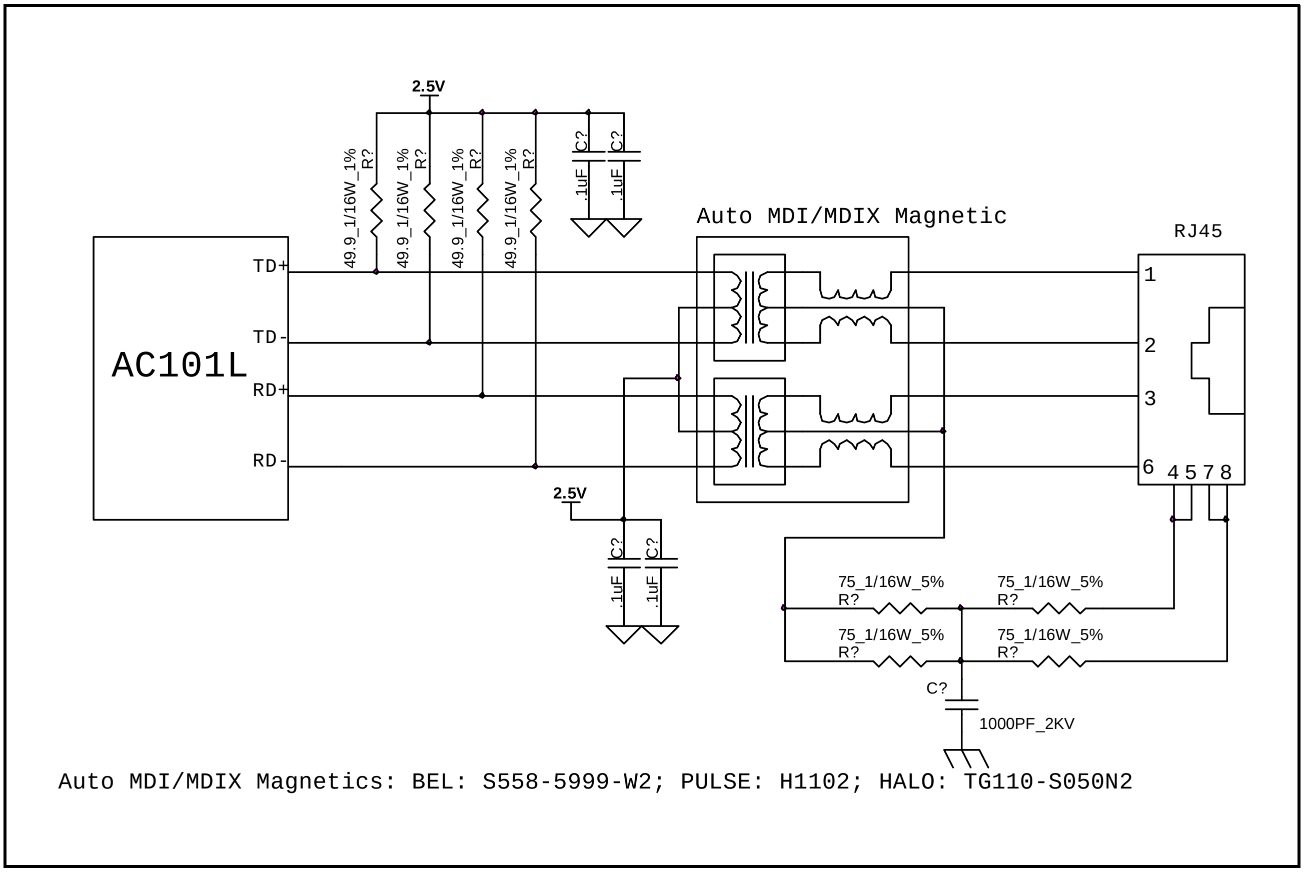


Figure 11: TX Application

Section 9: Electrical Characteristics

NOTE: The following electrical characteristics are design goals rather than characterized numbers.

ABSOLUTE MAXIMUM RATINGS

Table 43: Absolute Maximum Ratings

Parameter	*Symbol*	*Min*	*Max*	*Units*
Supply Voltage	3V3	GND-0.3	3.6	V
Input Voltage	V_I	GND-0.3	2.6	V
Input Current	I_I	-	TBD	mA
Storage Temperature	Ts	-40	+125	°C
Electrostatic Discharge	VESD	-	1000	V

RECOMMENDED OPERATING CONDITIONS

Table 44: Recommended Operating Conditions

Parameter	*Symbol*	*Pin*	*Operating Mode*	*Min*	*Typ*	*Max*	*Units*
Supply voltage AC101L	3V3	VCC33IN	-	3.135	3.3	3.465	V
Supply voltage AC101L	VCC	VCC, VCCPLL, VCC25OUT	-	2.375	2.5	2.625	V
High level input voltage	V_{IH}	All Digital inputs	-	2.2V	-	VCC[a]	V
High level input voltage	V_{IH}	SD	100BASE-FX	2.3	-	-	V
Low level input voltage	V_{IL}	All Digital inputs	-	-	-	0.8	V
Low level input voltage	V_{IL}	SD	100BASE-FX		-	1.7	V
Differential input voltage	V_{IDIFF}	RD ±	100BASE-FX	1.4	-	1.8	V
Common mode input voltage	V_{ICM}	RD ±	100BASE-TX	1.8	-	2.2	V
Common mode input voltage	V_{ICM}	RD ±	100BASE-FX	1.8	-	2.2	V
Ambient Operating Temperature AC101L	T_A	-	-	0	-	+70	°C

a. Can tolerate up to 3.3 V.

ELECTRICAL CHARACTERISTICS

Table 45: Electrical Characteristics

Parameter	Symbol	Pins	Conditions	Min	Typ	Max	Units
Supply Current	I_{CC}	VCC, VCC25OUT, VCCPLL	100BASE-TX	-	TBD	-	mA
Supply Current Power Down Mode	I_{CC}	VCC, VCC25OUT, VCCPLL	-	-	11	-	mA
High Level Output Voltage	V_{OH}	All Digital Outputs	I_{OH} = -12mA VCC=2.5V	VCC-0.4	-	-	V
High Level Output Voltage	V_{OH}	TD ±	Driving Load Magnetic Module	-	-	VCC+1.5	V
Low Level Output Voltage	V_{OL}	All Digital Outputs	I_{OL} = 8mA	-	-	0.4	V
Low Level Output Voltage	V_{OL}	TD ±	Driving Load Magnetic Module	VCC-1.5	-	-	-
Differential Output Voltage	V_{ODIFF}	TD ±	100BASE-FX Mode	1.5	-	1.7	V
Input Current	I_I	Digital inputs w/Pull-up Resistor	V_I = VCC	-	-	200	µA
Bias Voltage	V_{BIAS}	RBIAD	-	1.18	-	1.30	V

Section 10: Fiber Application Termination

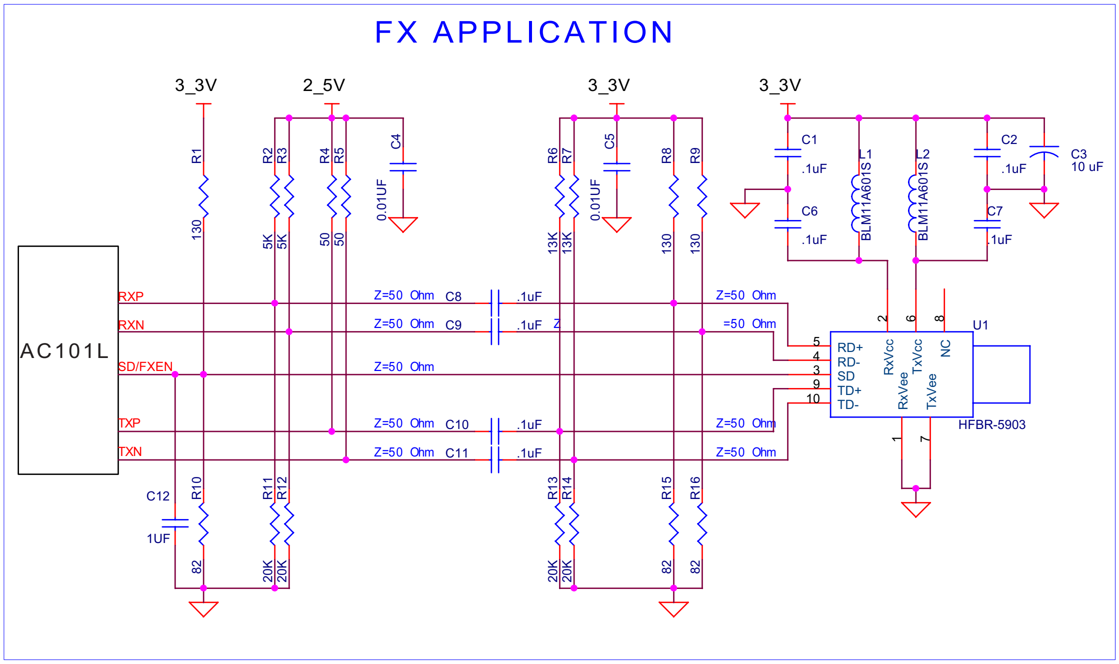


Figure 12: FX Application

Section 11: Power and Ground Filtering

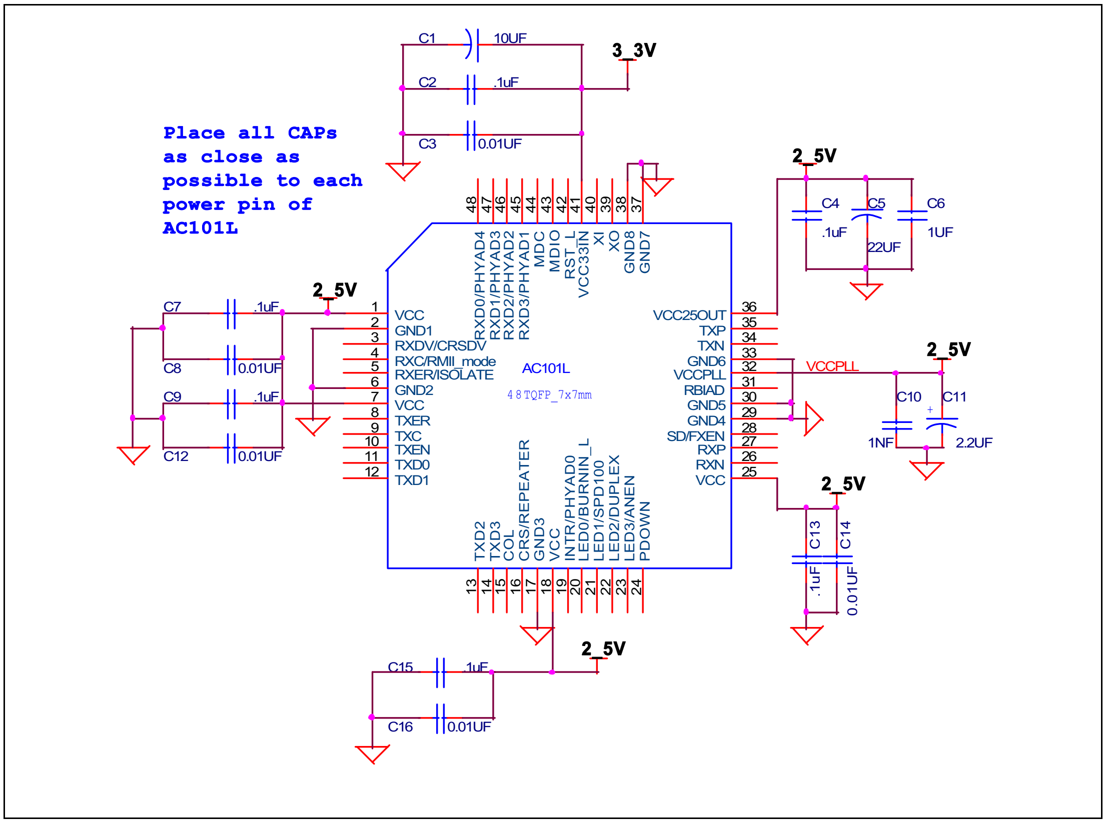
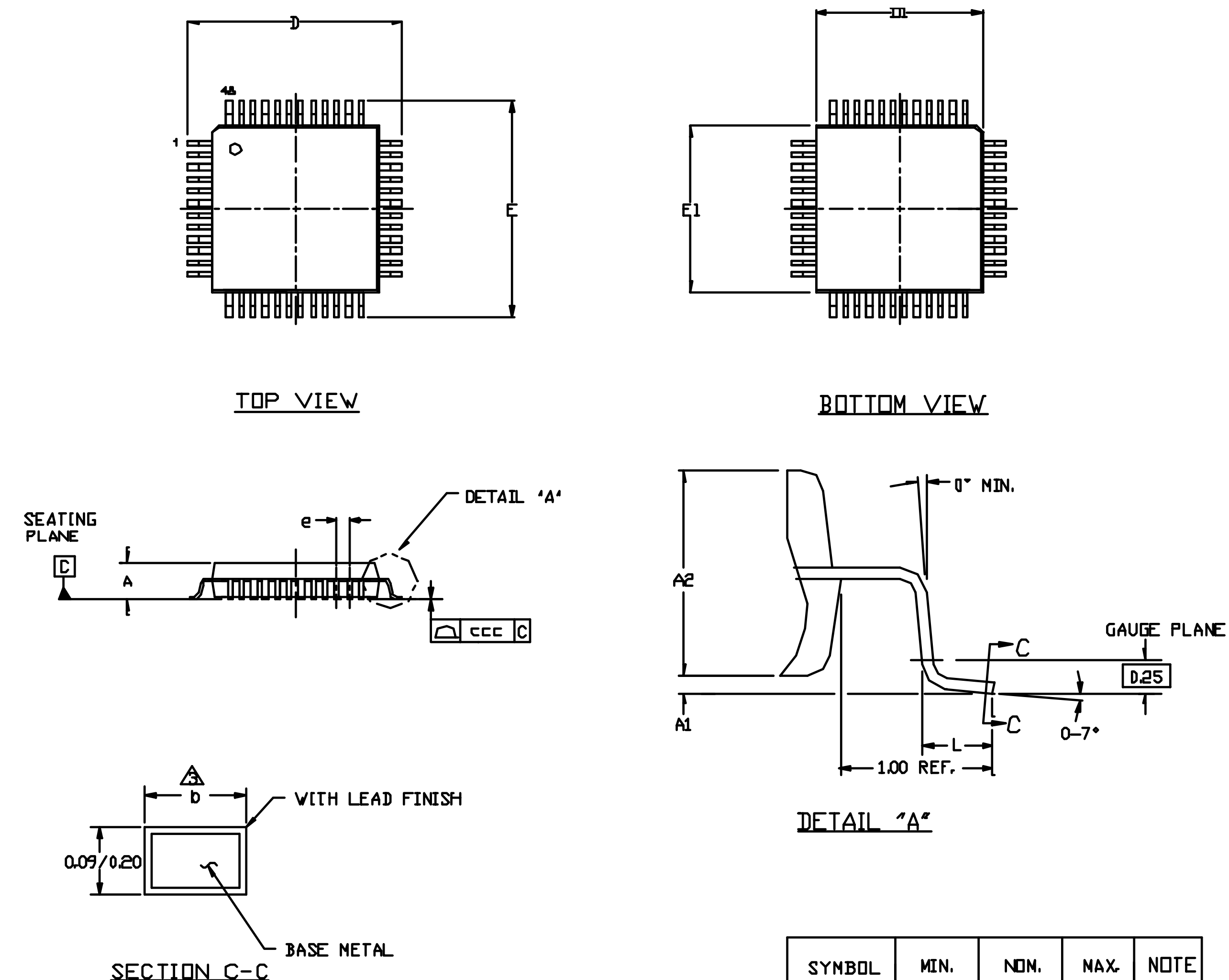


Figure 13: Power and Ground Filtering

Section 12: Mechanical Information



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-1994.
2. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS BY 0.20 MM, AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PKG.
3. (△) DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MIN.	NOM.	MAX.	NOTE
A	–	–	1.20	
A_1	0.05	0.10	0.15	
A_2	0.95	1.00	1.05	
D	9.00 BSC.			
D_1	7.00 BSC.			
E	9.00 BSC.			
E_1	7.00 BSC.			
L	0.45	0.60	0.75	
e	0.50 BSC.			
b	0.17	0.22	0.27	3
ccc	0.08			

Figure 14: Quad Flat Pack Outline (7 x 7 mm)

Section 13: Thermal Specifications

Table 46: Thermal Parameters

Airflow (feet per minute)	***0***	***100***	***200***	***400***	***600***
Theta JA (°C /W)	53.9	51.2	50	48.6	47.5
Theta JC (°C /W) at max junction temperature of 125 °C			24.7		

Section 14: Ordering Information

Part Number	Package	Ambient Temperature
AC101LKQT	48TQFP	0 °C to 70 °C

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