

FDP7030L / FDB7030L

N-Channel Logic Level PowerTrench[®] MOSFET

General Description

This N-Channel Logic Level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

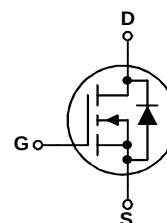
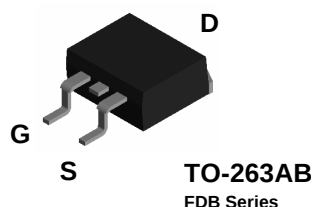
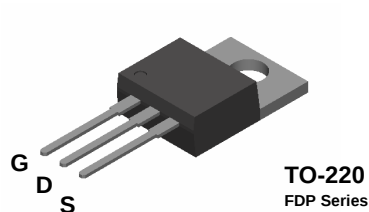
These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

Features

- 80A, 30 V $R_{DS(ON)} = 7 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 10 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- Critical DC electrical parameters specified at elevated temperature
- High performance trench technology for extremely low $R_{DS(ON)}$
- 175°C maximum junction temperature rating



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous (Note 1)	80	A
	– Pulsed (Note 1)	240	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	68	W
	Derate above 25°C	0.4	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-65 to $+175$	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDB7030L	FDB7030L	13"	24mm	800 units
FDP7030L	FDP7030L	Tube	n/a	45

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 15\text{ V}, I_D = 80\text{ A}$			114	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				80	A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		24		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		–5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 40\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 37\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 40\text{ A}, T_J = 125^\circ\text{C}$		5.2 6.5 7.2	7 10 11	mΩ
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$	60			A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 40\text{ A}$		115		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		2440		pF
C_{oss}	Output Capacitance			580		pF
C_{rss}	Reverse Transfer Capacitance			250		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		1.4		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		13	23	ns
t_r	Turn–On Rise Time			13	23	ns
$t_{d(off)}$	Turn–Off Delay Time			42	68	ns
t_f	Turn–Off Fall Time			15	27	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 40\text{ A},$ $V_{GS} = 5\text{ V}$		24	33	nC
Q_{gs}	Gate–Source Charge			7		nC
Q_{gd}	Gate–Drain Charge			9		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				80	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 40\text{ A}$ (Note 1)		0.9	1.3	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 40\text{ A},$		34		nS
Q_{rr}	Diode Reverse Recovery Charge	$dI_F/dt = 100\text{ A}/\mu\text{s}$		24		nC

Notes:1. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

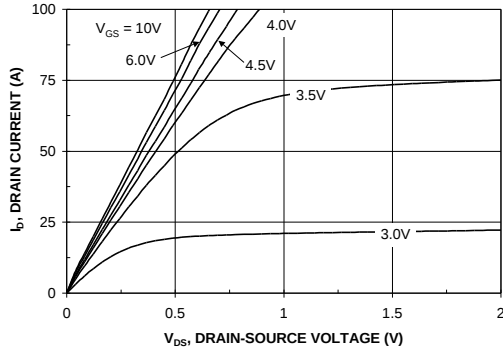


Figure 1. On-Region Characteristics.

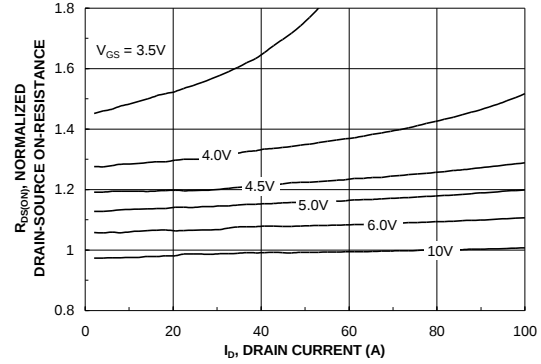


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

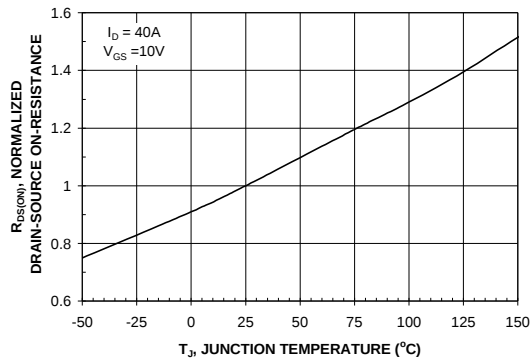


Figure 3. On-Resistance Variation with Temperature.

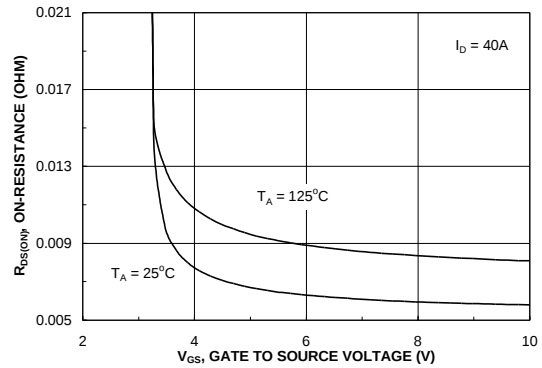


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

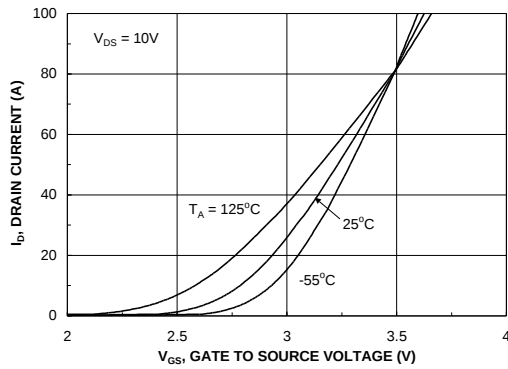


Figure 5. Transfer Characteristics.

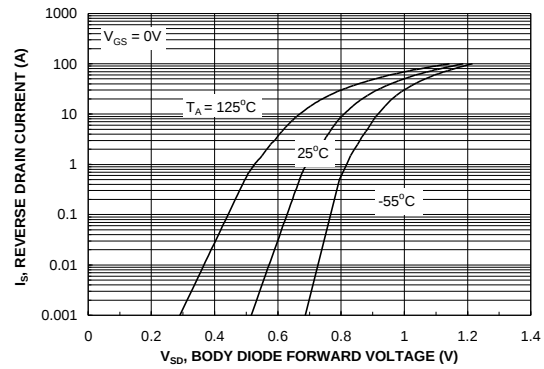


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

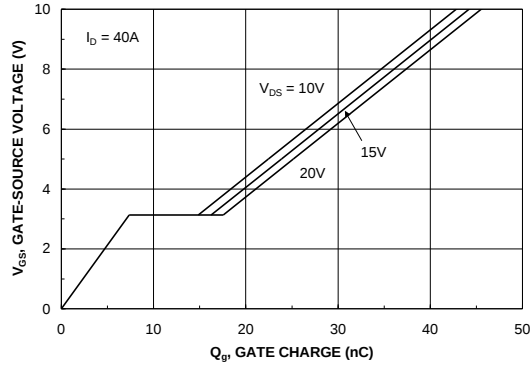


Figure 7. Gate Charge Characteristics.

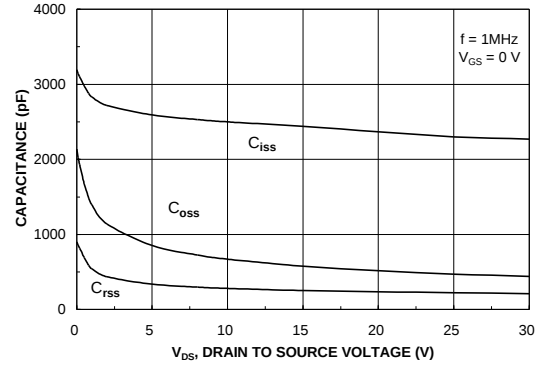


Figure 8. Capacitance Characteristics.

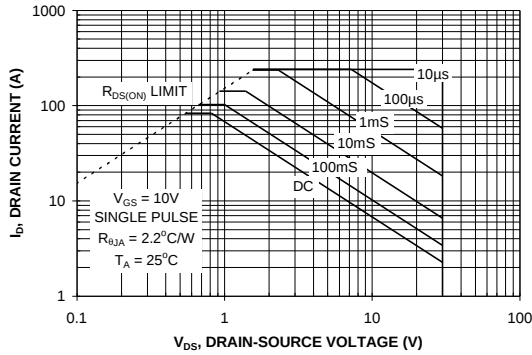


Figure 9. Maximum Safe Operating Area.

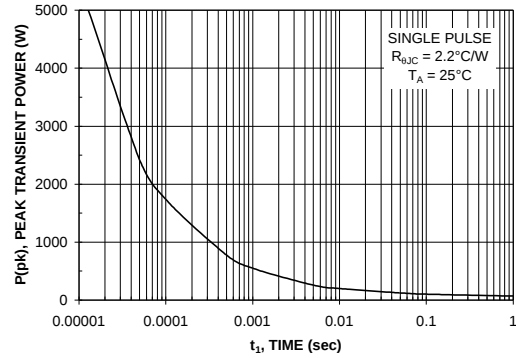


Figure 10. Single Pulse Maximum Power Dissipation.

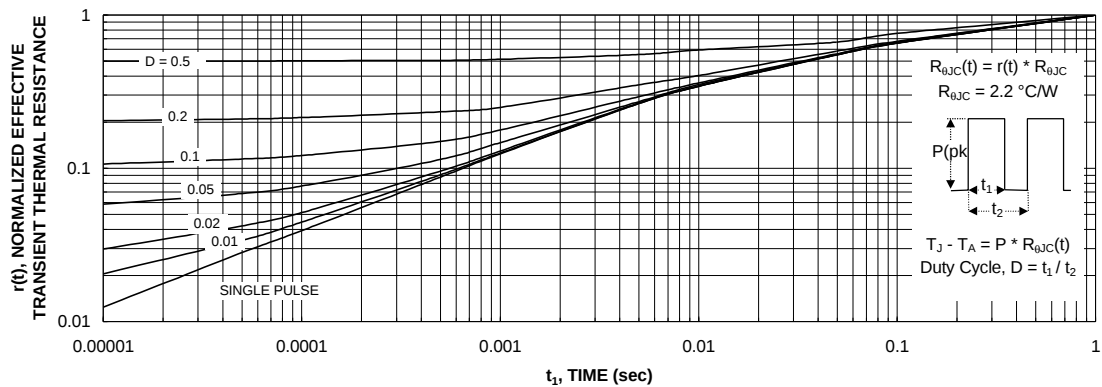


Figure 11. Transient Thermal Response Curve.

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