PM6652

Single-phase controller for Intel® MVP 6.5 render voltage regulator, CPU and VR11 CPU

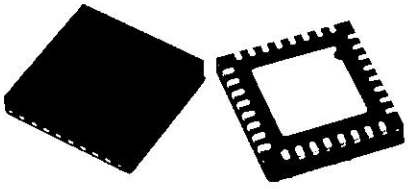
Datasheet – production data

Features

- 4.5 V to 36 V input voltage range
- 0.3 V to 1.5 V output voltage range
- IMVP6.5 GPU/CPU and VR11 CPU mode selection
- Very fast load transient response using constant-on-time loop control
- Remote voltage sensing
- Programmable droop function
- 7-bit dynamic voltage positioning (VID)
- Programmable PWM frequency
- Lossless current sense with inductor DCR
- Accurate inductor current sense with R_{SENSE}
- Negative current limit
- Boot diode embedded
- Latched OVP, UVP and overtemperature
- Pulse-skipping when suspend state is selected
- Output voltage ripple compensation
- Soft-start and soft-end
- Power good available
- Current monitor (IMON)
- Thermal throttling

Applications

- Intel mobile graphic core IMVP6.5
- Intel mobile CPU IMVP6.5
- Intel ATOM® VR11 based devices
- Notebook, netbook and nettop computers
- Handheld devices and PDAs



VFQFPN-32 5x5 mm

Description

The PM6652 is a single-phase, step-down SMPS controller with high precision 7-bit DAC. It has been designed to supply the CPU and the graphics core (render engine) of the Intel® mobile platform, according to Intel MVP6.5 specifications.

The PM6652 can also be configured to supply the 7-bit family, VR11 compliant, ATOM® processors.

The controller, based on constant on-time (COT) architecture, allows real-time dynamic switching of the core operating voltages and frequencies, working in both performance and suspend render states.

An embedded integrator control loop compensates the DC voltage error due to the output ripple.

The high efficiency at light load, achieved with pulse-skipping working mode, and the extremely low shutdown and quiescent adsorbed current, make the PM6652 the ideal choice in battery powered devices.

Table 1. Device summary

Order codes	Package	Packaging
PM6652	VFQFPN-32 5 x 5 mm (exposed pad)	Tray
PM6652TR		Tape and reel

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1 Typical application circuit

Figure 1. Typical application circuit - IMVP6.5 render core supply

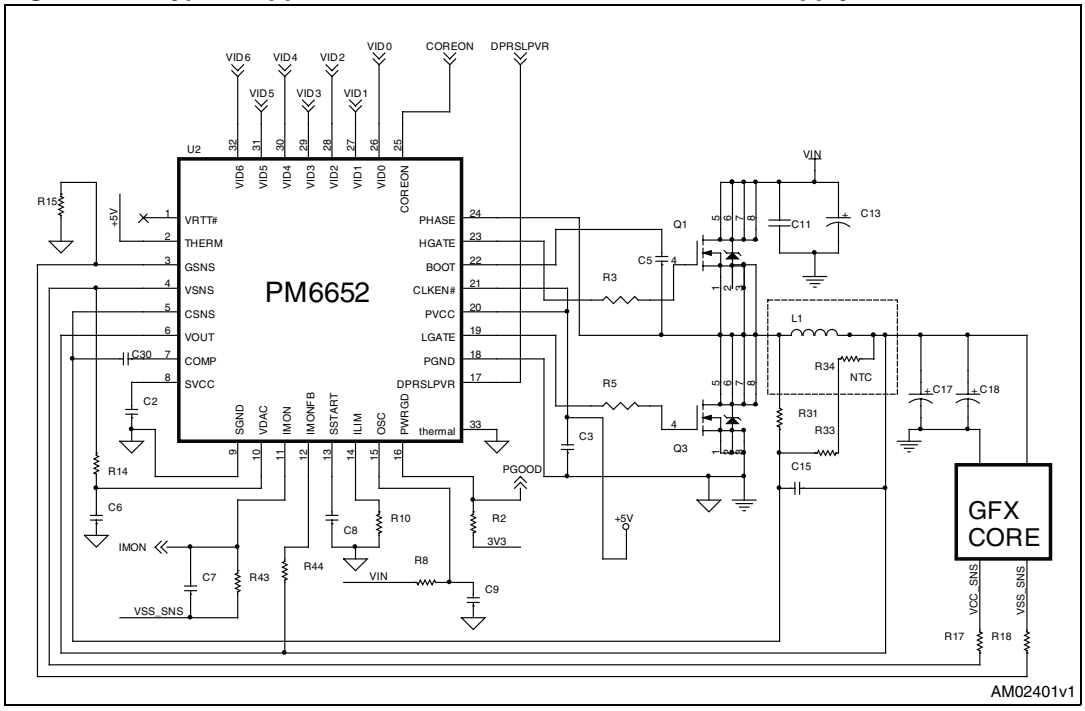


Figure 2. Typical application circuit - IMVP6.5 LV/ULV CPU supply

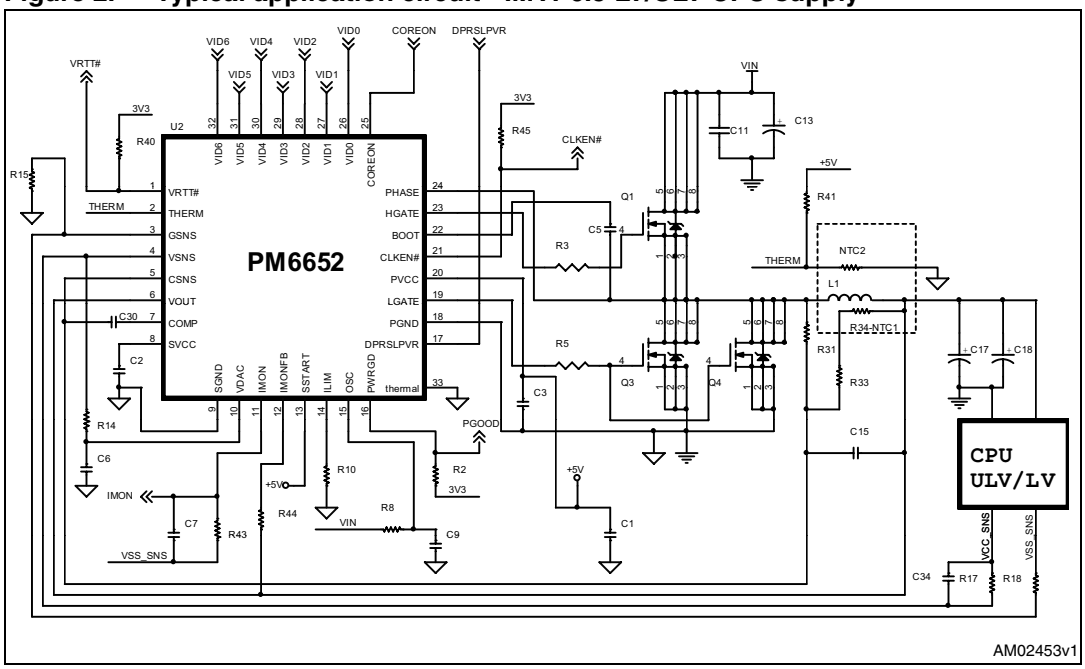
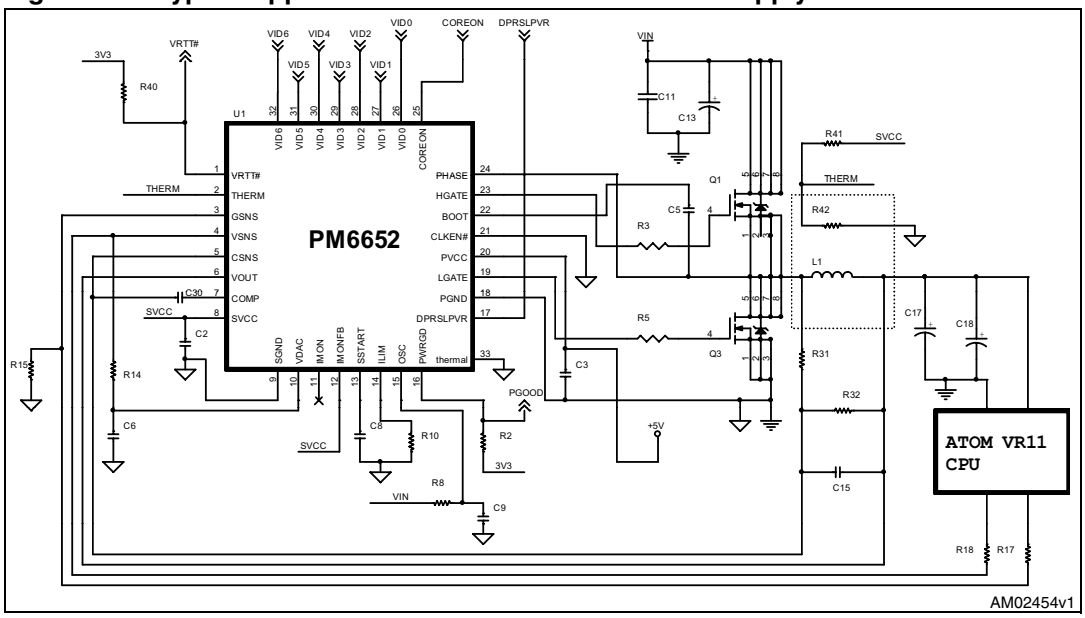


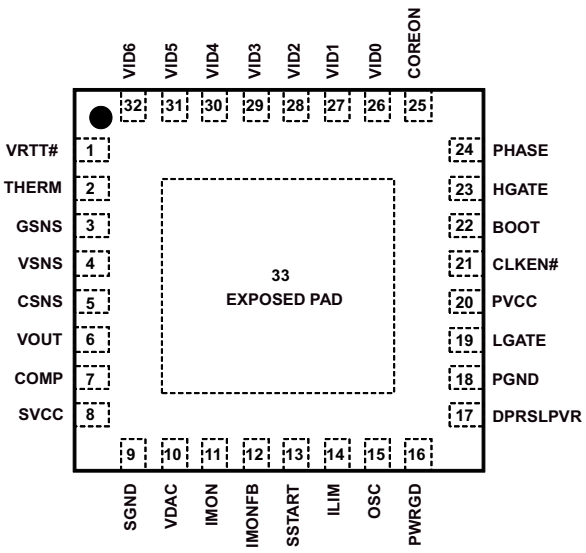
Figure 3. Typical application circuit – VR11 Atom CPU supply



2 Pin settings

2.1 Connections

Figure 4. PM6652 pinout (top view)



AM02402v1

2.2 Pin description

Figure 5. Pin functions

Pin n°	Name	Description
1	VRTT#	Thermal throttling indicator, open drain output.
2	THERM	Thermal throttling input. Connect to the central tap of NTC-based divider for MOS or inductor thermal monitoring.
3	GSNS	Output voltage ground remote sensing.
4	VSNS	Output voltage remote sensing.
5	CSNS	Current sensing input for droop function and IMON reporting. It represents the positive input of the differential current comparator. Connect to the inductor, for DCR sensing, or to a dedicated resistor for precision current sensing.
6	VOUT	Output voltage feedback. It also represents the negative input of the differential current comparator.
7	COMP	DC output voltage error compensation pin.
8	SVCC	+5 V analog and digital supply.
9	SGND	Analog and digital ground.

Figure 5. Pin functions (continued)

Pin n°	Name	Description
10	VDAC	Internal DAC reference output. Bypass to GND with a 10 nF capacitor.
11	IMON	Current monitor output. Bypass to remote ground through R-C network.
12	IMONFB	Current monitor gain setting pin. Connect to V_{OUT} through a resistor in the range 0.47 kΩ to 7 kΩ.
13	SSTART	Soft-start programming pin and mode of operation selection input.
14	ILIM	Current limit input. Connect ILIM to GND with a resistor to set the current limit threshold.
15	OSC	Frequency selection pin. Connect this pin to the input power supply rail through a resistor.
16	PWRGD	Power good signal (open drain output). High when VCC_GFX output voltage is within +200 mV/-300 mV of the programmed V_{DAC} value.
17	DPRSLPVR	Render suspend state enter and render suspend exit mode control input. Pulse-skipping or forced PWM working mode selection for IMVP6.5 CPU and VR11 mode.
18	PGND	Power ground.
19	LGATE	Low-side gate driver output.
20	PVCC	+5 V supply for internal driver supply.
21	CLKEN#	CLOCK ENABLE open drain output (active low) and mode of operation selection pin.
22	BOOT	Bootstrap capacitor connection. Input for the supply voltage of the high-side gate driver.
23	HGATE	High-side gate driver output.
24	PHASE	Switch node connection and return path for the high-side gate driver.
25	COREON	Switching regulator ON/OFF control input.
26	VID0	VIDs bits of the controller voltage programming DAC input. They allow programming of the no load output voltage, depending on the selected mode of operation. VID0 is the LSB and VID6 the MSB. Connect VIDx to a voltage <0.33 V to program a ‘0’; connect VIDx to a voltage >0.77 V to program a ‘1’.
27	VID1	
28	VID2	
29	VID3	
30	VID4	
31	VID5	
32	VID6	
33	EP	Exposed pad. Connect to SGND.

3 Electrical data

3.1 Maximum rating [a]

Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{PVCC}	PVCC to PGND		-0.3 to 6	V
V_{SVCC}	SVCC to SGND		-0.3 to 6	V
	SGND to PGND		-0.3 to 0.3	V
V_{BOOT}	BOOT to PHASE		-0.3 to 6	V
V_{HGATE}	HGATE to PHASE		-0.3 to V_{BOOT} +0.3	V
V_{PHASE}	PHASE to PGND		-0.3 to 37	V
V_{LGATE}	LGATE to PGND		-0.3 to V_{PVCC} +0.3	V
	VRTT#, THERM, GSNS, VSNS, CSNS, VOUT, COMP, VDAC, IMON, IMONFB, ILIM, OSC, PWRGD, DPRSLPVR, SSTART, CLKEN#, COREON, VIDx, to SGND		-0.3 to V_{SVCC} +0.3	V
	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “human body model” acceptance criteria: “Normal Performance”	All the pins	±1250	V

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance between junction and ambient	35	°C/W
T_J	Junction operating temperature range	-40 to 125	°C
T_A	Operating ambient temperature range	-40 to 85	
T_{STG}	Storage temperature range	-50 to 150	

a. Free air operating conditions unless otherwise specified. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{IN}	Input voltage range	4.5	-	36	V
V_{PVCC}	PVCC voltage range	4.5	-	5.5	V

4 Electrical characteristics

T_J = 25 °C, V_{IN} = +12 V, PVCC = +5 V if not otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
Supply section							
$I_{SVCC,QUIESCENT}$	IC supply current	COREON=5 V, DPRSLPVR=5 V, FB forced above the regulation point				850	µA
$I_{SVCC,SHDN}$	Operating current in shutdown	COREON=SGND, T_A=25 °C				1	µA
V_{SVCC} UVLO	SVCC undervoltage lockout upper threshold	Rising edge, controller disabled below this level			4.3	4.5	V
	SVCC undervoltage lockout lower threshold	Falling edge, controller enabled above this level		3.8	3.9		
	UVLO hysteresis				400		mV
On-time							
T_{on}	On-time duration	V_{CORE}=1.5 V	OSC=250 mV	820	920	1020	ns
			OSC=500 mV	410	470	530	
			OSC=1 V	210	248	280	
Off-time							
T_{OFFMIN}	Minimum off-time				250	400	ns
Integrator							
V_{COMP}	Overvoltage clamp	$V_{OVCLAMP}=V_{COMP}-V_{CSNS}$			80		mV
	Undervoltage clamp	$V_{UVCLAMP}=V_{COMP}-V_{CSNS}$			-140		mV
	Integrator offset			-2.5		2.5	mV
Voltages and DAC							
V_{DAC}	Internal DAC reference voltage accuracy	DAC codes from 0.8125 V to 1.5000 V		-0.7%		0.7%	mV
		DAC codes from 0.3000 V to 0.8000 V		-10		10	
V_{DAC} slew-rate	V_{DAC} output voltage slew rate after VIDs variation.	GFX mode selected, and DPRSLPVR asserted, positive V_{DAC} dV/dt only, or VR11 mode selected.		10	12.5		mV/µs
		GFX mode selected, and DPRSLPVR de-assert, or CPU mode selected.		5	6.25		mV/µs
$I_{leakVCC\_GFXC}$	V_{CORE} voltage sense leakage current					1	µA
VBOOT	Boot-up voltage	CPU or VR11 mode selected			1.100		V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Current sensing						
I_{CSNS}	Input leakage current				1	µA
	Current limit comparator offset	$V_{OFFS}=V_{PGND}-V_{PHASE}$	-4		4	mV
I_{LIM}	ILIM bias current		4.5	5	5.5	µA
	Zero-crossing comparator offset		-3.5		3.5	mV
High-side and low-side gate drivers						
	HGATE driver ON-resistance	HGATE high state (pull-up)		2.0	3	Ω
		HGATE low state (pull-down)		1.6	2.7	Ω
	LGATE driver ON-resistance	LGATE high state (pull-up)		1	1.7	Ω
		LGATE low state (pull-down)		0.6	1	Ω
UVP/OVP protections, PWRGD and CLKEN# signals						
OVP_{FIXED}	Fixed overvoltage threshold			1.55		V
$OVP_{LATCHED}$	Overvoltage threshold	Referred to V_{DAC} value		200		mV
$UVP_{LATCHED}$	Undervoltage threshold	Referred to V_{DAC} value		-300		mV
PWRGD	Upper threshold	Referred to V_{DAC} value		200		mV
	Lower threshold			-300		
I_{PWRGD}	PWRGD leakage current	PWRGD forced to 3.3 V			1	µA
V_{PWRGD}	Output low voltage	Isink=4 mA		250	350	mV
CLKEN#	Output low voltage	Isink=4 mA		250	350	mV
	CLKEN# leakage current	CLKEN# forced to 3.3 V; SSTART=5 V			1	µA
Current monitor section						
IMON	Current monitor output	$V_{CSNS} - V_{OUT}$ = 60 mV; RIMONFB=1.8 kΩ; R_{IMON}=10 kΩ	970	1000	1030	mV
		$V_{CSNS} - V_{OUT}$ = 30 mV; RIMONFB=1.8 kΩ; R_{IMON}=10 kΩ	474	500	526	
		$V_{CSNS} - V_{OUT}$ = 15 mV; RIMONFB=1.8 kΩ; R_{IMON}=10 kΩ	226	250	274	
	Current monitor clamp, referred to GSNS	8 kΩ<R_{IMON}<16 kΩ; GSNS-AGND<20 mV			1.15	V
	Current monitor input offset	I_{IMON} = 0 µA	0		1.0	mV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Soft-start section						
	Default soft-start slew rate	SSTART pin connected to AVCC	5	6.25		mV/µs
Soft-end section						
	VCC_GFX discharge resistance			7		Ω
Thermal throttling management						
THERM	Thermal detection trip threshold	Measured with respect to SGND		1.0		V
	Threshold hysteresis			200		mV
VRTT#	Output ON-resistance	THERM tied to SGND		7		Ω
$I_{VRTT\#}$	VRTT# leakage current	VRTT# forced to 3.3 V; THERM=5 V			1	µA
Power management						
COREON	SW regulator enable turn-on level		0.800			V
	SW regulator enable turn-off level				0.346	
$V_{DPRSLPVR}$	Render suspend pin thresholds	Render suspend (low)			0.346	V
		Render performance (high)	0.731			
VID_{IH}	VID high threshold		0.731			V
VID_{IL}	VID low threshold				0.346	V
I_{VID}	VID pull-up current				1	µA
Thermal shutdown						
T_{SHDN}	Shutdown temperature (1)			150		°C

1. Guaranteed by design. Not production tested.

5 Voltage identification (VID)

Table 6. VID for INTEL MVP 6.5 GFX core and CPU operation mode

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE
0	0	0	0	0	0	0	1.5000	1	0	0	0	0	0	0	0.7000
0	0	0	0	0	0	1	1.4875	1	0	0	0	0	0	1	0.6875
0	0	0	0	0	1	0	1.4750	1	0	0	0	0	1	0	0.6750
0	0	0	0	0	1	1	1.4625	1	0	0	0	0	1	1	0.6625
0	0	0	0	1	0	0	1.4500	1	0	0	0	1	0	0	0.6500
0	0	0	0	1	0	1	1.4375	1	0	0	0	1	0	1	0.6375
0	0	0	0	1	1	0	1.4250	1	0	0	0	1	1	0	0.6250
0	0	0	0	1	1	1	1.4125	1	0	0	0	1	1	1	0.6125
0	0	0	1	0	0	0	1.4000	1	0	0	1	0	0	0	0.6000
0	0	0	1	0	0	1	1.3875	1	0	0	1	0	0	1	0.5875
0	0	0	1	0	1	0	1.3750	1	0	0	1	0	1	0	0.5750
0	0	0	1	0	1	1	1.3625	1	0	0	1	0	1	1	0.5625
0	0	0	1	1	0	0	1.3500	1	0	0	1	1	0	0	0.5500
0	0	0	1	1	0	1	1.3375	1	0	0	1	1	0	1	0.5375
0	0	0	1	1	1	0	1.3250	1	0	0	1	1	1	0	0.5250
0	0	0	1	1	1	1	1.3125	1	0	0	1	1	1	1	0.5125
0	0	1	0	0	0	0	1.3000	1	0	1	0	0	0	0	0.5000
0	0	1	0	0	0	1	1.2875	1	0	1	0	0	0	1	0.4875
0	0	1	0	0	1	0	1.2750	1	0	1	0	0	1	0	0.4750
0	0	1	0	0	1	1	1.2625	1	0	1	0	0	1	1	0.4625
0	0	1	0	1	0	0	1.2500	1	0	1	0	1	0	0	0.4500
0	0	1	0	1	0	1	1.2375	1	0	1	0	1	0	1	0.4375
0	0	1	0	1	1	0	1.2250	1	0	1	0	1	1	0	0.4250
0	0	1	0	1	1	1	1.2125	1	0	1	0	1	1	1	0.4125
0	0	1	1	0	0	0	1.2000	1	0	1	1	0	0	0	0.4000
0	0	1	1	0	0	1	1.1875	1	0	1	1	0	0	1	0.3875
0	0	1	1	0	1	0	1.1750	1	0	1	1	0	1	0	0.3750
0	0	1	1	0	1	1	1.1625	1	0	1	1	0	1	1	0.3625
0	0	1	1	1	0	0	1.1500	1	0	1	1	1	0	0	0.3500
0	0	1	1	1	0	1	1.1375	1	0	1	1	1	0	1	0.3375
0	0	1	1	1	1	0	1.1250	1	0	1	1	1	1	0	0.3250
0	0	1	1	1	1	1	1.1125	1	0	1	1	1	1	1	0.3125

Table 6. VID for INTEL MVP 6.5 GFX core and CPU operation mode (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE
0	1	0	0	0	0	0	1.1000	1	1	0	0	0	0	0	0.3000
0	1	0	0	0	0	1	1.0875	1	1	0	0	0	0	1	0.2875
0	1	0	0	0	1	0	1.0750	1	1	0	0	0	1	0	0.2750
0	1	0	0	0	1	1	1.0625	1	1	0	0	0	1	1	0.2625
0	1	0	0	1	0	0	1.0500	1	1	0	0	1	0	0	0.2500
0	1	0	0	1	0	1	1.0375	1	1	0	0	1	0	1	0.2375
0	1	0	0	1	1	0	1.0250	1	1	0	0	1	1	0	0.2250
0	1	0	0	1	1	1	1.0125	1	1	0	0	1	1	1	0.2125
0	1	0	1	0	0	0	1.0000	1	1	0	1	0	0	0	0.2000
0	1	0	1	0	0	1	0.9875	1	1	0	1	0	0	1	0.1875
0	1	0	1	0	1	0	0.9750	1	1	0	1	0	1	0	0.1750
0	1	0	1	0	1	1	0.9625	1	1	0	1	0	1	1	0.1625
0	1	0	1	1	0	0	0.9500	1	1	0	1	1	0	0	0.1500
0	1	0	1	1	0	1	0.9375	1	1	0	1	1	0	1	0.1375
0	1	0	1	1	1	0	0.9250	1	1	0	1	1	1	0	0.1250
0	1	0	1	1	1	1	0.9125	1	1	0	1	1	1	1	0.1125
0	1	1	0	0	0	0	0.9000	1	1	1	0	0	0	0	0.1000
0	1	1	0	0	0	1	0.8875	1	1	1	0	0	0	1	0.0875
0	1	1	0	0	1	0	0.8750	1	1	1	0	0	1	0	0.0750
0	1	1	0	0	1	1	0.8625	1	1	1	0	0	1	1	0.0625
0	1	1	0	1	0	0	0.8500	1	1	1	0	1	0	0	0.0500
0	1	1	0	1	0	1	0.8375	1	1	1	0	1	0	1	0.0375
0	1	1	0	1	1	0	0.8250	1	1	1	0	1	1	0	0.0250
0	1	1	0	1	1	1	0.8125	1	1	1	0	1	1	1	0.0125
0	1	1	1	0	0	0	0.8000	1	1	1	1	0	0	0	0.0000
0	1	1	1	0	0	1	0.7875	1	1	1	1	0	0	1	0.0000
0	1	1	1	0	1	0	0.7750	1	1	1	1	0	1	0	0.0000
0	1	1	1	0	1	1	0.7625	1	1	1	1	0	1	1	0.0000
0	1	1	1	1	0	0	0.7500	1	1	1	1	1	0	0	0.0000
0	1	1	1	1	0	1	0.7375	1	1	1	1	1	0	1	0.0000
0	1	1	1	1	1	0	0.7250	1	1	1	1	1	1	0	0.0000
0	1	1	1	1	1	1	0.7125	1	1	1	1	1	1	1	OFF

Table 7. Voltage identification (VID) for INTEL VR11 operation mode

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE
0	0	0	0	0	0	0	1.5000	1	0	0	0	0	0	0	0.8125
0	0	0	0	0	0	1	1.5000	1	0	0	0	0	0	1	0.8000
0	0	0	0	0	1	0	1.5000	1	0	0	0	0	1	0	0.7875
0	0	0	0	0	1	1	1.5000	1	0	0	0	0	1	1	0.7750
0	0	0	0	1	0	0	1.5000	1	0	0	0	1	0	0	0.7625
0	0	0	0	1	0	1	1.5000	1	0	0	0	1	0	1	0.7500
0	0	0	0	1	1	0	1.5000	1	0	0	0	1	1	0	0.7375
0	0	0	0	1	1	1	1.5000	1	0	0	0	1	1	1	0.7250
0	0	0	1	0	0	0	1.5000	1	0	0	1	0	0	0	0.7125
0	0	0	1	0	0	1	1.5000	1	0	0	1	0	0	1	0.7000
0	0	0	1	0	1	0	1.4875	1	0	0	1	0	1	0	0.6875
0	0	0	1	0	1	1	1.4750	1	0	0	1	0	1	1	0.6750
0	0	0	1	1	0	0	1.4625	1	0	0	1	1	0	0	0.6625
0	0	0	1	1	0	1	1.4500	1	0	0	1	1	0	1	0.6500
0	0	0	1	1	1	0	1.4375	1	0	0	1	1	1	0	0.6375
0	0	0	1	1	1	1	1.4250	1	0	0	1	1	1	1	0.6250
0	0	1	0	0	0	0	1.4125	1	0	1	0	0	0	0	0.6125
0	0	1	0	0	0	1	1.4000	1	0	1	0	0	0	1	0.6000
0	0	1	0	0	1	0	1.3875	1	0	1	0	0	1	0	0.5875
0	0	1	0	0	1	1	1.3750	1	0	1	0	0	1	1	0.5750
0	0	1	0	1	0	0	1.3625	1	0	1	0	1	0	0	0.5625
0	0	1	0	1	0	1	1.3500	1	0	1	0	1	0	1	0.5500
0	0	1	0	1	1	0	1.3375	1	0	1	0	1	1	0	0.5375
0	0	1	0	1	1	1	1.3250	1	0	1	0	1	1	1	0.5250
0	0	1	1	0	0	0	1.3125	1	0	1	1	0	0	0	0.5125
0	0	1	1	0	0	1	1.3000	1	0	1	1	0	0	1	0.5000
0	0	1	1	0	1	0	1.2875	1	0	1	1	0	1	0	0.4875
0	0	1	1	0	1	1	1.2750	1	0	1	1	0	1	1	0.4750
0	0	1	1	1	0	0	1.2625	1	0	1	1	1	0	0	0.4625
0	0	1	1	1	0	1	1.2500	1	0	1	1	1	0	1	0.4500
0	0	1	1	1	1	0	1.2375	1	0	1	1	1	1	0	0.4375
0	0	1	1	1	1	1	1.2250	1	0	1	1	1	1	1	0.4250
0	1	0	0	0	0	0	1.2125	1	1	0	0	0	0	0	0.4125
0	1	0	0	0	0	1	1.2000	1	1	0	0	0	0	1	0.4000

Table 7. Voltage identification (VID) for INTEL VR11 operation mode (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE
0	1	0	0	0	1	0	1.1875	1	1	0	0	0	1	0	0.3875
0	1	0	0	0	1	1	1.1750	1	1	0	0	0	1	1	0.3750
0	1	0	0	1	0	0	1.1625	1	1	0	0	1	0	0	0.3625
0	1	0	0	1	0	1	1.1500	1	1	0	0	1	0	1	0.3500
0	1	0	0	1	1	0	1.1375	1	1	0	0	1	1	0	0.3375
0	1	0	0	1	1	1	1.1250	1	1	0	0	1	1	1	0.3250
0	1	0	1	0	0	0	1.1125	1	1	0	1	0	0	0	0.3125
0	1	0	1	0	0	1	1.1000	1	1	0	1	0	0	1	0.3000
0	1	0	1	0	1	0	1.0875	1	1	0	1	0	1	0	0.2875
0	1	0	1	0	1	1	1.0750	1	1	0	1	0	1	1	0.2750
0	1	0	1	1	0	0	1.0625	1	1	0	1	1	0	0	0.2625
0	1	0	1	1	0	1	1.0500	1	1	0	1	1	0	1	0.2500
0	1	0	1	1	1	0	1.0375	1	1	0	1	1	1	0	0.2375
0	1	0	1	1	1	1	1.0250	1	1	0	1	1	1	1	0.2250
0	1	1	0	0	0	0	1.0125	1	1	1	0	0	0	0	0.2125
0	1	1	0	0	0	1	1.0000	1	1	1	0	0	0	1	0.2000
0	1	1	0	0	1	0	0.9875	1	1	1	0	0	1	0	0.1875
0	1	1	0	0	1	1	0.9750	1	1	1	0	0	1	1	0.1750
0	1	1	0	1	0	0	0.9625	1	1	1	0	1	0	0	0.1625
0	1	1	0	1	0	1	0.9500	1	1	1	0	1	0	1	0.1500
0	1	1	0	1	1	0	0.9375	1	1	1	0	1	1	0	0.1375
0	1	1	0	1	1	1	0.9250	1	1	1	0	1	1	1	0.1250
0	1	1	1	0	0	0	0.9125	1	1	1	1	0	0	0	0.1125
0	1	1	1	0	0	1	0.9000	1	1	1	1	0	0	1	0.1000
0	1	1	1	0	1	0	0.8875	1	1	1	1	0	1	0	0.0875
0	1	1	1	0	1	1	0.8750	1	1	1	1	0	1	1	0.0750
0	1	1	1	1	0	0	0.8625	1	1	1	1	1	0	0	0.0625
0	1	1	1	1	0	1	0.8500	1	1	1	1	1	0	1	0.0500
0	1	1	1	1	1	0	0.8375	1	1	1	1	1	1	0	0.0375
0	1	1	1	1	1	1	0.8250	1	1	1	1	1	1	1	OFF

6 Typical operating characteristics

Measurement setup: V_{IN} = 10 V, F_{SW} = 320 kHz, V_{CORE} = 1.2375 V, DPRSLPVR = 0 V if not otherwise specified.

Figure 6. V_{CORE} turn-on and PGOOD rising - no load

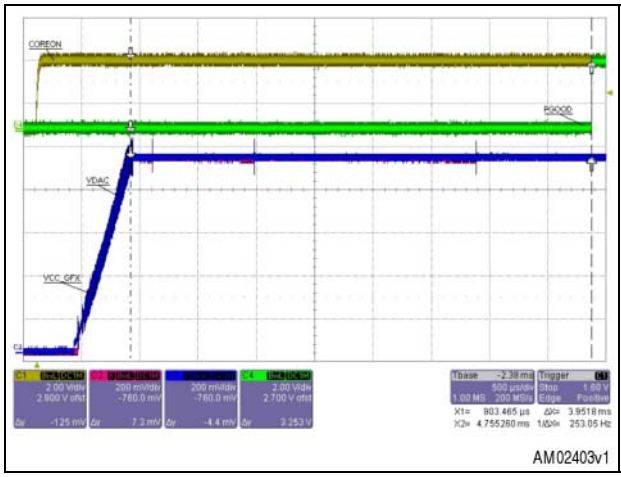


Figure 7. V_{CORE} turn-on - CPU IMVP6.5 mode

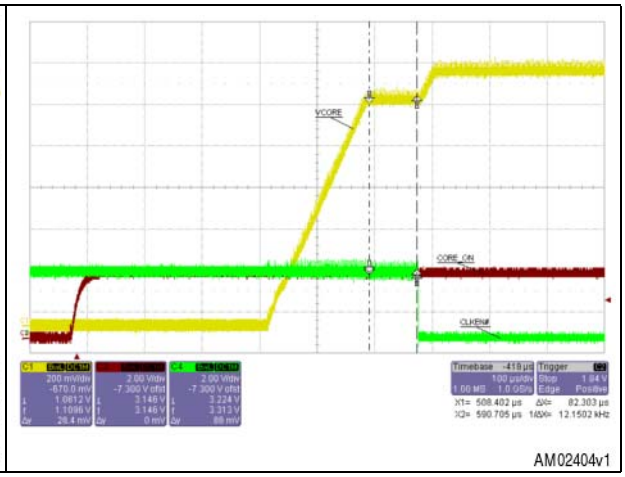


Figure 8. V_{CORE} working mode - DPRSLPVR asserted, no load

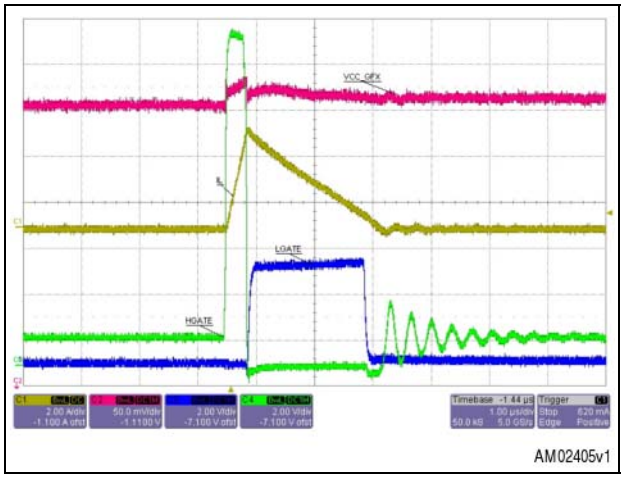


Figure 9. V_{CORE} working mode (0.9 V) - DPRSLPVR asserted, no load

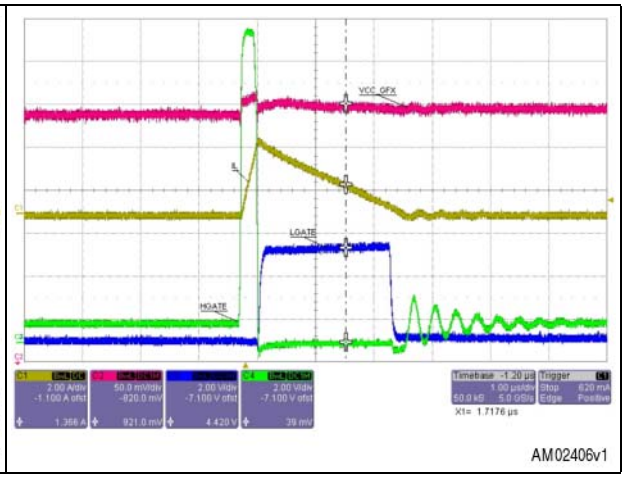


Figure 10. V_{CORE} working mode (0.4 V) - DPRSLPVR asserted, no load

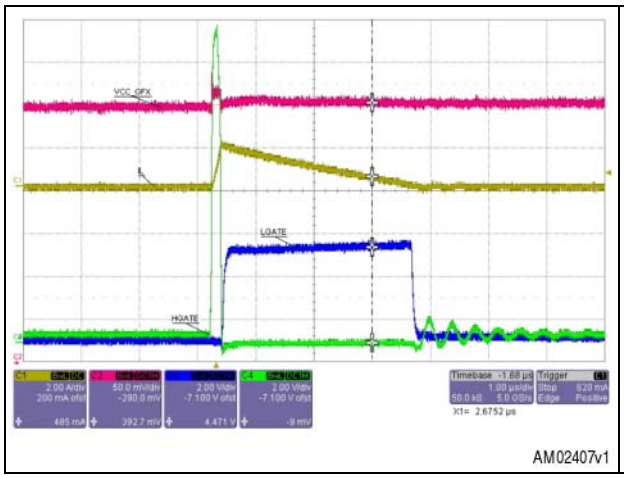


Figure 11. V_{CORE} working mode - DPRSLPVR not asserted, no load

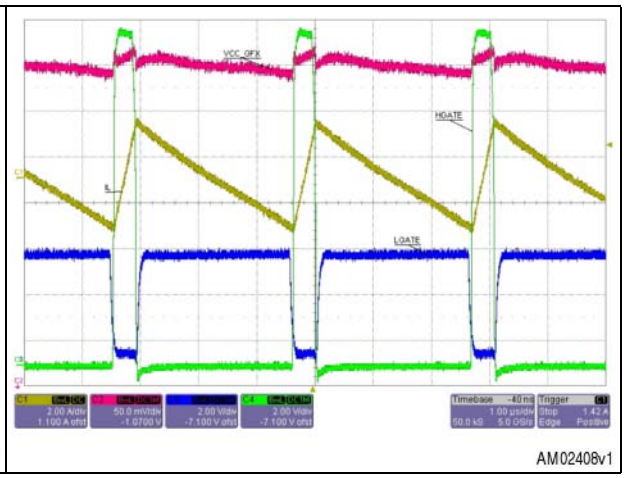


Figure 12. V_{CORE} working mode - DPRSLPVR not asserted, 10 A load

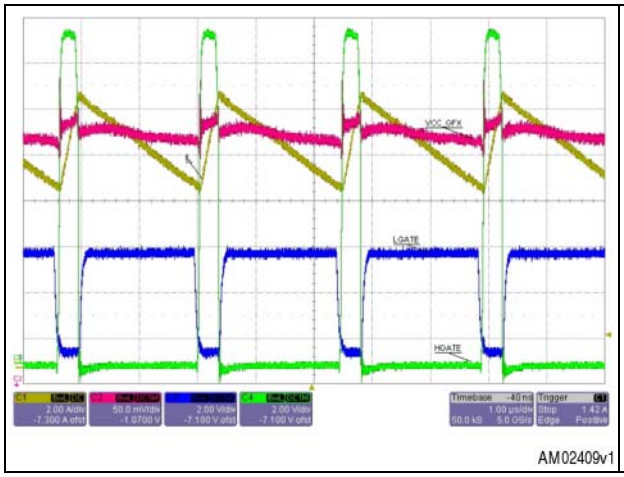


Figure 13. V_{CORE} working mode (0.9 V) - DPRSLPVR not asserted, no load

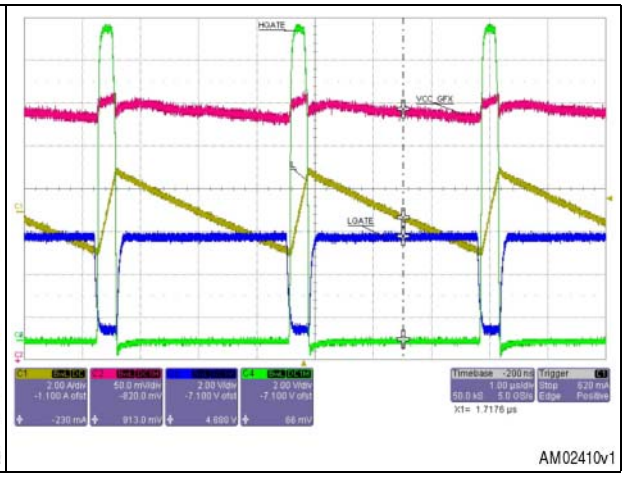


Figure 14. V_{CORE} working mode (0.4 V) - DPRSLPVR not asserted, no load

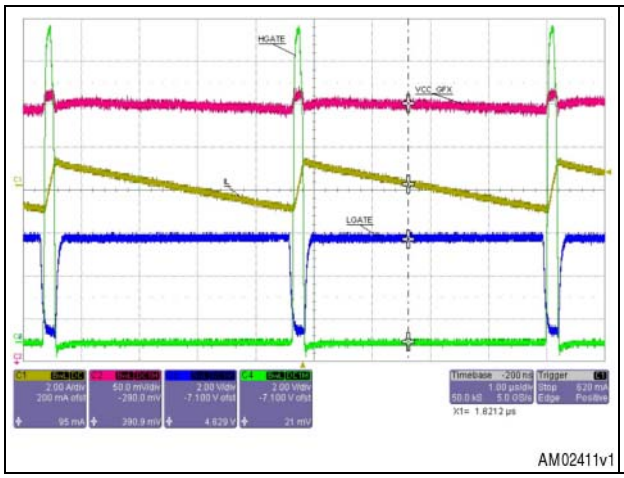


Figure 15. VID5 transition - entering and exiting suspend state (fast exit)

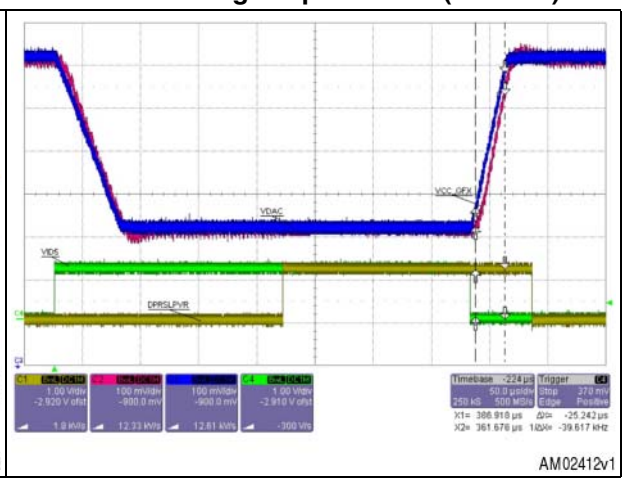


Figure 16. VID5 transition - entering and exiting suspend state (slow exit)

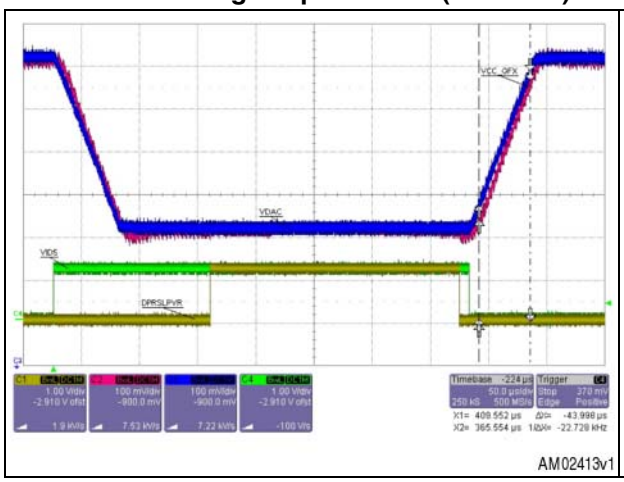


Figure 17. Droop function - 5 A to 15 A transient response

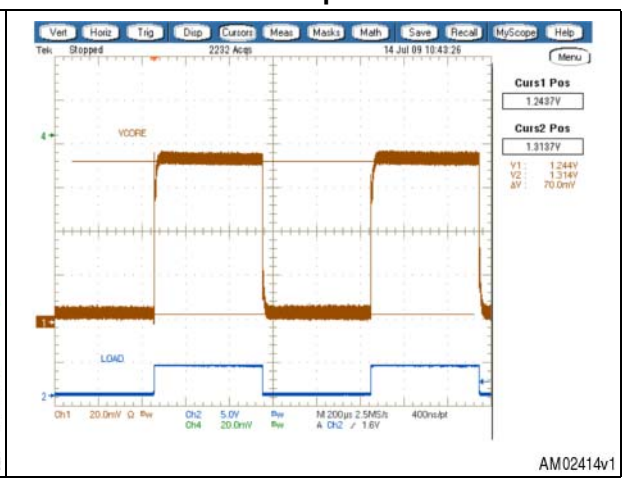


Figure 18. V_{CORE} VID step variation - VR11 mode

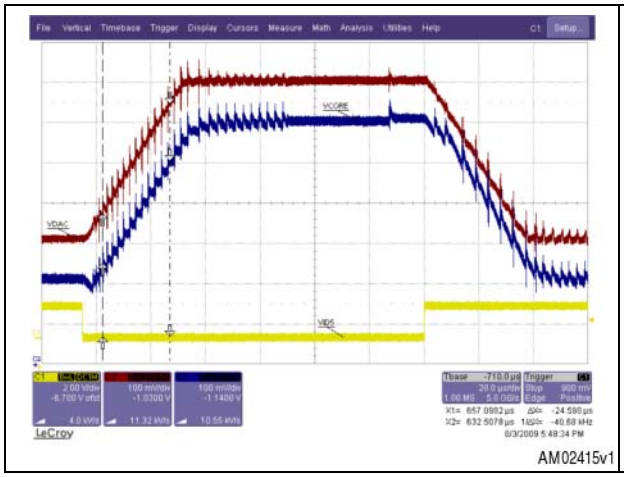


Figure 19. V_{CORE} soft-end - COREON pin de-assertion and PGOOD transition

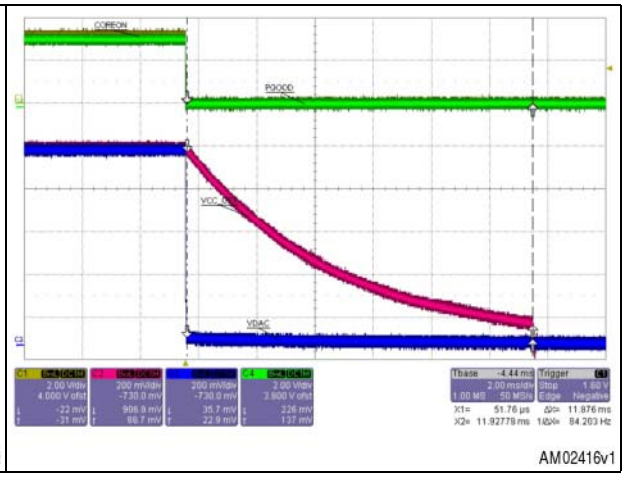


Figure 20. V_{CORE} overvoltage (+200 mV)

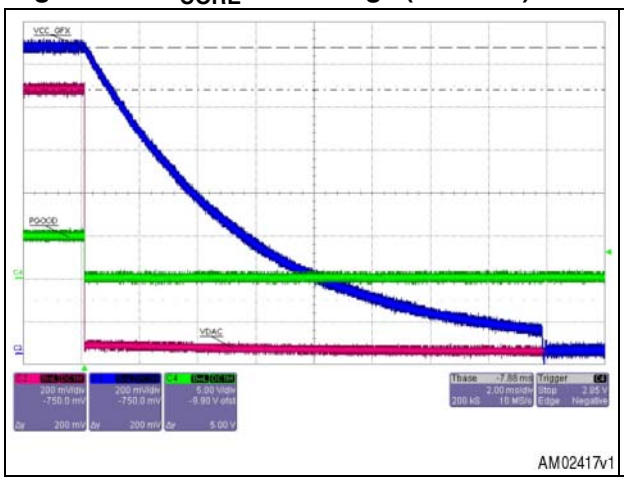


Figure 21. V_{CORE} undervoltage (-300 mV)

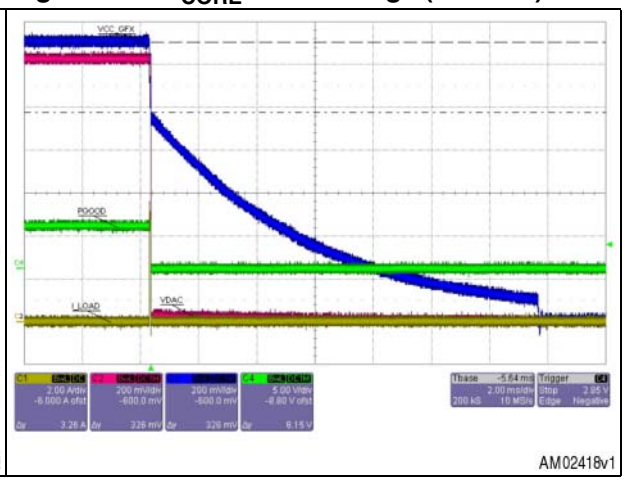


Figure 22. V_{CORE} efficiency (DPRSLPVR high and low)

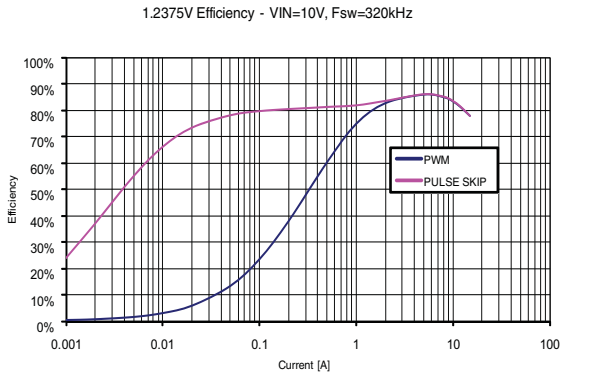
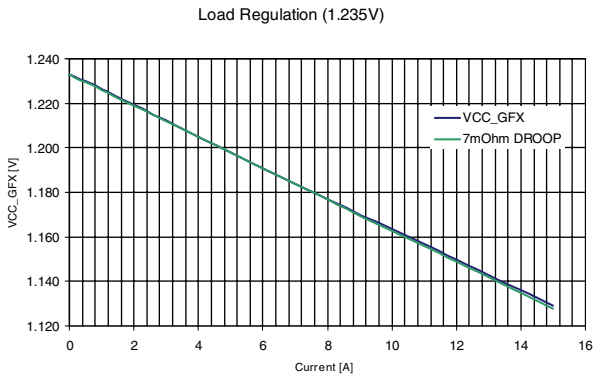
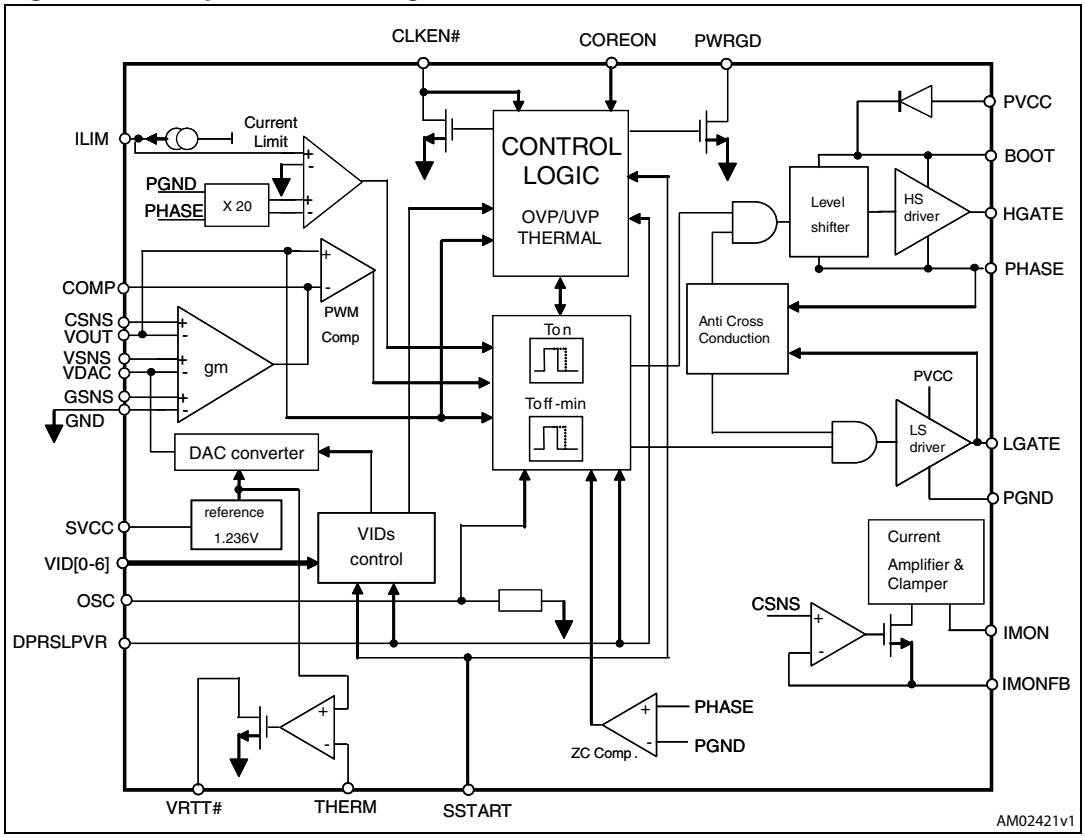


Figure 23. V_{CORE} load regulation - droop function



7 Block diagram

Figure 24. Simplified block diagram



8 Device description

The PM6652 is a single-phase, step-down controller which can be easily configured to regulate power to IMPV6.5 and VR11 devices, as listed below:

- The graphics (Render) core of the Intel® mobile Arrandale processor used on the Calpella platform
- The low voltage and ultra low voltage mobile CPU, used on the Calpella platform
- The VR11 compliant CPU, like Intel® ATOM 200/300 and Pineview-D CPU.

The supply mode and platform compliance are selected by acting on two multi-function pins (refer to *Section 8.2: Mode selection* for details), before the device turn-on.

The PM6652 is based on constant on-time control architecture. This type of control offers a very fast load transient response with a minimum external component count. A typical application circuit is shown in *Figure 1*. The controller includes a 7-bit digital-to-analog converter (DAC) that provides a reference voltage according to the VID pin settings (see *Table 6* and *Table 7*). The PM6652 also allows the adjusting of an active load line (or droop) control, proportional to the inductor DCR or dedicated precision resistor, according to IMVP6.5 specifications.

The switching frequency can be programmed in the range 200 kHz up to 600 kHz with an external resistor connected to the input voltage (see *Section 8.1: Constant on-time PWM control* for details).

In order to maximize the efficiency at very light load, a pulse-skipping control algorithm is performed. The PM6652 is also fully compliant with the fast and slow render suspend state exit mode, as required by IMVP 6.5 spec. for render core supply (see *Section 8.6: Voltage dynamic (VID) transitions* for details).

The device provides protection for overvoltage, undervoltage, overcurrent and overtemperature as well as power good (PWRGD), current monitor (IMON) and thermal throttling (VRTT#) signals for monitoring purposes. The clock enable output signal (CLKEN#), for appropriate platform power-up, is available in CPU supply mode only.

8.1 Constant on-time PWM control

The PM6652 controller uses a pseudo-fixed frequency, constant on-time (COT) controller as the core of the switching section. The COT controller uses a relatively simple algorithm, exploiting the ripple voltage due to inductor resistance DCR (or due to a sense resistor R_{SNS}) to trigger the fixed on-time one-shot generator.

Nearly constant switching frequency is achieved by the system loop in steady-state operating conditions, therefore avoiding the need for a clock generator. A slight switching frequency variation towards the load is the consequence of the switching regulator power losses, which implies the off-time duration decrease.

The on-time one-shot duration is directly proportional to the output voltage, sensed at the VOUT pin, and inversely proportional to the input voltage, sensed at the VOSC pin, as follows:

Equation 1

$$T_{ON} = K_{OSC} \frac{V_{OUT}}{V_{OSC}} + \tau$$

where K_{OSC} is a constant value (140 ns typ.) and τ is the internal propagation delay (40 ns typ.).

This leads to a nearly constant switching frequency, regardless of input and output voltages.

When the output voltage goes lower than the internal programmed voltage (see *Section 8.5: Droop function* for details), the on-time one-shot generator directly drives the high-side MOSFET for a fixed on-time, allowing the inductor current to increase; after the on-time, an off-time phase, in which the low-side MOSFET is turned on, follows.

If the DPRSLPVR control pin is set low, the low-side MOSFET is turned off only when the output voltage becomes lower than the programmed value again, and a new cycle begins. In this working mode the switching frequency is almost load independent, as shown below. Refer to *Section 8.4: Differential remote sensing* section for details about the light load, high-efficiency algorithm.

The duty cycle of the buck converter, in steady-state conditions, is given by:

Equation 2

$$D = \frac{V_{OUT}}{V_{IN}}$$

The switching frequency is therefore calculated as:

Equation 3

$$f_{SW} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{OSC} \frac{V_{OUT}}{V_{OSC}} + \tau} \cong \alpha_{OSC} \cdot \frac{1}{K_{OSC}}$$

where:

Equation 4

$$\alpha_{OSC} = \frac{V_{OSC}}{V_{IN}} = \frac{R_{INT}}{R_{INT} + R_{OSC}}$$

can be set by varying the external resistor R_{OSC}, placed between the VIN and VOSC pin. R_{INT} is the integrated switching frequency programming resistor (typ. 17 kΩ).

The resulting switching frequency is theoretically independent from battery and output voltage; actually the conduction losses due to MOSFET ON-resistance, inductor DCR and PCB traces can slightly influence the programmed value.

8.1.1 Constant on-time PWM architecture

Figure 24 shows the simplified block diagram of a constant on-time controller. A minimum off-time constraint (250 ns typ.) is introduced to allow inductor valley current sensing on the synchronous switch. A minimum on-time (70 ns) is also introduced to assure the startup switching sequence.

The PM6652 has a one-shot generator that turns on the high-side MOSFET when the following conditions are satisfied simultaneously:

- The PWM comparator is high
- The synchronous rectifier current is below the current limit threshold
- The minimum off-time has timed out.

Once the on-time has timed out, the high-side switch is turned off, while the synchronous switch is turned on, according to the anti-cross conduction circuitry management.

When the negative input voltage at the PWM comparator reaches the valley limit (determined by the output voltage), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

8.1.2 Output ripple compensation

In a classic constant on-time control, the system regulates the valley value of the output voltage and not the average value. In this condition, the half of the output voltage ripple is the equivalent DC static error.

To compensate this error, an integrator network has been introduced in the control loop, by connecting the CSNS pin to the COMP pin through a capacitor C_{INT} as shown in *Figure 25*. The ripple is generated by the output capacitor ESR and by the voltage drop on the sense resistor R_{SENSE} (inductor's DCR or dedicated sense resistor). Assuming that R_{OUT} is the cumulative output capacitors' ESR, C_{OUT} is the cumulative output capacitance and G_M is an internal parameter (Gm = 50 µs typ.), the loop stability requires that the C_{INT} value is:

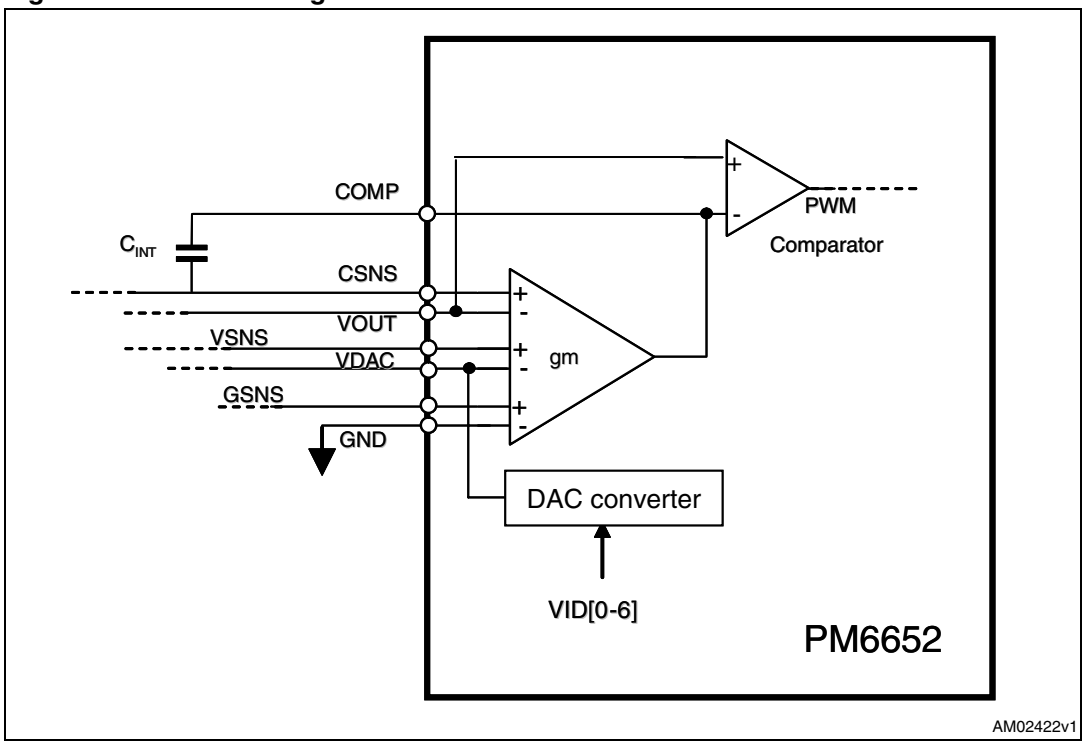
Equation 5

$$C_{INT} \geq g_M \cdot C_{OUT} \cdot R_{OUT}$$

The integrator amplifier generates a current, proportional to the DC input error, which sets the output voltage in order to compensate the total static error. In this way the DC output voltage value is independent of the output ripple, ensuring a very good line and load regulation.

In addition, C_{INT} provides an AC path for the R_{SENSE} voltage ripple. In steady-state condition, the voltage at COMP pin is the sum of the output voltage and the output ripple.

Figure 25. PM6652 integrator



8.2 Mode selection

The PM6652 has two multifunction pins which allow the selection of the supply mode of operation. There are three different modes, as shown in *Table 8*.

Table 8. PM6652 mode of operation selection

Feature	Mode of operation		
	GFX render IMVP6.5	**CPU core IMVP6.5**	**CPU core VR11**
VDAC Table	*Table 6*	*Table 6*	*Table 7 on page 18*
VOUT minimum voltage slew-rate	5 mV/µs, DPRSLPVR=LOW 10 mV/ìs, when DPRSLPVR=HIGH (render suspend fast exit mode)	5 mV/µs	10 mVµs
VBOOT voltage	Not required. See *Section 8.8: Soft-start and soft-end* for details.	1.1 V	1.1 V
CLKEN#	Not used. connect to 5 V.	Output required	Not used. connect to SGND.
Soft-start slew-rate	Programmable by ext. cap.	Fixed, 5 mV/µs minimum	Programmable by ext. cap.

8.3 Pulse-skip working mode

The PM6652 can obtain very high efficiency at light load if the low-side MOSFET is turned off when the inductor current becomes equal to zero. This feature is performed by the zero-crossing comparator (see the internal block diagram, *Figure 24*). In CPU and VR11 mode this feature is activated by asserting the DPRSLPVR pin. In GFX render mode the DPRSLPVR assertion implies also that the V_{DAC} minimum slew-rate is 10 mV/µs, for increasing the programmed output voltage, as required by IMPV6.5 specifications for render suspend fast exit mode (refer to *Section 8.6: Voltage dynamic (VID) transitions* for details).

8.4 Differential remote sensing

The PM6652 performs a differential remote sensing, between the VSNS and GSNS pins. The error between the sensed output voltage and the programmed one (VSNS - VDAC) and between the remote ground and local one (GSNS - GND) are the other two inputs of the integrator, as shown in *Figure 25*. The differential remote sense must be directly connected to the mobile processor differential feedback pins; only two catch resistors (100 Ω) are allowed to avoid any VR output voltage runaway, due to a lack of negative feedback when the processor is not mounted.

8.5 Droop function

In order to reduce the output capacitance amount, the PM6652 performs a load dependent behavior. The voltage sensed between pins CSNS and V_{OUT} is proportional to the load current:

Equation 6

$$C_{SNS} - V_{OUT} = R_{SNS} \cdot I_{LOAD}$$

Given the network shown in *Figure 25*, the resulting regulated output voltage is:

Equation 7

$$V_{CORE\_SS} - V_{GND\_SS} = V_{DAC} - \left(1 + \frac{R_2}{R_1}\right) \cdot R_{SNS} \cdot I_{LOAD}$$

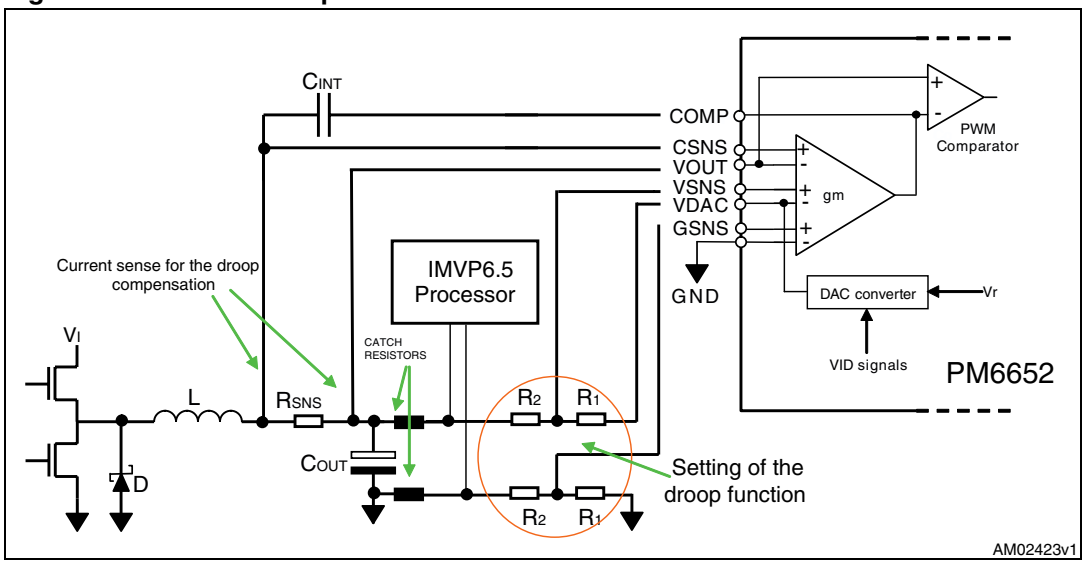
From the previous equation the equivalent droop resistance performed by the switching regulator is:

Equation 8

$$R_{DROOP} = \left(1 + \frac{R_2}{R_1}\right) \cdot R_{SNS} = G_D \cdot R_{SNS}$$

The sense resistor can be a dedicated precision resistor or the inductor's DCR as explained in *Section 8.7: Current sensing*.

Figure 26. PM6652 droop function



8.6 Voltage dynamic (VID) transitions

The integrated 7-bit digital-to-analog converter (DAC) can change its output voltage, with a 12.5 mV step, following *Table 6* and *Table 7*. After a VID change, the converter starts an internal bit rolling in order to ramp up (or ramp down) the V_{DAC} output with a minimum voltage slew-rate, as declared in *Table 8*. During this time and for a blanking time (typ. 30 µs) after the transition, the undervoltage and the variable overvoltage protections are disabled.

Given the previously described control loop, the switching regulator output always tracks the V_{DAC} reference, with the same voltage slew-rate.

Figure 27. GFX supply - VID step, skip mode

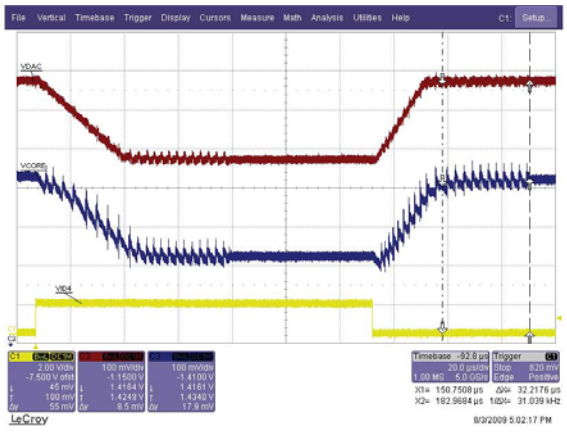
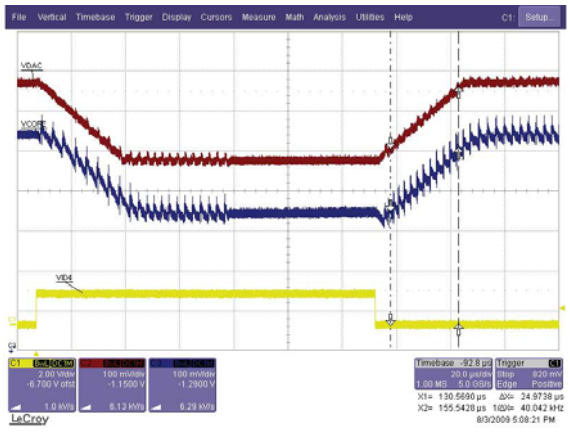


Figure 28. CPU IMVP6.5 - VID step, skip mode



In GFX render IMVP6.5 mode, if the DPRSLPVR control signal is asserted (DPRSLPVR = SVCC) the render suspend state is entered, enabling the pulse-skipping control mode. This high efficiency algorithm allows the low-side MOSFET to turn off when the inductor's current is zero; therefore the switching frequency becomes fully load-dependent, ensuring a very

high efficiency at light load. *Figure 8* and *Figure 11* show the inductor current waveform when the DPRSLPVR pin is asserted high or low.

When the DPRSLPVR control pin is still asserted high and the V_{DAC} ramp-up transition is requested, the render suspend fast exit is performed, by increasing the V_{DAC} output with a minimum voltage slew-rate of 10 mV//µs (*Figure 26*).

If the DPRSLPVR signal is de-asserted before any VIDs change, the V_{DAC} ramp-up transition is performed with a minimum voltage slew-rate of 5 mV/µs (render suspend slow exit).

In CPU IMVP6.5 and VR11 mode the minimum voltage slew-rate is fixed, as reported in *Table 8*, and the DPRSLPVR control signal, when asserted high, directly activates the pulse-skipping algorithm for higher light load efficiency.

8.7 Current sensing

Figure 29. Precision resistor current sensing

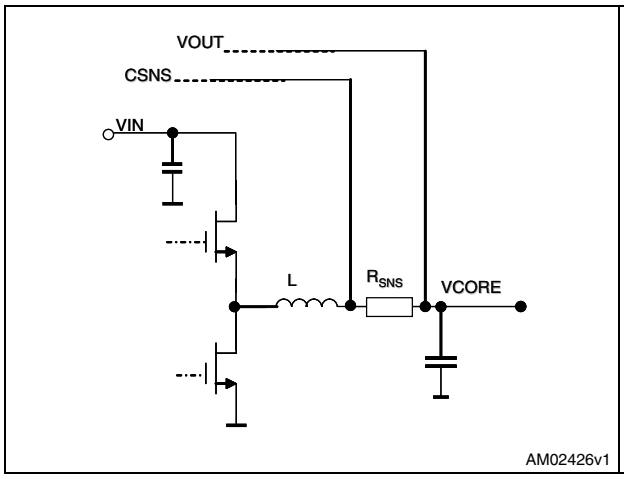
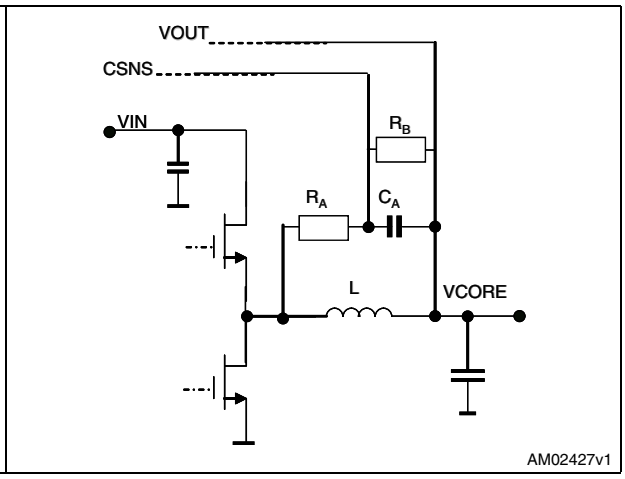


Figure 30. Inductor's DCR current sensing



As reported in *Equation 9* the voltage sensed between the CSNS and VOUT pins must be proportional to the output current. Two main techniques can be used: the precision RSNS resistor and the inductor's DCR current sensing (*Figure 29* and *Figure 30*). The first method is more precise and more expensive, since a dedicated precision component must be selected; on the other hand, the inductor's current sensing technique is cheaper but it's based on the parasitic inductor resistance whose accuracy is hardly lower than 10%. An R_S-C_S filter matched with the inductor's time constant is also required. If the inductor's DCR value is greater than the required droop an additional R_B resistor is necessary. In this case, the sensed current as suggested by *Equation 9* becomes:

Equation 9

$$C_{SNS} - V_{OUT} = \frac{R_B}{R_B + R_A} \cdot R_{DCR} \cdot I_{LOAD} \cdot \frac{1 + \frac{sL}{R_{DCR}}}{1 + s \cdot \tau_A}$$

$$\tau_A = R_A // R_B \cdot C_A$$

The previous equation also shows the frequency dependence of the DCR current sensing technique. During load variation the sensed DCR can also increase, if the time constant matching is not adequate; in order to avoid this situation the following equation must be verified:

Equation 10

$$\tau_A \geq \frac{L}{R_{DCR}} = \tau_L$$

Figure 31 shows the V_{CORE} load transient response when *Equation 10* is not verified whereas in *Figure 32* the load transient response shows a better time constant matching.

Figure 31. $\tau_L > \tau_C$

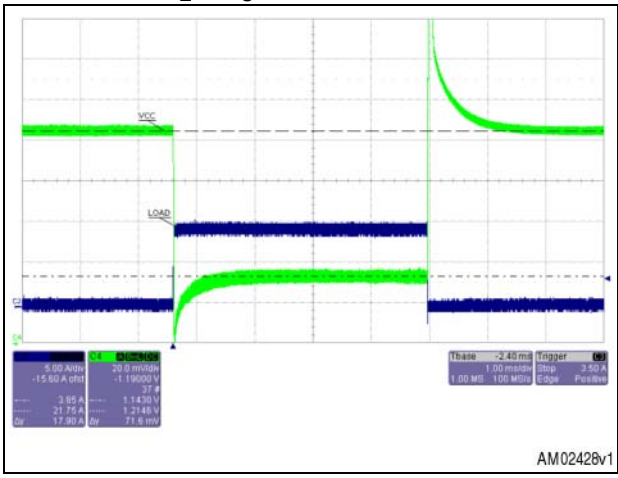
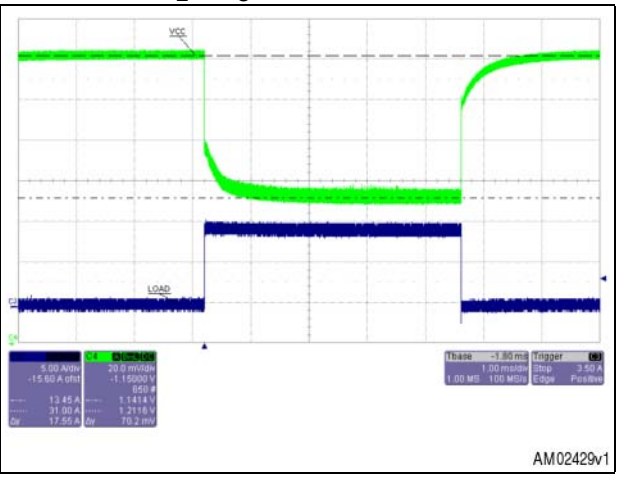


Figure 32. $\tau_L < \tau_C$



If a thermal compensation is required in order to compensate for the inductor's DCR variation, due to a temperature increase, RB is replaced by a complete network, based on an NTC (negative temperature coefficient) thermistor (Rn). *Figure 33* shows an example of an NTC-based thermal compensation network (Rs, Rp and Rn). The resulting RB1 equivalent resistance and NTC network attenuation are:

Equation 11

$$R_{B1}(T) = R_S + R_P // R_N(T)$$
$$G_{NTC} = \frac{R_{B1}}{R_{B1} + R_A}$$

and the time constant due to the CA capacitor may be computed as follows:

Equation 12

$$\tau_A = C_A \cdot (R_A // R_{B1})$$

In the PM6652 the CSNS and VOUT inputs are high-impedance pins so a very small leakage current can be measured, in the range of 50 nA to 100 nA. This leakage current, sourced by CSNS, is multiplied by the equivalent resistance measured across the CA

capacitor, i.e. RA//RB1, and the resulting voltage drop is found on the V_{CORE} output voltage, in agreement with *Equation 7*.

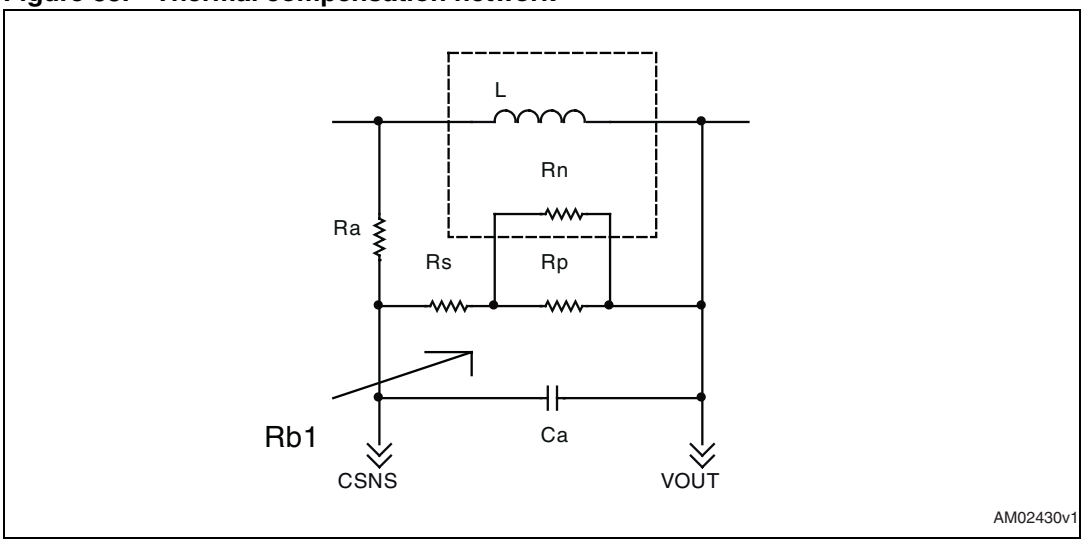
Equation 13

$$V_{LKG} = I_{LKG} \cdot R_A // R_{B1}$$

The result is an output voltage drop also at no load.

In order to avoid this no load voltage drop condition, the current sensing filter equivalent resistance, i.e. RA//RB1, should fall in the range of 1 kΩ -10 kΩ

Figure 33. Thermal compensation network



8.8 Soft-start and soft-end

The DAC voltage slew-rate at startup can be decreased, in order to limit the inrush current, in GFX and VR11 supply mode. A soft-start capacitor C_{SS} placed between the SSTART pin and SGND is charged and discharged with 50 µA (only at startup). The resulting soft-start capacitor voltage variation is exploited by the internal DAC to ramp up to the VIDs programmed value (in GFX mode) or to the VBOOT default voltage (in VR11 mode), with 12.5 mV steps. *Figure 36* shows the soft-start V_{DAC} voltage slew-rate vs. CSS capacitance.

If the SSTART pin is connected to SVCC, the V_{DAC} ramp-up (and V_{OUT} output voltage too) is performed with a minimum 5 mV/µs voltage slew-rate. This function is performed in CPU IMVP6.5 mode only.

Figure 34 and *Figure 35* show the different soft-start mechanism for GFX mode and CPU mode, assuming the following typical values for timing:

- TON = 350 µs
- TSTART depends on the soft-start programmed slew-rate and voltage; for CPU mode, the soft-start slew-rate is 6.25 mV/µs (typ.) and VBOOT = 1.1 V, so TSTART = 176 µs typ
- TBOOT = 70 µs
- TPG = 4 ms.

In CPU and VR11 mode the soft-start programmed voltage is VBOOT; the output voltage is driven to the VIDs programmed voltage value only after TBOOT delay. When the VR11 mode is selected the CLKEN# signal is not used as the output but only as the input pin. Refer to *Section 8.2* section for details.

Figure 34. IMVP6.5 GFX mode startup

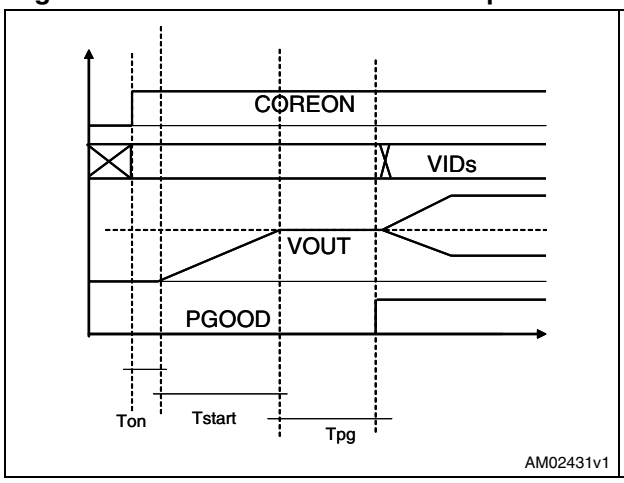


Figure 35. IMPV6.5 CPU mode startup

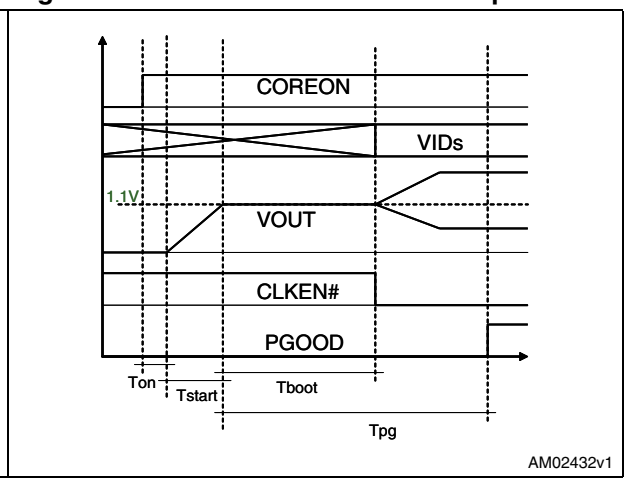
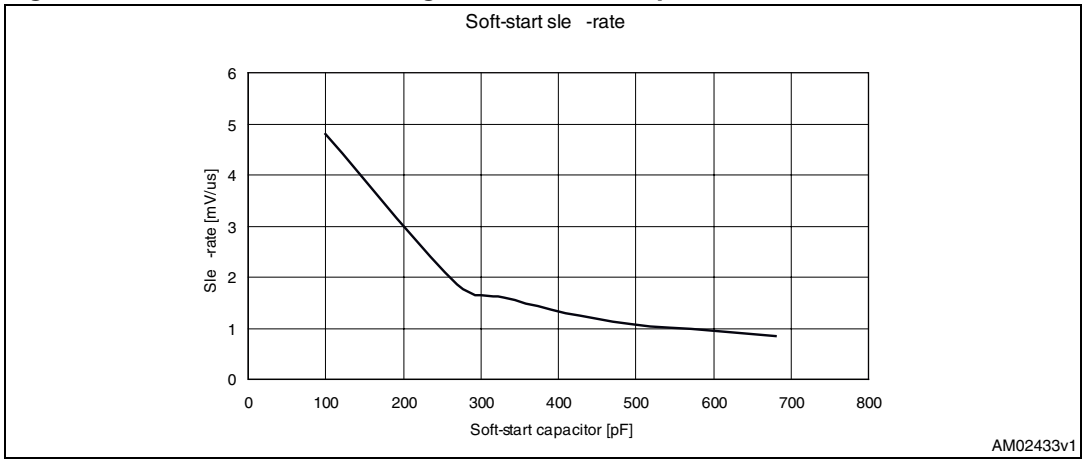


Figure 6 and *Figure 7* show the different turn-on behavior for GFX mode and CPU/VR11 mode.

When the COREON control pin is pulled down or the shut-down VIDs sequence is selected, VID[0,...,6]=[1111111], the turn-off sequence is performed. In order to avoid the output voltage going under ground, the output capacitor is discharged through a dedicated 7 Ω (typ.) internal discharge MOSFET, connected between the VOUT and SGND pins. When V_{OUT} voltage is lower than 100 mV the low-side external MOSFET is turned on. See *Figure 18* and *Figure 19* for the soft-end waveform details.

Figure 36. VDAC soft-start voltage slew-rate vs. capacitor value



8.9 Internal MOS drivers

The integrated high-current gate drivers allow different Power MOSFETs to be used.

The high-side driver, which is supplied by the +5 V rail, uses a bootstrap circuit with integrated boot diode. Only one external ceramic capacitor (100 nF or bigger) is required. The BOOT and PHASE pins work respectively as supply and return path for the high-side driver, while the low-side driver is directly fed through the PVCC and PGND pins.

An important feature of the PM6652 gate drivers is the adaptive anti-cross-conduction circuitry, which prevents high-side and low-side MOSFETs from being turned on at the same time. When the high-side MOSFET is turned off, the voltage at the PHASE node begins to fall. The low-side MOSFET is turned on only when the voltage at the PHASE node reaches an internal threshold in the range of 2.5 V to 1 V. Similarly, when the low-side MOSFET is turned off, the high-side one remains off until the LGATE pin voltage is above 0.8 V (typical value).

8.10 Monitoring and protection

8.10.1 Power good

The power good signal is an open drain output which requires an external pull-up resistor.

When V_{OUT} is lower than 300 mV or higher than 200 mV with respect to V_{DAC}, or when the COREON pin is de-asserted, the PWRGD pin is immediately forced low.

At startup, the PWRGD pin is allowed to rise only 4 ms after the V_{DAC} programmed value is reached, as shown in *Figure 6*, *Figure 34* and *Figure 35*.

8.10.2 Current monitor (IMON)

The voltage sensed between the CSNS and VOUT pins is mirrored across the RG external resistor (between IMONFB and VOUT pins) and the resulting current is multiplied by the current monitor block gain.

The typical gain value is:

Equation 14

$$G_{IMON,INT} = 3$$

The current monitor gain can be adjusted by choosing R_{IMON}, as shown in *Figure 39*, in order to program the required V_{IMON} at maximum load. The total IMON gain becomes:

Equation 15

$$\frac{V_{IMON}}{CSNS - VOUT} = G_{IMON,INT} \cdot \frac{R_{IMON}}{R_G}$$

$G_{IMON,INT}$=3 is a fixed internal parameter. The minimum suggested value for RG is equal to 400 Ω with maximum allowable IMONFB current lower than about I_{MAX} = 40 µA (typ.).

A good range for RG choice is [0.68 kΩ; 7 kΩ] with a maximum CSNS-VOUT voltage up to 60 mV.

If the current sourced by the IMONFB pin is greater than I_{MAX} for more than 4 ms (typ.) the average current limit fault is detected and the IC latches off: the MOS drivers are put in high impedance and the internal discharge MOSFET is turned on (see *Figure 37*). A COREON or SVCC toggle is required in order to restart the device.

Every time the IMONFB pin current becomes lower than I_{MAX}, the internal timer is reset (see *Figure 38*); as a consequence the inductor current which can cause the average current limit fault is given by:

Equation 16

$$i_{AVCL} = I_{OUT,AVCL} - \Delta I_L \geq \frac{I_{MAX} \cdot R_G}{R_{DCR}}$$

Figure 37. Average current limit - recovery

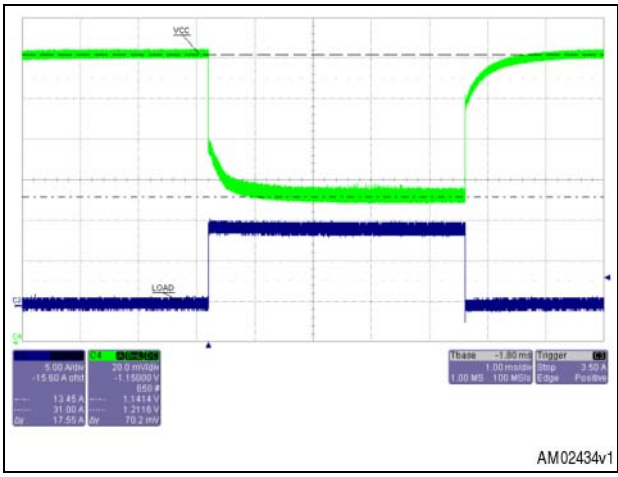
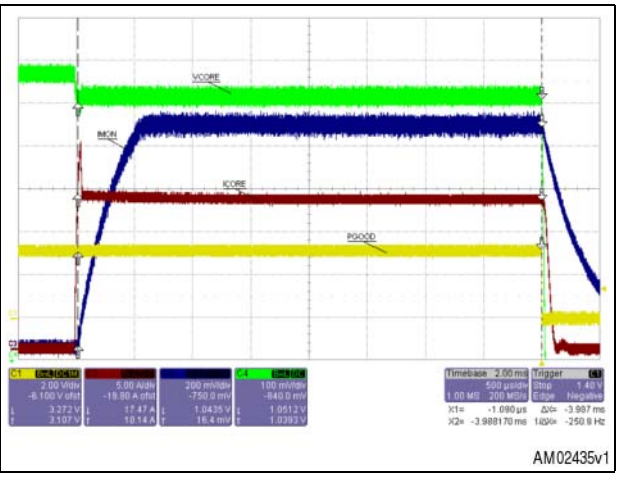


Figure 38. Average current limit detected



In order to set the right average current limit threshold, the PM6652 internal parameters and also external component accuracy must be considered.

A complete equation for the average current limit threshold worst case variation is:

Equation 17

$$\frac{\delta I_{AVCL,WC}}{I_{AVCL}} = \left(\frac{\delta R_G}{R_G}\right) + (\alpha_{IMAX}) + \left(\frac{V_{IMON,off}}{G_{SNS} \cdot R_{SNS} \cdot I_{AVCL}}\right) + \left(\frac{\delta R_{SNS}}{R_{SNS}}\right) + \left(\frac{\delta G_{SNS}}{G_{SNS}}\right)$$

assuming $\delta R_G/R_G$, the accuracy of R_G, α_{IMAX}<10%, the internal current reference error, $V_{IMON,off}$<1 mV the IMON maximum offset, G_{SNS} the NTC thermal compensation network attenuation (see *Equation 11*), $\delta R_{SNS}/R_{SNS}$ the inductor DCR or precision resistor accuracy and $\delta G_{SNS}/G_{SNS}$ the thermal compensation network gain error, due to NTC and others resistors accuracy (see *Equation 25*). If the thermal compensation network is not used and/or the current sensing filter resistor value is higher than the suggested one (as explained it *Section 8.7: Current sensing*) the previous equation must be modified in order to take into account the DCR thermal drift and current sensing additional offset.

Equation 18

$$\frac{\delta I_{AVCL}}{I_{AVCL}} = \frac{\delta I_{AVCL,WC}}{I_{AVCL}} + \left(\frac{V_{LKG}}{G_{SNS} \cdot R_{SNS} \cdot I_{AVCL}}\right) + \left(\frac{\delta R_{TH}}{R_{SNS}}\right)$$

given δV_{LKG} the voltage drop across the current sensing filter resistor, due to the CSNS pin leakage current (see *Equation 13*) and $\delta R_{TH}/R_{SNS}$ the current sensing element variation due to temperature increase.

If the current monitoring function is not required, IMONFB should be connected to SVCC and IMON can be left floating.

C_{FILT} (*Figure 39*) can be required by the CPU/GPU in order to filter the current monitor ripple due to inductor current ripple.

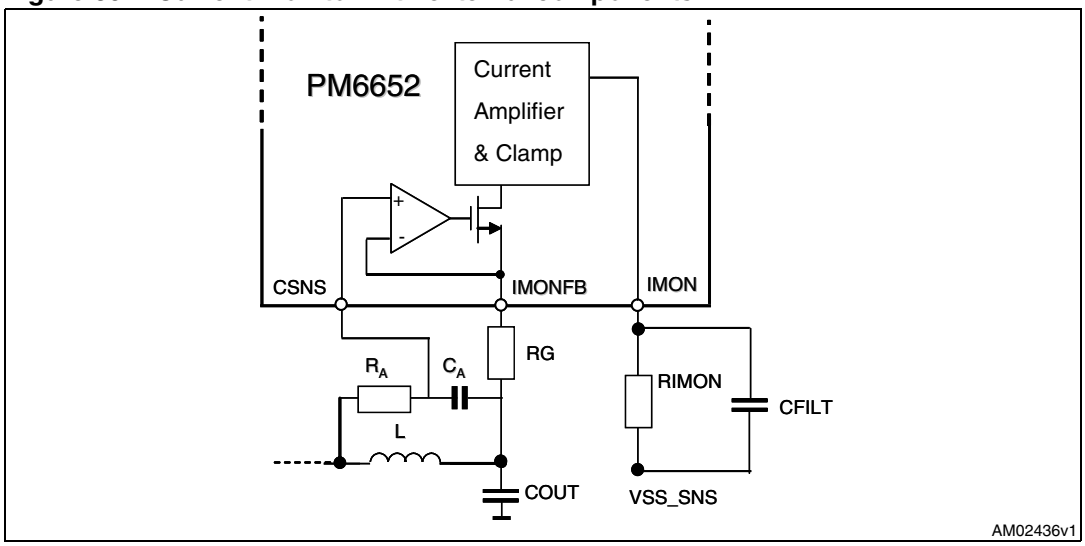
Equation 19

$$C_{FILT} \cdot R_{IMON} \geq \frac{L}{R_{DCR}}$$

A typical value for C_{FILT} is 47 nF or bigger (IMVP6.5 specifications suggest C_{FILT}*R_{IMON}>=300 µs).

The IMON voltage is limited to 1.15 V (maximum value), as required by IMVP6.5 specifications, in order to avoid any damage to the CPU. This feature is performed by limiting the current injected by the PM6652 IMON pin into the R_{IMON} resistor.

Figure 39. Current monitor with external components



8.10.3 Thermal throttling

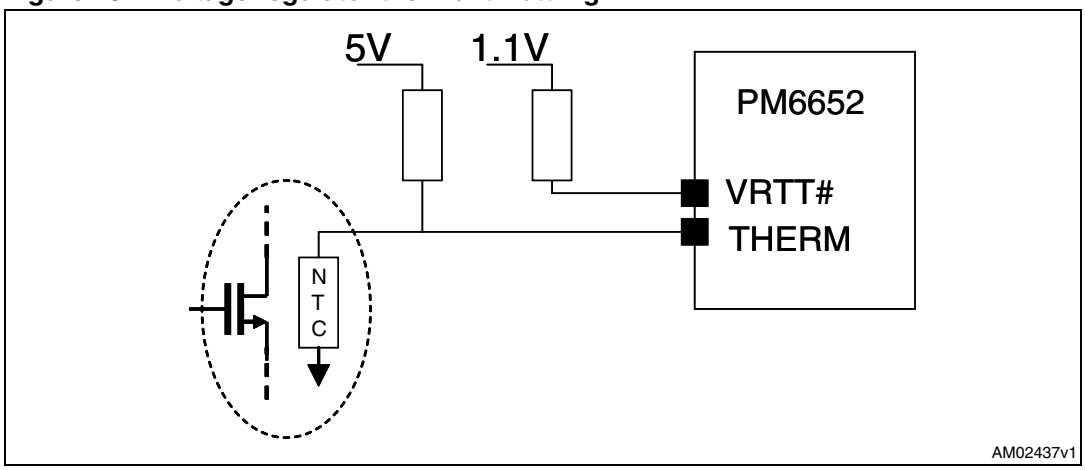
The voltage regulator thermal throttling function is used by the CPU in order to avoid catastrophic thermal damage.

The VRTT# open drain output pin is forced down when the THERM voltage is lower than an internal threshold (1.0 V typ. and 200 mV hysteresis). An external NTC resistor, placed near

the external MOSFET or the inductor, allows the controller to monitor the thermal status of the power components (see *Figure 40*).

In applications where this function is not required (in render core supply, for example) the THERM pin must be connected to 5 V and VRTT# can be left floating.

Figure 40. Voltage regulator thermal throttling



8.10.4 Overvoltage protection

The PM6652 can detect two kinds of V_{OUT} overvoltage:

- Fixed 1.55 V overvoltage threshold
- Variable +200 mV overvoltage threshold, referred to V_{DAC} reference voltage.

Both overvoltage protections are latched, so a COREON or SVCC toggle is required in order to restart the device.

If the fixed overvoltage threshold is reached, the high-side MOSFET is immediately turned off and the output capacitor is sharply discharged by turning on the low-side MOSFET. This fault protection is always active.

When a variable V_{OUT} overvoltage is detected, both high-side and low-side external MOSFETs are turned off and the output capacitor soft-discharge is performed. The internal discharge MOSFET is turned on until V_{OUT} is lower than about 100 mV, then the low-side MOSFET is turned on (see *Figure 20 on page 22*). This fault detection is masked during VID transitions and, during soft-start, until the power good signal is released.

8.10.5 Undervoltage protection

If the switching voltage regulator output falls below -300 mV, referred to V_{DAC} programmed voltage, the latched undervoltage fault is detected and the output capacitor soft-discharge is performed. The internal discharge MOSFET is turned on until VCC_GFX is lower than about 100 mV, then the low-side MOSFET is turned on (see *Figure 21*). This fault detection is masked during VID transitions and, during soft-start, until the power good signal is released.

The undervoltage protection can't be detected if the programmed V_{DAC} voltage is lower than 300 mV.

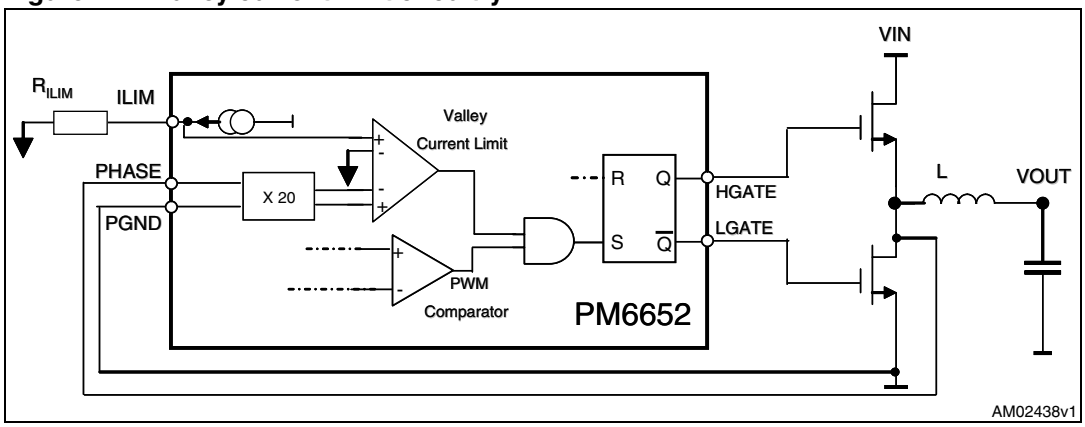
8.10.6 Overcurrent protection

The PM6652 controller can limit the maximum load current by skipping one or more switching cycles if the valley current limit is detected. The current limit sensing is independent from the current sensing for droop and IMON functions. Basically, the voltage drop sensed between the PGND and PHASE pins, when the low-side MOSFET is on, is compared with the voltage across the external R_{ILIM} resistor. The following equation helps to program the valley current limit value (see *Figure 41*):

Equation 20

$$R_{ILIM} \cdot 5\mu A = 20 \cdot (V_{PGND} - V_{PHASE})$$

Figure 41. Valley current limit circuitry



The maximum programmable voltage on pin ILIM is 3.5 V (typ.); as a consequence the maximum effective R_{ILIM} resistor is about 700 kΩ

If, starting from the previous equation, a higher resistance is required the resulting low-side MOSFET ON-resistance is not adequate for the designed application.

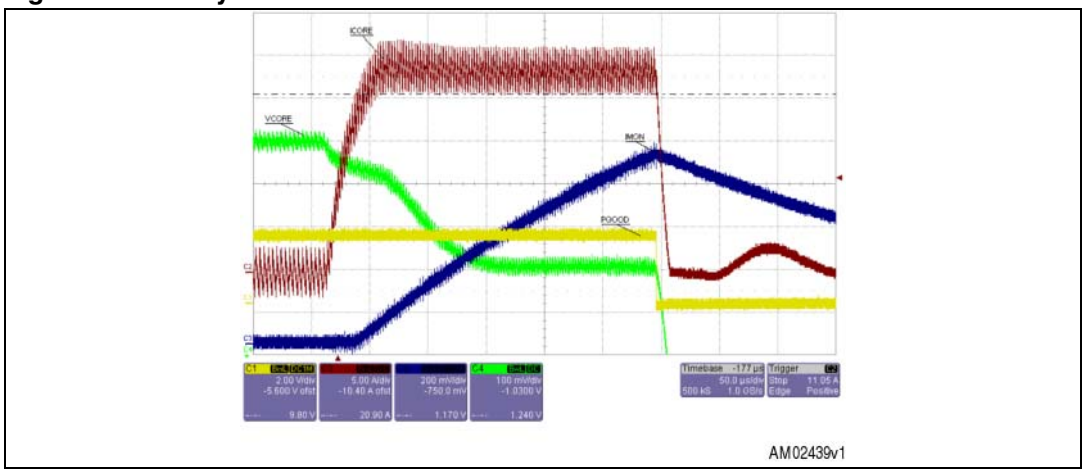
The maximum available load current, with the valley current limit technique, is equal to:

Equation 21

$$I_{LOAD,MAX} = I_{VCL} + \frac{1}{2} \cdot \Delta I_L$$

i.e. the maximum available current is the sum of the valley current limit value plus the half of the inductor current ripple. The valley current limit is sensed each switching cycle, during T_{OFF} time (when the low-side MOSFET is turned on). This fault protection is not latched but the typical behavior is the one shown in *Figure 42*:

Figure 42. Valley current limit detection



If the overload is not removed, the output capacitor keeps discharging until the UV fault is detected.

In order to set the right valley current limit threshold, the PM6652 internal parameters and also external component accuracy must be considered.

A complete computation of the valley current limit threshold worst case variation can be found in *Equation 22*.

Equation 22

$$\frac{\delta I_{L,VALL,WC}}{I_{L,VALL}} > \left(\frac{\delta R_{ILIM}}{R_{ILIM}}\right) + \left(\frac{\delta I_{LIIM}}{I_{LIIM}}\right) + \left(20 \cdot \frac{V_{OFFSET}}{I_{ILIM} \cdot R_{ILIM}}\right) + \left(\frac{\delta R_{DS,ON}}{R_{DS,ON}}\right)$$

The “key parameter” is the low-side MOSFET ON-resistance, $\delta R_{DS,ON}$, which takes into account the maximum ON-resistance value and its thermal drift. The other parameters, with the exception of R_{ILIM} (typical accuracy 1%), are all internal parameters: δI_{ILIM}<0.5 µA is the current reference variation and V_{OFFSET}<4 mV is the current limit comparator offset.

8.10.7 SVCC undervoltage protection

The PM6652 can detect an SVCC undervoltage (threshold 3.9 V typ.). When this fault occurs, the high-side MOSFET is turned off and the low-side MOSFET is turned on. The device is turned on again if the SVCC voltage is higher than 4.4 V (typ.). This fault protection is always active.

8.10.8 Thermal protection

If the device internal temperature is greater than 150 °C, the thermal shutdown is performed. The internal discharge MOSFET is turned on until V_{OUT} is lower than about 100 mV, then the low-side MOSFET is turned on.

A COREON or SVCC toggle is required to turn on again the device. This fault detection is masked during VID transitions and, during soft-start, until the power good signal is released.

8.11 System accuracy

8.11.1 VCORE accuracy

Starting from *Equation 7* and *Equation 9*, the programmed output voltage is given by:

Equation 23

$$V_{CC\_SNS} - V_{SS\_SNS} = V_{DAC} - G_D \cdot G_{SNS} \cdot (R_{SNS} \cdot I_{OUT})$$

- V_{DAC} is the internal reference voltage, i.e. the digital-to-analog converter output programmed by the 7 VIDs
- G_D is the droop gain, given by *Equation 8*
- G_{SNS} is the current sensing filter attenuation. This element is lower than 1 if there is an NTC thermal compensation network, typically used in DCR current sensing technique
- R_{SNS} is the current sensing element, i.e. the inductor DCR or the precision resistor.

The statistical variation of the output voltage is given by the following equation:

Equation 24

$$\delta V_{CORE,STAT} = \sqrt{(\delta V_{DAC})^2 + (G \cdot R_{SNS} \cdot I_{OUT})^2 \cdot \left(\left(\frac{\delta G_D}{G_D} \right)^2 + \left(\frac{\delta G_{SNS}}{G_{SNS}} \right)^2 \right) + (G \cdot I_{OUT} \cdot \delta R_{SNS})^2 + (G_D \cdot \delta V_{OFFSET})^2}$$

$$G = G_D \cdot G_{SNS}$$

- δV_{DAC} is the internal reference voltage error, lower than 0.7% of the programmed VID (refer to *Figure 5*)
- $\delta G_D/G_D$ and $\delta G_{SNS}/G_{SNS}$ are the statistical error of the droop gain and NTC network, if used. These two elements are only influenced by external components
- δR_{SNS} is the current sensing element (inductor's DCR or precision resistor) variation due to its accuracy
- $\delta V_{OFFSET} < 2.5$ mV is the PM6652 integrator maximum offset.

Based on *Equation 7*, the droop gain statistical error is:

Equation 25

$$G_D = 1 + \frac{R_2}{R_1}$$

$$\frac{\delta G_D}{G_D} = \frac{G_D - 1}{G_D} \sqrt{\left(\frac{\delta R_2}{R_2} \right)^2 + \left(\frac{\delta R_1}{R_1} \right)^2}$$

The same mathematical approach provides the following computation, based on *Equation 11*:

Equation 26

$$\frac{\delta G_{SNS}}{G_{SNS}} = (1 - G_{SNS}) \cdot \sqrt{\left(\frac{\delta R_A}{R_A}\right)^2 + \left(\frac{\delta R_{NTC}}{R_{NTC}}\right)^2 + \left(\frac{\delta R_S}{R_S}\right)^2 + \left(\frac{\delta R_P}{R_P}\right)^2}$$

As explained in *Section 8.7: Current sensing*, the current sensing filter, if not properly designed, can impact the overall accuracy. In this case *Equation 22* must be updated:

Equation 27

$$\delta V_{CORE} = \delta V_{CORE,STAT} + |\delta V_{LKG}| + |G \cdot I_{OUT} \cdot \delta R_{TH}|$$

given δV_{LKG} the voltage drop across the current sensing filter resistor, due to the CSNS pin leakage current (*Equation 13*).

Equation 27 also takes account of the sensing element variation due to thermal drift: this element is almost negligible if the NTC thermal compensation network is used.

8.11.2 Current reporting (IMON) accuracy

The current monitor feature (IMON), as described in *Section 8.10.2: Current monitor (IMON)*, has the following design equation:

Equation 28

$$V_{IMON} = G_{INT} \cdot \frac{R_{IMON}}{R_G} \cdot G_{SNS} \cdot R_{SNS} \cdot I_{OUT}$$

- G_{INT} = 3 is the internal fixed gain
- R_{IMON} and RG are external resistors for gain programming
- G_{SNS} is the current sensing filter attenuation
- R_{SNS} is the current sensing element.

The statistical error of the IMON function can be computed:

Equation 29

$$\frac{\delta V_{IMON,STAT}}{V_{IMON}} = \sqrt{\left(\frac{\delta R_{SNS}}{R_{RSNS}}\right)^2 + \left(\frac{\delta R_G}{R_{RG}}\right)^2 + \left(\frac{\delta R_{IMON}}{R_{IMON}}\right)^2 + \left(\frac{\delta G_{INT}}{G_{INT}}\right)^2 + \left(\frac{V_{IMON,off}}{G_{SNS} \cdot R_{SNS} \cdot I_{OUT}}\right)^2 + \left(\frac{\delta G_{SNS}}{G_{SNS}}\right)^2}$$

$\delta R_{SNS}/R_{SNS}$ is the current sensing element accuracy;

$\delta R_{IMON}/R_{IMON}$ and $\delta R_G/R_G$ are the external resistors accuracy;

$\delta G_{INT}/G_{INT}$ < 1% is the internal fixed gain error;

$V_{IMON,OFF}$ < 1 mV is the IMON maximum input offset;

$\delta G_{SNS}/G_{SNS}$ is the current sensing filter error (refer to *Equation 26* for details).

The IMON accuracy can be influenced by a not properly designed current sensing filter (as explained in *Section 8.7: Current sensing*) and by the current sensing element thermal drift, as summarized in *Equation 30*:

Equation 30

$$\frac{\delta V_{IMON}}{V_{IMON}} = \frac{\delta V_{IMON,STAT}}{V_{IMON}} + \left|\frac{V_{LKG}}{G_{SNS} \cdot R_{SNS} \cdot I_L}\right| + \left|\frac{\delta R_{TH}}{R_{SNS}}\right|$$

given δV_{LKG} the voltage drop across the current sensing filter resistor, due to the CSNS pin leakage current (see *Equation 13*).

9 Application ideas

9.1 Load transient response improvement with feedback capacitor

Referring to *Figure 2*, the droop gain network made by R14, R15, R17 and R18 can be improved by adding the feedback capacitor C34. As a consequence, the performed load line previously summarized in *Equation 8* is now described in *Equation 31* below:

Equation 31

$$R_{DROOP}(s) = G_D(s) \cdot R_{SNS}(s) = \left(1 + \frac{R_{17}}{R_{14}}\right) \cdot \left(\frac{1 + s \cdot C_{34} \cdot R_{17} // R_{14}}{1 + s \cdot C_{34} \cdot R_{17}}\right) \cdot R_{SNS}(s)$$

The sensed current information is still given by:

Equation 32

$$C_{SNS} - V_{OUT} = \frac{R_B}{R_A + R_B} \cdot R_{DCR} \cdot \frac{1 + \frac{sL}{R_{DCR}}}{1 + s \cdot R_A // R_B \cdot C_{15}} \cdot i_L(s) = R_{SNS}(s) \cdot i_L(s)$$

$$R_A = R_{31}$$

$$R_B = R_{33} + R_{34}$$

By joining the two previous results, the complete droop equation becomes:

Equation 33

$$R_{DROOP} = \left(1 + \frac{R_{17}}{R_{14}}\right) \cdot \frac{R_B}{R_A + R_B} \cdot R_{DCR} \cdot \frac{1 + s \cdot C_{34} \cdot R_{17} // R_{14}}{1 + s \cdot C_{34} \cdot R_{17}} \cdot \frac{1 + \frac{sL}{R_{DCR}}}{1 + s \cdot C_{15} \cdot R_A // R_B}$$

In order to get an almost flat droop function, from DC to high frequency, and a “squared” load transient response, the above equation requires two conditions:

- $C_{34}*R_{17}=L/R_{DCR}$
- $C_{34}*R_{17}//R_{14}=C_{15}*R_A//R_B$

If $R_{17}>R_{14}$ (typical application), $C_{15}*R_A//R_B< L/R_{DCR}$ so the high frequency sensed current is bigger compared to what can be sensed when the feedback capacitor is not mounted. This feature can be very helpful when low DCR inductors are used and the sensed current ripple, CSNS-V_{OUT}, is lower than about 10 mV_{PP}.

In order to avoid any output voltage undershoots during load transient, the above mentioned conditions should be translated into:

- $C_{34}*R_{17}\geq L/R_{DCR}$
- $C_{15}*R_A//R_B\geq C_{34}*R_{17}//R_{14}$

The two components used to fine tune the load transient response are C_{34} and C_{15}, since the other components are fixed when the droop is programmed and the inductor has already been selected.

The following waveforms provide a “visual” approach useful to understand the relationship between the load transient response and the two capacitance values.

Figure 43. C15 good and C34 OK

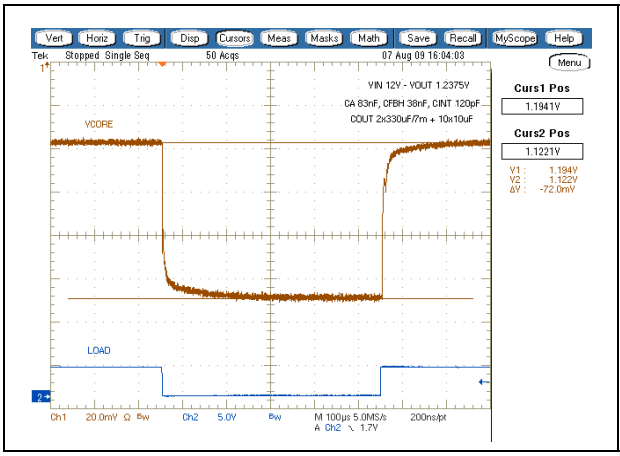


Figure 44. C15 big and C34 OK

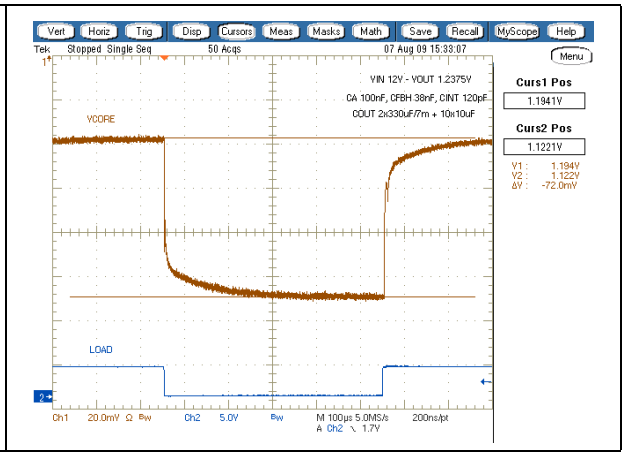


Figure 45. C15 small and C34 OK

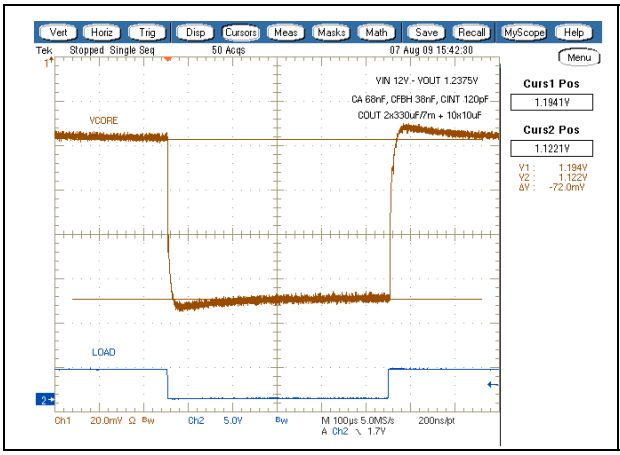


Figure 46. C15 good and C34 small

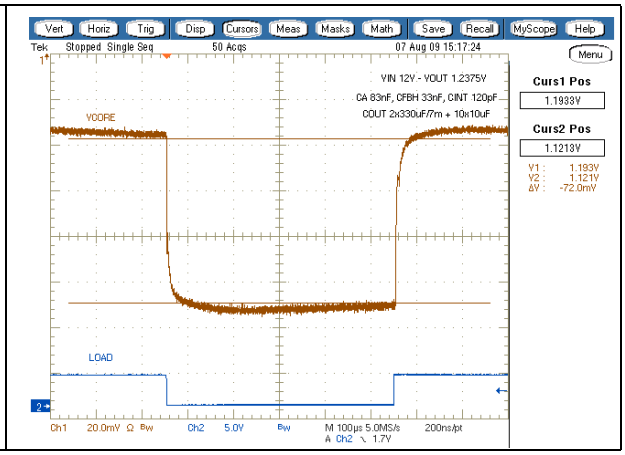


Figure 47. C15 good and C34 big

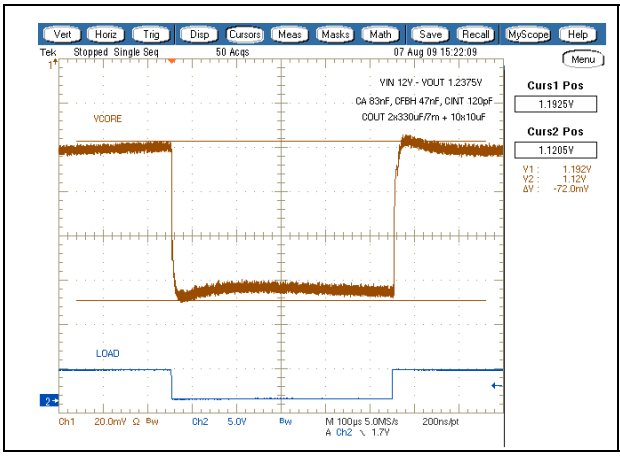
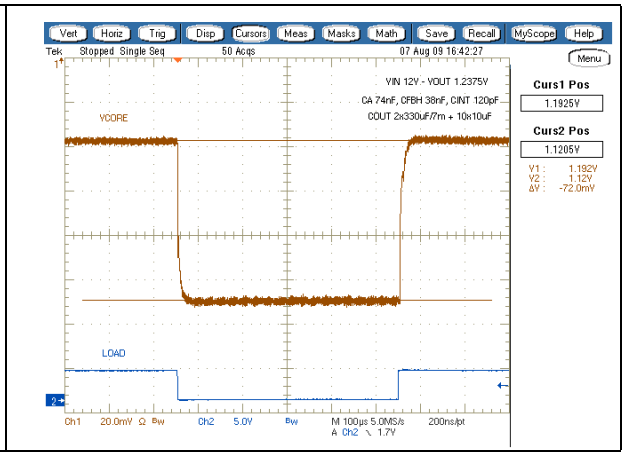


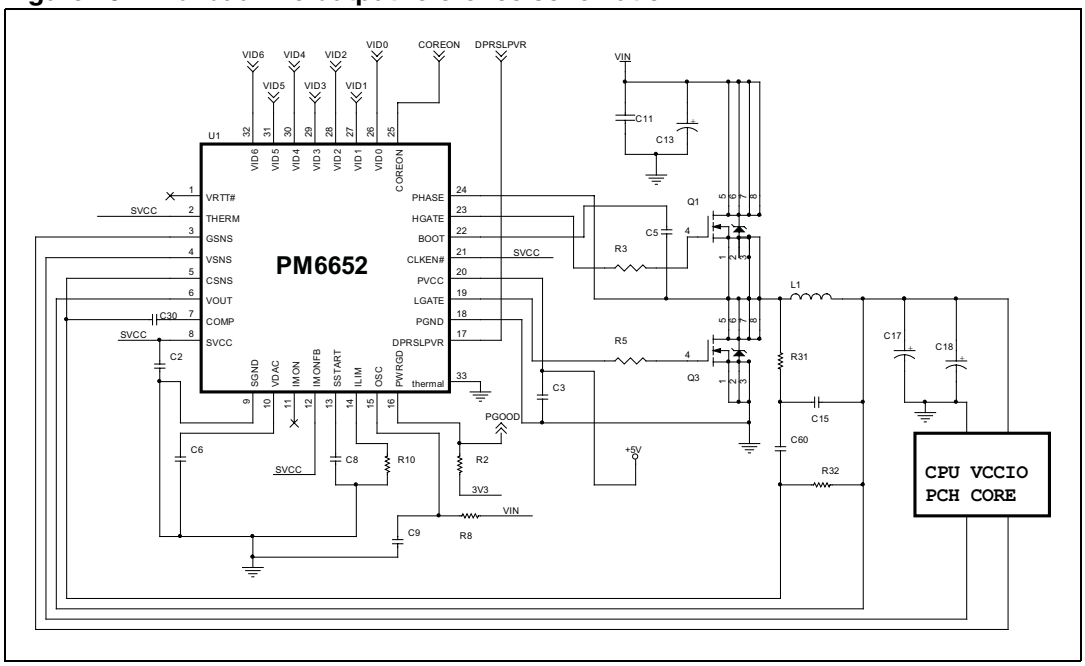
Figure 48. C15 OK and C34 OK



9.2 Voltage regulation without droop

PM6652 can be suitable also for high current DC-DC conversion requiring high precision load regulation and no load line function.

Figure 49. No load line output reference schematic



In *Figure 49* the typical current sensing filter (R31, C15) has been modified by adding C60 and R32, in order to disable the load line (or droop) function.

The switching regulator AC behavior is not affected by C60-R32 insertion if the following design rules are followed:

- C60<<C15
- C15*R31=L1/R_{DCR}
- $1/(2*\pi*R32*C60)$<<fsw
- R32 value should fall in the range 1 kΩ ÷ 10 kΩ, as suggested in *Section 8.7: Current sensing*.

With the modified current sensing filter the output voltage load regulation is almost independent of the output load, taking full advantage of the differential remote feedback. In fact *Equation 9* now becomes:

Equation 34

$$C_{SNS} - V_{OUT} = R_{DCR} \cdot i_L(s) \cdot \frac{1 + \frac{sL_1}{R_{DCR}}}{1 + s \cdot C_{15} \cdot R_{31}} \cdot \frac{s}{\frac{1}{C_{60}R_{32}} + s}$$

The previous result shows that the DC sensed current is zero; as a consequence, the DC output voltage is given by:

Equation 35

$$V_{CORE\_SS} - V_{GND\_SS} = V_{DAC}$$

If C60 is used in the current sensing network the IMON function and the average current limit feature are not available, since the DC sensed current is almost equal to zero (see *Section 8.10.2: Current monitor (IMON)* for details).

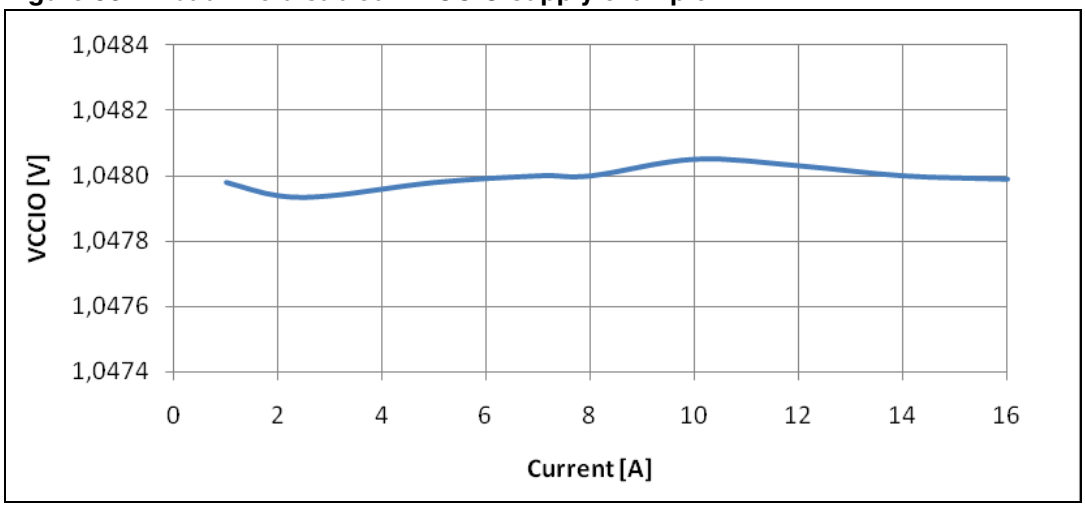
This application idea has been verified for IMVP7 VCCIO and PCH core supply, 1.05 V rail.

The 1.05 V rail is required to provide up to 16 A, with 8 A load transient in 150 ns. The following setup has been tested:

- Output capacitor: 4x330 µF/6 mΩ + 8x10 µF/X5R
- Inductor: 0.5 µH/26.9 ARMS/0.86 mΩ
- C15=100 nF; C60=3.3 nF; R31=R32=3.3 kΩ; C30=100 pF; R8=300 kΩ

The DC and AC performances have been evaluated.

Figure 50. Load line disabled – VCCIO supply example



The measured output voltage is almost constant in the full load range, with a maximum drift lower than 0.2 mV.

The output voltage ripple is close to 17 mV peak-to-peak, from 1 A to 16 A output load.

Figure 51. VCCIO output voltage ripple (1 A)

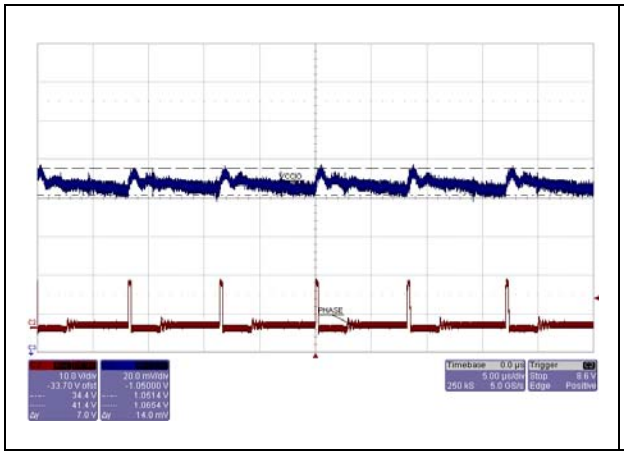
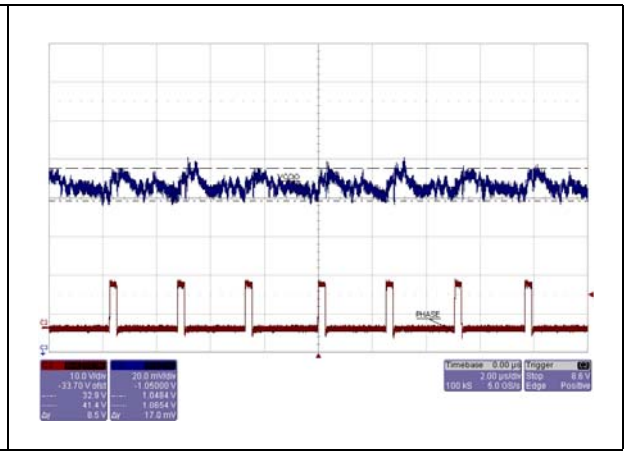


Figure 52. VCCIO output voltage ripple (16 A)



A few waveforms show the AC behavior during load transient (from 8 A to 16 A, in 150 ns), with different load transient frequency.

Figure 53. Load transient response - 5 kHz

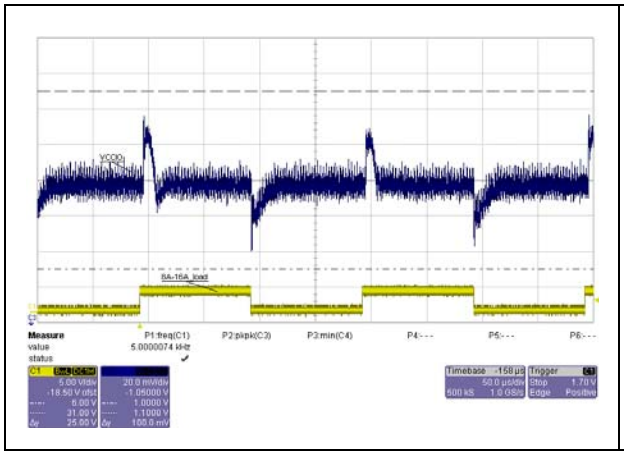


Figure 54. Load transient response - 40 kHz

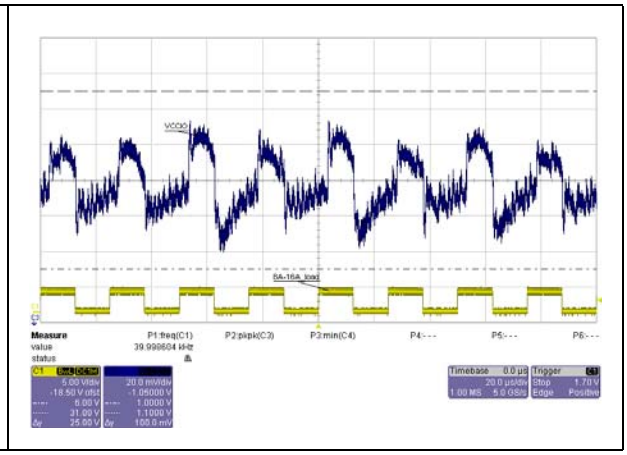


Figure 55. Load transient response - 100 kHz

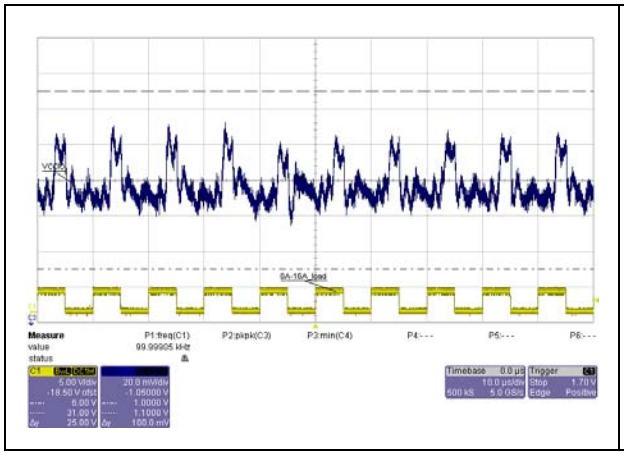
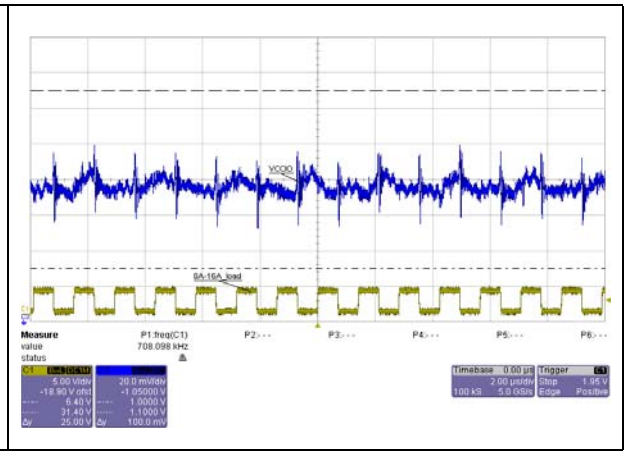


Figure 56. Load transient response - 300 kHz



10 Layout guidelines

The PM6652 has two separate grounds: PGND, the power ground, and SGND, the reference for IC internal circuitry. A 2-separate-grounds layout is based on the following guidelines:

- Design an analog/signal ground plane on one inner layer, connect this area to SGND and exposed pad (trough some vias)
- Design one power ground plane on one internal layer. Connect the SGND (signal ground) plane and PGND plane in one point (e.g. under the exposed pad or near the low-side MOSFET source). If the PGND plane and SGND plane are in different layers, use at least 2 vias for the connection. It is recommended not to use a resistor to connect the PGND plane and SGND plane.

Alternatively, a single ground PCB can be designed, taking into account the following suggestions (refer to *Figure 1*):

- Design one power ground plane on one internal layer
- Connect all the components referred to SGND (R15, C2, C6, C8, R10, C9) with a dedicated trace, then connect this trace to SGND (pin 9) and to the IC thermal pad
- Connect the IC thermal pad directly to the power ground, through some vias.

Other suggestions for a good layout follow:

- GSNS, VSNS: Route the remote feedback sensing nets coupled (7 mils separation) and 18 mils wide. Keep 25 mils separation from other signals (this is an Intel suggestion)
- CSNS, VOUT: Keep the current sensing signals directly from the current sensing element terminals (inductor pads, for DCR sensing, or precision resistor pads). Place the L-DCR filter, if required, near the inductor and route the current sensing nets coupled and far from noisy nets. Place the NTC thermistor, if required, as close as possible to the inductor. Use the GND/SGND plane for shielding
- IMON, IMONFB: Keep far from switching traces (use, if necessary, the GND/SGND plane for shielding) and place the output R-C filter close to the CPU
- LGATE, HGATE, PHASE: Design trace width > 20 mils and as short as possible (avoid using vias if possible). Keep the ratio 3 mils_width/100 mils_lenght even for traces longer than 500 mils (e.g. trace length: 2000 mils. design a trace width of about 60 mils). Keep far from signal traces to avoid noise coupling on signal traces. Place the gate resistor near the MOSFET gate
- BOOT: Place the ceramic capacitor close to the BOOT pin and PHASE pin; the trace must be > 20 mils and the spacing with another signal trace > 20 mils. Minimize the length of the loop between the PHASE pin and BOOT pin. Use at least 3 vias if a layer change is required
- SVCC, PVCC: Place the capacitor close to the SVCC/PVCC pin. Design trace width >= 20 mils. SVCC is internally connected to PVCC through a few Ω resistor (3 Ω typ.) so SVCC doesn't need to be externally connected to +5 V rail.

11 Package mechanical data

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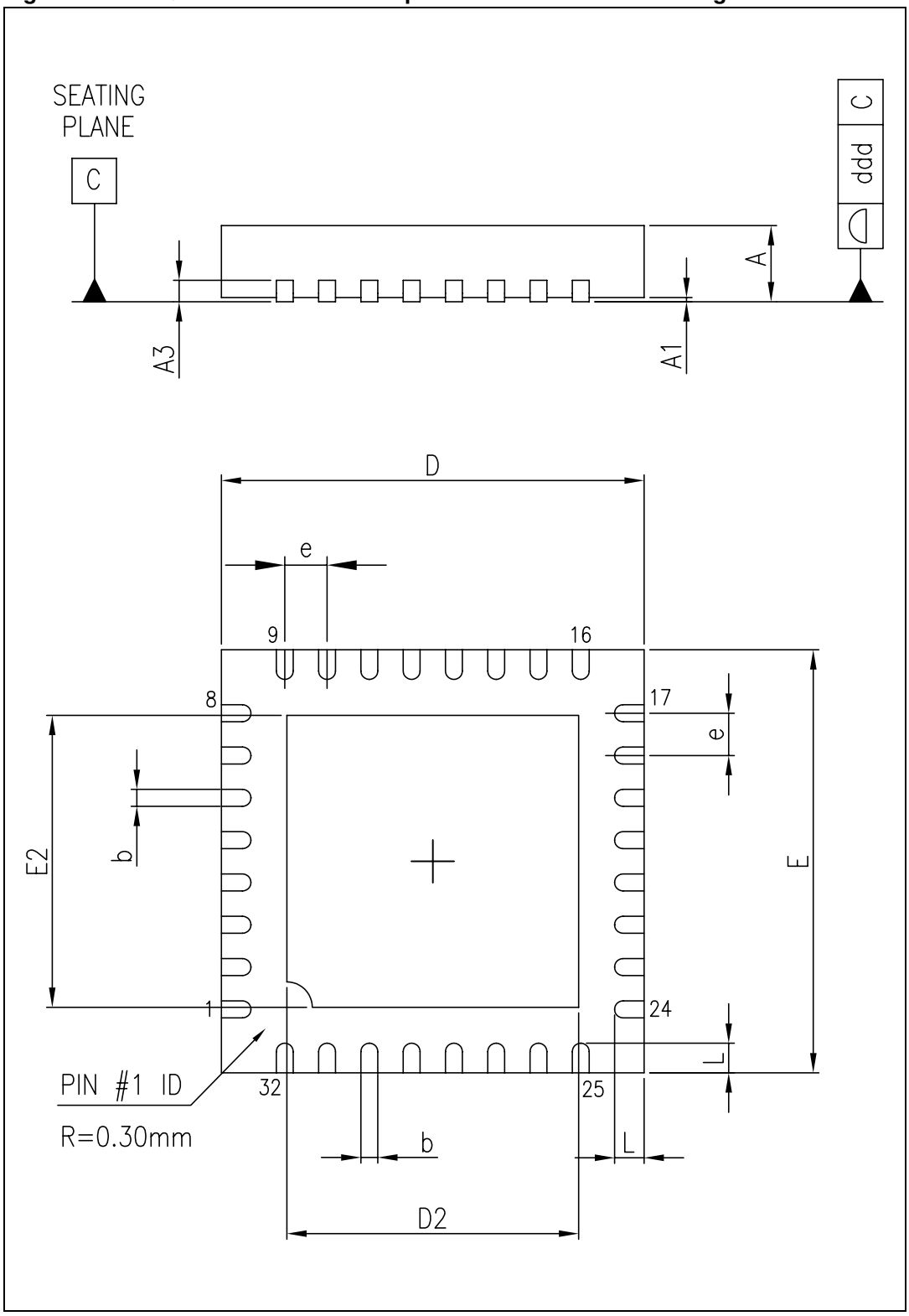
Table 9. VFQFPN 5x5x1.0 mm 32L pitch 0.50 mechanical data

Dim.	(mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	4.85	5.00	5.15
D2 (1)	2.90	3.10	3.20
E	4.85	5.00	5.15
E2 (2)	2.90	3.10	3.20
e		0.50	
L	0.30	0.40	0.50
ddd			0.05

1. Dimensions D2 and E2 are not in accordance with JEDEC.

Note: VFQFPN stands for thermally enhanced very thin fine pitch quad flat package no lead. Very thin: A = 1.00 mm max.

Figure 57. VFQFPN 5x5x1.0 mm 32L pitch 0.50 mechanical drawing



12 Revision history

Table 10. Document revision history

Date	Revision	Changes
04-Dec-2009	1	Initial release
28-Jan-2010	2	Updated cover page, *Table 2 on page 11*, *Table 4 on page 12* and *Section 8 on page 25* Added *Figure 2 on page 7* and *Figure 3 on page 8*
26-May-2010	3	Added *Section 9: Application ideas on page 44*
01-Feb-2012	4	Updated *Figure 22 on page 23*.
09-Mar-2012	5	New update of *Figure 22 on page 23*.

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