AP-680

APPLICATION NOTE

Multi-Source Solution for Intel® 28Fxx0B3 Advanced Boot Block and AMD* AM29LVxxxx

October 2001

NOTE: This document formerly known as *Multi-Source Solution for Intel® 28F160B3 Advanced Boot Block and AMD 29LV160.*

Order Number: 297876-004

CONTENTS

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 5937
Denver, CO 80217-9808

or call 1-800-879-4725
or visit Intel's Website at http://www.intel.com/design/flash

CG-041493

REVISION HISTORY

Date of Revision	Version	Description
10/28/97	-001	Original Version
12/02/97	-002	Updated 4-Mbit-package information Section 3.1.
12/01/98	-003	Major wording revision Added a description of 12 V Production Programming and In-System Hardware Block Locking Added a description of memory blocking differences Name of document changed from *Multi-Source Solution for Intel® 28F160 Advanced Boot Block and AMD 29LV160* technical paper
08/21/01	-004	Major wording revision Added new pin out diagram with Am29LV800, 160, 320 & 641 devices.
10/08/01	-005	Major wording revision

1.0 INTRODUCTION

This application note outlines how to design a single socket to support the Intel® 3-Volt Advanced Boot Block (B3) and the AMD* AM29LVxxx (LV) flash memory devices. For the sake of simplicity, only the Top-Boot-type devices are explained here. All considerations noted would be valid in a Bottom-Boot design as well. Please also see *AP-657 Designing with the Advanced+ Boot Block Flash Memory Architecture*. Section 2 defines the advantages in designing with the B3, while Section 3 presents a single-socket, multi-source solution.

2.0 Intel 3-VOLT ADVANCED BOOT BLOCK OVERVIEW

The Intel B3 products are available in 4-, 8-, 16-, 32-, and 64-Mbit densities. All are designed for low-voltage (2.7V – 3.6V core) applications requiring code execution and data storage within the same flash devices. The B3 series consists of eight 4-Kword blocks, either at the top address range (Top Boot), or bottom address ranges (Bottom Boot), followed by a number of 32-Kword blocks, depending on density. Please see the *3-Volt Advanced Boot Block Flash Memory* datasheet for details.

In addition, the Intel B3 offers the following advantages when designing a multi-source solution:

- Complete density pinout compatibility for an easy and less expensive upgrade path
- 1.65-2.5V or 2.7-3.6V output range levels
- 12-Volt Production Programming for fast programming during manufacturing
- Low voltage in-system hardware block locking
- Program Suspend functionality for real time applications
- Flash Data Integrator (FDI) software, plus a vast array of Intel® Memory Managers and design tools to reduce time to market

The following sections describe these features and advantages in more detail. Table 1 compares features offered by the B3 and the LV.

2.1 Pinout Compatibility

The B3 products provide density upgrades with complete pinout compatibility from 4-, 8-, 16-, 32-, and 64-Mbit densities:

- The 48-ball µBGA* CSP package—ideal for space constrained designs—is available in 8-, 16-, and 32-Mbit densities
- The 48-lead TSOP is available in 8-, 16-, 32-, and 64-Mbit densities for x16 functionality.

Pinout and package compatibility are extremely important for applications that may change their code or data requirements. Designing for compatibility reduces the impact of re-spinning the board and lengthens the application lifetime. To accommodate changing requirements, the design should be optimized for the highest density flash device available, and use the density that is required for the present design. Note that vfBGA and uBGA packages require a complete trace redesign because pin placement and pitch differences are not compatible.

2.2 12-Volt Production Programming

The Intel B3 products support production programming at 12V to significantly reduce programming time in a manufacturing line. This easily can be combined with 2.7V – 3.6V in-system programming. Please refer to *the 3-Volt Advanced Boot Block Flash Memory* datasheet for details.

2.3 In-System Hardware Block Locking

The B3 offers in-system hardware block locking for the lower two 8-Kbyte-parameter blocks for Bottom Boot, and upper 2 blocks on the Top-Boot devices. In-system block locking is possible by applying GND to WP# to lock the blocks, or V_{ih} (min) to WP# to unlock the blocks.

Am29LV800B, Am29LV160D, and Am29LV320D devices require an algorithm that uses 8.5V - 12.5V levels on either the #RESET or A9/#OE pins to change locking.

Additionally, when Vpp = GND, the entire device is write protected. Am29LV800B, Am29LV160D, and Am29LV320D devices do not separate the program/erase supply from the core power supply.

2.4 Program-Suspend to Read Functionality

The Intel B3 offers enhanced Program Suspend capabilities. While both the B3 and the LV offer Erase-Suspend to program or read, only B3 offers Program-Suspends to a read. This functionality can be important for real-time applications that require critical data within the maximum program time (which may be as large as 100 µs).

2.5 Memory Managers and Design Tools from Intel

Intel offers several flash memory managers to reduce design time and offer quicker time-to-market solutions including the following:

The **Intel® Flash Data Integrator (FDI)** software can be used for code plus data real-time solutions. The **Intel® VSB (Virtual Small Block) File Manager** VFM can be used for simple embedded file data storage applications.

Intel also offers a range of flash memory tools for every stage of system development that enable shorter development schedules with lower development costs.

For more information on software, refer to the Intel Flash website at: http://developer.intel.com/design/flash.

Table 1. Feature Comparison Between Intel B3 and LV

Feature	Intel 800/160/320/640 B3	AMD LV800B/160/320D/641D
12-Volt Production Programming	8 µs word write	11 µs word write
Lower voltage I/Os	1.65 V – 2.5 V or 2.7 V - 3.6 V	2.7 V- 3.6 V 1.8 V – 2.9 V (Am29LV641D only)
In-system hardware block locking	2.7 V – 3.6 V in system	Requires 8.5-12.5 V in system (except for Am29LV641D) *** note**
Program-Suspend to read	Yes	No
Erase-Suspend to read	Yes	Yes
Erase-Suspend to program	Yes	Yes

- See AMD Spec *22367*

3.0 DEVELOPING MULTI-SOURCED DESIGNS

This section describes the changes required to design a multi-source socket solution for the x16 B3 and LV. Similar methodologies may be applied for other densities.

Please note differences in these areas:

- Pinouts
- Blocking
- Command sets
- Timing notes

AC Specification Differences Related to Address/Data Latching

From a generic standpoint, Read and Write timing is very similar. See the specific datasheet on the particular density required for exact details.

3.2 Pinout Differences

Figure 1 shows the 48-lead TSOP pin-out differences between the B3 and the LV. Lower densities will have NC (No Connects) on the upper address pins. For example, a 16-Mbit device will have NC on Pins 9 and 10.

NCs are not bonded to the die and have no physical connection.

Pins 15 and 47 require special attention on Am29LV800B, Am29LV160D, and Am29LV320D. Note that the 28F640B3 is a direct pin-pin replacement for the Am29LV0641D

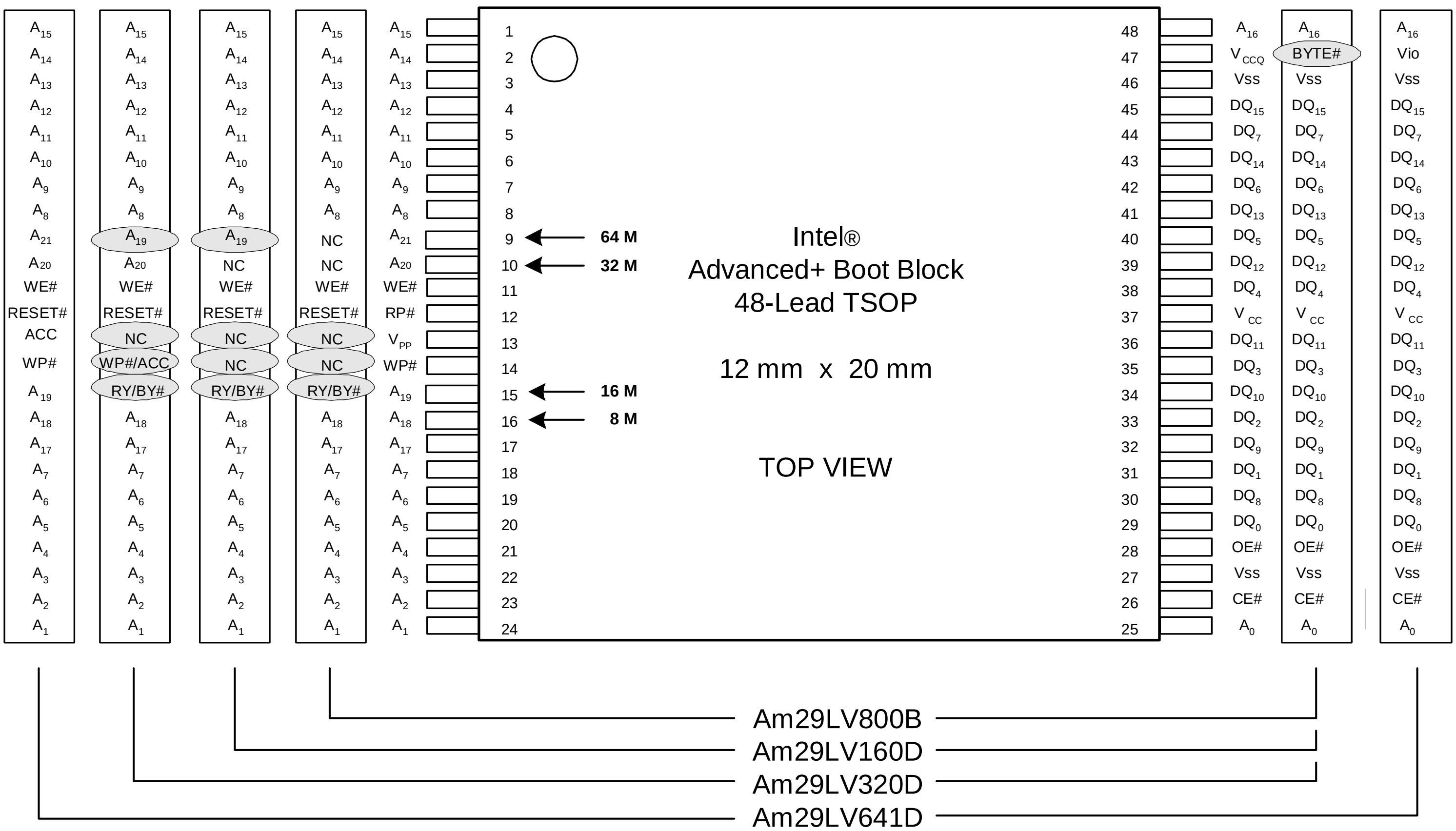

Figure 1. Comparison of 28FxxxB3 Advanced Boot Block 48-Lead TSOP Pinout Versus AMD 29LVxx

Table 2. Comparison of Intel and AMD 48-Lead TSOP Pinout

Pin	Intel	AMD* LV800B/ 160D / 320D	Replacement Issue
9	NC	A_{19} (Address 19)	No
13	V_{PP}	NC	No
14	WP#	NC, WP#/ACC	No
15	A_{19} (Address 19)	RY/BY#	Yes
47	V_{CCQ} (I/O voltage)	BYTE#	Must be between 2.7 V – 3.6 V multi-source solutions

Pin 15 on Intel B3 is the input address A_{19}. On the Am29LV800B, Am29LV160D, and Am29LV320D, Pin 15 is the RY/BY# pin, an open-drain output. This change will cause bus contention if not properly handled. Figure 2 provides a design method to alleviate this concern using a simple 10 KΩ resistor.

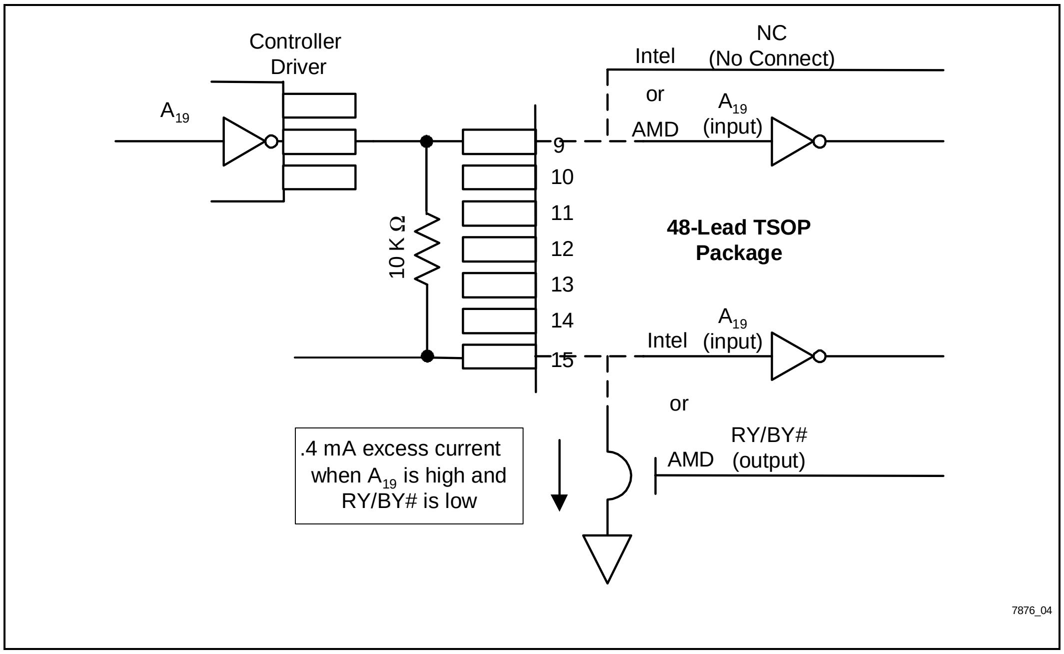

Figure 2. A Resistor Solution for Address A_{19} (Intel) and RY/BY# (AMD)

Pin 47 is the I/O supply pin on Intel B3, V_{CCQ}. However on the Am29LV800B, Am29LV160D, and Am29LV320D, it is the BYTE# pin. For an x16 multi-source design, both must be between 2.7V – 3.6V. The lower voltage (1.65V –

2.5V) I/O capability in Am29LV800B, Am29LV160D, and Am29LV320D is not supported.

3.3 Blocking

Intel B3 devices are designed with eight 4-Kword parameter blocks; the remainder of the array is divided into 32-Kword blocks. AM29LV800B, AM29LV160D, and AM29LV320D devices are designed with 8-Kword, two 4-Kword, and 16-Kword parameter blocks, with the remainder of the array divided into 32-Kword blocks (see Table Example). Note that the Am29LV800B, Am29LV160D, and Am29LV320D blocking is a subset of the B3 blocking (except for Am29LV0641D). Although the blocking architectures are similar, software must account for these parameter-block differences. For example, when erasing the one 16-Kword block of the LV device, four 4-Kword blocks must be erased on the B3 to account for the same address range. Note that the Am29LV0641D only has symmetrical blocks that are 32 Kwords in size.

Example: 16M-Bit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	INTEL B3	Size (KW)	LV	Size (KW)	LV	Size (KW)	INTEL B3
4	FF000-FFFFF	8	FE000-FFFFF	32	F8000-FFFFF	32	F8000-FFFFF
4	FE000-FEFFF			32	F0000-F7FFF	32	F0000-F7FFF
4	FD000-FDFFF	4	FD000-FDFFF	32	E8000-EFFFF	32	E8000-EFFFF
4	FC000-FCFFF	4	FC000-FCFFF	32	E0000-E7FFF	32	E0000-E7FFF
4	FB000-FBFFF	16	F8000-FBFFF	32	D8000-DFFFF	32	D8000-DFFFF
4	FA000-FAFFF			32	D0000-D7FFF	32	D0000-D7FFF
4	F9000-F9FFF			32	C8000-CFFFF	32	C8000-CFFFF
4	F8000-F8FFF			32	C0000-C7FFF	32	C0000-C7FFF
32	F0000-F7FFF	32	F0000-F7FFF	32	B8000-BFFFF	32	B8000-BFFFF
32	E8000-EFFFF	32	E8000-EFFFF	32	B0000-B7FFF	32	B0000-B7FFF
32	E0000-E7FFF	32	E0000-E7FFF	32	A8000-AFFFF	32	A8000-AFFFF
32	D8000-DFFFF	32	D8000-DFFFF	32	A0000-A7FFF	32	A0000-A7FFF
32	D0000-D7FFF	32	D0000-D7FFF	32	98000-9FFFF	32	98000-9FFFF
32	C8000-CFFFF	32	C8000-CFFFF	32	90000-97FFF	32	90000-97FFF
32	C0000-C7FFF	32	C0000-C7FFF	32	88000-8FFFF	32	88000-8FFFF
32	B8000-BFFFF	32	B8000-BFFFF	32	80000-87FFF	32	80000-87FFF
32	B0000-B7FFF	32	B0000-B7FFF	32	78000-7FFFF	32	78000-7FFFF
32	A8000-AFFFF	32	A8000-AFFFF	32	70000-77FFF	32	70000-77FFF
32	A0000-A7FFF	32	A0000-A7FFF	32	68000-6FFFF	32	68000-6FFFF
32	98000-9FFFF	32	98000-9FFFF	32	60000-67FFF	32	60000-67FFF
32	90000-97FFF	32	90000-97FFF	32	58000-5FFFF	32	58000-5FFFF
32	88000-8FFFF	32	88000-8FFFF	32	50000-57FFF	32	50000-57FFF
32	80000-87FFF	32	80000-87FFF	32	48000-4FFFF	32	48000-4FFFF
32	78000-7FFFF	32	78000-7FFFF	32	40000-47FFF	32	40000-47FFF
32	70000-77FFF	32	70000-77FFF	32	38000-3FFFF	32	38000-3FFFF
32	68000-6FFFF	32	68000-6FFFF	32	30000-37FFF	32	30000-37FFF
32	60000-67FFF	32	60000-67FFF	32	28000-2FFFF	32	28000-2FFFF
32	58000-5FFFF	32	58000-5FFFF	32	20000-27FFF	32	20000-27FFF
32	50000-57FFF	32	50000-57FFF	32	18000-1FFFF	32	18000-1FFFF

32	48000-4FFFF	32	48000-4FFFF	32	10000-17FFF	32	10000-17FFF
32	40000-47FFF	32	40000-47FFF	32	08000-0FFFF	32	08000-0FFFF
32	38000-3FFFF	32	38000-3FFFF	16	04000-07FFF	4	07000-07FFF
32	30000-37FFF	32	30000-37FFF			4	06000-06FFF
32	28000-2FFFF	32	28000-2FFFF			4	05000-05FFF
32	20000-27FFF	32	20000-27FFF			4	04000-04FFF
32	18000-1FFFF	32	18000-1FFFF	4	03000-03FFF	4	03000-03FFF
32	10000-17FFF	32	10000-17FFF	4	02000-02FFF	4	02000-02FFF
32	08000-0FFFF	32	08000-0FFFF	8	00000-01FFF	4	01000-01FFF
32	00000-0FFFF	32	00000-07FFF			4	00000-00FFF

3.4 Command Sets

Command sets are different between the Intel B3 and all AMD LV devices. The B3 commands are 2-cycle commands, whereas LV commands vary between 2 and 6 cycles. Table 3 shows common command sequence differences between the B3 and the LV devices. To determine which command set to use in an application, the algorithm in Figure 3 can be used to identify which device is in the application through the use of manufacturer identifier codes. If the algorithm returns an identification failure, another manufacturer's device resides in the socket. Note that this algorithm depends on the LV ignoring the B3 commands, and vice versa.

The Read Query Command (98H) could also be incorporated (if preferred) to use the "Common Flash Interface" (CFI) data. The CFI data structure contains information such as block size, density, command set, and electrical specifications. Once in this mode, read cycles from addresses are shown in Default. To return to read-array mode, write the Read Array command (FFH).

Table 3. Difference Comparison of Intel and AMD Command Set

Command	B3 (Addr/Data)	LV (Addr/Data)
Read Mode	XXXXH / FFH	XXXH/F0H
Read ID	XXXXH/90H	5555H/AAH, 2AAAH/55H 5555H/90H
Read Query	XXXXH/98H	55H/98H
Program	Addr/40H, Addr/Data	5555H/AAH, 2AAAH/55H, 5555H/A0H, Addr/Data
Erase	Blk Addr/20H, Blk Addr/D0H	5555H/AAH, 2AAAH/55H, 5555H/80H, 5555H/AAH 2AAAH/55H, Blk Addr/30H
Program Suspend	XXXXH/B0H	**Not Available**
Program Resume	XXXXH/D0H	**Not Available**
Erase Suspend	XXXXH/B0H	XXXXH/B0H
Erase Resume	XXXXH/D0H	XXXXH/30H

NOTE: Please refer to the appropriate datasheet for all command definitions.

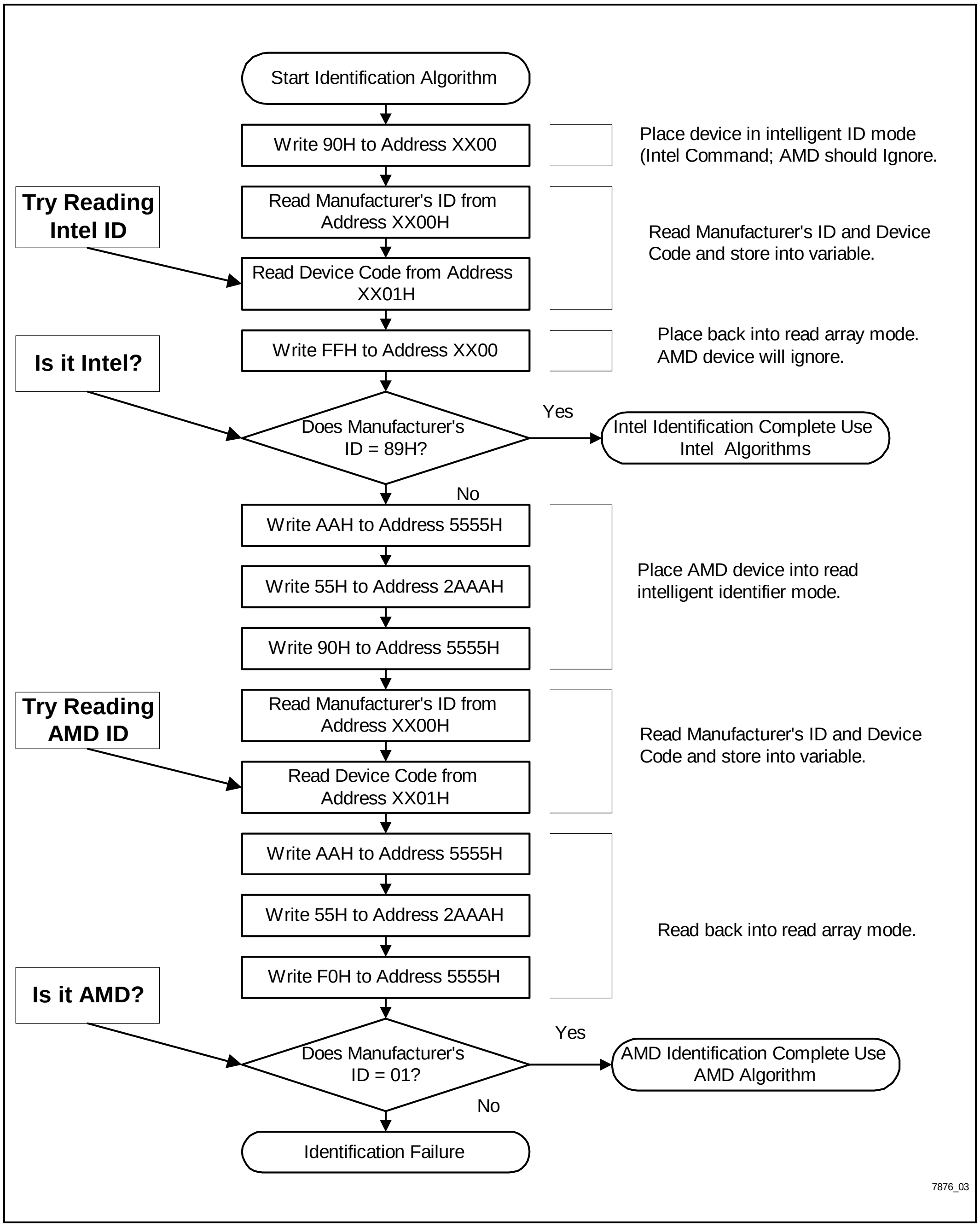

Figure 3. An Example of Manufacturer Identifier Algorithm

3.5 Command Completion Changes

Intel B3 devices use a status register for checking operation status, while AM29LV800B, AM29LV160D, and AM29LV320D devices use the Ready/Busy (RY/BY#) pin to indicate if an operation has been completed. Software should be designed to comprehend this difference, based on the identification algorithm discussed in Section 3.4.

4.0 SUMMARY

This application note focused on designing a multi-source solution between the Intel B3 and the LV devices. Advantages of designing with the Intel B3 include the following:

- Pin-out compatibility for easy upgrade path
- Lower IO voltages
- 12-Volt production programming for fast programming during manufacturing
- Low voltage block locking
- Program-Suspend functionality.
- Intel® Flash Data Integrator (FDI) software for code plus data real-time solutions, or
- Intel® Virtual Small Block (VSB) File Manager – VFM, for simple embedded file data storage applications.

Intel also offers a range of flash memory tools for every stage of system development that enable shorter development schedules with lower development costs.

To implement a multi-source design, users need to pay special attention to AC specifications, pinout differences, blocking differences, command-set differences, and command-completion differences.

APPENDIX A
ADDITIONAL INFORMATION[1,2]

Order Number	Document/Tool
290580	*3-Volt Advanced Boot Block Flash Memory; 28F004/400B3, 28F008/800B3, 28F016/160B3, 28F320B3, 28F640B3,* datasheet
Note 2	*Smart 3 Advanced Boot Block Software Algorithms (Assembly and C Drivers)*
Note 2	Schematic symbols, TimingDesigner* files, VHDL models, Verilog models, and IBIS models

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com/design/flash for technical documentation and tools.