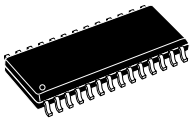
L6918 L6918A

5 BIT PROGRAMMABLE MULTIPHASE CONTROLLER

- OUTPUT CURRENT IN EXCESS OF 100A
- ULTRA FAST LOAD TRANSIENT RESPONSE
- REMOTE SENSE BUFFER
- INTEGRATED 2A GATE DRIVERS
- 5 BIT VID VOLTAGE POSITIONING, VRM 9.0
- 0.6% INTERNAL REFERENCE ACCURACY
- DIGITAL 2048 STEP SOFT-START
- OVP & OCP PROTECTIONS
- Rdson or Rsense CURRENT SENSING
- 1200KHz EFFECTIVE SWITCHING FREQUENCY, EXTERNALLY ADJUSTABLE
- POWER GOOD OUTPUT AND INHIBIT
- PACKAGE: SO28

APPLICATIONS

- HIGH DENSITY DC-DC FOR SERVERS AND WORKSTATIONS
- SUPPLY FOR HIGH CURRENT MICROPROCESSORS
- DISTRIBUTED POWER



SO28

ORDERING NUMBERS: L6918D, L6918AD
L6918DTR, L6918ADTR

DESCRIPTION

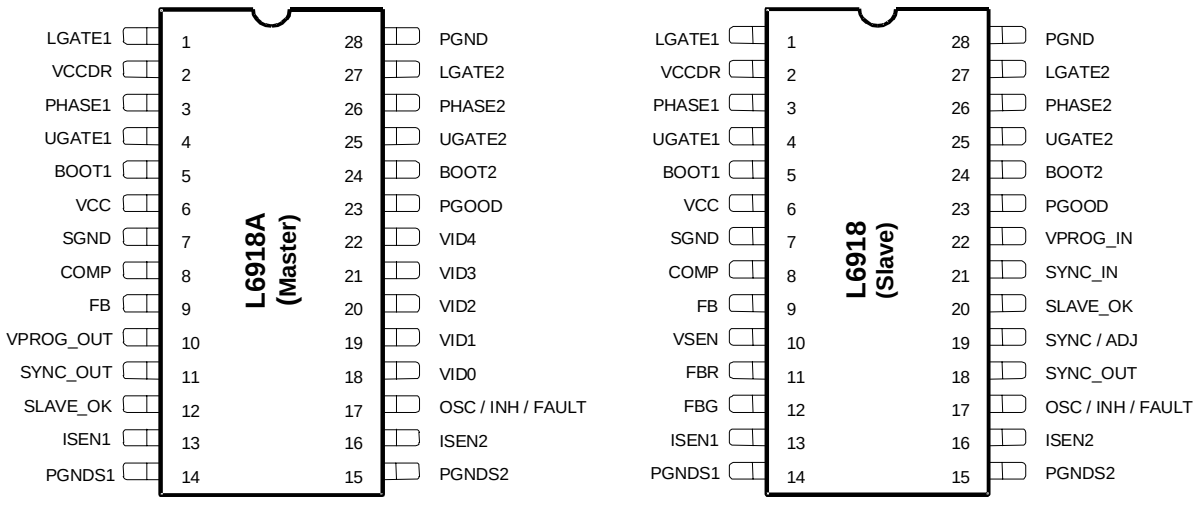
L6918A is a master device that it has to be combined with the L6918,slave, realizing a 4-phases topology, interleaved. The device kit is specifically designed to provide a high performance/high density DC/DC conversion for high current microprocessors and distributed power. Each device implements a dual-phase step-down controller with a 180° phase-shift between each phase.

A precise 5-bit DAC allows adjusting the output voltage from 1.100V to 1.850V with 25mV binary steps.

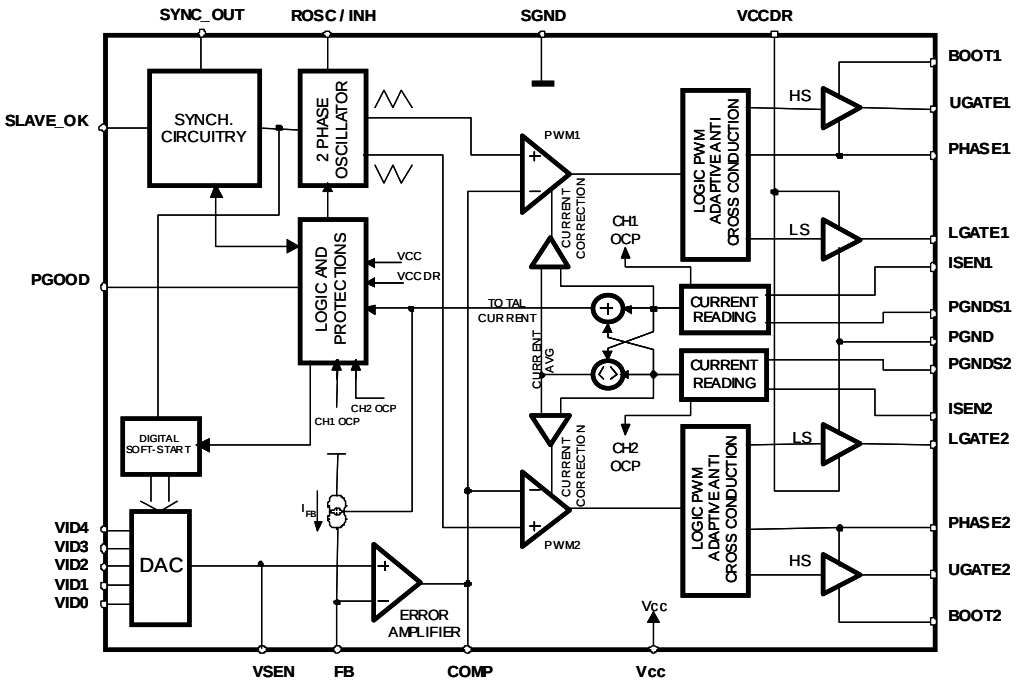
The high peak current gate drives affords to have high system switching frequency, typically of 1200KHz, and higher by external adjustement.

The device kit assure a fast protection against OVP, UVP and OCP. An internal crowbar, by turning on the low side mosfets, eliminates the need of external protection. In case of over-current, the system works in Constant Current mode.

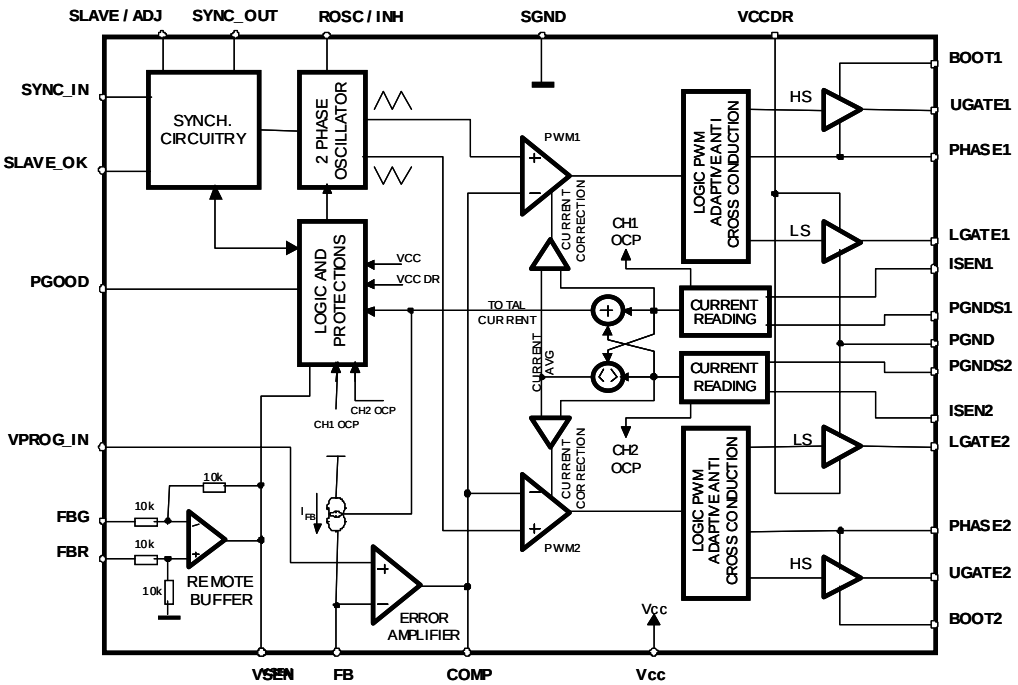
PIN CONNECTIONS



L6918A (MASTER) DEVICE BLOCK DIAGRAM



L6918 (SLAVE) DEVICE BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vcc, V_{CCDR}	To PGND	15	V
V_{BOOT}-V_{PHASE}	Boot Voltage	15	V
V_{UGATE1}-V_{PHASE1} V_{UGATE2}-V_{PHASE2}		15	V
	LGATE1, PHASE1, LGATE2, PHASE2 to PGND	-0.3 to Vcc+0.3	V
	VID0 to VID4	-0.3 to 5	V
	All other pins to PGND	-0.3 to 7	V
V_{PHASEx}	Sustainable Peak Voltage t<20nS @ 600kHz	26	V

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	60	°C / W
T_{max}	Maximum junction temperature	150	°C
$T_{storage}$	Storage temperature range	-40 to 150	°C
T_j	Junction Temperature Range	0 to 125	°C
P_{MAX}	Max power dissipation at Tamb=25°C	2	W

L6918A (MASTER) PIN FUNCTION

N.	Name	Description
1	LGATE1	Channel 1 low side gate driver output.
2	VCCDR	LS Mosfet driver supply. 5V or 12V buses can be used.
3	PHASE1	This pin is connected to the Source of the upper mosfet and provides the return path for the high side driver of channel 1.
4	UGATE1	Channel 1 high side gate driver output.
5	BOOT1	Channel 1 bootstrap capacitor pin. This pin supplies the high side driver. Connect through a capacitor to the PHASE1 pin and through a diode to Vcc (cathode vs. boot).
6	VCC	Device supply voltage. The operative supply voltage is 12V.
7	GND	All the internal references are referred to this pin. Connect it to the PCB signal ground.
8	COMP	This pin is connected to the error amplifier output and is used to compensate the control feedback loop.
9	FB	This pin is connected to the error amplifier inverting input and is used to compensate the voltage control feedback loop. A current proportional to the sum of the current sensed in both channel is sourced from this pin (50µA at full load, 70µA at the Over Current threshold). Connecting a resistor R_{FB} between this pin and VSEN pin allows programming the droop effect.
10	VPROG_OUT	Reference voltage output used for voltage regulation. This pin must be connected together with the slave device VPROG_IN pin. Filter to SGND with 1nF capacitor (a total 30nF distributed capacitance is allowed).
11	SYNC_OUT	Synchronization output signal. From this pin exits a square - 50% duty cycle - 5Vpp –90 deg phase shifted wave clock signal that the Slave device PLL locks to. Connect this pin to the Slave SYNC_IN pin.
12	SLAVE_OK	Open-drain input/output used for start-up and to manage protections as shown in the timing diagram. Internally pulled-up. Connect together with other IC's SLAVE_OK pin. Filter with 1nF capacitor vs. SGND.

L6918A (MASTER) PIN FUNCTION (continued)

N.	Name	Description
13	ISEN1	Channel 1 current sense pin. The output current may be sensed across a sense resistor or across the low-side mosfet RdsON. This pin has to be connected to the low-side mosfet drain or to the sense resistor through a resistor Rg in order to program the current intervention for each phase at 140% as follow: $I_{OCPx} = \frac{35\mu A \cdot R_g}{R_{sense}}$ Where 35µA is the current offset information relative to the Over Current condition (offset at OC threshold minus offset at zero load).The net connecting the pin to the sense point must be routed as close as possible to the PGNDS1 net in order to couple in common mode any picked-up noise.
14	PGNDS1	Channel 1 Power Ground sense pin. The net connecting the pin to the sense point must be routed as close as possible to the ISEN1 net in order to couple in common mode any picked-up noise.
15	PGNDS2	Channel 2 Power Ground sense pin. The net connecting the pin to the sense point must be routed as close as possible to the ISEN2 net in order to couple in common mode any picked-up noise.
16	ISEN2	Channel 2 current sense pin. The output current may be sensed across a sense resistor or across the low-side mosfet $Rds_{ON.}$ This pin has to be connected to the low-side mosfet drain or to the sense resistor through a resistor Rg in order to program the current intervention for each phase at 140% as follow: $I_{OCPx} = \frac{35\mu A \cdot R_g}{R_{sense}}$ Where 35µA is the current offset information relative to the Over Current condition (offset at OC threshold minus offset at zero load). The net connecting the pin to the sense point must be routed as close as possible to the PGNDS2 net in order to couple in common mode any picked-up noise.
17	OSC/INH FAULT	Oscillator switching frequency pin. Connecting an external resistor from this pin to GND, the external frequency is increased according to the equation: $f_S = 300KHz + \frac{14.82 \cdot 10^6}{R_{OSC}(K\Omega)}$ Connecting a resistor from this pin to Vcc (12V), the switching frequency is reduced according to the equation: $f_S = 300KHz + \frac{12.91 \cdot 10^7}{R_{OSC}(K\Omega)}$ If the pin is not connected, the switching frequency is 300KHz. Forcing the pin to a voltage lower than 0.8V, the device stop operation and enter the inhibit state; all mosfets are turned OFF.
18 to 22	VID0-4	Voltage Identification pins. These input are internally pulled-up and TTL compatible. They are used to program the output voltage as specified in Table 1 and to set the over voltage and power good thresholds. Connect to GND to program a ‘0’ while leave floating to program a ‘1’.
23	PGOOD	This pin is an open collector output and is pulled low if the output voltage is not within the above specified thresholds. It must be connected with the Slave’s PGOOD pin. If not used may be left floating.
24	BOOT2	Channel 2 bootstrap capacitor pin. This pin supplies the high side driver. Connect through a capacitor to the PHASE2 pin and through a diode to Vcc (cathode vs. boot).
25	UGATE2	Channel 2 high side gate driver output.
26	PHASE2	This pin is connected to the source of the upper mosfet and provides the return path for the high side driver of channel 2.
27	LGATE2	Channel 2 low side gate driver output.
28	PGND	Power ground pin. This pin is common to both sections and it must be connected through the closest path to the low side mosfets source pins in order to reduce the noise injection into the device.

L6918 (SLAVE) PIN FUNCTION

N.	Name	Description
1	LGATE1	Channel 1 low side gate driver output.
2	VCCDR	LS Mosfet driver supply. 5V or 12V buses can be used.
3	PHASE1	This pin is connected to the Source of the upper mosfet and provides the return path for the high side driver of channel 1.
4	UGATE1	Channel 1 high side gate driver output.
5	BOOT1	Channel 1 bootstrap capacitor pin. This pin supplies the high side driver. Connect through a capacitor to the PHASE1 pin and through a diode to Vcc (cathode vs. boot).
6	VCC	Device supply voltage. The operative supply voltage is 12V.
7	GND	All the internal references are referred to this pin. Connect it to the PCB signal ground.
8	COMP	This pin is connected to the error amplifier output and is used to compensate the control feedback loop.
9	FB	This pin is connected to the error amplifier inverting input and is used to compensate the voltage control feedback loop. A current proportional to the sum of the current sensed in both channel is sourced from this pin (50µA at full load, 70µA at the Over Current threshold). Connecting a resistor R_{FB} between this pin and VSEN pin allows programming the droop effect.
10	VSEN	Connected to the output voltage it is able to manage Over & Under-voltage conditions and the PGOOD signal. It is internally connected with the output of the Remote Sense Buffer for Remote Sense of the regulated voltage. If no Remote Sense is implemented, connect it directly to the regulated voltage in order to manage OVP, UVP and PGOOD.
11	FBR	Remote sense buffer non-inverting input. It has to be connected to the positive side of the load to perform a remote sense. If no remote sense is implemented, connect directly to the output voltage (in this case connect also the VSEN pin directly to the output regulated voltage).
12	FBG	Remote sense buffer inverting input. It has to be connected to the negative side of the load to perform a remote sense. Pull-down to ground if no remote sense is implemented.
13	ISEN1	Channel 1 current sense pin. The output current may be sensed across a sense resistor or across the low-side mosfet Rds_{ON}. This pin has to be connected to the low-side mosfet drain or to the sense resistor through a resistor Rg in order to program the current intervention for each phase at 140% as follow: $$I_{OCPx} = \frac{35\mu A \cdot R_g}{R_{sense}}$$ Where 35µA is the current offset information relative to the Over Current condition (offset at OC threshold minus offset at zero load). The net connecting the pin to the sense point must be routed as close as possible to the PGNDS1 net in order to couple in common mode any picked-up noise.
14	PGNDS1	Channel 1 Power Ground sense pin. The net connecting the pin to the sense point must be routed as close as possible to the ISEN1 net in order to couple in common mode any picked-up noise.
15	PGNDS2	Channel 2 Power Ground sense pin. The net connecting the pin to the sense point must be routed as close as possible to the ISEN2 net in order to couple in common mode any picked-up noise.

L6918 (SLAVE) PIN FUNCTION (continued)

N.	Name	Description
16	ISEN2	Channel 2 current sense pin. The output current may be sensed across a sense resistor or across the low-side mosfet Rds_{ON}. This pin has to be connected to the low-side mosfet drain or to the sense resistor through a resistor Rg in order to program the current intervention for each phase at 140% as follow: $$I_{OCPx} = \frac{35\mu A \cdot R_g}{R_{sense}}$$ Where 35µA is the current offset information relative to the Over Current condition (offset at OC threshold minus offset at zero load). The net connecting the pin to the sense point must be routed as close as possible to the PGNDS2 net in order to couple in common mode any picked-up noise.
17	OSC/INH FAULT	Oscillator switching frequency pin. Connecting an external resistor from this pin to GND, the external frequency is increased according to the equation: $$f_S = 300KHz + \frac{14.82 \cdot 10^6}{R_{OSC}(K\Omega)}$$ Connecting a resistor from this pin to Vcc (12V), the switching frequency is reduced according to the equation: $$f_S = 300KHz + \frac{12.91 \cdot 10^7}{R_{OSC}(K\Omega)}$$ If the pin is not connected, the switching frequency is 300KHz. Forcing the pin to a voltage lower than 0.8V, the device stops operation and enters the inhibit state; all mosfets are turned OFF. The pin is forced high when an over voltage is detected. This condition is latched; to recover it is necessary turn off and on VCC.
18	SYNC_OUT	Output synchronization signal. A 60° phase shift signal exits when the device works as a Slave while no signal exits when the device works as an adjustable.
19	SYNC / ADJ	Slave or Adjustable operation. Connecting this pin to GND the device becomes an adjustable two-phase controller using an external reference for its regulation. No soft start is implemented in this condition, so it must be performed with external circuitry. The device switches using its internal oscillator according to the frequency set by R_{OSC}. Leaving this pin floating, the device works as a Slave two-phase controller. It uses the reference sourced from the master device and an internal PLL locks the synchronization signal sourced from the master device.
20	SLAVE_OK	Open-drain output used for start-up and to manage protections as shown in the timing diagram. Internally pulled-up. Connect together with other IC's SLAVE_OK pin. Filter with 1nF capacitor vs. SGND.
21	SYNC_IN	Synchronization input signal locked during the slave operation. Connect to the master SYNC_OUT pin.
22	VPROG_IN	Reference voltage input used for voltage regulation. This pin must be connected together with the other's slave (if present) to the VPROG_OUT pin of the master device. Filter to SGND with 1nF capacitor (a total 30nF distributed capacitance is allowed). If the device works as an Adjustable (SYNC/ADJ to GND), this is the reference used for the regulation.
23	PGOOD	This pin is an open collector output and is pulled low if the output voltage is not within the above specified thresholds. It must be connected with the master's PGOOD pin. If not used may be left floating.

L6918 (SLAVE) PIN FUNCTION (continued)

N.	Name	Description
24	BOOT2	Channel 2 bootstrap capacitor pin. This pin supplies the high side driver. Connect through a capacitor to the PHASE2 pin and through a diode to Vcc (cathode vs. boot).
25	UGATE2	Channel 2 high side gate driver output.
26	PHASE2	This pin is connected to the Source of the upper mosfet and provides the return path for the high side driver of channel 2.
27	LGATE2	Channel 2 low side gate driver output.
28	PGND	Power ground pin. This pin is common to both sections and it must be connected through the closest path to the low side mosfets source pins in order to reduce the noise injection into the device.

ELECTRICAL CHARACTERISTCS

(Vcc=12V±10%, TJ=0°C to 70°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vcc SUPPLY CURRENT						
I_{CC}	Vcc supply current	HGATEx and LGATEx open V_{CCDR}=V_{BOOT}=12V	7.5	10	12.5	mA
I_{CCDR}	V_{CCDR} supply current	LGATEx open; V_{CCDR}=12V	2	3	4	mA
I_{BOOTx}	Boot supply current	HGATEx open; PHASEx to PGND V_{CC}=V_{BOOT}=12V	0.5	1	1.5	mA
POWER-ON						
	Turn-On V_{CC} threshold	V_{CC} Rising; V_{CCDR}=5V	7.8	9	10.2	V
	Turn-Off V_{CC} threshold	V_{CC} Falling; V_{CCDR}=5V	6.5	7.5	8.5	V
	Turn-On V_{CCDR} Threshold	V_{CCDR} Rising; V_{CC}=12V	4.2	4.4	4.6	V
	Turn-Off V_{CCDR} Threshold	V_{CCDR} Falling; V_{CC}=12V	4.0	4.2	4.4	V
OSCILLATOR AND INHIBIT						
f_{OSC}	Initial Accuracy	OSC = OPEN OSC = OPEN; Tj=0°C to 125°C	278 270	300	322 330	kHz kHz
$f_{OSC,Rosc}$	Total Accuracy	R_T to GND=74kΩ	450	500	550	kHz
ΔVosc	Ramp Amplitude			2		V
d_{MAX}	Maximum duty cycle	OSC = OPEN	45	50	-	%
INH	Inhibit threshold	I_{SINK}=5mA	0.8	0.85	0.9	V
REFERENCE AND DAC only for L6918A (MASTER)						
V_{PROG_OUT}	Reference Voltage Accuracy	VID0 to VID4 see Table1	-0.6	-	0.6	%
I_{DAC}	VID pull-up Current	VIDx = GND	4	5	6	µA
	VID pull-up Voltage	VIDx = OPEN	3.1	-	3.4	V
ERROR AMPLIFIER						
	DC Gain			80		dB
SR	Slew-Rate	COMP=10pF		15		V/µS
	Offset		-7		7	mV
DIFFERENTIAL AMPLIFIER (REMOTE BUFFER) only for L6918 (SLAVE)						
	DC Gain			1		V/V
CMRR	Common Mode Rejection Ratio			40		dB
	Input Offset	FBR=1.100V to1.850V; FBG=GND	-12		12	mV
DIFFERENTIAL CURRENT SENSING						
I_{ISEN1}, I_{ISEN2}	Bias Current	I_{LOAD} = 0%	45	50	55	µA

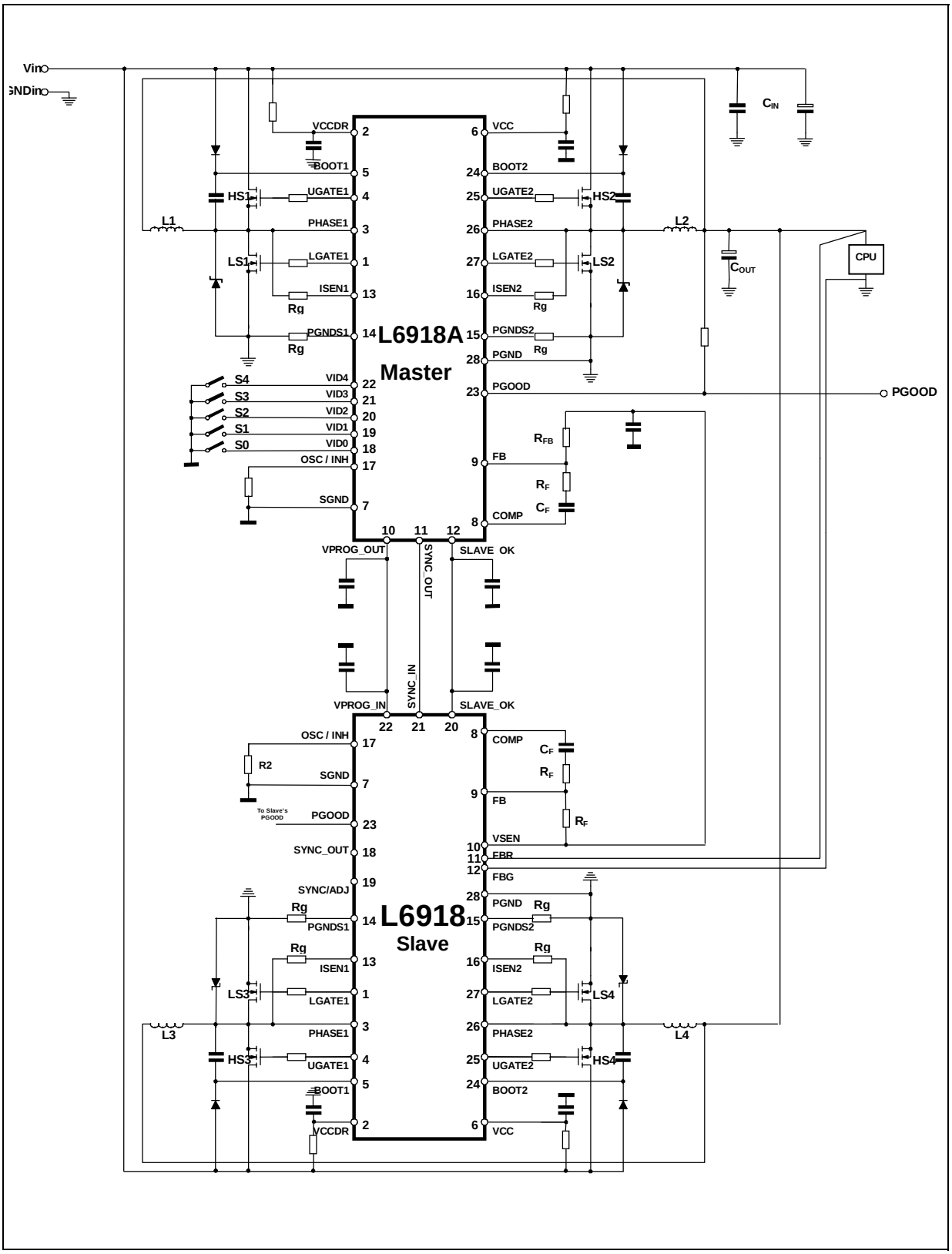
ELECTRICAL CHARACTERISTCS (continued)
(Vcc=12V±10%, TJ=0°C to 70°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{PGNDSx}	Bias Current		45	50	55	µA
I_{ISEN1}, I_{ISEN2}	Bias Current at Over Current Threshold		80	85	90	µA
I_{FB}	Active Droop Current	I_{LOAD} = 0		0	1	µA
		I_{LOAD} = 100%	47.5	50	52.5	µA
GATE DRIVERS						
$t_{RISE\ HGATE}$	High Side Rise Time	V_{BOOTx}-V_{PHASEx}=10V; C_{HGATEx} to PHASEx=3.3nF		15	30	nS
I_{HGATEx}	High Side Source Current	V_{BOOTx}-V_{PHASEx}=10V		2		A
R_{HGATEx}	High Side Sink Resistance	V_{BOOTx}-V_{PHASEx}=12V;	1.5	2	2.5	Ω
$t_{RISE\ LGATE}$	Low Side Rise Time	V_{CCDR}=10V; C_{LGATEx} to PGNDx=5.6nF		30	55	nS
I_{LGATEx}	Low Side Source Current	V_{CCDR}=10V		1.8		A
R_{LGATEx}	Low Side Sink Resistance	V_{CCDR}=12V	0.7	1.1	1.5	Ω
PROTECTIONS						
PGOOD	Upper Threshold (V_{SEN} / VPROG_IN)	V_{SEN} Rising	109	112	115	%
PGOOD	Lower Threshold (V_{SEN} / VPROG_IN)	V_{SEN} Falling	87	90	93	%
OVP	Over Voltage Threshold (V_{SEN} / VPROG_IN)	V_{SEN} Rising	114	117	120	%
UVP	Under Voltage Trip (V_{SEN} / VPROG_IN)	V_{SEN} Falling	55	60	65	%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD} = -4mA	0.3	0.4	0.5	V

Table 1. VID Settings (only for L6918A)

VID4	VID3	VID2	VID1	VID0	Output Voltage (V)	VID4	VID3	VID2	VID1	VID0	Output Voltage (V)
0	0	0	0	0	**1.850**	1	0	0	0	0	**1.450**
0	0	0	0	1	**1.825**	1	0	0	0	1	**1.425**
0	0	0	1	0	**1.800**	1	0	0	1	0	**1.400**
0	0	0	1	1	**1.775**	1	0	0	1	1	**1.375**
0	0	1	0	0	**1.750**	1	0	1	0	0	**1.350**
0	0	1	0	1	**1.725**	1	0	1	0	1	**1.325**
0	0	1	1	0	**1.700**	1	0	1	1	0	**1.300**
0	0	1	1	1	**1.675**	1	0	1	1	1	**1.275**
0	1	0	0	0	**1.650**	1	1	0	0	0	**1.250**
0	1	0	0	1	**1.625**	1	1	0	0	1	**1.225**
0	1	0	1	0	**1.600**	1	1	0	1	0	**1.200**
0	1	0	1	1	**1.575**	1	1	0	1	1	**1.175**
0	1	1	0	0	**1.550**	1	1	1	0	0	**1.150**
0	1	1	0	1	**1.525**	1	1	1	0	1	**1.125**
0	1	1	1	0	**1.500**	1	1	1	1	0	**1.100**
0	1	1	1	1	**1.475**	1	1	1	1	1	**Shutdown**

FOUR PHASE REFERENCE SCHEMATICS

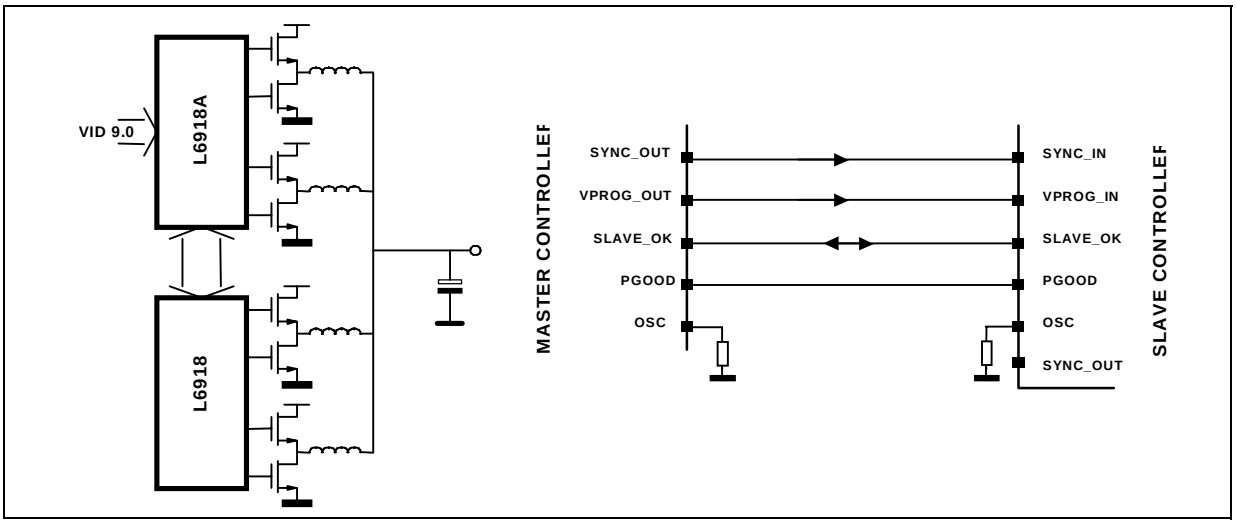


DEVICES DESCRIPTION

The devices are integrated circuit realized in BCD technology. They provide, in kit, a complete control logic and protections sets for a high performance four-phases step-down DC-DC converter optimized for microprocessors supply and High Density DC-DC converters. They are designed to drive N-Channel mosfets in an interleaved four-phase synchronous-rectified buck topology. Each controller provides a 180 deg phase shift between its two phases and a 90deg phase-shifted synchronization signal is passed from the master to the slave controller that locks the signal through a PLL. The resulting four-phases converter synchronized together results in a 90 deg phase shift on each phase, allowing a consistent reduction of the input capacitors ripple current, minimizing also the size and the power losses. The output voltage of the converter can be precisely regulated, programming the master's VID pins, from 1.100V to 1.850V with 25mV binary steps. The reference for the regulation is passed from the master device to the slave device through apposite pin likewise the synchronization signal. Each device provides an average current-mode control with fast transient response. They include a 300kHz free-running oscillator externally adjustable up to 600kHz, realized in order to multiply by 4 times the equivalent system frequency. The error amplifier features a 15MHz gain-bandwidth product and 10V/µs slew rate that permits high converter bandwidth for fast transient performances. Current information is read in all the devices across the lower mosfets R_{DSON} or across a sense resistor in fully differential mode. The current information corrects the PWM output in order to equalize the average current carried the two phases of each device. Current sharing between the two phases of each device is then limited at ±10% over static and dynamic conditions. Current sharing between devices is assured by the droop function. The device protects against over-current, with an OCP threshold for each phase, entering in constant current mode. Since the current is read across the low side mosfets, the constant current keeps constant the bottom of the inductors current triangular waveform. When an under voltage is detected the Slave device latches. The Slave device also perform an over voltage protection that disable immediately both devices turning ON the lower driver and driving high the FAULT pin. Over Load condition are transmitted from the Slave device(s) to the master through the SLAVE_OK line.

MASTER - SLAVE INTERACTIONS

Figure 1. Four Phase connection with L6918 family



Master and slave devices are connected together in order to realize four-phase high performance step-down DC/DC converter. Four-phase converter is implemented using L6918A master and one L6918 slave devices as shown in figure 1.

A communication bus is implemented among all the controllers involved in the regulation. This bus consists in the following lines:

– **Reference (VPROG_IN / VPROG_OUT pins):** Unidirectional line.
The devices share the reference for the regulation. The reference is programmed through the master device VID pins. It exits from the master through the VPROG_OUT pin and enters the slave device through the VPROG_IN pin(s). Filter externally with at least 1nF capacitor.

– **Clock Signal (SYNC_IN / SYNC_OUT pins):** Unidirectional line.
A synchronization signal exits from the Master device through the SYNC_OUT pin with 90 deg phase-shift and enters the Slave device through the SYNC_IN pin. The Slave device locks that signal through an internal PLL for its regulation. An auxiliary synchronization signal exits from the Slave through the SYNC_OUT.

– **SLAVE_OK Bus (SLAVE_OK pins):** Bi-directional line.
While the supply voltages are increasing, this line is hold to GND by all the devices. The Slave device sets this line free (internally 5V pulled-up) when it is ready for the Soft-Start. After that this line is freed, the Master device starts the Soft Start (for further details about Soft-Start, see the relevant section).
During normal operation, the line is pulled low by the Slave device if an Over / Under voltage is detected (See relevant section).

– **PGOOD pins:**
PGOOD pins are connected together and pulled-up. During Soft-Start, the master device hold down this line while during normal regulation the slave device de-assert the line if PGOOD has been lost.

Connections between the devices are shown in figure 1.

OSCILLATOR

The devices have been designed in order to operate on each phase at the same switching frequency of the internal oscillator. So, input and output resulting frequencies are four times bigger.

The oscillator is present in all the devices. Since the Master oscillator sets the main frequency for the regulation, the Slave oscillator gives an offset to the Slave's PLL. In this way the PLL is able to lock the synchronization signal that enters from its SYNC_IN pin; it is able to recover up to ±15% offset in the synchronization signal frequency. It is then necessary to program the switching frequency for all the devices involved in the multi-phase conversion as follow.

The switching frequency is internally fixed to 300kHz. The internal oscillator generates the triangular waveform for the PWM charging and discharging with a constant current an internal capacitor. The current delivered to the oscillator is typically 25µA (Fsw = 300KHz) and may be varied using an external resistor (R_{OSC}) connected between OSC pin and GND or Vcc. Since the OSC pin is maintained at fixed voltage (typ. 1.235V), the frequency is varied proportionally to the current sunk (forced) from (into) the pin considering the internal gain of 12KHz/µA.

In particular connecting it to GND the frequency is increased (current is sunk from the pin), while connecting ROSC to Vcc=12V the frequency is reduced (current is forced into the pin), according to the following relationships:

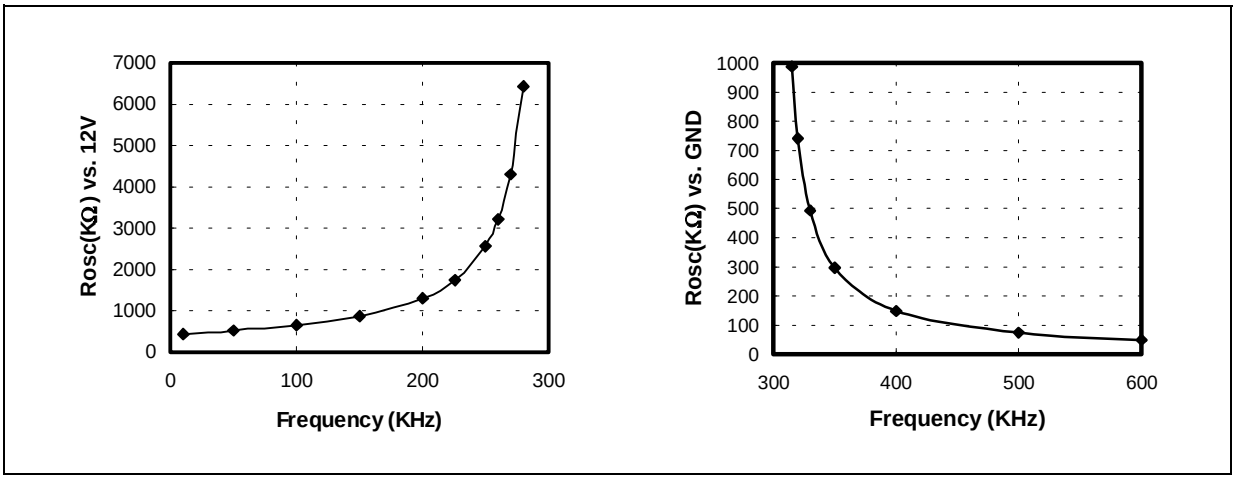
$$R_{OSC}\text{ vs. GND: } f_S = 300kHz + \frac{1.237}{R_{OSC}(K\Omega)} \cdot 12\frac{KHz}{\mu A} = 300KHz + \frac{14.82 \cdot 10^6}{R_{OSC}(K\Omega)}$$

$$R_{OSC}\text{ vs. 12V: } f_S = 300kHz + \frac{12 - 1.237}{R_{OSC}(K\Omega)} \cdot 12\frac{KHz}{\mu A} = 300KHz - \frac{12.918 \cdot 10^7}{R_{OSC}(K\Omega)}$$

Note that forcing a 25µA current into this pin, the device stops switching because no current is delivered to the oscillator.

Figure 2 shows the frequency variation vs. the oscillator resistor ROSC considering the above reported relationships.

Figure 2. R_{OSC} vs. Switching Frequency



DIGITAL TO ANALOG CONVERTER (ONLY FOR MASTER DEVICE L6918A)

The built-in digital to analog converter allows the adjustment of the output voltage from 1.100V to 1.850V with 25mV as shown in the previous table 1. The internal reference is trimmed to ensure the precision of ±0.6% and a zero temperature coefficient around the 70° C. The internal reference voltage for the regulation is programmed by the voltage identification (VID) pins. These are TTL compatible inputs of an internal DAC that is realized by means of a series of resistors providing a partition of the internal voltage reference. The VID code drives a multiplexer that selects a voltage on a precise point of the divider. The DAC output is delivered to an amplifier obtaining the VPROG voltage reference (i.e. the set-point of the error amplifier). Internal pull-ups are provided for the VID pins (realized with a 5µA current generator); in this way, to program a logic "1" it is enough to leave the pin floating, while to program a logic "0" it is enough to short the pin to GND.

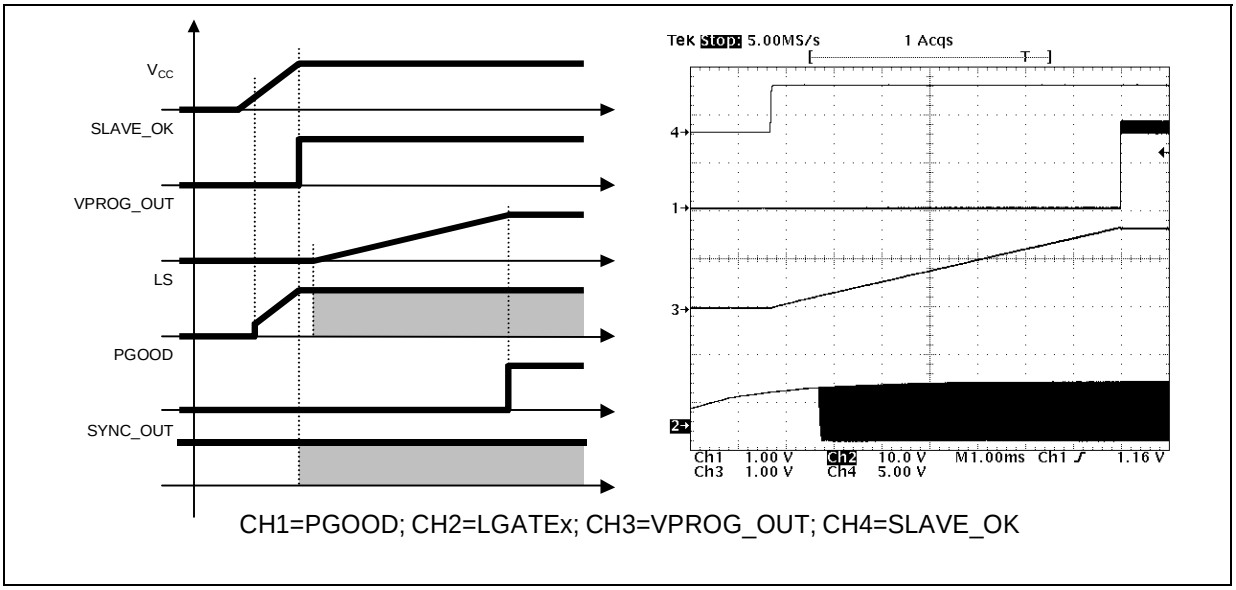
The voltage identification (VID) pin configuration also sets the power-good thresholds (PGOOD) and the Over/ Under voltage protection (OVP/UVP) thresholds.

The reference for the regulation is generated into the master device and delivered to the slave device through the VPROG_OUT / VPROG_IN pins.
Programming the "11111" VID code, the device enters the NOCPU state: both devices keeps all mosfets OFF and the condition is latched. Cycle the power supply to restart operation. Moreover, in this condition, the OVP protection is still active into the slave device with a 0.8V threshold.

SOFT START AND INHIBIT

At start-up a ramp is generated from the master device increasing its loop reference from 0V to the final value programmed by VID in 2048 clock periods. The same reference is present on the VPROG_OUT pin, producing an increasing loop reference also into the slave device. In this way all the devices involved in the multi-phase conversion start together with the same increasing reference (See Figure 3).
Before soft start, the lower power MOS are turned ON after that VCCDR reaches 2V (independently by Vcc value) to discharge the output capacitor and to protect the load from high side mosfet failures. Once soft start begins, the reference is increased and also the upper MOS begins to switch: the output voltage starts to increase with closed loop regulation. At the end of the digital soft start, the Power Good comparator is enabled and the PGOOD signal is then driven high (See fig. 3). The Under Voltage comparator is enabled when the reference voltage reaches 0.8V.
The Soft-Start will not take place, if both VCC and VCCDR pins are not above their own turn-on thresholds. The soft-start takes place, and the Master device starts to increase the reference, only if the SLAVE_OK bus is at high level. The Slave device keeps this line shorted to GND until it is ready for the start-up while the master keeps this line free before soft-start; anyway, this line is shorted to GND if VCC and VCCDR are not above the turn-ON threshold. During normal operation, if any under-voltage is detected on one of the two supplies, the devices are shutdown.

Figure 3. Soft Start



CH1=PGOOD; CH2=LGATEx; CH3=VPROG_OUT; CH4=SLAVE_OK

Forcing the master OSC/INH/FAULT pin to a voltage lower than 0.8V, the devices enter in INHIBIT mode: all the power mosfets are turned off until this condition is removed. When this pin is freed, the OSC/INH/FAULT pin reaches the band-gap voltage and the soft start begin as previously explained.

In INHIBIT mode the Slave device still have both OVP and UVP protection active referring the thresholds to the incoming reference present at the VPROG_IN pin if this one is greater than 0.8V. Otherwise (VPROG_IN < 0.8V) UVP is disabled and the OVP threshold is fixed at 0.8V.

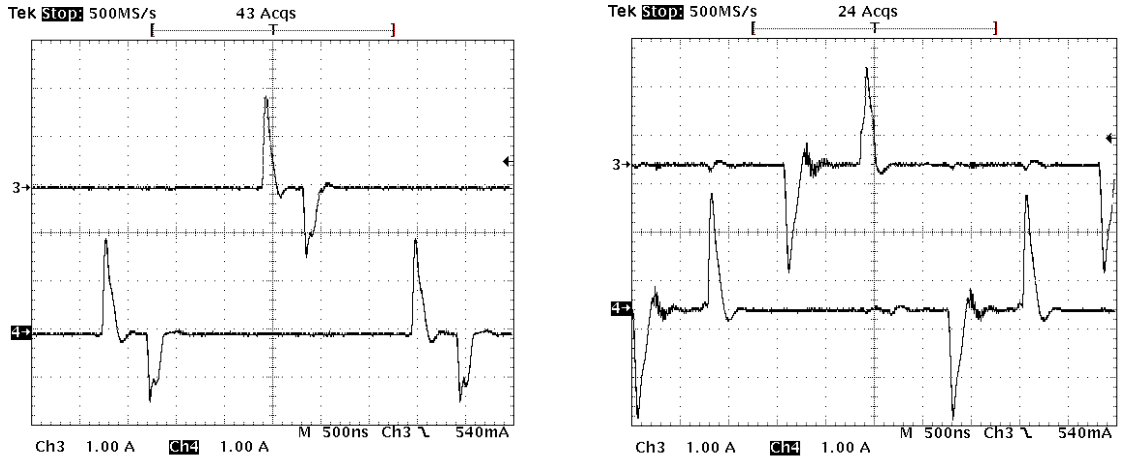
DRIVER SECTION

The integrated high-current drivers allow using different types of power MOS (also multiple MOS to reduce the RDSON), maintaining fast switching transition.

The drivers for the high-side mosfets use BOOT pins for supply and PHASE pins for return. The drivers for the low-side mosfets use VCCDRV pin for supply and PGND pin for return. A minimum voltage of 5V at VCCDRV pin is required to start operations of the device. The controller embodies a sophisticated anti-shoot-through system to minimize low side body diode conduction time so maintaining good efficiency saving the use of Schottky diodes. The conduction time is reduced to few nanoseconds assuring that high-side and low-side mosfets are never switched on simultaneously: when the high-side mosfet turns off, the voltage on its source begins to fall; when the voltage reaches 2V, the low-side mosfet gate drive is applied with 30ns delay. When the low-side mosfet turns off, the voltage at LGATE pin is sensed. When it drops below 1V, the high-side mosfet gate drive is applied with a delay of 30ns. If the current flowing in the inductor is negative, the source of high-side mosfet will never drop. To allow the turning on of the low-side mosfet even in this case, a watchdog controller is enabled: if the source of the high-side mosfet don't drop for more than 240ns, the low side mosfet is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

The BOOT and VCCDRV pins are separated from IC's power supply (VCC pin) as well as signal ground (SGND pin) and power ground (PGND pin) in order to maximize the switching noise immunity.
The peak current is shown for both the upper and the lower driver of the two phases in figure 4.A 10nF capacitive load has been used.
For the upper drivers, the source current is 1.9A while the sink current is 1.5A with V_{BOOT}-V_{PHASE} = 12V; similarly, for the lower drivers, the source current is 2.4A while the sink current is 2A with V_{CCDR} = 12V.

Figure 4. Drivers peak current: High Side (left) and Low Side (right)



CH3 = HGATE1; CH4 = HGATE2

CH3 = LGATE1; CH4 = LGATE2

CURRENT READING AND OVER CURRENT

Each device involved in the four phase conversion has its own current reading circuitry and over current protection. As a results, the OCP network design for each device must be performed fort half of the maximum output current.

The current flowing trough each phase is read using the voltage drop across the low side mosfets R_{DSON} or across a sense resistor (R_{SENSE}) and internally converted into a current. The transconductance ratio is issued by the external resistor Rg placed outside the chip between ISENx and PGNDSx pins toward the reading points. The full differential current reading rejects noise and allows to place sensing element in different locations without affecting the measurement's accuracy. The current reading circuitry reads the current during the time in which the low-side mosfet is on (OFF Time). During this time, the reaction keeps the pin ISENx and PGNDSx at the same voltage while during the time in which the reading circuitry is off, an internal clamp keeps these two pins at the same voltage sinking from the ISENx pin the necessary current (Needed if low-side mosfet R_{dsON} sense is implemented to avoid absolute maximum rating overcome on ISENx pin).

The proprietary current reading circuit allows a very precise and high bandwidth reading for both positive and negative current. This circuit reproduces the current flowing through the sensing element using a high speed Track & Hold Tran conductance amplifier. In particular, it reads the current during the second half of the OFF time reducing noise injection into the device due to the high side mosfet turn-on (See fig. 5). Track time must be at least 200ns to make proper reading of the delivered current.
This circuit sources a constant 50µA current from the PGNDSx pin and keeps the pins ISENx and PGNDSx at the same voltage. Referring to figure 5, the current that flows in the ISENx pin is then given by the following equation:

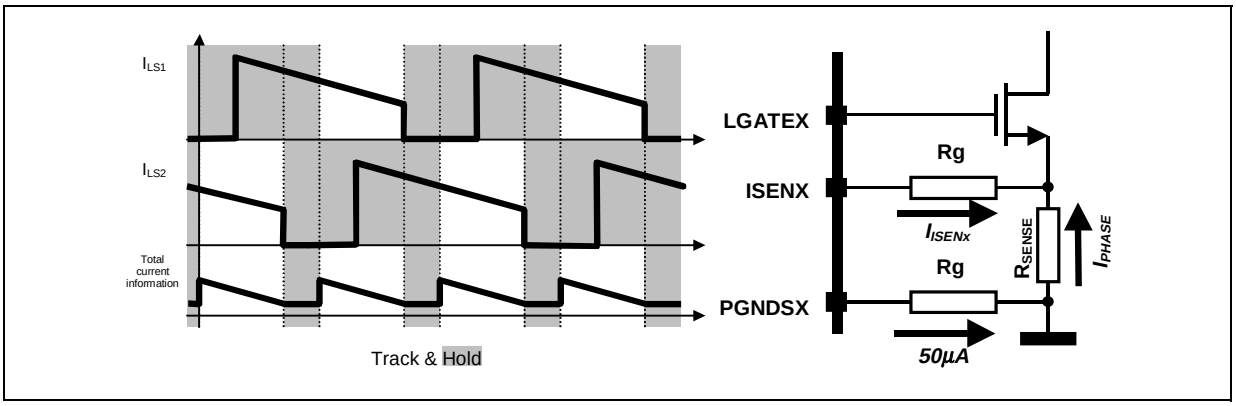
$$I_{ISENx} = 50\mu A + \frac{R_{SENSE} \cdot I_{PHASE}}{R_g} = 50\mu A + I_{INFOx}$$

Where R_{SENSE} is an external sense resistor or the R_{dsON} of the low side mosfet and Rg is the transconductance resistor used between ISENx and PGNDSx pins toward the reading points; I_{PHASE} is the current carried by each phase.
The current information reproduced internally is represented by the second term of the previous equation as follow:

$$I_{INFOx} = \frac{R_{SENSE} \cdot I_{PHASE}}{R_g}$$

Since the current is read in differential mode, also negative current information is kept; this allow the device to check for dangerous returning current between the two phases assuring the complete equalization between the phase's currents.

Figure 5. Current reading timing (left) and circuit (right)



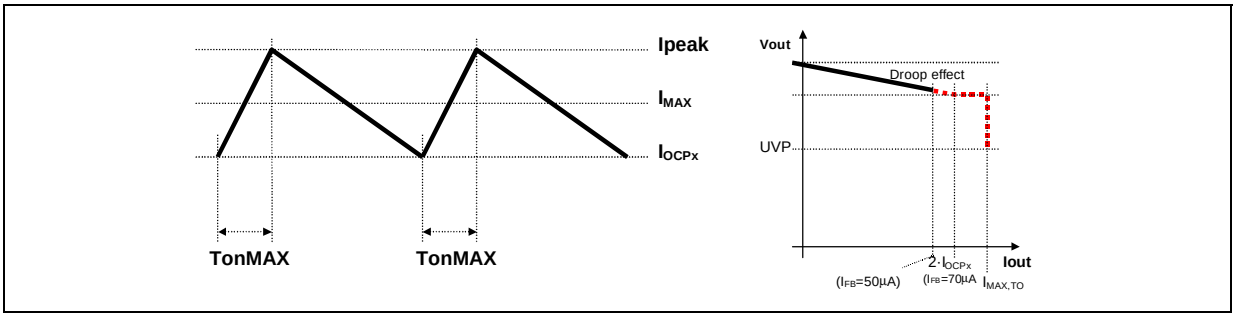
From the current information for each phase, information about the total current delivered (I_{FB}=II$_{NFO1}$+I_{INFO2}) and the average current for each phase (I_{AVG}=(I_{INFO1}+I_{INFO2})/2) is taken. I_{INFOX} is then compared to I_{AVG} to give the correction to the PWM output in order to equalize the current carried by the two phases.

The transconductance resistor Rg can be designed in order to have current information of 25µA per phase at full nominal load; the over current intervention threshold is set at 140% of the nominal (II$_{NFOx}$ = 35µA). According to the above relationship, the over current threshold (I_{OCPx}) for each phase, which has to be placed at one half of the total delivered maximum current, results:

$$I_{OCPx} = \frac{35\mu A \cdot R_g}{R_{SENSE}} \qquad R_g = \frac{I_{OCPx} \cdot R_{SENSE}}{35\mu A}$$

An over current is detected when the current flowing into the sense element is greater than IOCP (I_{INFOx}>35µA): the device enters in Quasi-Constant-Current operation. The low-side mosfets stays ON until IINFO becomes lower than 35µA skipping clock cycles. The high side mosfets can be turned ON with a T_{ON} imposed by the control loop at the next available clock cycle and the device works in the usual way until another OCP event is detected.
The device limits the bottom of the inductor current triangular waveform. So the average current delivered can slightly increase also in Over Current condition since the current ripple increases. In fact, the ON time increases due to the OFF time rise because of the current has to reach the I_{OCP} bottom. The worst-case condition is when the duty cycle reaches its maximum value (d=50% internally limited). When this happens, the device works in Constant Current and the output voltage decrease as the load increase. Crossing the UVP threshold causes the Slave device to pull down the SLAVE_OK line. All mosfets are turned off and all the devices involved in the regulation stop working. Cycle the power supply to restart operation.
Figure 6 shows the constant current working condition

Figure 6. Constant Current operation



It can be observed that the peak current (Ipeak) is greater than the 140% but it can be determined as follow:

$$Ipeak = I_{OCPx} + \frac{V_{IN} - Vout_{min}}{L} \cdot Ton_{MAX} = I_{OCPx} + \frac{V_{IN} - Vout_{MIN}}{L} \cdot 0.5 \cdot T$$

Where $Vout_{MIN}$ is the minimum output voltage (UVP threshold).

The device works in Constant-Current, and the output voltage decreases as the load increase, until the output voltage reaches the under-voltage threshold ($Vout_{MIN}$). When this threshold is crossed, all mosfets are turned off, the FAULT pin is driven high and the device stops working. Cycle the power supply to restart operation. The maximum average current during the Constant-Current behavior results:

$$I_{MAX,TOT} = 2 \cdot I_{MAX} = 2 \cdot \left(I_{OCPx} + \frac{Ipeak - I_{OCPx}}{2} \right)$$

In this particular situation, the switching frequency results reduced.
The ON time is the maximum allowed (T_{onMAX}) while the OFF time depends on the application:

$$T_{OFF} = L \cdot \frac{Ipeak - I_{OCPx}}{V_{OUT}} \qquad f = \frac{1}{Ton_{MAX} + T_{OFF}}$$

Over current is set anyway when I_{INFOx} reaches 35µA. The full load value is only a convention to work with convenient values for I_{FB}. Since the OCP intervention threshold is fixed, to modify the percentage with respect to the load value, it can be simply considered that, for example, to have on OCP threshold of 170%, this will correspond to I_{INFOx} = 35µA (I_{FB} = 70µA). The full load current will then correspond to I_{INFOx} = 20.5µA (I_{FB} = 41µA).

INTEGRATED DROOP FUNCTION

The devices use the droop function to satisfy the requirements of high performance microprocessors, reducing the size and the cost of the output capacitor.

This method "recovers" part of the drop due to the output capacitor ESR in the load transient, introducing a dependence of the output voltage on the load current

As shown in figure 7, the ESR drop is present in any case, but using the droop function the total deviation of the output voltage is minimized. In practice the droop function introduces a static error proportional to the output current that can be represented by an equivalent output resistance R_{OUT}. Since the device has an average current mode regulation, the information about the total current delivered is used to implement the Droop Function. This current (equal to the sum of both I_{INFOx}) is sourced from the FB pin. Connecting a resistor between this pin and Vout, the total current information flows only in this resistor because the compensation network between

FB and COMP has always a capacitor in series (See fig. 8). The voltage regulated by each device is then equal to:

$$V_{OUT} = VID - R_{FB} \cdot I_{FB} = VID - R_{FB} \cdot \frac{R_{SENSE}}{Rg} \cdot I_{OUT}$$

Where I_{OUT} is the output current of each device (equal to the total load current I_{LOAD} divided by the number of devices N)

Since I_{FB} depends on the current information about the two phases of each device, the output characteristic vs. load current is given by:

$$V_{OUT} = VID - R_{FB} \cdot I_{OUT} = VID - R_{FB} \cdot \frac{R_{SENSE}}{Rg} \cdot I_{OUT} = VID - R_{FB} \cdot \frac{R_{SENSE}}{Rg} \cdot \frac{I_{LOAD}}{2}$$

Where R_{OUT} is the equivalent output resistance due to the droop function and I_{OUT} is still the output current of each device (that is the total current delivered to the load I_{LOAD} divided by 2.

Figure 7. Output transient response without (a) and with (b) the droop function

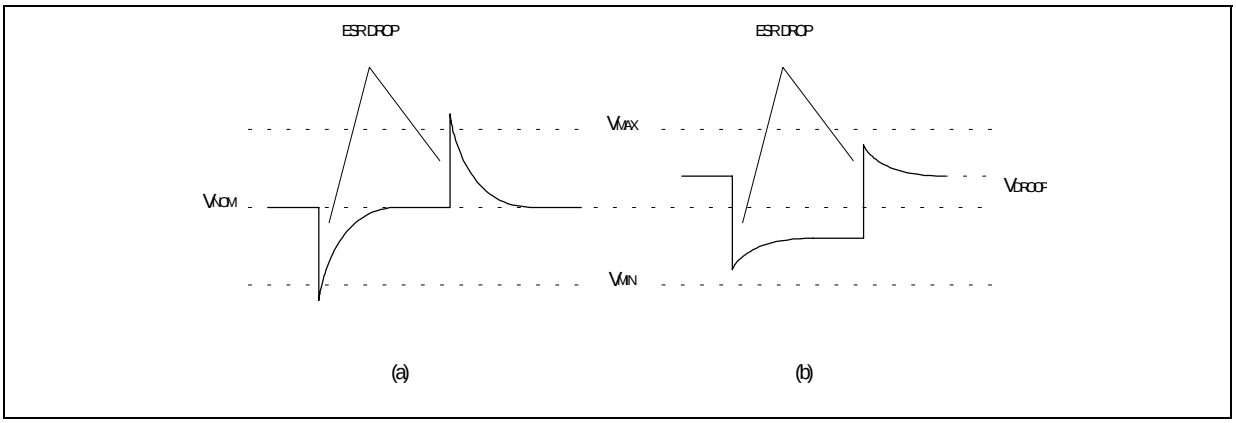
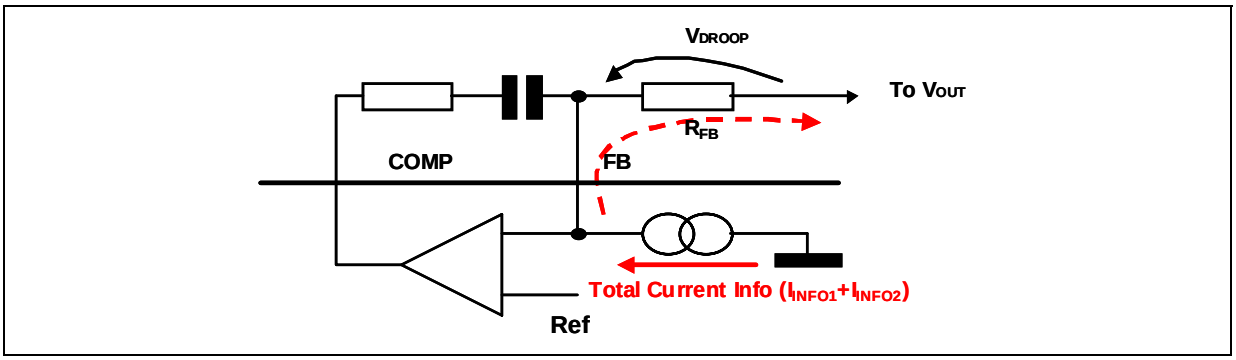


Figure 8. Active Droop Function Circuit



The feedback current is equal to 50µA at nominal full load ($I_{FB} = I_{INFO1} + I_{INFO2}$) and 70µA at the OCP intervention threshold, so the maximum output voltage deviation is equal to:

$$\Delta V_{FULL\_POSITIVE\_LOAD} = +R_{FB} \cdot 50\mu A \qquad \Delta V_{OL\_INTERVENTION} = +R_{FB} \cdot 70\mu A$$

Droop function is provided only for positive load; if negative load is applied, and then IINFOx<0, no current is sunk from the FB pin. The device regulates at the voltage programmed by the VID.

OUTPUT VOLTAGE MONITORING AND PROTECTION: POWER GOOD

The output voltage is monitored by the Slave device through the pin VSEN. If it is not within +12/-10% (typ.) of the programmed value, the PGOOD output is forced low. PGOOD is always active in the Slave device, also during soft-start. PGOOD in the Master device has the only masking function during soft-start. Since the master has not the output voltage sense, it keeps the PGOOD to GND during soft-start and after this step it is freed.

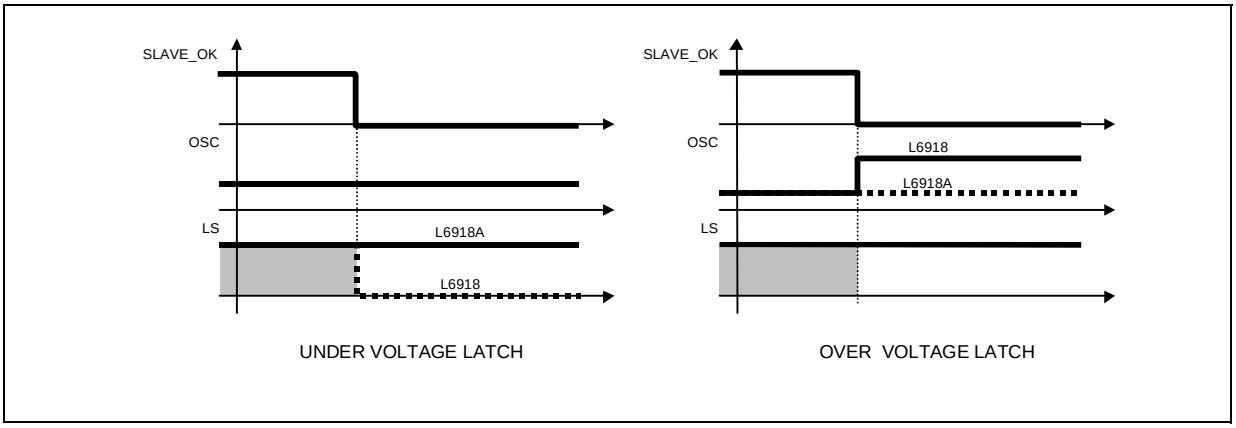
The Slave device provides Over-Voltage protection: when the voltage sensed by VSEN reaches 117% (typ.) of the reference voltage present at the VPROG_IN pin, the Slave device stops switching keeping the LS mosfets ON. The FAULT pin is driven high (5V) and the SLAVE_OK line is pulled low. The master device then stops switching keeping the LS mosfets ON, too. Since the condition is latched, power supply (Vcc) turn off and on is required to restart operations.

Under voltage protection is also provided and still detected by the Slave device. If the output voltage drops below the 60% (typ.) of the reference voltage present at the VPROG_IN pin for more than one clock period, the Slave device stops switching turning OFF all mosfets and pulling down the SLAVE_OK line: the Master device stops switching with LS mosfets ON. The OSC/INH/FAULT is not driven high in this case.

Both Over Voltage and Under Voltage are active also during soft start (Under Voltage after than Vout reaches 0.8V). During soft-start the reference voltage used to determine the UV threshold is the increasing voltage driven by the 2048 soft start digital counter. Moreover, OVP is always active, even during INHIBIT (see relevant section).

Over / Under Voltage behavior are shown in Figure 9.

Figure 9. OVP and UVP latch



REMOTE VOLTAGE SENSE

A remote sense buffer is integrated into the device to allow output voltage remote sense implementation without any additional external components. In this way, the output voltage programmed is regulated between the remote buffer inputs compensating motherboard trace losses or connector losses if the device is used for a VRM module.

The very low offset amplifier senses the output voltage remotely through the pins FBR and FBG (FBR is for the regulated voltage sense while FBG is for the ground sense) and reports this voltage internally at VSEN pin with unity gain eliminating the errors. Keeping the FBR and FBG traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

If remote sense is not required, the output voltage is sensed by the VSEN pin connecting it directly to the output voltage. In this case the FBG and FBR pins must be connected anyway to the regulated voltage

INPUT CAPACITOR

The input capacitor is designed considering mainly the input rms current that depends on the duty cycle as reported in figure. Considering the four phase topology, the input rms current is highly reduced comparing with single or dual phase operation.

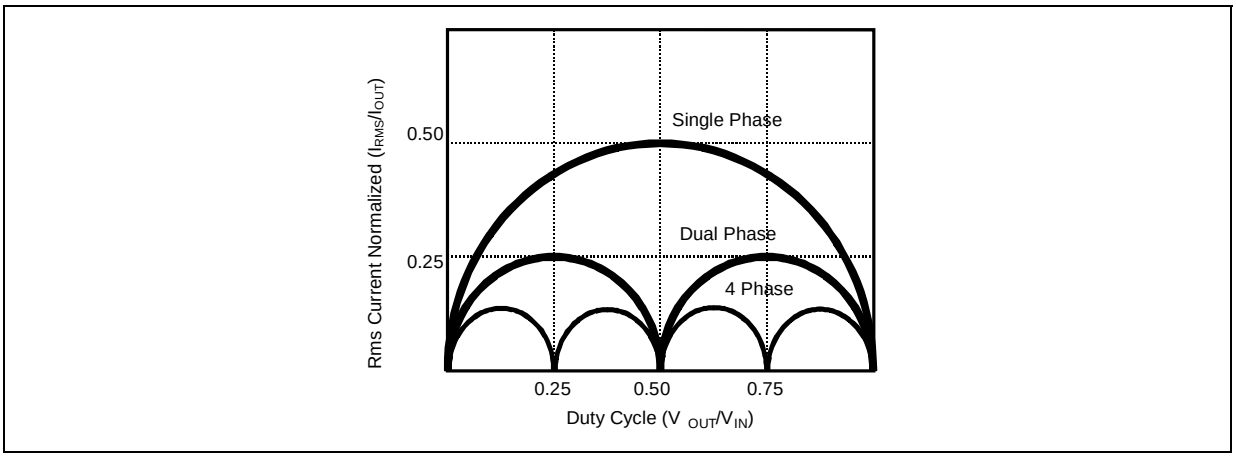
It can be observed that the input rms value is one half of the dual-phase equivalent input current in the worst-case condition that happens for D=1/8, 3/8,5/8 and 7/8.

The power dissipated by the input capacitance is then equal to:

$$P_{RMS} = ESR \cdot (I_{RMS})^2$$

Input capacitor is designed in order to sustain the ripple relative to the maximum load duty cycle. To reach the high rms value needed by the CPU power supply application and also to minimize components cost, the input capacitance is realized by more than one physical capacitor. The equivalent rms current is simply the sum of the single capacitor's rms current.

Figure 10. Input rms Current vs. Duty Cycle.



OUTPUT CAPACITOR

Since the microprocessors require a current variation beyond 100A doing load transients, with a slope in the range of tenth A/µs, the output capacitor is a basic component for the fast response of the power supply.

Dual phase topology reduces the amount of output capacitance needed because of faster load transient response (switching frequency is doubled at the load connections). Current ripple cancellation due to the 180° phase shift between the two phases also reduces requirements on the output ESR to sustain a specified voltage ripple.

When a load transient is applied to the converter's output, for first few microseconds the current to the load is supplied by the output capacitors. The controller recognizes immediately the load transient and increases the duty cycle, but the current slope is limited by the inductor value.

The output voltage has a first drop due to the current variation inside the capacitor (neglecting the effect of the ESL):

$$\Delta V_{OUT} = \Delta I_{OUT} \cdot ESR$$

A minimum capacitor value is required to sustain the current during the load transient without discharge it. The voltage drop due to the output capacitor discharge is given by the following equation:

$$\Delta V_{OUT} = \frac{\Delta i_{OUT}^2 \cdot L}{2 \cdot C_{OUT} \cdot (V_{INmin} \cdot D_{MAX} - V_{OUT})}$$

Where D_{MAX} is the maximum duty cycle value. The lower is the ESR, the lower is the output drop during load transient and the lower is the output voltage static ripple.

INDUCTOR DESIGN

The inductance value is defined by a compromise between the transient response time, the efficiency, the cost and the size. The inductor has to be calculated to sustain the output and the input voltage variation to maintain the ripple current ΔI_L between 20% and 30% of the maximum output current. The inductance value can be calculated with this relationship:

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

Where f_{SW} is the switching frequency, V_{IN} is the input voltage and V_{OUT} is the output voltage.

Increasing the value of the inductance reduces the ripple current but, at the same time, reduces the converter response time to a load transient. The response time is the time required by the inductor to change its current from initial to final value. Since the inductor has not finished its charging time, the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitance required.
The response time to a load transient is different for the application or the removal of the load: if during the application of the load the inductor is charged by a voltage equal to the difference between the input and the output voltage, during the removal it is discharged only by the output voltage. The following expressions give approximate response time for DI load transient in case of enough fast compensation network response:

$$t_{application} = \frac{L \cdot \Delta I}{V_{IN} - V_{OUT}} \qquad t_{removal} = \frac{L \cdot \Delta I}{V_{OUT}}$$

The worst condition depends on the input voltage available and the output voltage selected. Anyway the worst case is the response time after removal of the load with the minimum output voltage programmed and the maximum input voltage available.

Figure 11. Inductor ripple current vs. Vout

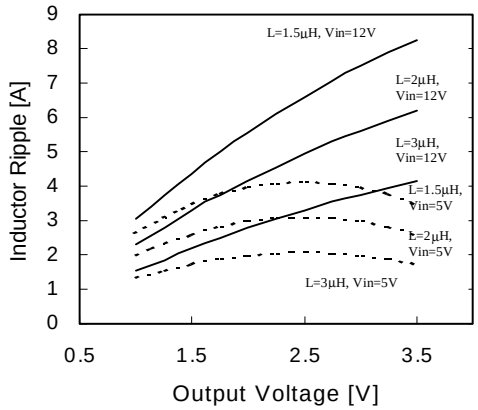
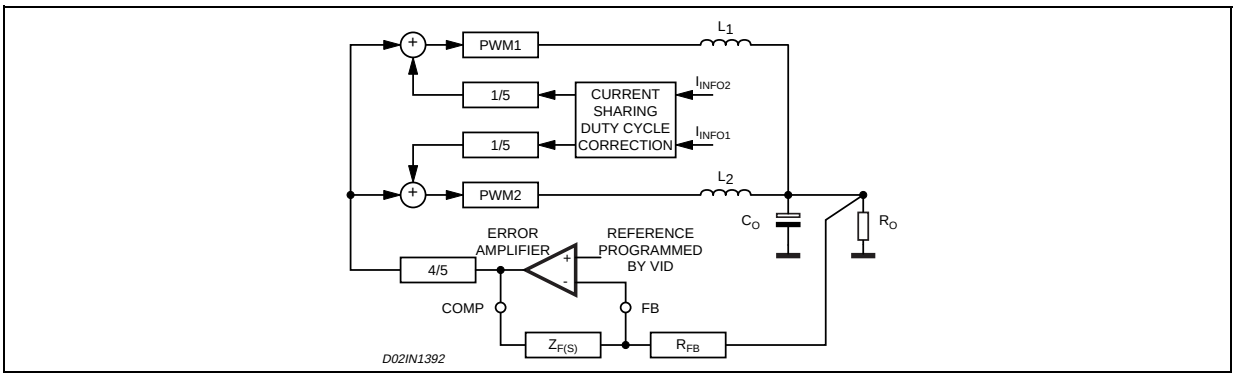


Figure 12 – Inductor ripple current vs. Vout

MAIN CONTROL LOOP

The four phases control loop is composed by two dual phases devices that are independent each other. So, the compensation network and the control loop stability of each device don't depend on the other except for the fact that the other converter represents a load for this one.
The L6918/A control loop is composed by the Current Sharing control loop and the Average Current Mode control loop. Each loop gives, with a proper gain, the correction to the PWM in order to minimize the error in its regulation: the Current Sharing control loop equalize the currents in the inductors while the Average Current Mode control loop fixes the output voltage equal to the reference programmed by VID. Figure 12 reports the block diagram of the main control loop

Figure 12. Main Control Loop Diagram



CURRENT SHARING (CS) CONTROL LOOP

The devices are configured to work in a four synchronized phase application. Since the application is composed by two-phase devices that share reference and synchronization signals, the current sharing between the phases is realized in two different steps:

1. Sharing between the phases of the same device;
2. Sharing between devices.

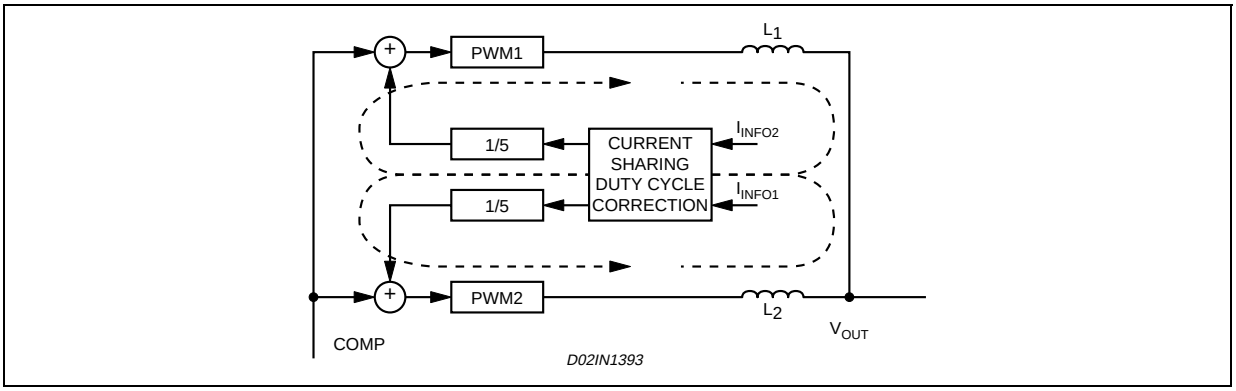
The Current Sharing between phases of the same device uses the internal current information to correct the PWM signal in order to equalize the current. Active current sharing is implemented using the information from Tran conductance differential amplifier in an average current mode control scheme. A current reference equal to the average of the read current (I_{AVG}) is internally built; the error between the read current and this reference is converted to a voltage with a proper gain and it is used to adjust the duty cycle whose dominant value is set by the error amplifier at COMP pin (See fig. 13).
The current sharing control is a high bandwidth control allowing current sharing even during load transients.

The current sharing error is affected by the choice of external components; choose precise Rg resistor (±1% is necessary) to sense the current. The current sharing error is internally dominated by the voltage mismatch of Tran conductance differential amplifier between phases; considering a voltage mismatch equal to 2mV across the sense resistor, the current reading error is given by the following equation:

$$\frac{\Delta I_{READ}}{I_{MAX}} = \frac{2mV}{R_{SENSE} \cdot I_{MAX}}$$

Where ΔI_{READ} is the difference between one phase current and the ideal current ($I_{MAX/2}$).
For Rsense=4mΩ and Imax=40A the current sharing error is equal to 2.5%, neglecting errors due to Rg and Rsense mismatches.

Figure 13. Current Sharing Control Loop.



The current sharing between devices uses the droop function. Each device can be modeled with its Thevenin equivalent circuit (that is an ideal voltage source equal to the programmed voltage by VIDs and its related output resistance R_{OUT}), while the whole converter is modeled by the same ideal voltage source and an equivalent output resistance $R_{DROOP}=R_{OUT}/2$;

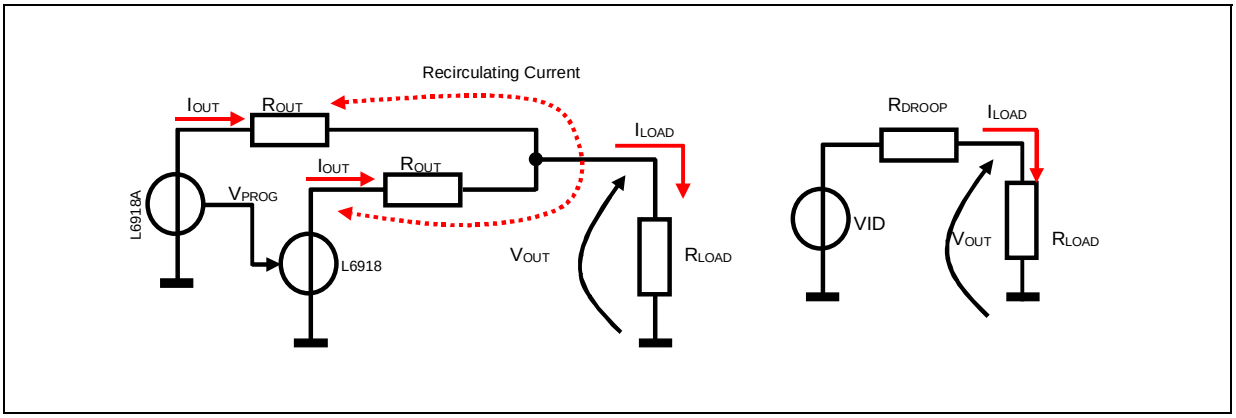
Considering this modelization reported in figure 14, it can be seen that the recirculating current between devices depends on the accuracy of the regulation.
The accuracy of the voltage source is given by the offset of the master error amplifier Vos (6mV typ) and depends on the ratio between this offset and the output voltage variation with load (R_{OUT},I_{OUT}). The mismatch between the regulated voltages causes a converter to source a current that is sunk by the other one. The accuracy related to droop resistance depends on precision of feedback current of the device I_{FB}, sense resistors R_{SENSE}, Transconductance resistors Rg and feedback resistors R_{FB}.
The current sharing error (CSE) results:

$$CSE = \frac{\Delta I_{OUT}}{I_{OUT}} \equiv \sqrt{\frac{1}{2}\left(\frac{Vos}{R_{OUT}\cdot I_{OUT}}\right)^2 + \frac{1}{2}\left(\frac{\Delta I_{FB}}{I_{FB}}\right)^2 + \frac{1}{2}\left(\frac{\Delta R_{FB}}{R_{FB}}\right)^2 + \frac{2}{2}\left(\frac{\Delta R_{SENSE}}{R_{SENSE}}\right)^2 + \frac{4}{2}\left(\frac{\Delta R_g}{R_g}\right)^2}$$

Considering the external resistors tolerance of 1%, the typical current feedback accuracy of 2.5µA/50µA (5%), 4 phases operation, Error Amplifier offset Vos=6mV, droop resistance R_{DROOP}=1.5mΩ (R_{OUT}=2,R_{DROOP}) and I_{LOAD}=60A ($I_{OUT}=I_{LOAD}/2$), it results:

$$CSE = \sqrt{\frac{1}{2}\left(\frac{0.006V}{1.5m\Omega\cdot 60A}\right)^2 + \frac{1}{2}\left(\frac{2.5\mu A}{50\mu A}\right)^2 + \frac{1}{2}(0.01)^2 + \frac{2}{2}(0.01)^2 + \frac{4}{2}(0.01)^2} = 0.062(6.2\%)$$

Figure 14. Equivalent Circuit for current sharing error calculation



AVERAGE CURRENT MODE (ACM) CONTROL LOOP

The average current mode control loop is reported in figure 15. The current information I_{FB} sourced by the FB pin flows into R_{FB} implementing the dependence of the output voltage from the read current.

The ACM control loop gain results (obtained opening the loop after the COMP pin):

$$G_{LOOP}(s) = -\frac{PWM \cdot Z_F(s) \cdot (R_{DROOP} + Z_P(s))}{(Z_P(s) + Z_L(s)) \cdot \left[\frac{Z_F(s)}{A(s)} + \left(1 + \frac{1}{A(s)}\right) \cdot R_{FB}\right]}$$

where:

- $R_{DROOP} = \frac{Rsense}{Rg} \cdot R_{FB}$ is the equivalent output resistance determined by the droop function;
- $Z_P(s)$ is the impedance resulting by the parallel of the output capacitor (and its ESR) and the applied load Ro;
- $Z_F(s)$ is the compensation network impedance;
- $Z_L(s)$ is the parallel of the two inductor impedance;
- A(s) is the error amplifier gain;
- $PWM = \frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}}$ is the ACM PWM transfer function where ΔV_{osc} is the oscillator ramp amplitude and has a typical value of 2V

Removing the dependence from the Error Amplifier gain, so assuming this gain high enough, the control loop gain results:

$$G_{LOOP}(s) = -\frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{Z_F(s)}{Z_P(s) + Z_L(s)} \cdot \left(\frac{Rs}{Rg} + \frac{Z_P(s)}{R_{FB}}\right)$$

With further simplifications, it results:

$$G_{LOOP}(s) = -\frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{Z_F(s)}{R_{FB}} \cdot \frac{Ro + R_{DROOP}}{Ro + \frac{R_L}{2}} \frac{1 + s \cdot Co \cdot (R_{DROOP} // Ro + ESR)}{s^2 \cdot Co \cdot \frac{L}{2} + s \cdot \left[\frac{L}{2 \cdot Ro} + Co \cdot ESR + Co \cdot \frac{R_L}{2}\right] + 1}$$

Considering now that in the application of interest it can be assumed that $Ro >> R_L$; $ESR << Ro$ and $R_{DROOP} << Ro$, it results:

$$G_{LOOP}(s) = -\frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{Z_F(s)}{R_{FB}} \cdot \frac{1 + s \cdot Co \cdot (R_{DROOP} + ESR)}{s^2 \cdot Co \cdot \frac{L}{2} + s \cdot \left[\frac{L}{2 \cdot Ro} + Co \cdot ESR + Co \cdot \frac{R_L}{2}\right] + 1}$$

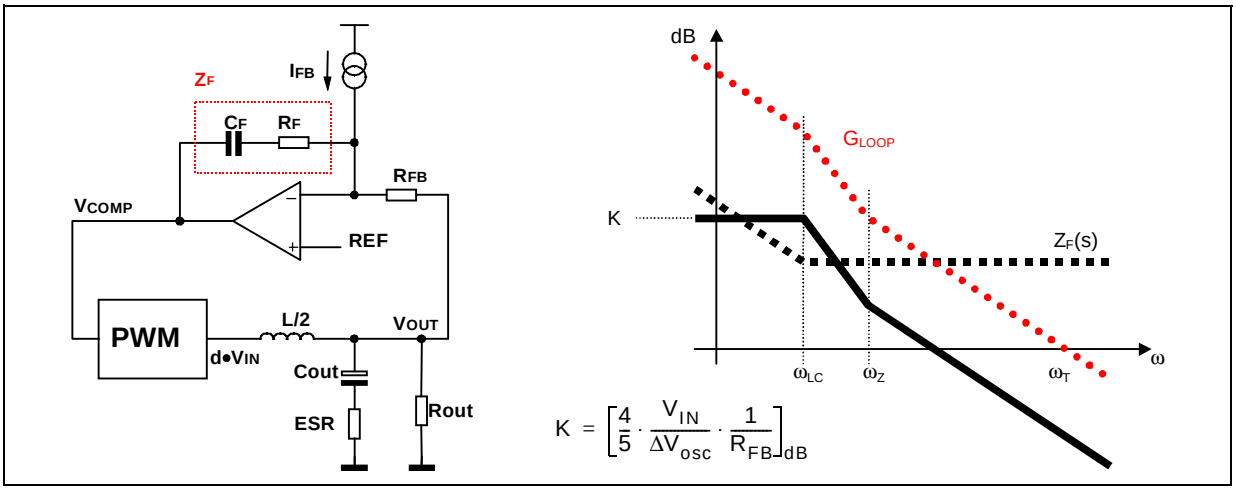
The ACM control loop gain is designed to obtain a high DC gain to minimize static error and cross the 0dB axes with a constant -20dB/dec slope with the desired crossover frequency ωT. Neglecting the effect of $Z_F(s)$, the transfer function has one zero and two poles. Both the poles are fixed once the output filter is designed and the zero is fixed by ESR and the Droop resistance.

To obtain the desired shape an R_F-C_F series network is considered for the $Z_F(s)$ implementation.

A zero at $\omega_f = 1/R_F C_F$ is then introduced together with an integrator. This integrator minimizes the static error

while placing the zero in correspondence with the L-C resonance a simple -20dB/dec shape of the gain is assured (See Figure 15). In fact, considering the usual value for the output filter, the LC resonance results to be at frequency lower than the above reported zero.

Figure 15. ACM Control Loop Gain Block Diagram (left) and Bode Diagram (right).



Compensation network can be simply designed placing $\omega_Z=\omega_{LC}$ and imposing the cross-over frequency ω_T as desired obtaining:

$$R_F = \frac{R_{FB}\cdot\Delta V_{OSC}}{V_{IN}}\cdot\frac{5}{4}\cdot\omega_T\cdot\frac{L}{2\cdot(R_{DROOP}+ESR)} \qquad C_F = \frac{\sqrt{Co\cdot\frac{L}{2}}}{R_F}$$

In a four phase operation (since the four phase converter is realized by two dual phase converters in parallel that shares current using droop), also the other sub-system in parallel must be considered. In particular, in the above reported relationships, it must be considered with Co and ESR the total output capacitance and equivalent ESR while the output impedance Zo of the other sub-system must be considered in parallel to the output capacitance Co and to the load Ro.

The output impedance of the other sub-system in parallel results:

$$Zo(s) = \frac{Z_L(s)+\frac{4}{5}\cdot\frac{V_{IN}}{\Delta V_{OSC}}\cdot\frac{Rsense}{Rg}\cdot Z_F(s)}{1+\frac{4}{5}\cdot\frac{V_{IN}}{\Delta V_{OSC}}\cdot\frac{Z_F(s)}{R_{FB}}}$$

Considering Zo in parallel to Ro, it can be verified that the R_F and C_F design relationships are still valid.

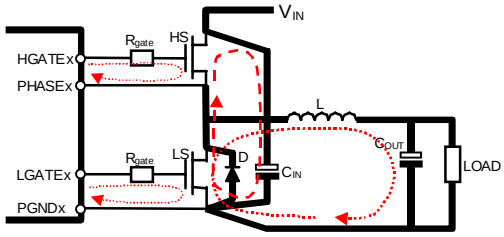
LAYOUT GUIDELINES

Since the device manages control functions and high-current drivers, layout is one of the most important things to consider when designing such high current applications.
A good layout solution can generate a benefit in lowering power dissipation on the power paths, reducing radiation and a proper connection between signal and power ground can optimize the performance of the control loops.
Integrated power drivers reduce components count and interconnections between control functions and drivers, reducing the board space.
Here below are listed the main points to focus on when starting a new layout and rules are suggested for a correct implementation.

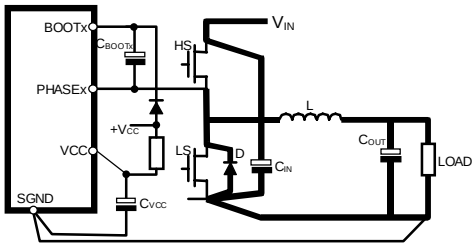
Power Connections.

These are the connections where switching and continuous current flows from the input supply towards the load. The first priority when placing components has to be reserved to this power section, minimizing the length of each connection as much as possible.
To minimize noise and voltage spikes (EMI and losses) these interconnections must be a part of a power plane and anyway realized by wide and thick copper traces. The critical components, i.e. the power transistors, must be located as close as possible, together and to the controller. Considering that the "electrical" components reported in figure are composed by more than one "physical" component, a ground plane or "star" grounding connection is suggested to minimize effects due to multiple connections.
Fig. 16a shows the details of the power connections involved and the current loops. The input capacitance (CIN), or at least a portion of the total capacitance needed, has to be placed close to the power section in order to eliminate the stray inductance generated by the copper traces. Low ESR and ESL capacitors are required.

Figure 16. Power connections and related connections layout guidelines (same for both phases).



a. PCB power and ground planes areas



b. PCB small signal components placement

Power Connections Related.

Fig.16b shows some small signal components placement, and how and where to mix signal and power ground planes.

The distance from drivers and mosfet gates should be reduced as much as possible. Propagation delay times as well as for the voltage spikes generated by the distributed inductance along the copper traces are so minimized. In fact, the further the mosfet is from the device, the longer is the interconnecting gate trace and as a consequence, the higher are the voltage spikes corresponding to the gate PWM rising and falling signals. Even if these spikes are clamped by inherent internal diodes, propagation delays, noise and potential causes of instabilities are introduced jeopardizing good system behavior. One important consequence is that the switching losses for the high side mosfet are significantly increased.
For this reason, it is suggested to have the device oriented with the driver side towards the mosfets and the GATEx and PHASEx traces walking together toward the high side mosfet in order to minimize distance (see fig 17). In addition, since the PHASEx pin is the return path for the high side driver, this pin must be connected directly to the High Side mosfet Source pin to have a proper driving for this mosfet. For the LS mosfets, the return path is the PGND pin: it can be connected directly to the power ground plane (if implemented) or in the same way to the LS mosfets Source pin. GATEx and PHASEx connections (and also PGND when no power ground plane is implemented) must also be designed to handle current peaks in excess of 2A (30 mils wide is suggested).

Figure 17. Device orientation (left) and sense nets routing (right).

Gate resistors of few ohms help in reducing the power dissipated by the IC without compromising the system efficiency.

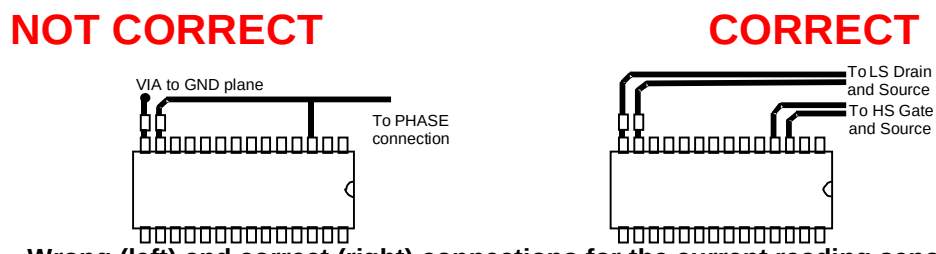
The placement of other components is also important:

- The bootstrap capacitor must be placed as close as possible to the BOOTx and PHASEx pins to minimize the loop that is created.
- Decoupling capacitor from Vcc and SGND placed as close as possible to the involved pins.
- Decoupling capacitor from VCCDR and PGND placed as close as possible to those pins. This capacitor sustains the peak currents requested by the low-side mosfet drivers.
- Refer to SGND all the sensible components such as frequency set-up resistor (when present) and also the optional resistor from FB to GND used to give the positive droop effect.
- Connect SGND to PGND on the load side (output capacitor) to avoid undesirable load regulation effect and to ensure the right precision to the regulation when the remote sense buffer is not used.
- An additional 100nF ceramic capacitor is suggested to place near HS mosfet drain. This helps in reducing noise.
- PHASE pin spikes. Since the HS mosfet switches in hard mode, heavy voltage spikes can be observed on the PHASE pins. If these voltage spikes overcome the max breakdown voltage of the pin, the device can absorb energy and it can cause damages. The voltage spikes must be limited by proper layout, the use of gate resistors, Schottky diodes in parallel to the low side mosfets and/or snubber network on the low side mosfets, to a value lower than 26V, for 20nSec, at Fosc of 600kHz max.

Current Sense Connectio ns.

- **Remote Buffer:** The input connections for this component must be routed as parallel nets from the FBG/FBR pins to the load in order to compensate losses along the output power traces and also to avoid the pick-up of any common mode noise. Connecting these pins in points far from the load will cause a non-optimum load regulation, increasing output tolerance.
- **Current Reading:** The Rg resistor has to be placed as close as possible to the ISENx and PGNDSx pins in order to limit the noise injection into the device. The PCB traces connecting these resistors to the reading point must be routed as parallel traces in order to avoid the pick-up of any common mode noise. It's also important to avoid any offset in the measurement and to get a better precision, to connect the traces as close as possible to the sensing elements, dedicated current sense resistor or low side mosfet R_{dsON}.
- Moreover, when using the low side mosfet R_{dsON} as current sense element, the ISENx pin is practically connected to the PHASEx pin. DO NOT CONNECT THE PINS TOGETHER AND THEN TO THE HS SOURCE! The device won't work properly because of the noise generated by the return of the high side driver. In this case route two separate nets: connect the PHASEx pin to the HS Source (route together with HGATEx) with a wide net (30 mils) and the ISENx pin to the LS Drain (route together with PGNDSx). Moreover, the PGNDSx pin is always connected, through the Rg resistor, to the PGND: DO NOT CONNECT DIRECTLY TO THE PGND! In this case the device won't work properly. Route anyway to the LS mosfet source (together with ISENx net).
  Right and wrong connections are reported in Figure 18.
  Symmetrical layout is also suggested to avoid any unbalance between the two phases of the converter

Figure 18. PCB layout connections for sense nets.



Wrong (left) and correct (right) connections for the current reading sensing nets.

Interconnections between devices.

Master and Slave devices share reference and other signals for the regulation. To avoid noise injection into devices, it is recommended to route these nets carefully.

- **VPROG_IN / VPROG_OUT:** This is the reference for the regulation. It must be routed far away from any noisy trace and guarded by ground traces in order to avoid noise injection into the device. It can be filtered with a 30nF maximum of distributed capacitance vs. signal ground.
- **SLAVE_OK:** This signal is used by the devices for the start-up synchronization and also to communicate UVP from Slave to Master device. It must be filtered by 1nF capacitor near the pin of each device to avoid the noise to cause false protection's trigger.

Demo Board Description

The L6918 demo board shows the operation of the device in a four phases application. This evaluation board allows output voltage adjustability (1.100V - 1.850V) through the switches S0-S4 and high output current capability.

The board has been laid out with the possibility to use up to two D^2PACK mosfets for the low side switch in order to give maximum flexibility in the mosfet choice.

The four layers demo board's copper thickness is of 70µm in order to minimize conduction losses considering the high current that the circuit is able to deliver.

Demo board schematic circuit is reported in Figure 19.

Several jumpers allow setting different configurations for the device: JP3, JP4 and JP5 allow configuring the remote buffer as desired. Simply shorting JP4 and JP5 the remote buffer is enabled and it senses the output voltage on-board; to implement a real remote sense, leave these jumpers open and connect the FBG and FBR connectors on the demo board to the remote load. To avoid using the remote buffer, simply short all the jumpers JP3, JP4 and JP5. Local sense through the R7 is used for the regulation.

The input can be configured in different ways using the jumpers JP1, JP2 and JP6; these jumpers control also the mosfet driver supply voltage. Anyway, power conversion starts from V_{IN} and the device is supplied from V_{CC} (See Figure 20).

Figure 19. Demo Board Schematic

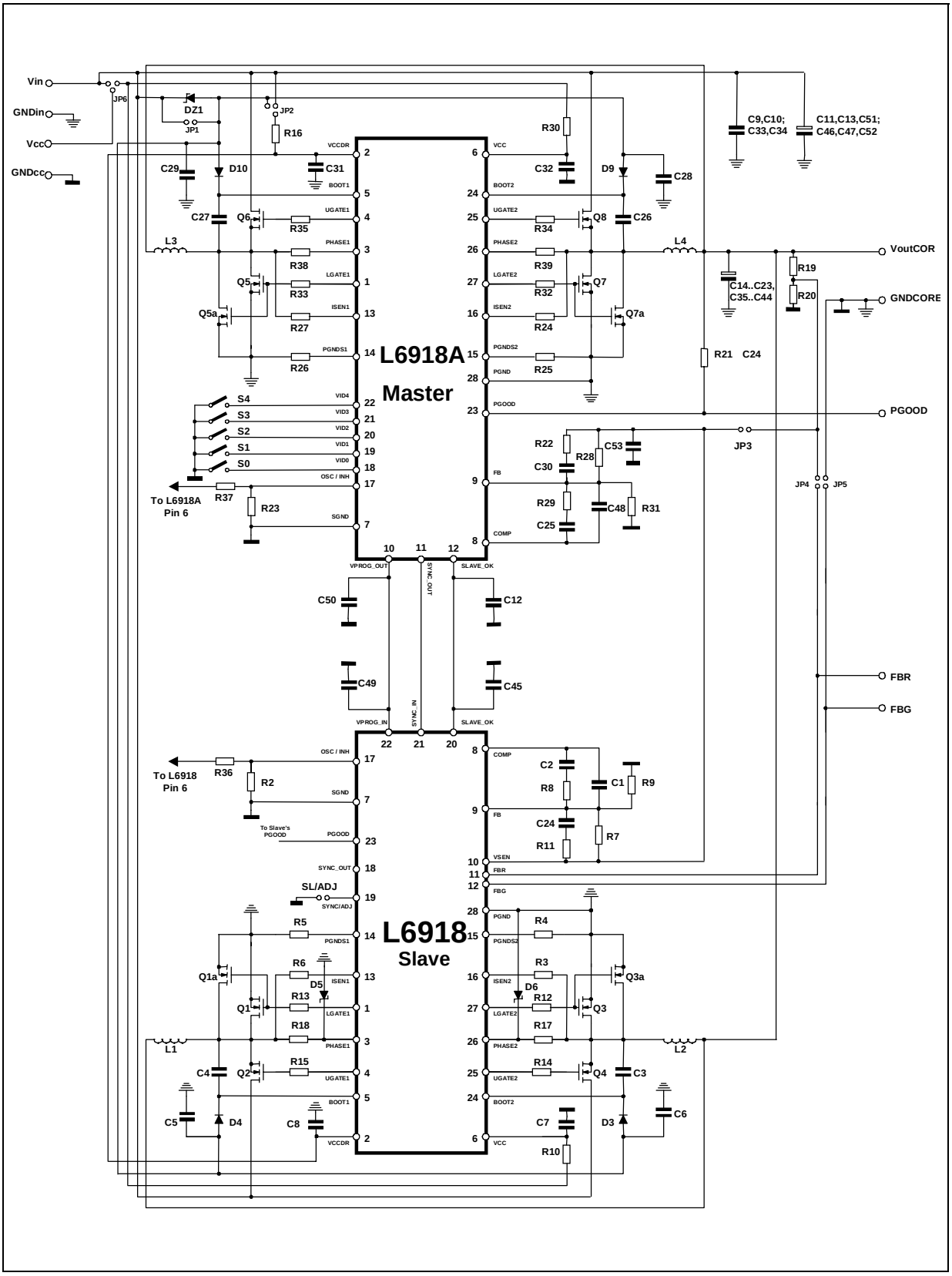
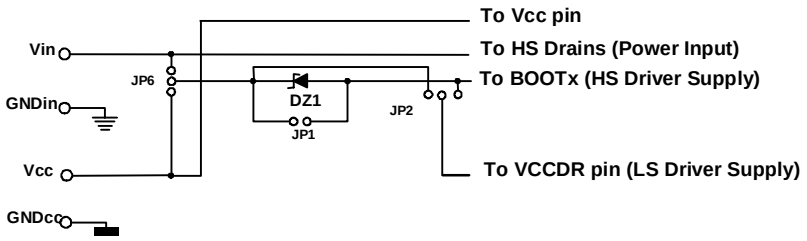


Figure 20. Power supply configuration



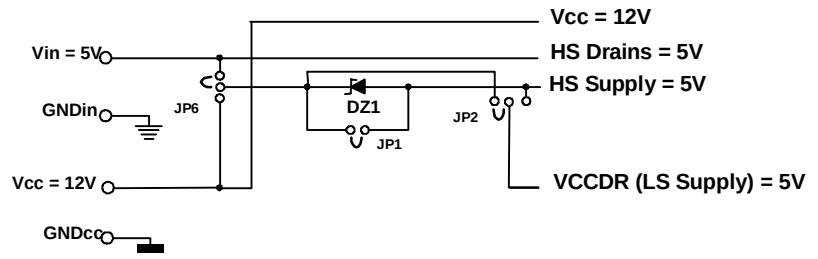
Two main configurations can be distinguished: Single Supply (V_{CC} = V_{IN} = 12V) and Double Supply (V_{CC} = 12V V_{IN} = 5V or different).

– Single Supply: In this case JP6 has to be completely shorted. The device is supplied with the same rail that is used for the conversion. With an additional zener diode DZ1 a lower voltage can be derived to supply the mosfets driver if Logic level mosfet are used. In this case JP1 must be left open so that the HS driver is supplied with V_{IN}-V_{DZ1} through BOOTx and JP2 must be shorted to the left to use V_{IN} or to the right to use V_{IN}-V_{DZ1} to supply the LS driver through VCCDR pin. Otherwise, JP1 must be shorted and JP2 can be freely shorted in one of the two positions.

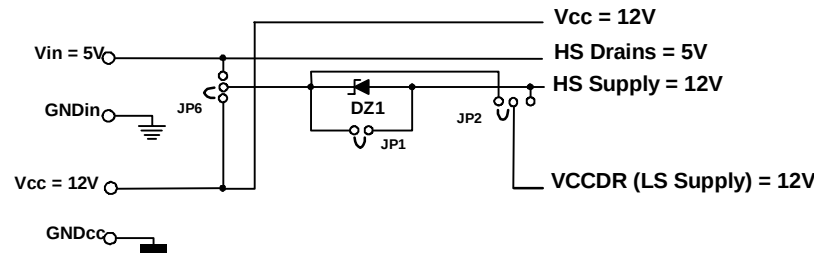
– Double Supply: In this case V_{CC} supply directly the controller (12V) while VIN supplies the HS drains for the power conversion. This last one can start indifferently from the 5V bus (Typ.) or from other buses allowing maximum flexibility in the power conversion. Supply for the mosfet driver can be programmed through the jumpers JP1, JP2 and JP6 as previously illustrated. JP6 selects now V_{CC} or V_{IN} depending on the requirements.

Some examples are reported in the following Figures 21 and 22.

Figure 21. Jumpers configuration: Double Supply

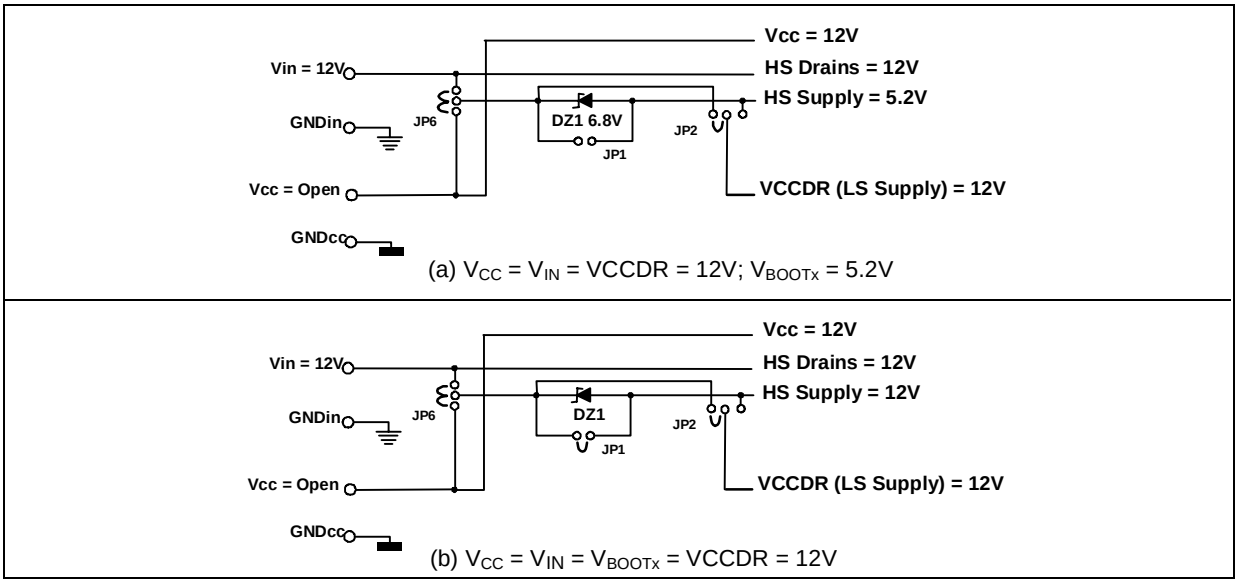


(a) V_{CC} = 12V; V_{BOOTx} = VCCDR = V_{IN} = 5V



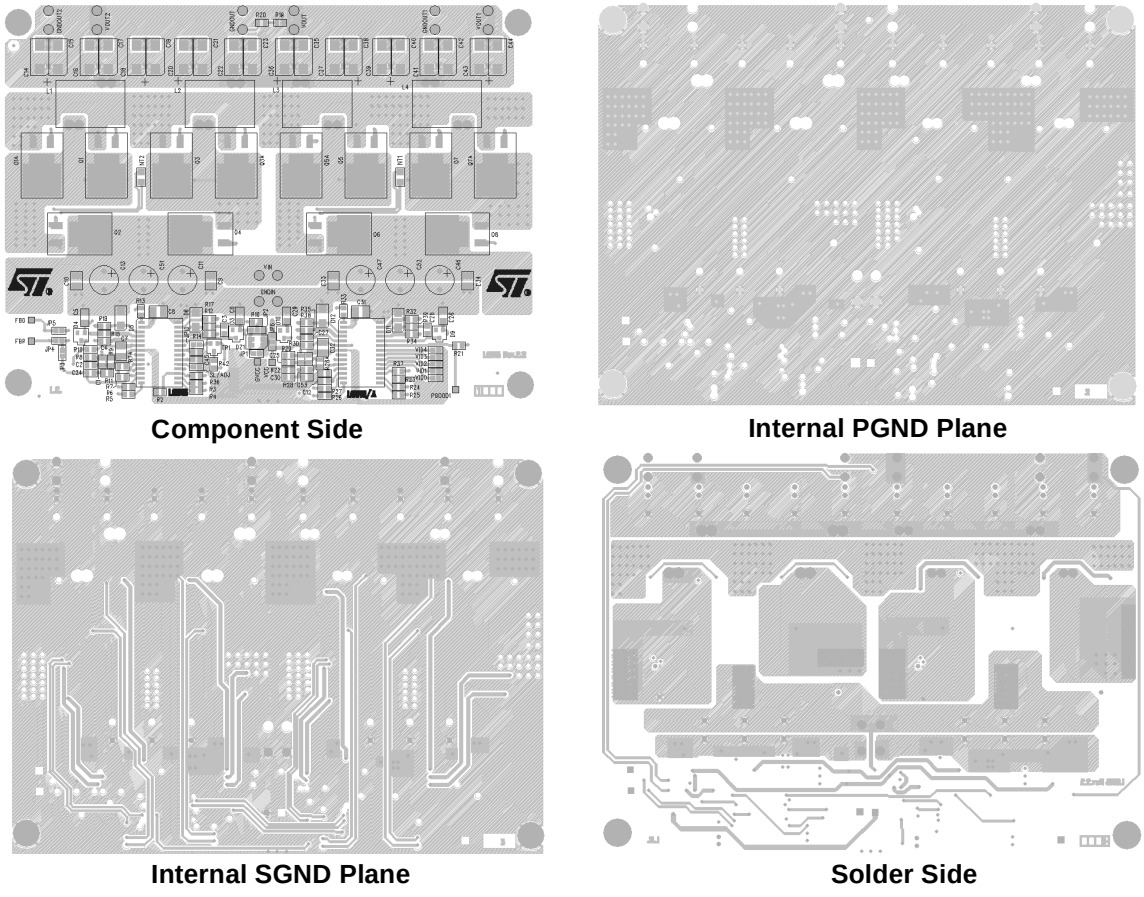
(b) V_{CC} = V_{BOOTx} = VCCDR = 12V; V_{IN} = 5V

Figure 22. Jumpers configuration: Single Supply



PCB AND COMPONENT LAYOUT

Figure 23. PCB and Components Layouts (Dimensions: 10.8mm x 14.5mm)



CPU Power Supply: $12V_{IN}$; $1.45V_{OUT}$; $110A_{DC}$

Considering the high slope for the load transient, a high switching frequency has to be used. In addition to fast reaction, this helps in reducing output and input capacitor. Inductance value is also reduced.

A switching frequency of 200kHz for each phase is then considered allowing large bandwidth for the compensation network. Considering the high output current, power conversion will start from the 12V bus.

– Current Reading Network and Over Current:
Since the maximum output current is I_{MAX} = 110A, the over current threshold has been set to 110A (27.5A x 4) in the worst case (max mosfet temperature). Since the device limits the valley of the triangular ripple across the inductors, the current ripple must be considered too. Considering the inductor core saturation, a current ripple of 10A has to be considered so that the OCP threshold in worst case becomes OCPx = 22A (27.5A-5A). Considering to sense the output current across the low-side mosfets RdsON (two in parallel to reduce equivalent R_{dsON}), each STB90NF03L has 6.5mΩ max at 25°C that becomes 9.1mΩ at 100°C considering the temperature variation; the resulting transconductance resistor Rg has to be:

$$Rg = I_{OCPx} \cdot \frac{R_{dsON}}{35\mu} = 22 \cdot \frac{4.5m}{35\mu} = 2.7k\Omega \quad \text{(R3 to R6; R24 to R27)}$$

– Droop function Design:
Considering a voltage drop of 85mV at full load, the feedback resistor R_{FB} has to be:

$$R_{FB} = \frac{85mV}{70\mu A} = 1.2k\Omega \quad \text{(R7)}$$

– Inductor design:
Transient response performance needs a compromise in the inductor choice value: the biggest the inductor, the highest the efficient but the worse the transient response and vice versa. Considering then an inductor value of 1µH, the current ripple becomes:

$$\Delta I = \frac{Vin - Vout}{L} \cdot \frac{d}{Fsw} = \frac{12 - 1.4}{1\mu} \cdot \frac{1.4}{12} \cdot \frac{1}{200k} = 6.2A \quad \text{(L1, L2)}$$

– Output Capacitor:
Ten Rubycon MBZ (3300µF / 6.3V / 12mΩ max ESR) has been used implementing a resulting ESR of 1.2mΩ resulting in an ESR voltage drop of 52A*1.2mΩ = 62mV after a 52A load transient.

– Compensation Network:
A voltage loop bandwidth of 20kHz is considered to let the device fast react after load transient.
The R_F C_F network results:

$$R_F = \frac{R_{FB} \cdot \Delta V_{OS}}{V_{IN}} \cdot \frac{5}{4} \cdot \omega_T \cdot \frac{L}{2 \cdot (R_{DROOP} + ESR)} = \frac{1.2K \cdot 2}{12} \cdot \frac{5}{4} \cdot 20k \cdot 2\Pi \cdot \frac{1\mu}{2 \cdot \left(\frac{4.5m}{2.7} \cdot 1k + 1.2m\right)} = 3.9k\Omega \quad \text{(R8)}$$

$$C_F = \frac{\sqrt{Co \cdot \frac{L}{2}}}{R_F} = \frac{\sqrt{6 \cdot 3300\mu \cdot \frac{1\mu}{2}}}{3.9k} = 22nF \quad \text{(C2)}$$

Further adjustments can be done on the work bench to fit the requirements and to compensate layout parasitic components.

Part List

Resistors			
R2, R9, R20, R23, R31, R42	Not Mounted		SMD 0805
R3, R4, R5, R6 R24, R25, R26, R27	2.7K	1%	SMD 0805
R7, R28	1.2K	1%	SMD 0805
R11, R22	510		SMD 0805
R12 to R19 R32, R33, R34, R35, R38, R39	0		SMD 0805
R8, R29	3.9K		SMD 0805
R10, R30	82		SMD 0805
R21	10K		SMD 0805
R36, R37	1M	1%	SMD 0805
Capacitors			
C1, C48	Not Mounted		SMD 0805
C2, C25	47n		SMD 0805
C24, C30	100n		SMD 0805
C3, C4, C26, C27	100n		SMD 0805
C5, C6, C7, C28, C29, C32	1µ		SMD 0805
C8, C31	10µ		SMD 1206
C9, C10, C33, C34	10µ or 22µ / 16V	TDK Multilayer Ceramic	SMD 1206
C11, C13, C46, C47, C51, C52	1800µ / 16V	Rubycon MBZ	Radial 23x10.5
C12, C45, C49, C50	1n		SMD 0805
C53	1n		SMD 0805
C14, C16, C18, C20, C22 C35, C37, C39, C41, C43	3300µ /6.3V	Rubycon MBZ	Radial 23x10.5
Diodes			
D3, D4, D9, D10	1N4148		SOT23
DZ1	Not Mounted		MINIMELF
Mosfets			
Q1, Q1A, Q3, Q3A, Q5, Q5A, Q7, Q7A	STB90NF03L	STMicroelectronics	D2PACK
Q2, Q4, Q6, Q8	STB90NF03L	STMicroelectronics	D2PACK
Inductors			
L1, L2, L3, L4	1µ	77121 Core / 5 Turns 2 x 1.5 mm	
Controllers			
U2	L6918	STMicroelectronics	SO28

STATIC PERFORMANCES

Figure 24 shows the demo board measured efficiency versus load current in steady state conditions without air-flow at ambient temperature.

Figure 24. System Efficiency

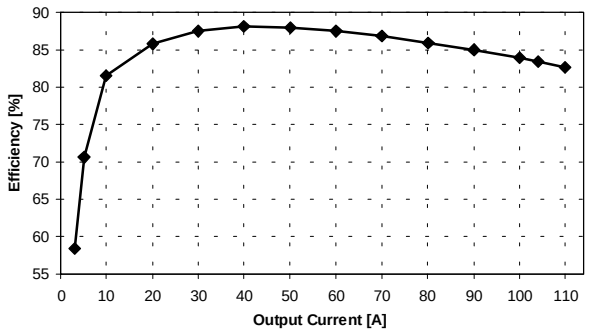
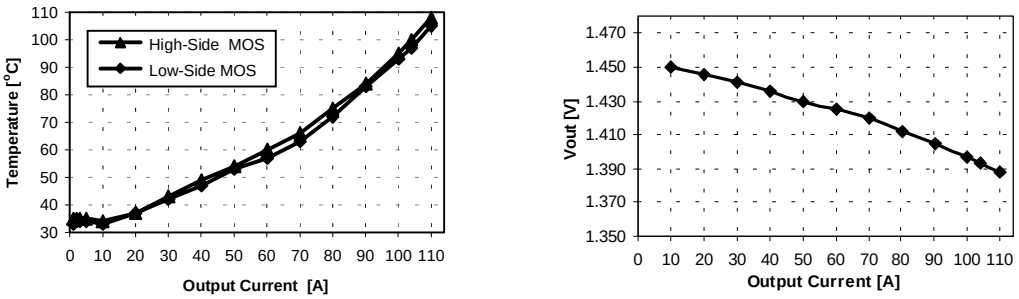


Figure 25 shows the mosfets temperature versus output current in steady state condition without any air-flow or heat sink. It can be observed that the mosfets are under 100°C in any conditions. Load regulation is also reported from 10A to 110A.

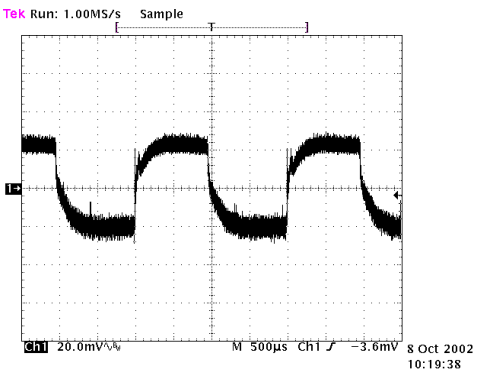
Figure 25. Mosfet Temperature and Load Regulation.



DYNAMIC PERFORMANCES

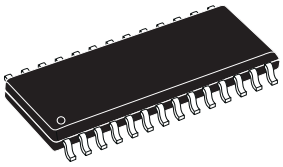
Figure 26 shows the system response to a load transient from 0A to 110A. The output voltage is contained in the ±50mV range. Additional output capacitors can help in reducing the initial voltage spike mainly due to the ESR.

Figure 26. 110A Load Transient Response.



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



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