1 MSPS, 12-Bit, Simultaneous Sampling SAR ADC with PGA and Four Comparators

Data Sheet **AD7262**

FEATURES

- Dual simultaneous sampling 12-bit, 2-channel analog-to-digital converter (ADC)
- True differential analog inputs
- Programmable gain stage: ×1, ×2, ×3, ×4, ×6, ×8, ×12, ×16, ×24, ×32, ×48, ×64, ×96, ×128
- Throughput rate per ADC
  - 1 MSPS for AD7262
  - 500 kSPS for AD7262-5
- Analog input impedance: >1 GΩ
- Wide input bandwidth
  - −3 dB bandwidth: 1.7 MHz at gain = 2
- 4 on-chip comparators
- SNR: 73 dB typical at gain = 2, 66 dB typical at gain = 32
- Device offset calibration, system gain calibration
- On-chip reference: 2.5 V
- −40°C to +105°C operation
- High speed serial interface
  - SPI/QSPI™/MICROWIRE/DSP compatible
- 48-lead LFCSP and LQFP

GENERAL DESCRIPTION

The AD7262/AD7262-5 are dual, 12-bit, high speed, low power, successive approximation ADCs that operate from a single 5 V power supply. The AD7262 features throughput rates of up to 1 MSPS per on-chip ADC. The AD7262-5 features throughput rates of up to 500 kSPS. Two complete ADC functions allow simultaneous sampling and conversion of two channels. Each ADC is preceded by a true differential analog input with a PGA. There are 14 gain settings available: ×1, ×2, ×3, ×4, ×6, ×8, ×12, ×16, ×24, ×32, ×48, ×64, ×96, and ×128.

The AD7262/AD7262-5 contain four comparators. Comparator A and Comparator B are optimized for low power, while Comparator C and Comparator D have fast propagation delays. The AD7262/AD7262-5 feature a calibration function to remove any device offset error and programmable gain adjust registers to allow for input path (for example, sensor) offset and gain compensation. The AD7262/AD7262-5 have an on-chip 2.5 V reference that can be disabled if an external reference is preferred.

The AD7262/AD7262-5 are ideally suited for monitoring small amplitude signals from a variety of sensors. They include all the functionality needed for monitoring the position feedback signals from a variety of analog encoders used in motor control systems.

FUNCTIONAL BLOCK DIAGRAM

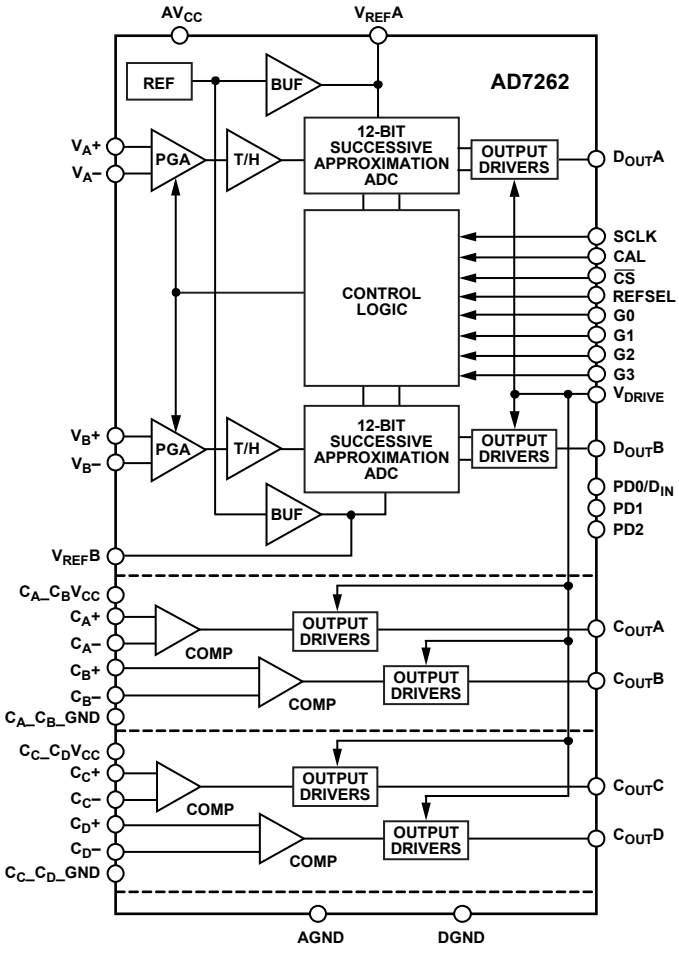

Figure 1.

PRODUCT HIGHLIGHTS

1. Integrated PGA with a variety of flexible gain settings to allow detection and conversion of low level analog signals.
2. Each PGA is followed by a dual simultaneous sampling ADC, featuring throughput rates of 1 MSPS per ADC for the AD7262. The conversion results of both ADCs are simultaneously available on separate data lines or in succession on one data line if only one serial port is available.
3. Four integrated comparators that can be used to count signals from pole sensors in motor control applications.
4. Internal 2.5 V reference.

Rev. C Document Feedback

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7/2008—Revision 0: Initial Version

SPECIFICATIONS

AV_{CC} = 4.75 V to 5.25 V, $C_A\_C_BV_{CC}$ = $C_C\_C_DV_{CC}$ = 2.7 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, f_{SAMPLE} = 1 MSPS and f_{SCLK} = 40 MHz for AD7262, f_{SAMPLE} = 500 kSPS and f_{SCLK} = 20 MHz for AD7262-5, V_{REF} = 2.5 V internal/external; T_A = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]					f_{IN} = 100 kHz sine wave
Signal-to-Noise Ratio (SNR)[2]	70	73		dB	PGA gain setting = 2
Signal-to-(Noise + Distortion) Ratio (SINAD)[2]	70	72		dB	
Total Harmonic Distortion (THD)[2]		−85	−77	dB	
Spurious-Free Dynamic Range (SFDR)[2]		−97		dB	
Common-Mode Rejection Ratio (CMRR)[3]		−76		dB	For PGA gain setting = 2, ripple frequency of 50 Hz/60 Hz; see Figure 17 and Figure 18
ADC-to-ADC Isolation[3]		−90		dB	
Bandwidth[3]		1.2		MHz	@ −3 dB; PGA gain setting = 128
		1.7		MHz	@ −3 dB; PGA gain setting = 2
DC ACCURACY					
Resolution			12	Bits	
Integral Nonlinearity[2]		±0.5	±1	LSB	
Differential Nonlinearity[2]		±0.5	±0.99	LSB	Guaranteed no missed codes to 12 bits
Positive Full-Scale Error[2]		±0.122	±0.305	% FSR	Pregain calibration
		±0.018		% FSR	Postgain calibration
Positive Full-Scale Error Match		±0.061		% FSR	
Zero Code Error[2]		±0.092	±0.244	% FSR	Preoffset and pregain calibration
		±0.012		% FSR	Postoffset and postgain calibration
Zero Code Error Match		±0.061		% FSR	
Negative Full-Scale Error[2]		±0.122	±0.305	% FSR	Pregain calibration
		±0.018		% FSR	Postgain calibration
Negative Full-Scale Error Match		±0.061		% FSR	
Zero Code Error Drift		2.5		µV/°C	
ANALOG INPUT					
Input Voltage Range, V_{IN}+ and V_{IN}−	$V_{CM} \pm \frac{V_{REF}}{2 \times Gain}$			V	V_{CM} = AV_{CC}/2; PGA gain setting ≥ 2
Common-Mode Voltage Range, V_{CM}	V_{CM} − 100 mV		V_{CM} + 100 mV	V	V_{CM} = 2; PGA gain setting = 1; see Figure 19[4]
	(V_{CC}/2) − 0.4		(V_{CC}/2) + 0.2	V	V_{CM} = AV_{CC}/2; PGA gain setting = 2
	(V_{CC}/2) − 0.4		(V_{CC}/2) + 0.4	V	V_{CM} = AV_{CC}/2; 3 ≤ PGA gain setting ≤ 32
	(V_{CC}/2) − 0.6		(V_{CC}/2) + 0.8	V	V_{CM} = AV_{CC}/2; PGA gain setting ≥ 48
DC Leakage Current		±0.001	±1	µA	
Input Capacitance[3]		5		pF	
Input Impedance[3]		1		GΩ	
REFERENCE INPUT/OUTPUT					
Reference Output Voltage[5]	2.495	2.5	2.505	V	2.5 V ± 5 mV max @ 25°C
Reference Input Voltage Range		2.5		V	
DC Leakage Current		±0.3	±1	µA	External reference applied to Pin V_{REF}A/Pin V_{REF}B
Input Capacitance[3]		20		pF	
V_{REF}A, V_{REF}B Output Impedance[3]		4		Ω	
Reference Temperature Coefficient		20		ppm/°C	
V_{REF} Noise[3]		20		µV rms	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
Input High Voltage, V_{INH}	$0.7 \times V_{DRIVE}$			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}			±1	μA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]		4		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2			V	
Output Low Voltage, V_{OL}			0.4	V	
Floating State Leakage Current			±1	μA	
Floating State Output Capacitance[3]		5		pF	
Output Coding		Twos complement			
CONVERSION RATE					
Conversion Time			$19 \times t_{SCLK}$	ns	
Track-and-Hold Acquisition Time	400			ns	
Throughput Rate			1	MSPS	AD7262
			500	kSPS	AD7262-5
COMPARATORS					
Input Offset					
Comparator A and Comparator B		±2	±4	mV	T_A = 25°C to 105°C only
Comparator C and Comparator D		±2	±4	mV	
Offset Voltage Drift		0.5		μV/°C	All comparators
Input Common-Mode Range[3]		0 to 4		V	$C_A\_C_BV_{CC}$ = 5 V
		0 to 1.7		V	$C_A\_C_BV_{CC}$ = 2.7 V
Input Capacitance[3]		4		pF	
Input Impedance[3]		1		GΩ	
I_{DD} Normal Mode (Static)[6]					25 pF load, C_{OUT}x = 0 V, V_{CM} = AV_{CC}/2, $V_{OVERDRIVE}$ = 200 mV differential
Comparator A and Comparator B		3		μA	$C_A\_C_BV_{CC}$ = 3.3 V
		6	8.5	μA	$C_A\_C_BV_{CC}$ = 5.25 V
Comparator C and Comparator D		60		μA	$C_C\_C_DV_{CC}$ = 3.3 V
		120	170	μA	$C_C\_C_DV_{CC}$ = 5.25 V
Propagation Delay Time					V_{CM} = AV_{CC}/2, $V_{OVERDRIVE}$ = 200 mV differential
High to Low, t_{PHL}					
Comparator A and Comparator B		1.4	3.5	μs	$C_A\_C_BV_{CC}$ = 2.7 V
		0.95		μs	$C_A\_C_BV_{CC}$ = 5 V
Comparator C and Comparator D		0.20	0.32	μs	$C_C\_C_DV_{CC}$ = 2.7 V
		0.13		μs	$C_C\_C_DV_{CC}$ = 5 V
Low to High, t_{PLH}					
Comparator A and Comparator B		2	4	μs	$C_A\_C_BV_{CC}$ = 2.7 V
		0.93		μs	$C_A\_C_BV_{CC}$ = 5 V
Comparator C and Comparator D		0.18	0.28	μs	$C_C\_C_DV_{CC}$ = 2.7 V
		0.12		μs	$C_C\_C_DV_{CC}$ = 5 V
Delay Matching					V_{CM} = AV_{CC} 2, $V_{OVERDRIVE}$ = 200 mV differential
Comparator A and Comparator B		±250		ns	
Comparator C and Comparator D		±10		ns	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					Digital inputs = 0 V or V_{DRIVE}
AV_{CC}	4.75		5.25	V	
$C_A\_C_BV_{CC}$, $C_C\_C_DV_{CC}$	2.7		5.25	V	
V_{DRIVE}	2.7		5.25	V	
I_{DD}					
ADC Normal Mode (Static)		20	31.5	mA	AV_{CC} = 5.25 V
ADC Normal Mode (Dynamic)		23	33.3	mA	AV_{CC} = 5.25 V
Shutdown Mode		0.5	1	µA	AV_{CC} = 5.25 V, ADCs and comparators powered down
Power Dissipation					
ADC Normal Mode (Static)		105	165	mW	
ADC Normal Mode (Dynamic)		120	175	mW	
Shutdown Mode		2.625	5.25	µW	

[1] These specifications were determined without the use of the gain calibration feature.
[2] See the Terminology section.
[3] Samples tested during initial release to ensure compliance; they are not subject to production testing.
[4] For PGA gain = 1; to use the full analog input range ($V_{CM} \pm V_{REF}/2$) of the AD7262, the V_{CM} voltage should be dropped to lie within a range from 1.95 V to 2.05 V.
[5] Refers to Pin $V_{REF}A$ or Pin $V_{REF}B$.
[6] This specification includes the I_{DD} for both comparators. The I_{DD} per comparator is the specified value divided by two.

TIMING SPECIFICATIONS

AV_{CC} = 4.75 V to 5.25 V, $C_A\_C_BV_{CC}$ = $C_C\_C_DV_{CC}$ = 2.7 V to 5.25 V, V_{REF} = 2.5 V internal/external; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}		Unit	Description
	2.7 V ≤ V_{DRIVE} ≤ 3.6 V	4.75 V ≤ V_{DRIVE} ≤ 5.25 V		
f_{SCLK}	200	200	kHz min	
	40	40	MHz max	AD7262[2]
	32	32	MHz typ	AD7262[2]
	20	20	MHz max	AD7262-5
$t_{CONVERT}$	19 × t_{SCLK}	19 × t_{SCLK}	ns max	t_{SCLK} = 1/f_{SCLK}
	475	475	ns max	AD7262
	950	950	ns max	AD7262-5
t_{QUIET}	13	13	ns min	Minimum time between end of serial read/bus relinquish and next falling edge of $\overline{CS}$
t_2	10	10	ns min	$\overline{CS}$ to SCLK setup time
t_3[3]	15	15	ns max	Delay from 19th SCLK falling edge until $D_{OUT}A$ and $D_{OUT}B$ are three-state disabled
t_4	29	23	ns max	Data access time after SCLK falling edge
t_5	15	13	ns min	SCLK to data valid hold time
t_6	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK high pulse width
t_7	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK low pulse width
t_8	13	13	ns min	$\overline{CS}$ rising edge to falling edge pulse width
t_9	13	13	ns max	$\overline{CS}$ rising edge to $D_{OUT}A$, $D_{OUT}B$, high impedance/bus relinquish
t_{10}	5	5	ns min	SCLK falling edge to $D_{OUT}A$, $D_{OUT}B$, high impedance
	35	35	ns max	SCLK falling edge to $D_{OUT}A$, $D_{OUT}B$, high impedance
t_{11}	2	2	µs min	Minimum CAL pin high time
t_{12}	2	2	µs min	Minimum time between the CAL pin high and the $\overline{CS}$ falling edge
t_{13}	3	3	ns min	D_{IN} setup time prior to SCLK falling edge
t_{14}	3	3	ns min	D_{IN} hold time after SCLK falling edge
$t_{POWER-UP}$	240	240	µs max	Internal reference, with a 1 µF decoupling capacitor
	15	15	µs max	With an external reference, 10 µs typical

[1] Sample tested during initial release to ensure compliance. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of AV_{CC}) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used. See the Terminology section.
[2] See the Serial Interface section.
[3] The time required for the output to cross 0.4 V or 2.4 V.

TIMING DIAGRAM

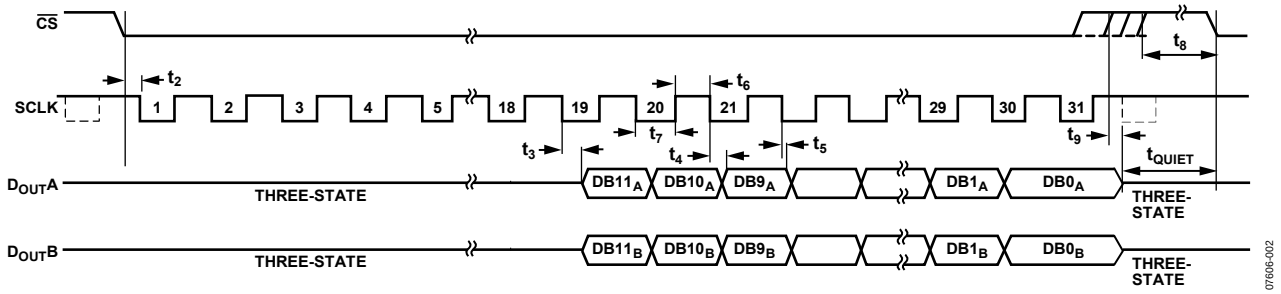


Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DRIVE} to DGND	−0.3 V to AV_{CC}
V_{DRIVE} to AGND	−0.3 V to AV_{CC}
AV_{CC} to AGND/DGND	−0.3 V to +7 V
C_A_$C_B V_{CC}$ to C_A_C_B_GND	−0.3 V to +7 V
C_C_$C_D V_{CC}$ to C_C_C_D_GND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
C_A_C_B_GND/C_C_C_D_GND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND	−0.3 V to AV_{CC} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
$V_{REF}A/V_{REF}B$ Input to AGND	−0.3 V to AV_{CC} + 0.3 V
$C_{OUT}A/C_{OUT}B/C_{OUT}C/C_{OUT}D$ to GND	−0.3 V to V_{DRIVE} + 0.3 V
$C_A\pm/C_B\pm/C_C\pm/C_D\pm$ to C_A_C_B_GND/C_C_C_D_GND	−0.3 V to C_A_$C_B V_{CC}/C_C$_$C_D V_{CC}$ + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
LFCSP	
θ_{JA} Thermal Impedance	30°C/W
θ_{JC} Thermal Impedance	3°C/W
LQFP	
θ_{JA} Thermal Impedance	55°C/W
θ_{JC} Thermal Impedance	16°C/W
Pb-Free Temperature, Soldering Reflow	255°C
ESD	2 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

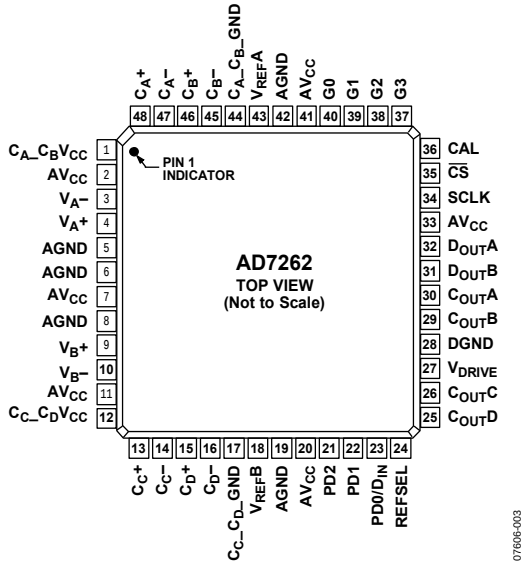
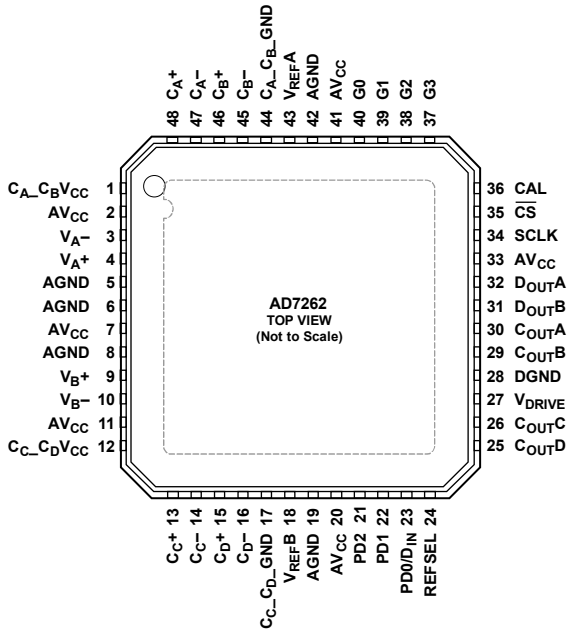


Figure 3. 48-Lead LQFP Pin Configuration



NOTES
1. THE EXPOSED METAL PADDLE ON THE BOTTOM OF THE LFCSP PACKAGE MUST BE SOLDERED TO PCB GROUND FOR PROPER HEAT DISSIPATION AND ALSO FOR NOISE AND MECHANICAL STRENGTH BENEFITS.

Figure 4. 48-Lead LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
2, 7, 11, 20, 33, 41	AV_{CC}	Analog Supply Voltage, 4.75 V to 5.25 V. This is the supply voltage for the analog circuitry on the AD7262/AD7262-5. All AV_{CC} pins can be tied together. Decouple this supply to AGND with a 100 nF ceramic capacitor per supply and a 10 µF tantalum capacitor.
1	$C_A\_C_BV_{CC}$	Comparator Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for Comparator A and Comparator B. Decouple this supply to $C_A\_C_B\_GND$. AV_{CC}, $C_C\_C_DV_{CC}$, and $C_A\_C_BV_{CC}$ can be tied together.
12	$C_C\_C_DV_{CC}$	Comparator Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for Comparator C and Comparator D. Decouple this supply to $C_C\_C_D\_GND$. AV_{CC}, $C_C\_C_DV_{CC}$, and $C_A\_C_BV_{CC}$ can be tied together.
4, 3	V_A+, V_A-	Analog Inputs of ADC A. True differential input pair.
9, 10	V_B+, V_B-	Analog Inputs of ADC B. True differential input pair.
43, 18	$V_{REF}A$, $V_{REF}B$	Reference Input/Output. Decoupling capacitors connect to these pins to decouple the internal reference buffer for each respective ADC. Typically, 1 µF capacitors are required to decouple the reference. Provided the output is buffered, the on-chip reference can be taken from these pins and applied externally to the rest of a system.
34	SCLK	Serial Clock. Logic input. A serial clock input provides the SCLK for accessing the data from the AD7262/AD7262-5. This clock is also used as the clock source for the conversion process. A minimum of 31 clocks is required to perform the conversion and access the 12-bit result.
36	CAL	Logic Input. Initiates an internal offset calibration.
21	PD2	Logic Input. Places the AD7262/AD7262-5 in selected shutdown mode in conjunction with the PD1 and PD0 pins (see Table 7).
22	PD1	Logic Input. Places the AD7262/AD7262-5 in selected shutdown mode in conjunction with the PD2 and PD0 pins (see Table 7).

Pin No.	Mnemonic	Description
23	PD0/D_{IN}	Logic Input/Data Input. Places the AD7262/AD7262-5 in selected shutdown mode in conjunction with the PD2 and PD1 pins (see Table 7). If all gain selection pins, G0 to G3, are tied low, this pin acts as the data input pin, and all programming is via the control register (see Table 8). Data to be written to the AD7262/AD7262-5 control register is provided on this input and is clocked into the register on the falling edge of SCLK.
35	$\overline{CS}$	Chip Select. Active low logic input. This input initiates conversions on the AD7262/AD7262-5.
48, 47, 46, 45	C_A+, C_A-, C_B+, C_B-	Comparator Inputs. These pins are the inverting and noninverting analog inputs for Comparator A and Comparator B. These two comparators have very low power consumption.
13, 14, 15, 16	C_C+, C_C-, C_D+, C_D-	Comparator Inputs. These pins are the inverting and noninverting analog inputs for Comparator C and Comparator D. This pair of comparators offers very fast propagation delays.
5, 6, 8, 19, 42	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7262/AD7262-5. Refer all analog input signals and any external reference signal to this AGND voltage. All AGND pins should connect to the AGND plane of a system. The AGND, DGND, C_A_C_B_GND, and C_C_C_D_GND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis. C_A_C_B_GND and C_C_C_D_GND can be tied to AGND.
28	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7262/AD7262-5. Connect the DGND pin to the DGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
30, 29, 26, 25	C_{OUT}A, C_{OUT}B, C_{OUT}C, C_{OUT}D	Comparator Outputs. These pins provide a CMOS (push-pull) output from each respective comparator. These are digital output pins with logic levels determined by the V_{DRIVE} supply.
32, 31	D_{OUT}A, D_{OUT}B	Serial Data Outputs. The data output from the AD7262/AD7262-5 is supplied to each pin as a serial data stream in twos complement format. The bits are clocked out on the falling edge of the SCLK input. A total of 31 SCLKs is required to perform the conversion and access the 12-bit data. During the conversion process, the data output pins are in three-state and, when the conversion is completed, the 19th SCLK edge clocks out the MSB. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs. The data is provided MSB first. If $\overline{CS}$ is held low for an additional 14 SCLK cycles on either D_{OUT}A or D_{OUT}B following the initial 31 SCLKs, the data from the other ADC follows on the D_{OUT} pin. This allows data from a simultaneous conversion on both ADCs to be gathered in serial format on either D_{OUT}A or D_{OUT}B using only one serial port.
40, 39, 38, 37	G0, G1, G2, G3	Logic Inputs. These pins program the gain setting of the front-end amplifiers. If all four pins are tied low, the PD0 pin acts as a data input pin, D_{IN}, and all programming is made via the control register (see Table 6).
27	V_{DRIVE}	Logic Power Supply Input, 2.7 V to 5.25 V. The voltage supplied at this pin determines at what voltage the interface operates, including the comparator outputs. Decouple this pin to DGND.
44, 17	C_A_C_B_GND, C_C_C_D_GND	Comparator Ground. This is the ground reference point for all comparator circuitry on the AD7262/AD7262-5. Both the C_A_C_B_GND pin and the C_C_C_D_GND pin must connect to the GND plane of a system and can be tied to AGND. The DGND, AGND, C_A_C_B_GND, and C_C_C_D_GND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
24	REFSEL	Internal/External Reference Selection. Logic input. If this pin is tied to a logic high voltage, the on-chip 2.5 V reference is used as the reference source for both ADC A and ADC B. If the REFSEL pin is tied to GND, an external reference can be supplied to the AD7262/AD7262-5 through the V_{REF}A and/or V_{REF}B pin.
	EPAD	Exposed Metal Paddle. The exposed metal paddle on the bottom of the LFCSP package must be soldered to PCB ground for proper heat dissipation and also for noise and mechanical strength benefits.

TYPICAL PERFORMANCE CHARACTERISTICS

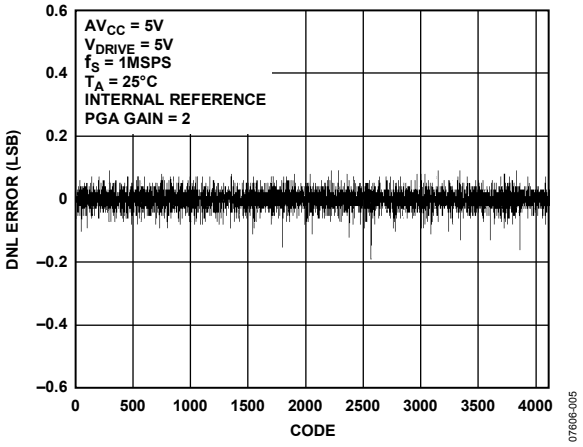


Figure 5. Typical DNL at Gain of 2

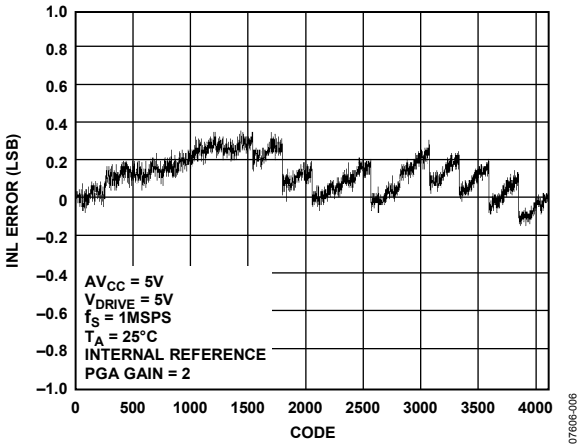


Figure 6. Typical INL at Gain of 2

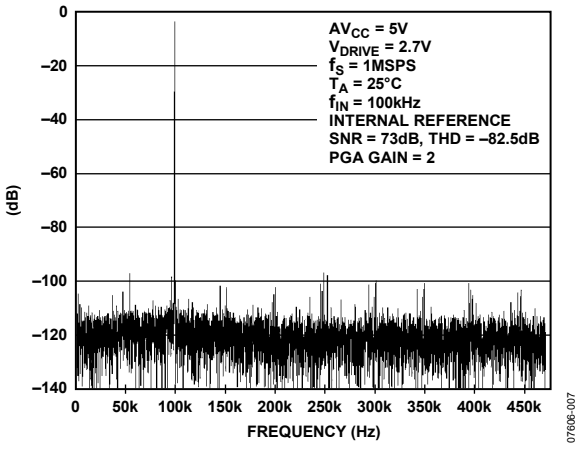


Figure 7. 3 dB Typical FFT at Gain of 2

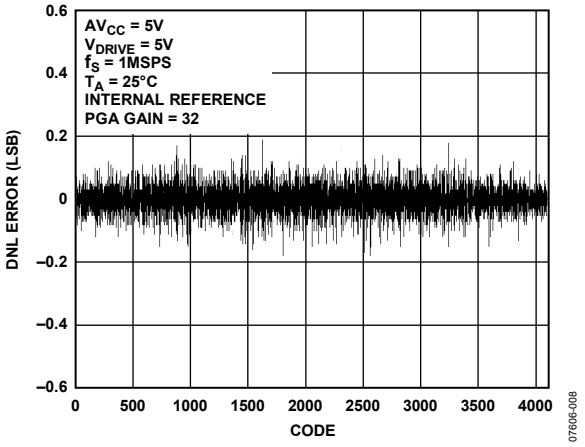


Figure 8. Typical DNL at Gain of 32

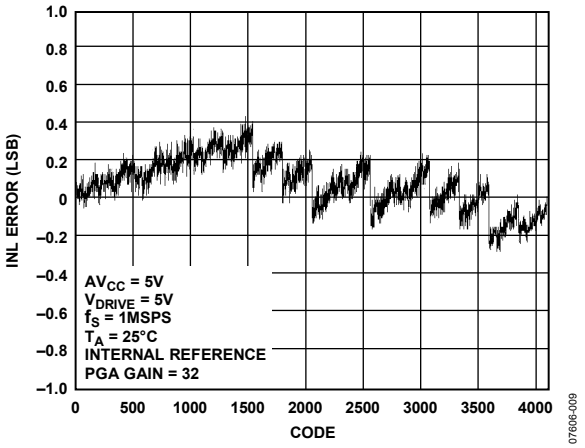


Figure 9. Typical INL at Gain of 32

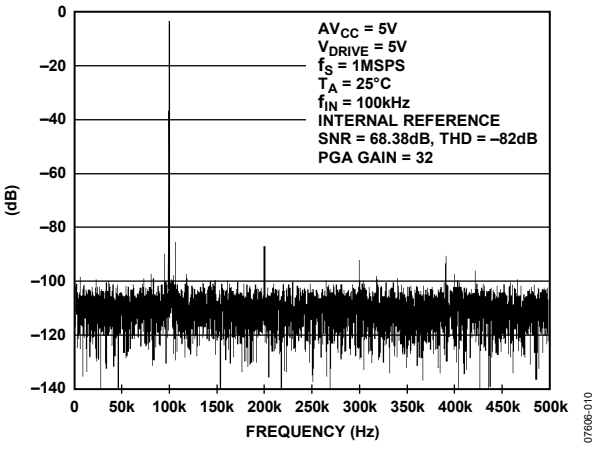


Figure 10. Typical FFT at Gain of 32

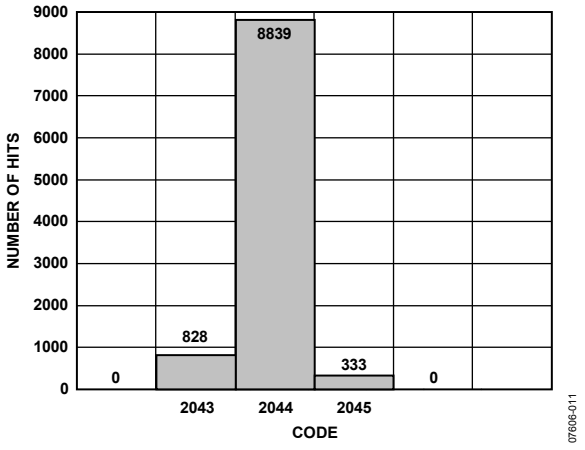


Figure 11. Histogram of Codes for 10k Samples at Gain of 2

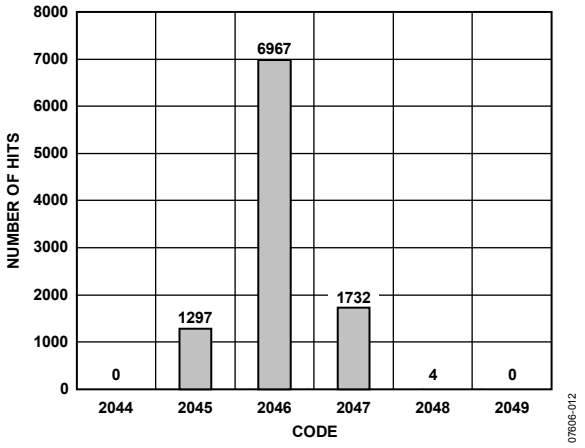


Figure 12. Histogram of Codes for 10k Samples at Gain of 32

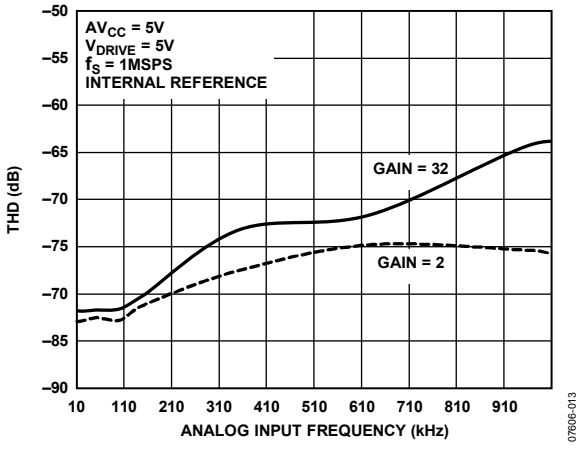


Figure 13. THD vs. Analog Input Frequency up to 1 MHz at Gain of 2 and 32

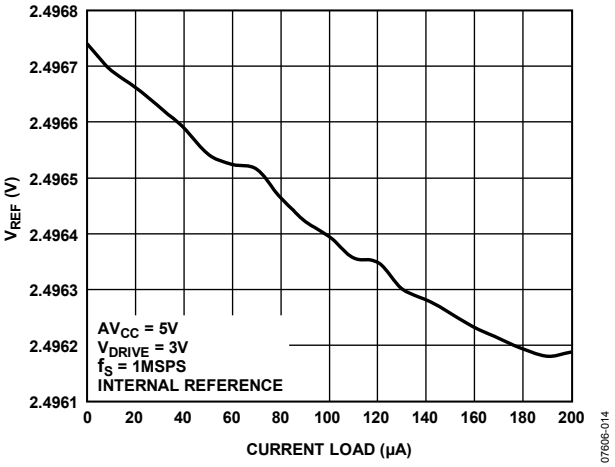


Figure 14. V_{REF} vs. Reference Output Current Load

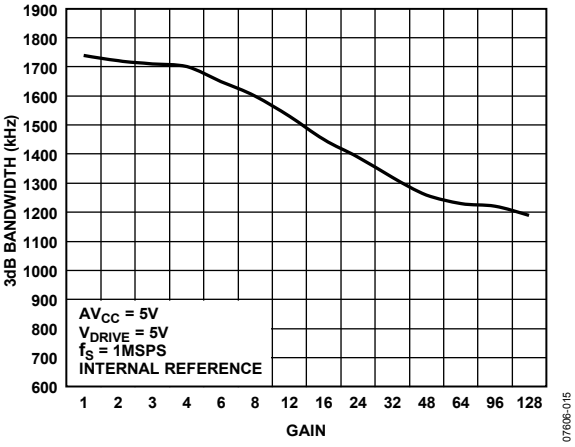


Figure 15. 3 dB Bandwidth vs. Gain

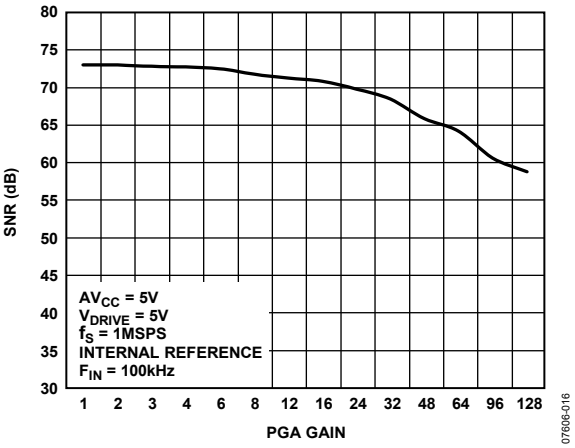


Figure 16. SNR vs. PGA Gain for an Analog Input Tone of 100 kHz

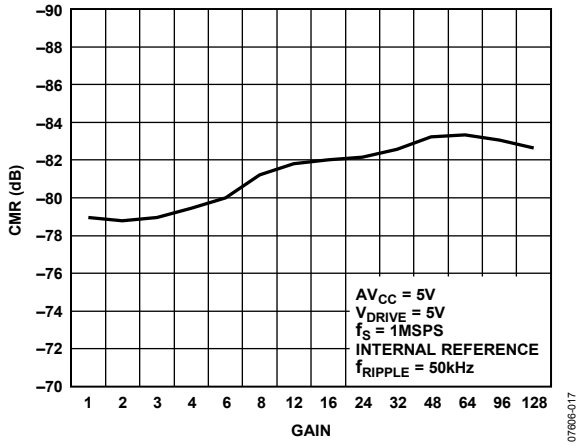


Figure 17. Common-Mode Rejection vs. Gain

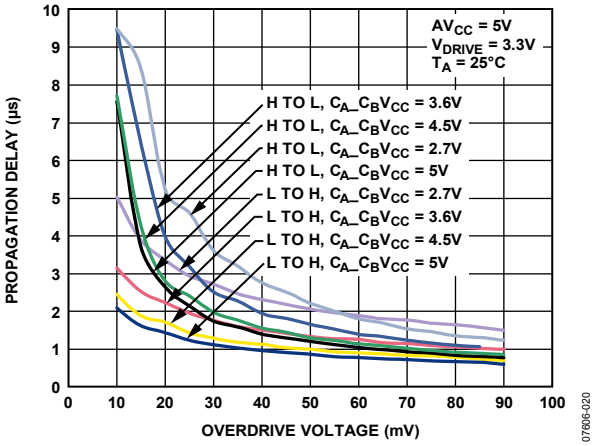


Figure 20. Propagation Delay for Comparator A and Comparator B vs. Overdrive Voltage for Various Supply Voltages

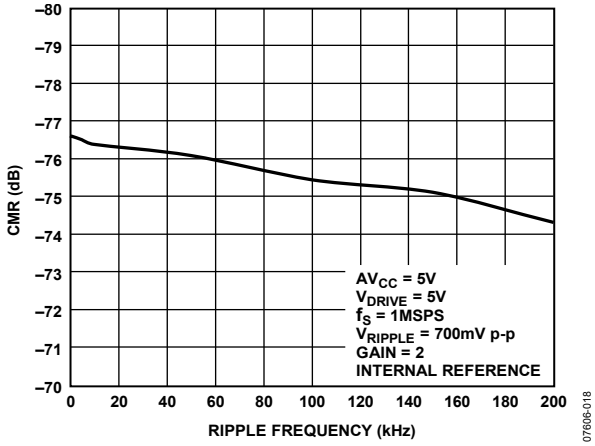


Figure 18. Common-Mode Rejection vs. Common-Mode Ripple Frequency

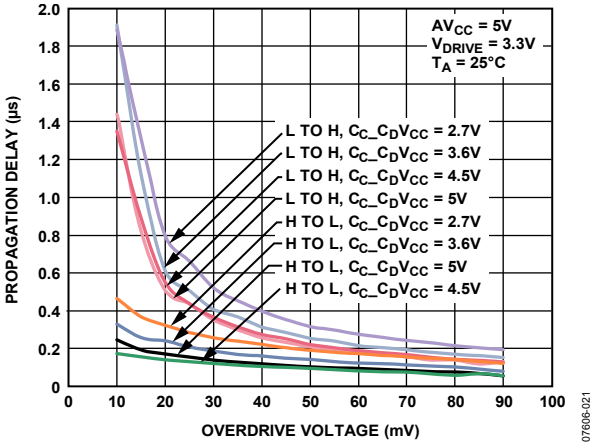


Figure 21. Propagation Delay for Comparator C and Comparator D vs. Overdrive Voltage for Various Supply Voltages

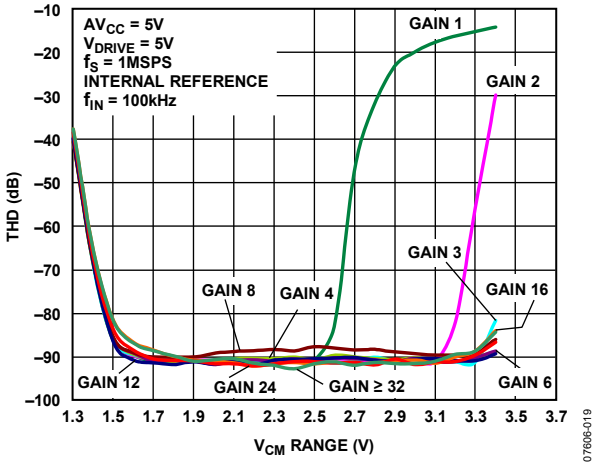


Figure 19. THD vs. Common-Mode Range for Various PGA Gain Settings

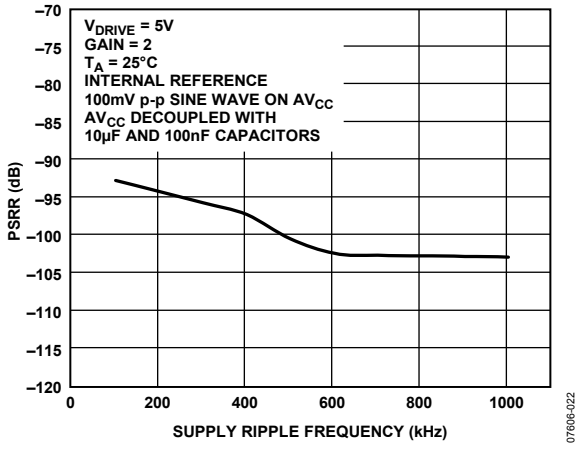


Figure 22. Power Supply Rejection Ratio vs. Supply Ripple Frequency?

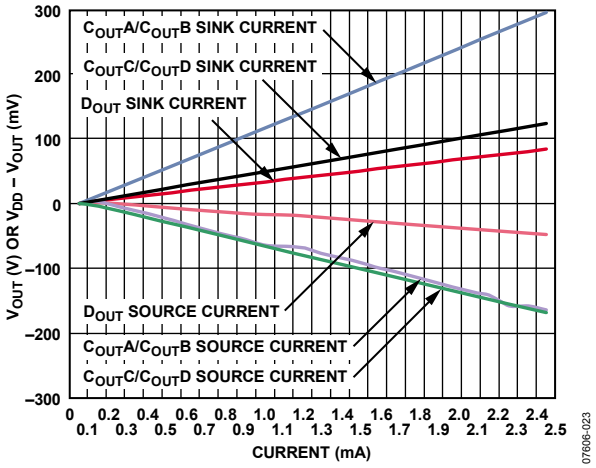


Figure 23. D_{OUT} and C_{OUT} Source and Sink Current

TERMINOLOGY

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)
Integral nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a single (1) LSB point below the first code transition, and full scale, a single (1) LSB point above the last code transition.

Zero Code Error
This is the deviation of the midscale transition (all 1s to all 0s) from the ideal VIN voltage, that is, VCM – ½ LSB.

Positive Full-Scale Error
This is the deviation of the last code transition (011 … 110) to (011 … 111) from the ideal, that is,

$$V_{CM} + \left(\frac{V_{REF}}{2 \times Gain}\right) - 1\,\text{LSB}$$

after the zero code error has been adjusted out.

Negative Full-Scale Error
This is the deviation of the first code transition (10 … 000) to (10 … 001) from the ideal, that is,

$$V_{CM} - \left(\frac{V_{REF}}{2 \times Gain}\right) + 1\,\text{LSB}$$

after the zero code error has been adjusted out.

Zero Code Error Match
This is the difference in zero code error across both ADCs.

Positive Full-Scale Error Match
This is the difference in positive full-scale error across both ADCs.

Negative Full-Scale Error Match
This is the difference in negative full-scale error across both ADCs.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of a conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of a conversion.

Signal-to-(Noise + Distortion) Ratio
This ratio is the measured ratio of signal-to-(noise + distortion) at the output of the analog-to-digital converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all non-fundamental signals up to half the sampling frequency (fS/2), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise.

The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

Signal-to-(Noise + Distortion) = (6.02*N* + 1.76*)* dB

Thus for a 12-bit converter, this is 86 dB.

Total Harmonic Distortion (THD)
Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7262/AD7262-5, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental, and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic, or spurious noise, is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to fS/2, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

ADC-to-ADC Isolation
ADC-to-ADC isolation is a measure of the level of crosstalk between the ADC A and ADC B. It is measured by applying a full-scale, 100 kHz sine wave signal to all unselected input channels and determining how much that signal is attenuated in the selected channel with a 40 kHz signal. The figure given is the worst case.

PSRR (Power Supply Rejection)
Variations in power supply affect the full-scale transition but not the linearity of the converter. Power supply rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value (see Figure 22).

Propagation Delay Time, Low to High (t_{PLH})
Propagation delay time from low to high is defined as the time taken from the 50% point on a low to high input signal until the digital output signal reaches 50% of its final low value.

Propagation Delay Time, High to Low (t_{PHL})
Propagation delay time from high to low is defined as the time taken from the 50% point on a high to low input signal until the digital output signal reaches 50% of its final high value.

Comparator Offset
Comparator offset is the measure of the density of digital 1s and 0s in the comparator output when the negative analog terminal of the comparator input is held at a static potential and the analog input to the positive terminal of the comparators is varied proportionally about the static negative terminal voltage.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7262/AD7262-5 are fast, dual, simultaneous sampling, differential, 12-bit, serial ADCs. The AD7262/AD7262-5 contain two on-chip differential programmable gain amplifiers, two track-and-hold amplifiers, and two successive approximation analog-to-digital converters with a serial interface with two separate data output pins. The AD7262/AD7262-5 also include four on-chip comparators. They are housed in a 48-lead LFCSP and in a 48-lead LQFP, offering the user considerable space-saving advantages over alternative solutions. The AD7262/AD7262-5 require a low voltage 5 V ± 5% AV_{CC} to power the ADC core and supply the digital power, a 5.25 V to 2.7 V C_A_$C_B V_{CC}$, C_C_$C_D V_{CC}$ supply for the comparators, and a 2.7 V to 5.25 V V_{DRIVE} supply for interface power.

The on-board PGA allows the user to select from 14 programmable gain stages: ×1, ×2, ×3, ×4, ×6, ×8, ×12, ×16, ×24, ×32, ×48, ×64, ×96, and ×128. The PGA accepts fully differential analog signals. The gain can be selected either by setting the logic state of the G0 to G3 pins or by programming the control register.

The serial clock input accesses data from the part while also providing the clock source for each successive approximation ADC. The AD7262/AD7262-5 have an on-chip 2.5 V reference that can be disabled when an external reference is preferred. If the internal reference is used elsewhere in a system, the output from $V_{REF}A$ and $V_{REF}B$ must first be buffered. If the internal reference is the preferred option, the user must tie the REFSEL pin to a logic high voltage. Alternatively, if the REFSEL pin is tied to GND, an external reference can be supplied to both ADCs through the $V_{REF}A$ and $V_{REF}B$ pins (see the Reference section).

The AD7262/AD7262-5 also feature a range of power-down options to allow the user great flexibility with the independent circuit components while allowing for power savings between conversions. The power-down feature is implemented via the control register or the PD0 to PD2 pins, as described in the Control Register section.

COMPARATORS

The AD7262/AD7262-5 have four on-chip comparators. Comparator A and Comparator B have ultralow power consumption, with static power consumption typically less than 10 µW with a 3.3 V supply. Comparator C and Comparator D feature very fast propagation delays of 130 ns for a 200 mV differential overdrive. These comparators have push-pull output stages that operate from the V_{DRIVE} supply. This feature allows operation with a minimum amount of power consumption.

Each pair of comparators operates from its own independent supply, C_A_$C_B V_{CC}$ and C_C_$C_D V_{CC}$. The comparators are specified for supply voltages from 2.7 V to 5.25 V. If desired, C_A_$C_B V_{CC}$ and C_C_$C_D V_{CC}$ can be tied to the AV_{CC} supply. The four comparators on the AD7262/AD7262-5 are functional with C_A_$C_B V_{CC}$/C_C_$C_D V_{CC}$ greater than or equal to 1.8 V. However, no specifications are guaranteed for comparator supplies less than 2.7 V. The wide range of supply voltages ensures that the comparators can be used in a variety of battery backup modes.

The four on-chip comparators on the AD7262/AD7262-5 are ideally suited for monitoring signals from pole sensors in motor control systems. The comparators can be used to monitor signals from Hall effect sensors or the inner tracks from an optical encoder. One of the comparators can be used to count the index marker or z marker, which is used on startup to place the motor in a known position.

OPERATION

The AD7262/AD7262-5 have two successive approximation ADCs, each based around two capacitive DACs and two programmable gate amplifiers.

The ADC itself comprises control logic, a SAR, and two capacitive DACs. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor amplifiers to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code.

Each ADC is preceded by its own programmable gain stage. The PGA features high analog input impedance, true differential analog inputs that allow the output from any source or sensor to be connected directly to the PGA inputs without any requirement for additional external buffering. The variable gain settings ensure that the device can be used for amplifying signals from a variety of sources. The AD7262/AD7262-5 offer the flexibility to choose the most appropriate gain setting to use the wide dynamic range of the device.

ANALOG INPUTS

Each ADC in the AD7262/AD7262-5 has two high impedance differential analog inputs. Figure 24 shows the equivalent circuit of the analog input structure of the AD7262/AD7262-5. It consists of a fully differential input amplifier that buffers the analog input signal and provides the gain selected by using the gain pins or the control register.

The two diodes provide ESD protection. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. Exceeding 300 mV causes these diodes to become forward-biased and to start conducting current into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part. The C1 capacitors in Figure 24 are typically 5 pF and can primarily be attributed to pin capacitance.

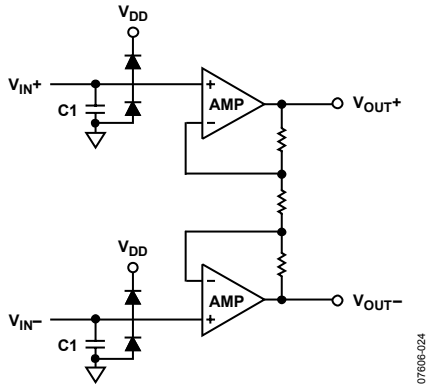


Figure 24. Analog Input Structure

The AD7262/AD7262-5 can accept differential analog inputs from

$$V_{CM} - \left(\frac{V_{REF}}{2 \times Gain}\right) \text{ to } V_{CM} + \left(\frac{V_{REF}}{2 \times Gain}\right)$$

Table 5 details the analog input range for the AD7262/AD7262-5 for the various PGA gain settings. Here, V_{REF} = 2.5 V and V_{CM} = 2.5 V (AV_{CC}/2, with AV_{CC} = 5 V).

Table 5. Analog Input Range for Various PGA Gain Settings

PGA Gain Setting	Analog Input Range for V_{IN}+ and V_{IN}–
1	0.75 V to 3.25 V[1]
2	1.875 V to 3.125 V
3	2.083 V to 2.916 V
4	2.187 V to 2.813 V
6	2.292 V to 2.708 V
8	2.344 V to 2.656 V
12	2.396 V to 2.604 V
16	2.422 V to 2.578 V
24	2.448 V to 2.552 V
32	2.461 V to 2.539 V
48	2.474 V to 2.526 V
64	2.480 V to 2.520 V
96	2.487 V to 2.513 V
128	2.490 V to 2.510 V

[1] For V_{CM} = 2 V. If V_{CM} = AV_{CC} /2, the analog input range for V_{IN}+ and V_{IN}– is 1.6 V to 3.4 V.

When a full-scale step input is applied to either differential input on the AD7262/AD7262-5 while the other analog input is held at a constant voltage, 3 µs of settling time is typically required prior to capturing a stable digital output code.

Transfer Function

The AD7262/AD7262-5 output is twos complement, and the ideal transfer characteristic is shown in Figure 25. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSB, and so on). The LSB size is dependent on the analog input range selected. The LSB size for the AD7262/AD7262-5 is shown in the following equation:

$$2 \times \left(\frac{\left(V_{CM} + \left(\frac{V_{REF}}{2 \times Gain}\right)\right) - \left(V_{CM} - \left(\frac{V_{REF}}{2 \times Gain}\right)\right)}{4096} \right)$$

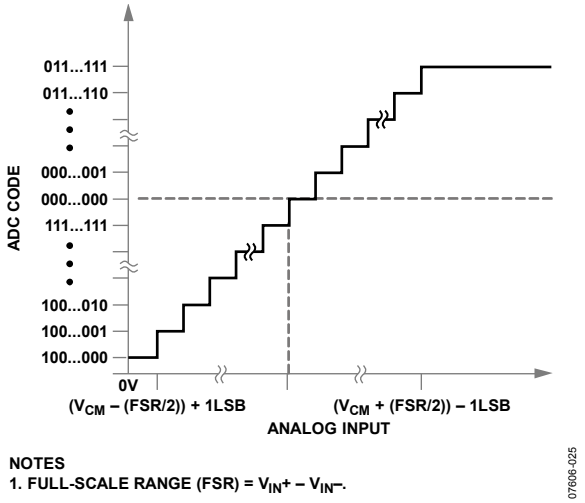


Figure 25. Twos Complement Transfer Function

V_{DRIVE}

The AD7262/AD7262-5 have a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the ADC and the comparators to interface easily to both 3 V and 5 V processors. For example, when the AD7262/AD7262-5 are operated with AV_{CC} = 5 V, the V_{DRIVE} pin can be powered from a 3 V supply, allowing a large analog input range with low voltage digital processors.

REFERENCE

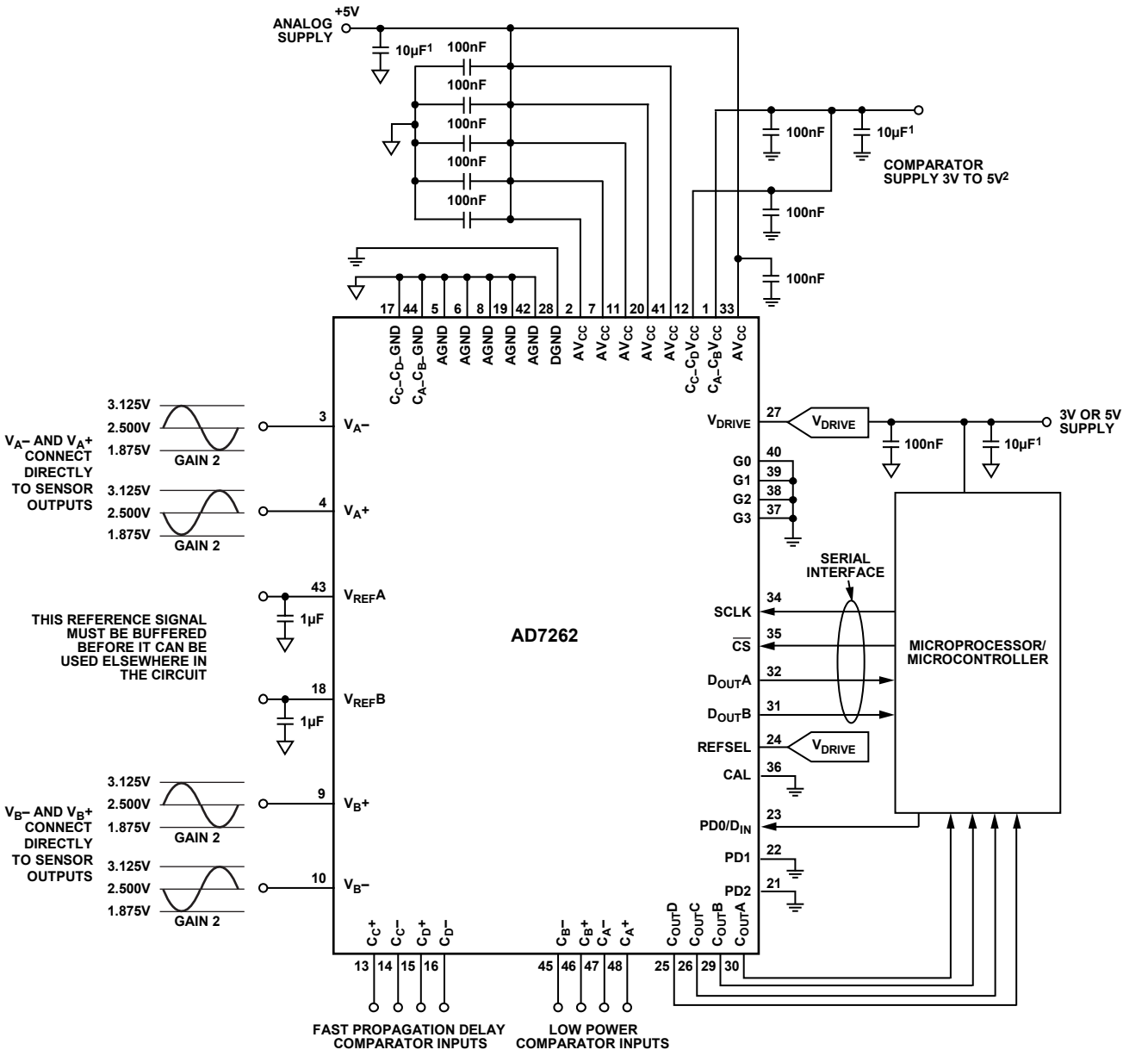
The AD7262/AD7262-5 can operate with either the internal 2.5 V on-chip reference or an externally applied reference. The logic state of the REFSEL pin determines whether the internal reference is used. The internal reference is selected for both ADCs when the REFSEL pin is tied to logic high. If the REFSEL pin is tied to AGND, an external reference can be supplied through the $V_{REF}A$ and/or $V_{REF}B$ pins. On power-up, the REFSEL pin must be tied to either a low or high logic state for the part to operate. Suitable reference sources for the AD7262/AD7262-5 include AD780, AD1582, ADR431, REF193, and ADR391.

The internal reference circuitry consists of a 2.5 V band gap reference and a reference buffer. When the AD7262/AD7262-5 are operated in internal reference mode, the 2.5 V internal reference is available at the $V_{REF}A$ and $V_{REF}B$ pins, which should be decoupled to AGND using a 1 μF capacitor. It is recommended that the internal reference be buffered before applying it elsewhere in the system. The internal reference is capable of sourcing up to 90 μA of current when the converter is static. If the internal reference operation is required for the ADC conversion, the REFSEL pin must be tied to logic high on power-up. The reference buffer requires 240 μs to power up and charge the 1 μF decoupling capacitor during the power-up time.

TYPICAL CONNECTION DIAGRAMS

Figure 26 and Figure 27 are typical connection diagrams for the AD7262/AD7262-5. In these configurations, the AGND pin is connected to the analog ground plane of the system, and the DGND pin is connected to the digital ground plane of the system. The analog inputs on the AD7262/AD7262-5 are true differential and have an input impedance in excess of 1 GΩ; thus, no driving op amps are required. The AD7262/AD7262-5 can operate with either an internal or an external reference. In Figure 26, the AD7262/AD7262-5 are configured to operate in control register mode; thus, G0 to G3, PD1, and PD2 can be connected to ground (low logic state). Figure 27 has the gain pins configured for a gain of 2 setup; thus, the device is in pin-driven mode. Both circuit configurations illustrate the use of the internal 2.5 V reference

The $C_A\_C_BV_{CC}$ and the $C_C\_C_DV_{CC}$ pins can be connected to either a 3 V or a 5 V supply voltage. The AV_{CC} pin must be connected to a 5 V supply. All supplies should be decoupled with a 100 nF capacitor at the device pin, and some supply sources may require a 10 μF capacitor where the source is supplied to the circuit board. The V_{DRIVE} pin is connected to the supply voltage of the microprocessor. The voltage applied to the V_{DRIVE} input controls the voltage of the serial interface. V_{DRIVE} can be set to 3 V or 5 V.



1THESE CAPACITORS ARE PLACED AT THE SUPPLY SOURCE AND MAY NOT BE REQUIRED IN ALL SYSTEMS.
2THIS SUPPLY CAN BE CONNECTED TO THE ANALOG 5V SUPPLY IF REQUIRED.

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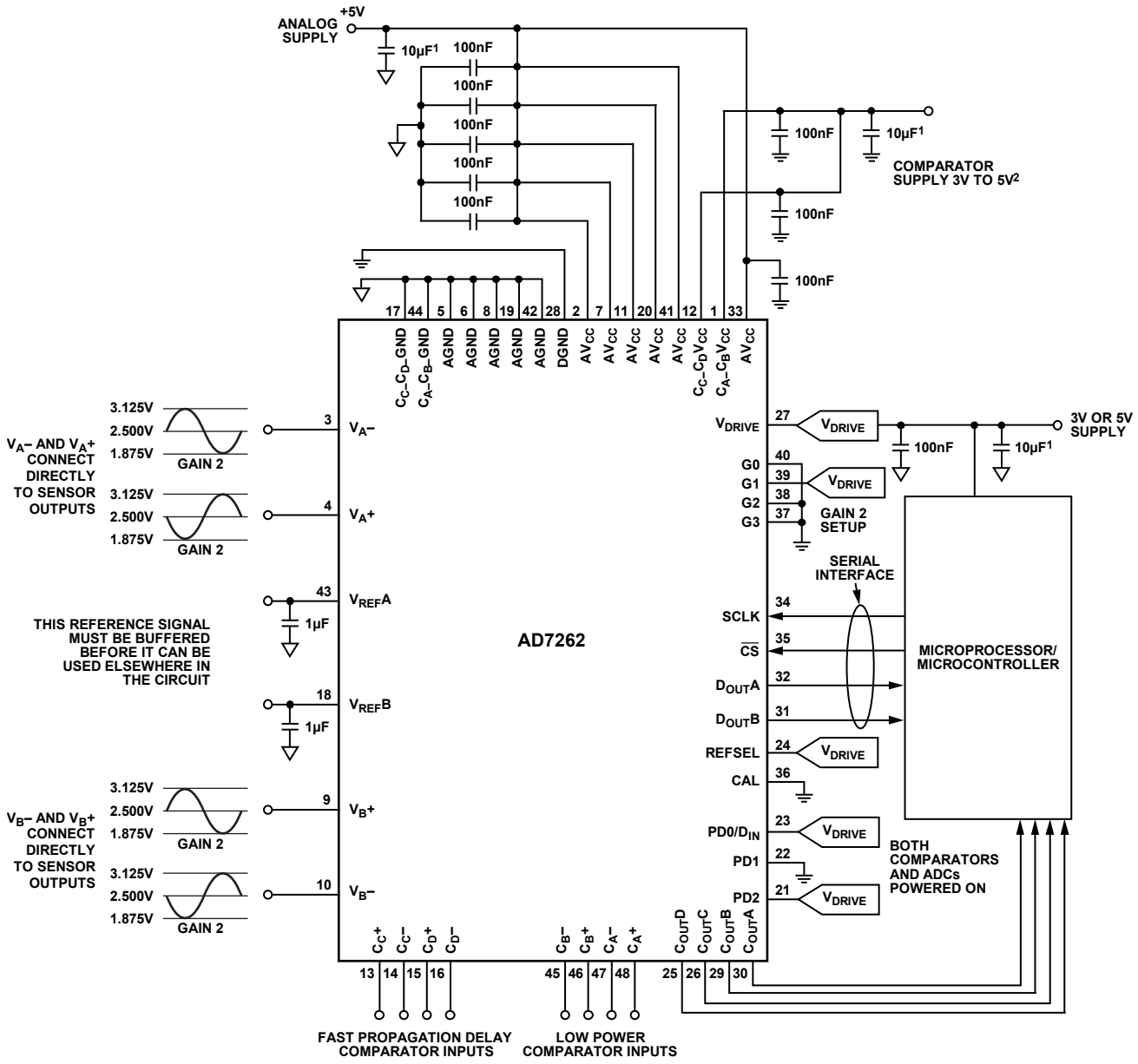
Figure 26. Typical Connection Diagram for the AD7262/AD7262-5 in Control Register Mode (All Gain Pins Tied to Ground) Configured for a PGA Gain of 2



1THESE CAPACITORS ARE PLACED AT THE SUPPLY SOURCE AND MAY NOT BE REQUIRED IN ALL SYSTEMS.
2THIS SUPPLY CAN BE CONNECTED TO THE ANALOG 5V SUPPLY IF REQUIRED.

Figure 27. Typical Connection Diagram for the AD7262/AD7262-5 in Pin-Driven Mode with Gain of 2 and Both ADCs and Comparators Fully Powered On

Comparator Application Details

The comparators on the AD7262/AD7262-5 have been designed with no internal hysteresis, allowing users the flexibility to add external hysteretic if required for systems operating in noisy environments. If the comparators on the AD7262/AD7262-5 are used with external hysteresis, some external resistors and capacitors are required, as shown in Figure 28. The value of R_F and R_S, the external resistors, can be determined using the following equation, depending on the amount of hysteresis required in the application:

$$V_{HYS} = \frac{R_S}{R_S + R_F} \times C_x\_C_x V_{CC}$$

where $C_x\_C_x V_{CC} = C_A\_C_B V_{CC}$ or $C_C\_C_D V_{CC}$.

The amount of hysteresis chosen must be sufficient to eliminate the effects of analog noise at the comparator inputs, which may affect the stability of the comparator outputs. The level of hysteresis required in any system depends on the noise in the system; thus, the values of R_F and R_S need to be carefully selected to eliminate any noise effects. To increase the level of hysteresis in the system, increase the value of R_S or R_F. For example, R_F = 10 MΩ, R_S = 1 kΩ give 330 μV of hysteresis with a $C_x\_C_x V_{CC}$ of 3.3 V; if hysteresis is increased to 1 mV, R_S = 3.1 kΩ. In certain applications, a load capacitor (100 pF) may be required on the comparator outputs to suppress high frequency transient glitches.

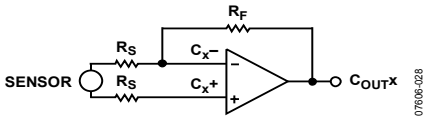


Figure 28. Recommended Comparator Connection Diagram

APPLICATION DETAILS

The AD7262/AD7262-5 have been specifically designed to meet the requirements of any motor control shaft position feedback loop. The devices can interface directly to multiple sensor types, including optical encoders, magneto resistive sensors, and Hall effect sensors. Flexible analog inputs that incorporate programmable gain ensure that identical board design can be used for a variety of sensors, which results in reduced design cycles and costs.

The two simultaneous sampling ADCs are used to sample the sine and cosine outputs from the sensor. No external buffering is required between the sensor/transducer and the analog inputs of the AD7262/AD7262-5. The on-chip comparators can be used to monitor the pole sensors, which can be Hall effect sensors or the inner tracks from an optical encoder.

Figure 29 shows how the AD7262/AD7262-5 can be used in a typical application. An optical encoder is shown in Figure 29, but other sensor types could as easily be used. Figure 29 indicates a typical application configuration only, and there are several other configurations that render equally effective results.

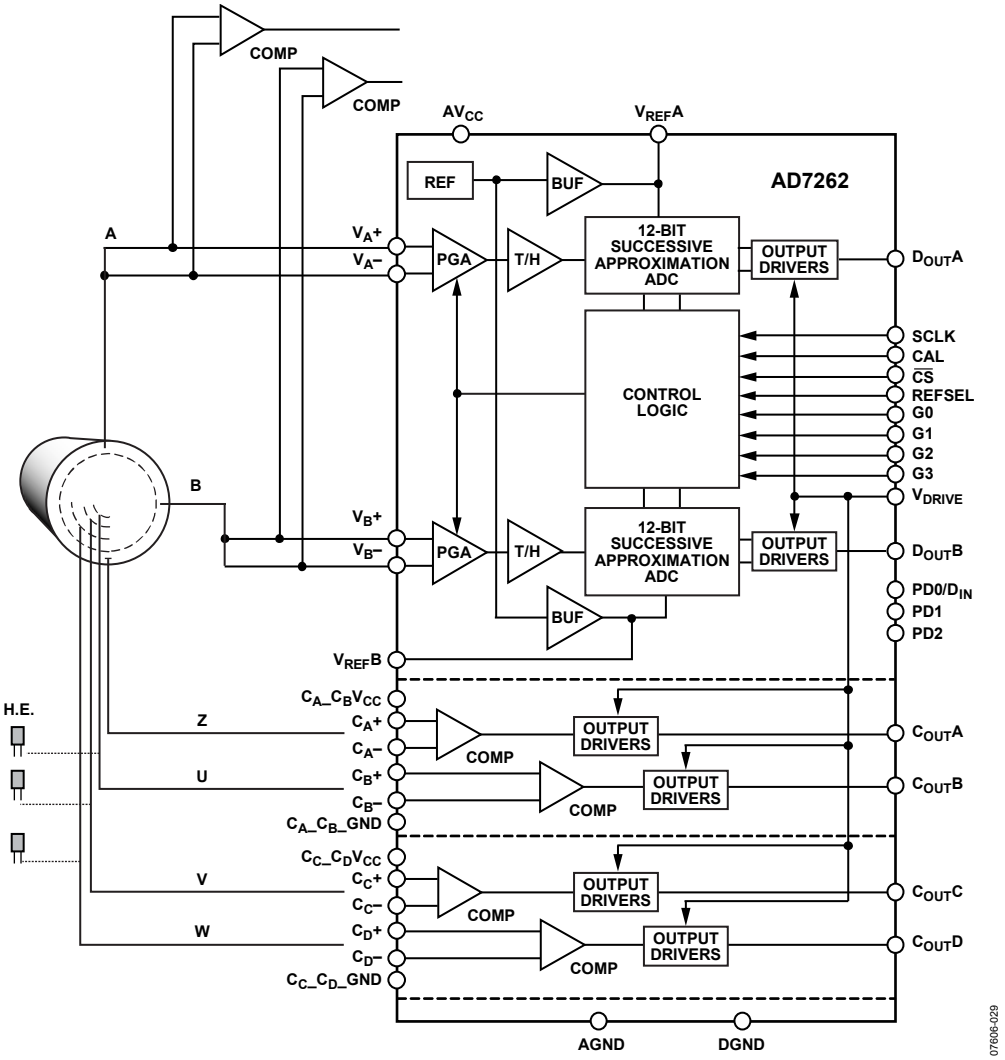


Figure 29. Typical System Connection Diagram with Optical Encoder

MODES OF OPERATION

The AD7262/AD7262-5 allow the user to choose between two modes of operation, pin-driven mode and control register mode.

PIN-DRIVEN MODE

In pin-driven mode, the user can select the gain of the PGA, the power-down mode, internal or external reference, and initiate a calibration of the offset for both ADC A and ADC B. These functions are implemented by setting the logic levels on the gain pins (G3 to G0), the power-down pins (PD2 to PD0), the REFSEL pin, and the CAL pin, respectively.

The logic state of Pin G3 to Pin G0 determines which mode of operation is selected. Pin-driven mode is selected if at least one of the gain pins is set to a logic high state. Alternatively, if all four gain pins are connected to a logic low, the control register mode of operation is selected.

GAIN SELECTION

The on-board PGA allows the user to select from 14 programmable gain stages: ×1, ×2, ×3, ×4, ×6, ×8, ×12, ×16, ×24, ×32, ×48, ×64, ×96, and ×128. The PGA accepts fully differential analog signals and provides three key functions, which include selecting gains for small amplitude input signals, driving the ADCs switched capacitive load, and buffering the source from the switching effects of the SAR ADCs. The AD7262/AD7262-5 offer the user great flexibility in user interface, providing gain selection via the control register or by driving the gain pins to the desired logic state. The AD7262/AD7262-5 have four gain pins, G3, G2, G1 and G0, as shown in Figure 3. Each gain setting is selected by setting up the appropriate logic state on each of the four gain pins, as outlined in Table 6. If all four gain pins are connected to a logic low level, the part is put in control register mode and the gain settings are selected via the control register.

Table 6. Gain Selection

G3	G2	G1	G0	Gain
0	0	0	0	Software control via control register
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	6
0	1	1	0	8
0	1	1	1	12
1	0	0	0	16
1	0	0	1	24
1	0	1	0	32
1	0	1	1	48
1	1	0	0	64
1	1	0	1	96
1	1	1	0	128

POWER-DOWN MODES

The AD7262/AD7262-5 offer the user a number of power-down options to enable individual device components to be powered down independently. These options can be chosen to optimize the power dissipation for different application requirements. The power-down modes can be selected by either programming the device via the control register or by driving the PD pins to the appropriate logic levels. By setting the PD pins to a logic low level when in pin-driven mode, all four comparators and both ADCs can be powered down. The PD2 and PD0 pins must be set to logic high and the PD1 pin set to logic low to power up all circuitry on the AD7262/AD7262-5. The PD pin configurations for the various power-down options are outlined in Table 7.

Table 7. Power-Down Modes

PD2	PD1	PD0	Comparator A, Comparator B	Comparator C, Comparator D	ADC A, ADC B
0	0	0	Off	Off	Off
0	0	1	Off	Off	On
0	1	0	Off	On	Off
0	1	1	On	Off	Off
1	0	0	On	On	Off
1	0	1	On	On	On
1[1]	1[1]	1[1]	Off	Off	Off

[1] PD2 = PD1 = PD0 = 1 resets the AD7262/AD7262-5 when in pin-driven mode only.

The AV_{CC} and V_{DRIVE} supplies must continue to be supplied to the AD7262/AD7262-5 when the comparators are powered up but the ADCs are powered-down. External diodes can be used from the $C_A\_C_BV_{CC}$ and/or $C_C\_C_DV_{CC}$ to both the AV_{CC} and the V_{DRIVE} supplies to ensure they retain a supply at all instances.

The AD7262/AD7262-5 can be reset in pin-driven mode only by setting the PDx pins to a logic high state. When the device is reset, all the registers are cleared and the four comparators and the two ADCs are left powered down.

In normal mode of operation with the ADCs and comparators powered on, the $C_A\_C_BV_{CC}/C_C\_C_DV_{CC}$ supply and the AV_{CC} supply can be at different voltage levels, as indicated in Table 1. When the comparators on the AD7262/AD7262-5 are in power-down mode, and the $C_A\_C_BV_{CC}/C_C\_C_DV_{CC}$ supplies are at a potential 0.3 V greater than or less than the AV_{CC} supply, the supplies consume more current than would be the case if both sets of supplies were at the same potential. This configuration does not damage the AD7262/AD7262-5 but results in additional current flowing in any or all of the AD7262/AD7262-5 supply pins. This is due to ESD protection diodes within the device. In applications where power consumption in power-down mode is critical, it is recommended that the $C_A\_C_BV_{CC}/C_C\_C_DV_{CC}$ supply and the AV_{CC} supply be held at the same potential.

Power-Up Conditions

On power-up, the status of the gain pins determine which mode of operation is selected, as outlined in the Gain Selection section. All registers are set to 0 by default.

If the AD7262/AD7262-5 are powered up in pin-driven mode, the gain pins and the PDx pins should be configured to the appropriate logic states and a calibration initiated if required.

Alternatively, if the AD7262/AD7262-5 are powered up in control register mode, the comparators and ADCs are powered down and the default gain is 1. Thus, powering up in control register mode requires a write to the device to power up the comparators and the ADCs.

It takes 15 µs to power up the AD7262/AD7262-5 when using an external reference. When the internal reference is used, 240 µs are required to power up the AD7262/AD7262-5 with a 1 µF decoupling capacitor.

CONTROL REGISTER

The control register on the AD7262/AD7262-5 is a 12-bit read and write register, which is used to control the device when not in pin-driven mode. The PD0/D_{IN} pin serves as the serial D_{IN} pin for the AD7262/AD7262-5 when the gain pins are set to 0 (that is, the part is not in pin-driven mode). The control register can be used to select the gain of the PGAs, the power-down modes, and the calibration of the offset for both ADC A and ADC B. When operating in the control register mode, PD1 and PD2 should be connected to a low logic state.

These functions can also be implemented by setting the logic levels on the gain pins, the power-down pins, and the CAL pin, respectively. The control register can also be used to read the offset and gain registers.

Data is loaded from the PD0/D_{IN} pin of the AD7262/AD7262-5 on the falling edge of SCLK when $\overline{CS}$ is in a logic low state. The control register is selected by first writing the appropriate four WR bits, as outlined in Table 10. The 12 data bits must then be clocked into the control register of the device. Thus, on the 16th falling SCLK edge, the LSB is clocked into the device. One more SCLK cycle is then required to write to the internal device registers. In total, 17 SCLK cycles are required to successfully write to the AD7262/AD7262-5. The data is transferred on the PD0/D_{IN} line while the conversion result is being processed. The data transferred on the D_{IN} line corresponds to the AD7262/ AD7262-5 configuration for the next conversion.

Only the information provided on the 12 falling clock edges after the $\overline{CS}$ falling edge and the initial four write address bits is loaded to the control register. The PD0/D_{IN} pin should have a logic low state for the four bits RD3 to RD0 when using the control register to select the power-down modes or gain setting or when initializing a calibration. The RD bits should also be set to a logic low level to access the ADC results from both D_{OUT}A and D_{OUT}B.

The power-up status of all bits is 0 and the MSB denotes the first bit in the data stream. The bit functions are outlined in Table 8 and Table 9.

Table 8. Control Register Bits

MSB											LSB
Bit 11	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RD3	RD2	RD1	RD0	CAL	PD2	PD1	PD0	G3	G2	G1	G0

Table 9. Control Register Bit Function Description

Bits	Mnemonic	Description
11 to 8	RD3 to RD0	Register address bits. These bits select which register the subsequent read is from. See Table 11.
7	CAL	Setting this bit high initiates an internal offset calibration. Once the calibration is completed, this pin can be reset low, and the internal offset, which is stored in the on-chip offset registers, is automatically removed from the ADC results.
6 to 4	PD2 toPD0	Power-down bits. These bits select which power-down mode is programmed. See Table 7.
3 to 0	G3 to G0	Gain selection bits. These bits select which gain setting is used on the front-end PGA. See Table 6.

Table 10. Write Address Bits

WR3	WR2	WR1	WR0	Read Register Addressed
0	0	0	1	Control register

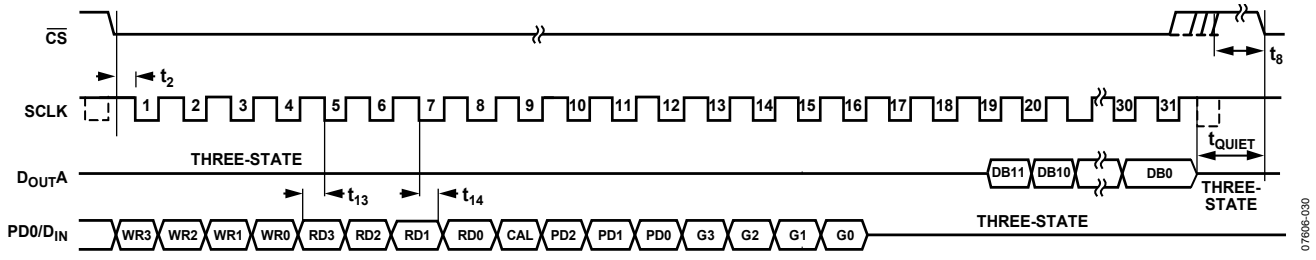


Figure 30. Timing Diagram for a Write Operation to the Control Register

ON-CHIP REGISTERS

The AD7262/AD7262-5 contain a control register, two offset registers for storing the offsets for each ADC, and two external gain registers for storing the gain error. The control register and the offset and gain registers are read and write registers. On power-up, all registers in the AD7262/AD7262-5 are set to 0.

Addressing the On-Chip Registers

Writing to a Register

Data is loaded from the PD0/D_{IN} pin of the AD7262/AD7262-5 on the falling edge of SCLK when $\overline{CS}$ is in a logic low state. Four address bits and 12 data bits must be clocked into the device. Thus, on the 16th falling SCLK edge, the LSB is clocked into the AD7262/AD7262-5. One more SCLK cycle is then required to write to the internal device registers. In total, 17 SCLK cycles are required to successfully write to the AD7262/AD7262-5. The control and offset registers are 12-bits registers; the gain registers are 7-bit registers.

When writing to a register, the user must first write the address bits corresponding to the selected register. Table 11 shows the decoding of the address bits. The four RD bits are written MSB first, that is, RD3 followed by RD2, RD1, and RD0. The AD7262/AD7262-5 decodes these bits to determine which register is being addressed. The subsequent 12 bits of data are written to the addressed register.

When writing to the external gain registers, the seven bits of data immediately after the four address bits are written to the register. However, 17 SCLK cycles are still required, and the PD0/D_{IN} pin of the AD7262/AD7262-5 should be tied low for the five additional clock cycles.

Table 11. Read and Write Register Addresses

RD3	RD2	RD1	RD0	Comment
0	0	0	0	ADC result (default)
0	0	0	1	Control register
0	0	1	0	Offset ADC A internal
0	0	1	1	Offset ADC B internal
0	1	0	0	Gain ADC A external
0	1	0	1	Gain ADC B external

Reading from a Register

The internal offset of the device, which has been measured by the AD7262/AD7262-5 and stored in the on-chip registers during the calibration, can be read back by the user. The content of the external gain registers can also be read. To read the content of any register, the user must first write to the control register by writing 0001 to the WR3 to WR0 bits via the PD0/D_{IN} pin, as outlined in Table 10. The next four bits in the control register are the RD bits, which are used to select the desired register from which to read. The appropriate 4-bit address for each of the offset and gain registers is outlined in Table 11. The remaining eight SCLK cycles bits are used to set the remaining bits in the control register to the desired state for the next ADC conversion.

The 19th SCLK falling edge clocks out the first data bit of the digital code corresponding to the value stored in the selected internal device register on the D_{OUT}A pin. D_{OUT}B outputs the conversion result from ADC B. Once the selected register has been read, the control register must be reset to output the ADC results for future conversions. This is achieved by writing 0001 to the WR3 to WR0 bits, followed by 0000 to the RD bits. The remaining eight bits in the control register should then be set to the required configuration for the next ADC conversion.

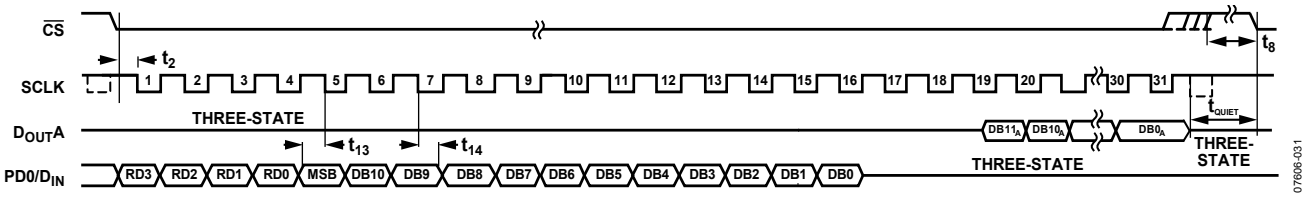


Figure 31. Timing Diagram for Writing to a Register

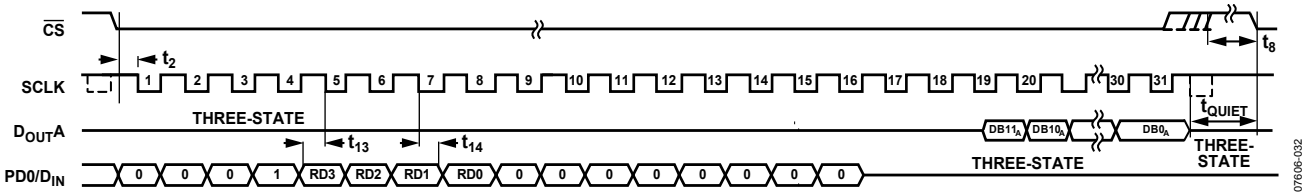


Figure 32. Timing Diagram for a Read Operation with PD0/D_{IN} as an Input

SERIAL INTERFACE

Figure 33 and Figure 34 show the detailed timing diagrams for the serial interfacing of the AD7262/AD7262-5. The serial clock provides the conversion clock and controls the transfer of information from the AD7262/AD7262-5 after the conversion. The AD7262/AD7262-5 has two output pins corresponding to each ADC. Data can be read from the AD7262/AD7262-5 using both $D_{OUT}A$ and $D_{OUT}B$. Alternatively, a single output pin of the user's choice can be used. The SCLK input signal provides the clock source for the serial interface.

The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, at which point the analog input is sampled. The conversion is also initiated at this point and requires a minimum of 19 SCLKs to complete. The $D_{OUT}x$ lines remain in three-state while the conversion is taking place. On the 19th SCLK falling edge, the AD7262/AD7262-5 return to track mode and the $D_{OUT}A$ and $D_{OUT}B$ lines are enabled. The data stream consists of 12 bits of data, MSB first.

The MSB of the conversion result is clocked out on the 19th SCLK falling edge to be read by the microcontroller or DSP on either the subsequent SCLK falling edge (20th falling edge) or the 20th SCLK rising edge. The choice of whether to read on the rising or falling SCLK edge depends on the SCLK frequency being used. When the maximum SCLK frequency of 40 MHz is used with a V_{DRIVE} voltage of 5 V, the maximum specified access time (t_4) is 23 ns, resulting in 2 ns of setup time, which may not be sufficient for most DSPs or microcontrollers. Under these conditions, it is recommended to use the rising SCLK edge to read the data. In this case, the MSB of the conversion result is clocked out on the 19th SCLK falling edge to be read on the 20th SCLK rising edge, as shown in Figure 33. The remaining data is then clocked out by subsequent SCLK falling edges. When using a 40 MHz SCLK frequency, the 20th falling clock edge on the serial clock clocks out the second data bit, which is provided for reading on the 21st SCLK rising edge. The remainder of the 12-bit result follows, with the final bit in the data transfer being valid on the 31st rising edge. The LSB is provided on the 30th falling clock edge.

An alternative to reading on the rising SCLK edge is to use a slower SCLK frequency. If a slower SCLK frequency is used, for example 32 MHz with the AD7262, this enables reading on the subsequent falling SCLK edge after the data has been clocked out, as illustrated in Figure 35. A throughput rate of 1 MSPS can still be achieved for the AD7262 when a 32 MHz SCLK frequency is used. The remaining data is then clocked out by subsequent SCLK falling edges. When using a 32 MHz or less SCLK frequency with the AD7262 or when using the AD7262-5, the 20th falling clock edge on the serial clock has the MSB provided for reading and also clocks out the second data bit. The remainder of the 12-bit result follows, with the final bit in the data transfer being valid on the 31st falling edge. The LSB is provided on the 30th falling clock edge.

On the rising edge of $\overline{CS}$, $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. If $\overline{CS}$ is not brought high after 31 SCLKs but is instead held low for an additional 14 SCLK cycles, the data from ADC B is output on $D_{OUT}A$ after the ADC A result. Likewise, the data from ADC A is output on $D_{OUT}B$ after the ADC B result. This is illustrated in Figure 34, which shows the $D_{OUT}A$ example. In this case, the D_{OUT} line in use goes back into three-state on the 47th SCLK falling edge or the rising edge of $\overline{CS}$, whichever occurs first.

If the falling edge of SCLK coincides with the falling edge of $\overline{CS}$, the falling edge of SCLK is not acknowledged by the AD7262 and the next falling edge of SCLK is the first one registered after the falling edge of $\overline{CS}$.

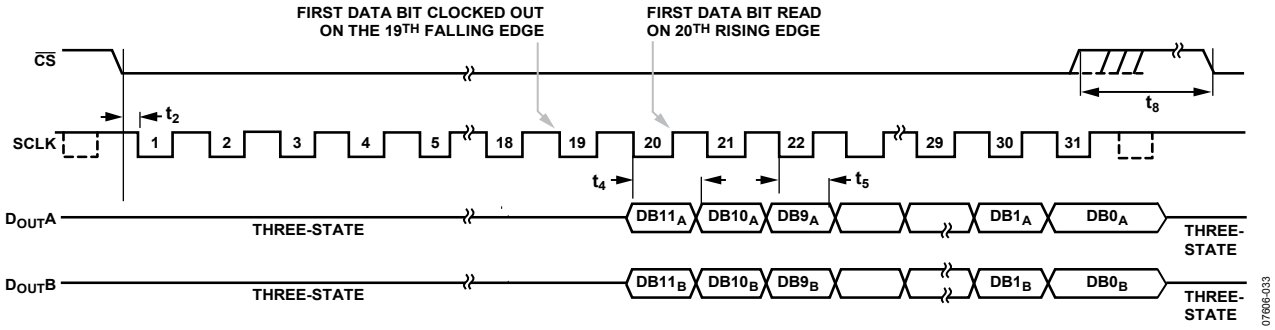


Figure 33. Serial Interface Timing Diagram When Reading Data on the 20th Rising SCLK Edge with a 40 MHz SCLK

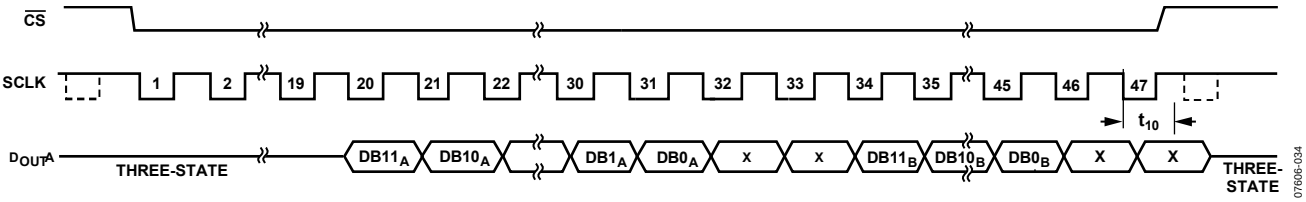


Figure 34. Reading Data from Both ADCs on One D_{OUT} Line with 47 SCLKs

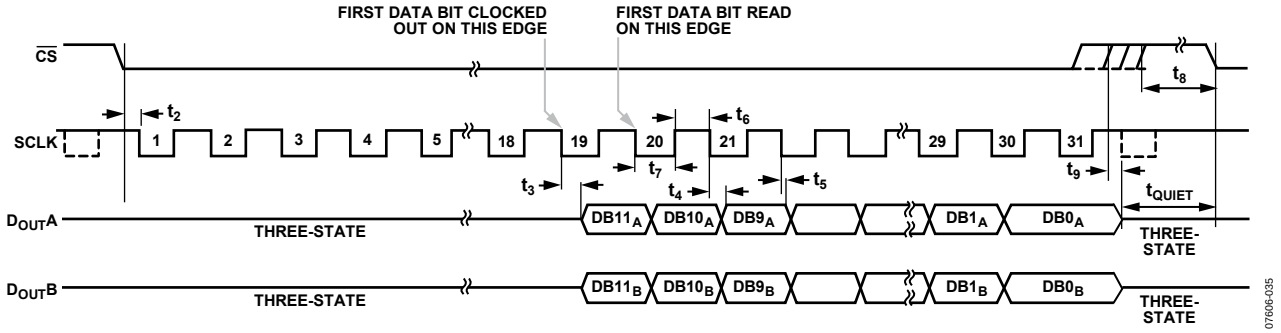


Figure 35. Serial Interface Timing Diagram When Reading Data on the Falling SCLK Edge with a Slow SCLK Frequency

CALIBRATION

INTERNAL OFFSET CALIBRATION

The AD7262/AD7262-5 allow the user to calibrate the device offset using the CAL pin. This is achieved by setting the CAL pin to a high logic level, which initiates a calibration on the next $\overline{CS}$ falling edge. The calibration requires one full conversion cycle, which contains a $\overline{CS}$ falling edge followed by 19 SCLKs to complete. The CAL pin can remain high for more than one conversion if desired, and the AD7262/AD7262-5 continue to calibrate.

The CAL pin should only be driven high when the $\overline{CS}$ pin is high or after 19 SCLK cycles have elapsed when $\overline{CS}$ is low (that is, between conversions). The CAL pin must be driven high t_{12} ns before $\overline{CS}$ goes low. If the $\overline{CS}$ pin goes low before the t_{12} has elapsed, the calibration result is inaccurate for the current conversion, but, provided that the CAL pin remains high, the subsequent calibration conversion is correct. If the CAL pin is set to a logic high state during a conversion, that conversion result is corrupted.

Provided that the CAL pin has been held high for a minimum of one conversion, and once t_{12} and t_{11} have been adhered to, the calibration is complete after the 19th SCLK cycle, and the CAL pin can be driven to a logic low state. The next $\overline{CS}$ falling edge after the CAL pin has been driven to a low logic state initiates a conversion of the differential analog input signal for both ADC A and ADC B.

Alternatively, one can use the control register to initiate an offset calibration. This is done by setting the CAL bit in the control register to 1. The calibration is then initiated on the next $\overline{CS}$ falling edge, but the current conversion is corrupted. The ADCs on the AD7262/AD7262-5 must remain fully powered up to complete the internal calibration.

The AD7262/AD7262-5 registers store the offset value that can be accessed easily by the user (see the Reading from a Register section). When the device is calibrating, the differential analog inputs for each respective ADC are shorted together internally and a conversion is performed. A digital code representing the offset is stored internally in the offset registers, and subsequent conversion results have this measured offset removed.

When the AD7262/AD7262-5 are calibrated, the calibration results stored in the internal device registers are only relevant for the particular PGA gain selected at the time of calibration. If the PGA gain is changed, the AD7262/AD7262-5 must be recalibrated. If the device is not recalibrated when the PGA gain is changed, the offset for the previous gain setting continues to be removed from the digital output code, which may lead to inaccuracies.

The offset range, which can be calibrated for, is ±128 least significant bits at a gain of 1. The maximum offset voltage, which can be calibrated for, is reduced as the gain of the PGA is increased.

Table 12 details the maximum offset voltage, which can be removed by the AD7262/AD7262-5 without compromising the available digital output code range. The least significant bit size is $AV_{CC}/2^{BITS}$, which is 5/4096 or 1.22 mV for the AD7262/AD7262-5. The maximum removable offset voltage is given by

$$\pm 128 \text{ LSB} \times \frac{1.22 \text{ mV}}{Gain}$$

Table 12. Offset Range

Gain	Maximum Removable Offset Voltage
1	±156.16 mV
2	±78.08 mV
3	±52.053 mV
32	±4.88 mV[1]

[1] This is the maximum removable offset for PGA gain ≥ 32.

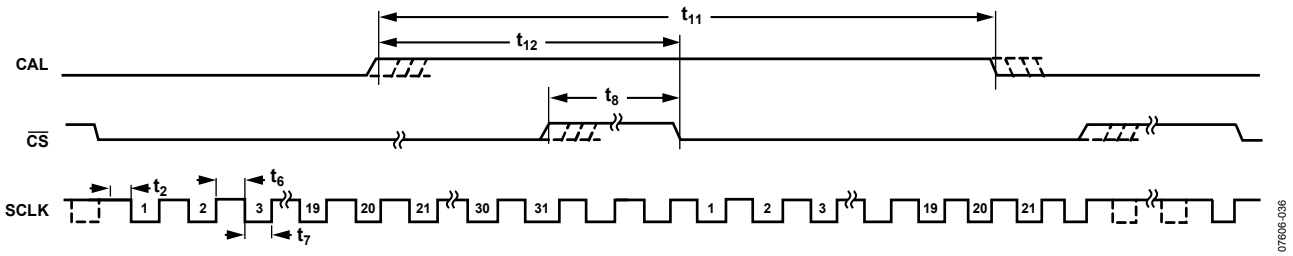


Figure 36. Calibration Timing Diagram

ADJUSTING THE OFFSET CALIBRATION REGISTERS

The internal offset calibration register can be adjusted manually to compensate for any signal path offset from the sensors to the ADC. Here, no internal calibration is required, and the CAL pin can remain at a low logic state. By changing the contents of the offset register, different amounts of offset on the analog input signal can be compensated for. To determine the digital code to be written to the offset register

1. Configure the sensor to its offset state.
2. Perform a number of conversions using the AD7262/AD7262-5.
3. Take the mean digital output code from both $D_{OUT}A$ and $D_{OUT}B$. This is a 12-bit result and the offset register is 12 bits; thus, the result can be stored directly in the offset register.
4. Write the digital code to the offset registers to calibrate the AD7262/AD7262-5.

If a +10 mV offset is present in the analog input signal and the gain of the PGA is 2, the code that needs to be written to the offset register to compensate for the offset is

$$\frac{+10\text{ mV}}{(1.22\text{ mV}/2)} = 16.39 = 0000\ 0001\ 0000$$

If a − 10 mV offset is present in the analog input signal and the gain of the PGA is 2, the code that needs to be written to the offset register to compensate for the offset is

$$\frac{-10\text{ mV}}{(305\ \mu\text{V}/2)} = -16.39 = 1000\ 0001\ 0000$$

SYSTEM GAIN CALIBRATION

The AD7262/AD7262-5 also allow the user to write to an external gain register, thus enabling the removal of any overall system gain error. Both ADC A and ADC B have independent external gain registers, allowing the user to calibrate independently the gain on both ADC A and ADC B signal paths. The gain calibration feature can be used to implement accurate gain matching between ADC A and ADC B.

The system calibration function is used by setting the sensors to which the AD7262/AD7262-5 are connected to a 0 gain state. The AD7262/AD7262-5 convert this analog input to a digital output code, which corresponds to the system gain and is available on the $D_{OUT}x$ pins. This digital output code can then be stored in the appropriate external register. For details on how to write to a register, see the Writing to a Register section and Table 11.

The gain calibration register contains seven bits of data. By changing the contents of the gain register, different amounts of gain on the analog input signal can be compensated for. The MSB is a sign bit, while the remaining six bits store the multiplication factor, which is used to adjust the analog input range. The gain register value is effectively multiplied by the analog input to scale the conversion result over the full range. Increasing the gain register multiplication factor compensates for a larger analog input range, and decreasing the gain register multiplier compensates for a smaller analog input range. Each bit in the gain calibration register has a resolution of 2.4×10^{-4} V (1/4096). A maximum of 1.538% of the analog range can be calibrated for. The multiplier factor stored in the gain register can be decoded as outlined in Table 13.

The gain registers can be cleared by writing all 0s to each register, as described in the Writing to a Register section. For accurate gain calibration, both the positive and negative full-scale digital output codes should be measured prior to determining the multiplication factor that is written to the gain register.

Table 13. Decoding of Multiplication Factors for Gain Calibration

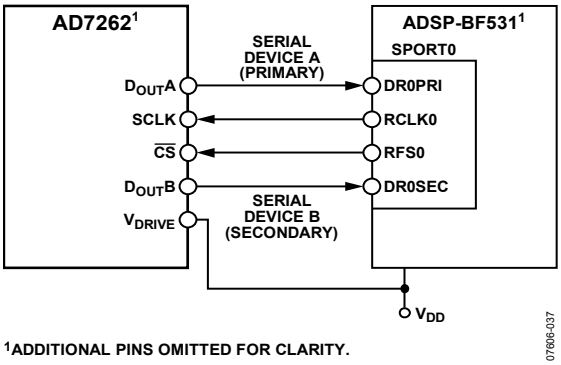
Analog Input	Digital Gain Error	Gain Register Code	Multiplier Equation	Multiplier Value	Comments
V	LSB	(Sign bit + 6 bits)	(1 ± x/4096)		
V_{IN} max	0 LSB	0 000000	1 − 0/4096	1	Sign bit = 0, which implies negative sign in multiplier equation
V_{IN} max − 244 µV	−2 LSB	0 000001	1 − 1/4096	0.999755859	Sign bit = 0, which implies negative sign in multiplier equation
V_{IN} max − (63 × 244 µV)	−126 LSB	0 111111	1 − 63/4096	0.98461914	Sign bit = 0, which implies negative sign in multiplier equation
V_{IN} max	0 LSB	1 000000	1 + 0/4096	1	Sign bit = 1, which implies plus sign in multiplier equation
V_{IN} max + 244 µV	+2 LSB	1 000001	1 + 1/4096	1.000244141	Sign bit = 1, which implies plus sign in multiplier equation
V_{IN} max + (63 × 244 µV)	+126 LSB	1 111111	1 + 63/4096	1.015380859	Sign bit = 1, which implies plus sign in multiplier equation

MICROPROCESSOR INTERFACING

The serial interface on the AD7262/AD7262-5 allows the parts to connect directly to a range of different microprocessors. This section explains how to interface the AD7262/AD7262-5 with the Analog Devices, Inc., Blackfin® DSP, the ADSP-BF531.

AD7262/AD7262-5 TO ADSP-BF531

The ADSP-BF531 and the rest of the Blackfin microprocessor family of DSPs interface directly to the AD7262/AD7262-5 without any glue logic required. The V_{DRIVE} pin of the AD7262/AD7262-5 takes the same supply voltage as that of the ADSP-BF531. This allows the ADC to operate at a higher supply voltage than its serial interface and, therefore, the ADSP-BF531, if necessary. The availability of secondary receive registers on the serial ports of the Blackfin DSPs means only one serial port is necessary to read from both D_{OUT} pins simultaneously. Figure 37 shows both $D_{OUT}A$ and $D_{OUT}B$ of the AD7262/AD7262-5 connected to Serial Port 0 of the ADSP-BF531. The SPORT0 Receive Configuration 1 register and SPORT0 Receive Configuration 2 register must be set up as outlined in Table 14 and Table 15.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 37. Interfacing the AD7262 to the ADSP-BF531

Table 14. The SPORT0 Receive Configuration 1 Register (SPORT0_RCR1)

Setting	Description
RCKFE = 1	Sample data with falling edge of RSCLK
LRFS = 1	Active low frame signal
RFSR = 1	Frame every word
IRFS = 1	Internal receive frame sync (RFS) used
RLSBIT = 0	Receive MSB first
RDTYPE = 00	Zero fill
IRCLK = 1	Internal receive clock
RSPEN = 1	Receive enabled
SLEN = 11110	31-bit data-word
TFSR = RFSR = 1	

Table 15. The SPORT0 Receive Configuration 2 Register (SPORT0_RCR2)

Setting	Description
RXSE = 1	Secondary side enabled

APPLICATION HINTS

GROUNDING AND LAYOUT

The analog and digital supplies to the AD7262/AD7262-5 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The printed circuit board (PCB) that houses the AD7262/AD7262-5 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All five AGND pins of the AD7262/AD7262-5 should be sunk in the AGND plane. Digital and analog ground planes should be joined in only one place. If the AD7262/AD7262-5 are in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point, that should be established as close as possible to the ground pins on the AD7262/AD7262-5.

Avoid running digital lines under the device because this couples noise onto the die. However, the analog ground plane should be allowed to run under the AD7262/AD7262-5 to avoid noise coupling. The power supply lines to the AD7262/ AD7262-5 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, fast switching signals, such as clocks, should be shielded with digital ground, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feedthrough within the board, traces on opposite sides of the board should run at right angles to each other. A microstrip technique is the best method but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum capacitors in parallel with 100 nF capacitors to GND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface-mount types. These low ESR and ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

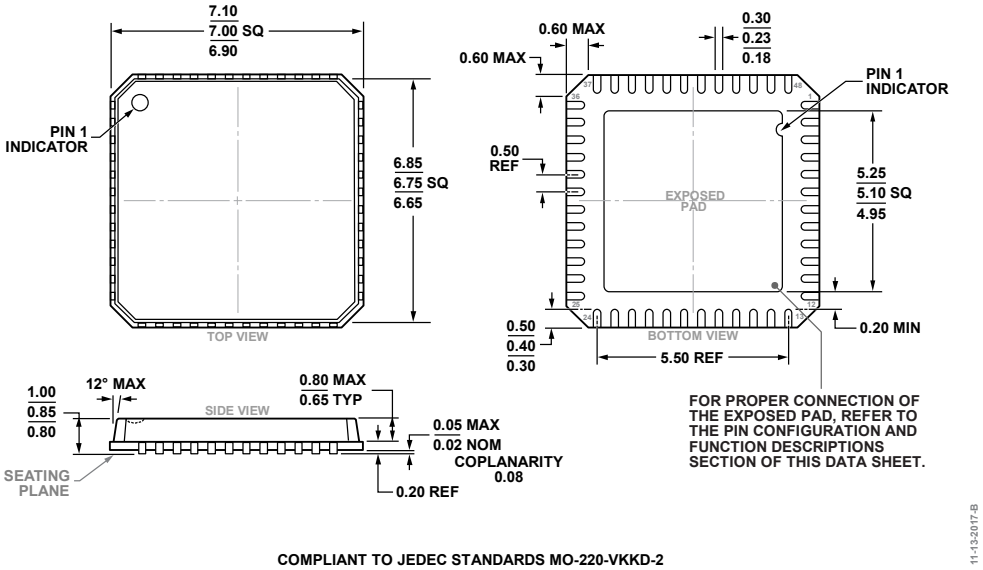
PCB DESIGN GUIDELINES FOR LFCSP

The land on the chip scale packages (CP-48-1) are rectangular. The PCB pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width, thereby having a portion of the pad exposed. To ensure that the solder joint size is maximized, the land should be centered on the pad.

The bottom of the chip scale package has a thermal pad. The thermal pad on the PCB should be at least as large as the exposed pad. On the PCB, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern to ensure that shorting is avoided.

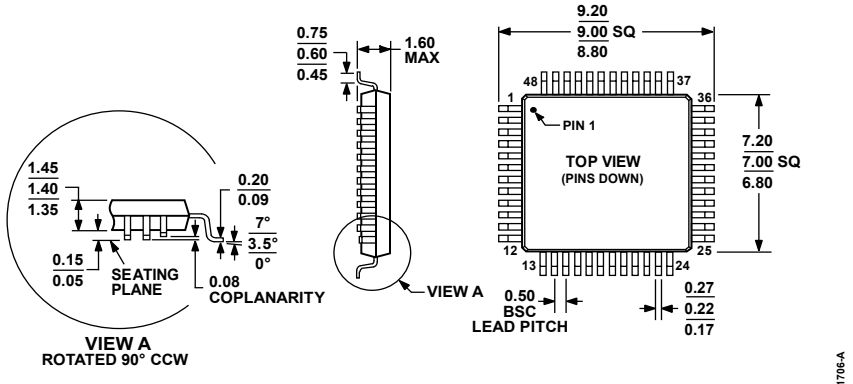
To improve thermal performance of the package, use thermal vias on the PCB, incorporating them into the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via. The user should connect the PCB thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 38. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.85 mm Package Height
(CP-48-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 39. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7262BCPZ-RL7	−40°C to +105°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-1
AD7262BSTZ	−40°C to +105°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD7262BSTZ-RL7	−40°C to +105°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD7262BSTZ-5	−40°C to +105°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD7262BSTZ-5-RL7	−40°C to +105°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
EVAL-AD7262EDZ		Evaluation Board	
EVAL-CED1Z		Development Board	

[1] Z = RoHS Compliant Part.

NOTES

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