



DS26503

T1/E1/J1 BITS Element

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GENERAL DESCRIPTION

The DS26503 is a building-integrated timing-supply (BITS) clock-recovery element. It also functions as a basic T1/E1 transceiver. The receiver portion can recover a clock from T1, E1, and 6312kHz synchronization timing interfaces. In T1 and E1 modes, the Synchronization Status Message (SSM) can also be recovered. The transmit portion can directly interface to T1 or E1 interfaces as well as source the SSM in T1 and E1 modes. The DS26503 can translate between any of the supported inbound synchronization clock rates to any supported outbound rate. A separate output is provided to source a 6312kHz clock. The device is controlled through a parallel, serial, or hardware controller port.

APPLICATIONS

BITS Timing
Rate Conversion
Basic Transceiver

ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|-----------|----------------|-------------|
| DS26503L | 0°C to +70°C | 64 LQFP |
| DS26503LN | -40°C to +85°C | 64 LQFP |

FEATURES

- G.703 2048kHz Synchronization Interface Compliant
- G.703 6312kHz Japanese Synchronization Interface Compliant
- Interfaces to Standard T1/J1 (1.544MHz) and E1 (2.048MHz)
- Interface to CMI-Coded T1/J1 and E1
- Short- and Long-Haul Line Interface
- Transmit and Receive T1 and E1 SSM Messages with Message Validation
- T1/E1 Jitter Attenuator with Bypass Mode
- Fully Independent Transmit and Receive Functionality
- Internal Software-Selectable Receive- and Transmit-Side Termination for 75Ω/100Ω/110Ω/120Ω
- Monitor Mode for Bridging Applications
- Accepts 16.384MHz, 12.8MHz, 8.192MHz, 4.096MHz, 2.048MHz, or 1.544MHz Master Clock
- 8-Bit Parallel Control Port, Multiplexed or Nonmultiplexed, Intel or Motorola
- Serial (SPI) Control Port
- Hardware Control Mode
- Provides LOS, AIS, and LOF Indications Through Hardware Output Pins
- Fast Transmitter-Output Disable Through Device Pin for Protection Switching
- IEEE 1149.1 JTAG Boundary Scan
- 3.3V Supply with 5V-Tolerant Inputs and Outputs

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.

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1. FEATURES

1.1 General

- 64-pin, 10mm x 10mm LQFP package
- 3.3V supply with 5V-tolerant inputs and outputs
- Evaluation kits
- IEEE 1149.1 JTAG Boundary Scan
- Driver source code available from the factory

1.2 Line Interface

- Requires a single master clock (MCLK) for E1, T1, or J1 operation. Master clock can be 2.048MHz, 4.096MHz, 8.192MHz, 12.8MHz (**available in CPU interface mode only**), or 16.384MHz. Option to use 1.544MHz, 3.088MHz, 6.176MHz, or 12.5552MHz for T1-only operation.
- Fully software configurable
- Short- and long-haul applications
- Automatic receive sensitivity adjustments
- Ranges include 0dB to -43dB or 0dB to -12dB for E1 applications; 0dB to -36dB or 0dB to -15dB for T1 applications
- Receive level indication in 2.5dB steps from -42.5dB to -2.5dB
- Internal receive termination option for 75 Ω , 100 Ω , 110 Ω , and 120 Ω lines
- Monitor application gain settings of 20dB, 26dB, and 32dB
- G.703 receive-synchronization signal mode
- Flexible transmit-waveform generation
- T1 DSX-1 line build-outs
- E1 waveforms include G.703 waveshapes for both 75 Ω coax and 120 Ω twisted cables
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Square-wave output
- Open-drain output option
- Transmitter power-down
- Transmitter 50mA short-circuit limiter with exceeded indication of current limit
- Transmit open-circuit-detected indication

1.3 Jitter Attenuator (T1/E1 Modes Only)

- 32-bit or 128-bit crystal-less jitter attenuator
- Requires only a 2.048MHz master clock for both E1 and T1 operation with the option to use 1.544MHz for T1 operation
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

1.4 Framer/Formatter

- Full receive and transmit path transparency
- T1 framing formats include D4 and ESF
- E1 framing formats include FAS and CRC4
- Detailed alarm and status reporting with optional interrupt support
- RLOF, RLOS, and RAIS alarms interrupt on change of state
- Japanese J1 support includes:
 - Ability to calculate and check CRC6 according to the Japanese standard
 - Ability to generate yellow alarm according to the Japanese standard

1.5 Test and Diagnostics

- Remote and Local Loopback

1.6 Control Port

- 8-bit parallel or serial control port
- Multiplexed or nonmultiplexed buses
- Intel or Motorola formats
- Supports polled or interrupt-driven environments
- Software access to device ID and silicon revision
- Software-reset supported with automatic clear on power-up
- Hardware controller port
- Hardware reset pin

2. SPECIFICATIONS COMPLIANCE

The DS26503 meets all applicable sections of the latest telecommunications specifications including those in the following tables.

Table 2-1. T1-Related Telecommunications Specifications

| |
|--|
| ANSI T1.102 - Digital Hierarchy Electrical Interface |
| ANSI T1.231 - Digital Hierarchy–Layer 1 in Service Performance Monitoring |
| ANSI T1.403 - Network and Customer Installation Interface–DS1 Electrical Interface |
| TR62411 |
| (ANSI) “Digital Hierarchy – Electrical Interfaces” |
| (ANSI) “Digital Hierarchy – Formats Specification” |
| (ANSI) “Digital Hierarchy – Layer 1 In-Service Digital Transmission Performance Monitoring” |
| (ANSI) “Network and Customer Installation Interfaces–DS1 Electrical Interface” |
| (AT&T) “Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Super frame Format” |
| (AT&T) “High Capacity Digital Service Channel Interface Specification” |
| (TTC) “Frame Structures on Primary and Secondary Hierarchical Digital Interfaces” |
| (TTC) “ISDN Primary Rate User-Network Interface Layer 1 Specification” |

Table 2-2. E1-Related Telecommunications Specifications

| |
|--|
| ITU-T G.703 Physical/Electrical Characteristics of G.703 Hierarchical Digital Interfaces |
| ITU-T G.736 Characteristics of Synchronous Digital Multiplex Equipment operating at 2048kbps |
| ITU-T G.742 Second-Order Digital Multiplex Equipment Operating at 8448kbps |
| ITU-T G.772 |
| ITU-T G.775 |
| ITU-T G.823 The control of jitter and wander within digital networks, which are based on 2.048kbps hierarchy |
| ETSI 300 233 |
| (ITU) "Synchronous Frame Structures used at 1544, 6312k, 2048, 8488, and 44,736kbps Hierarchical Levels" |
| (ITU) "Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704" |
| (ITU) "Characteristics of primary PCM Multiplex Equipment Operating at 2048kbps" |
| (ITU) Characteristics of a synchronous digital multiplex equipment operating at 2048kbps" |
| (ITU) "Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria" |
| (ITU) "The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048kbps Hierarchy" |
| (ITU) "Primary Rate User-Network Interface – Layer 1 Specification" |
| (ITU) "Error Performance Measuring Equipment Operating at the Primary Rate and Above" |
| (ITU) "In-service code violation monitors for digital systems" |
| (ETSI) "Integrated Services Digital Network (ISDN); Primary rate User-Network Interface (UNI); Part 1/ Layer 1 specification" |
| (ETSI) "Transmission and multiplexing; Physical/electrical characteristics of hierarchical digital interfaces for equipment using the 2048kbps-based plesiochronous or synchronous digital hierarchies" |
| (ETSI) "Integrated Services Digital Network (ISDN); Access digital section for ISDN primary rate" |
| (ETSI) "Integrated Services Digital Network (ISDN); Attachment requirements for terminal equipment to connect to an ISDN using ISDN primary rate access" |
| (ETSI) "Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2048kbps digital unstructured leased lines (D2048U) attachment requirements for terminal equipment interface" |
| (ETSI) "Business Telecommunications (BTC); 2048kbps digital structured leased lines (D2048S); Attachment requirements for terminal equipment interface" |
| (ITU) "Synchronous Frame Structures used at 1544, 6312, 2048, 8488, and 44,736kbps Hierarchical Levels" |
| (ITU) "Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704" |

3. BLOCK DIAGRAMS

Figure 3-1. Block Diagram

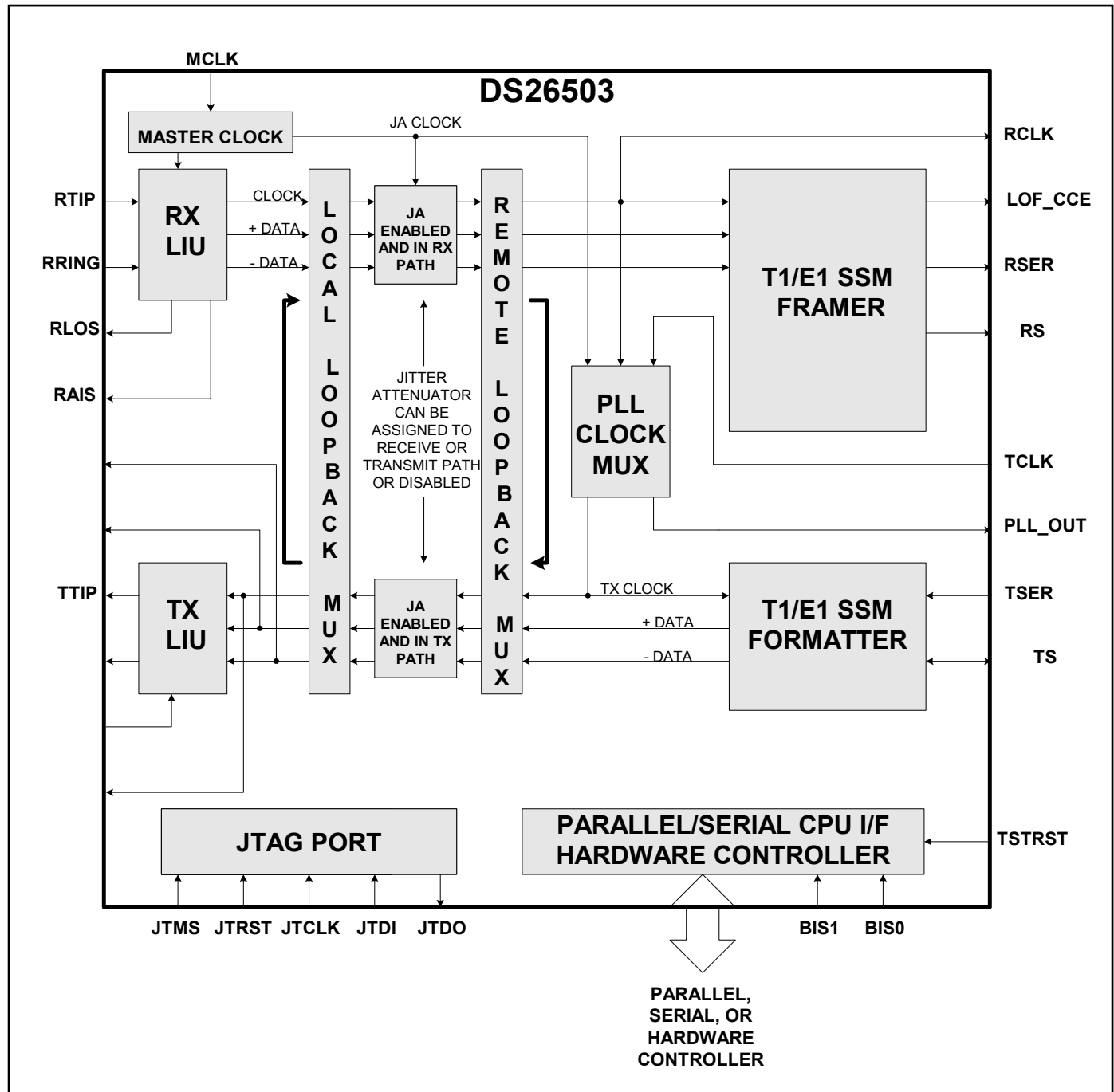


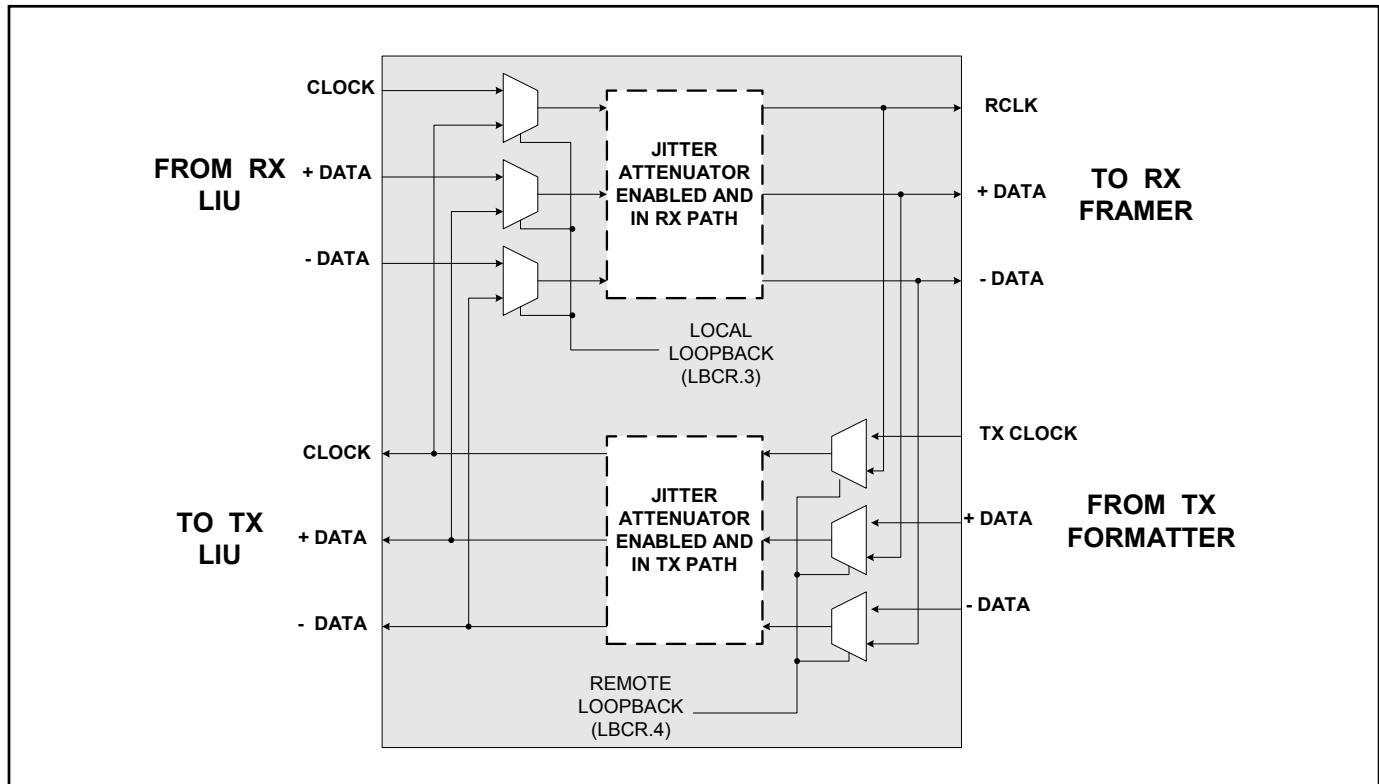
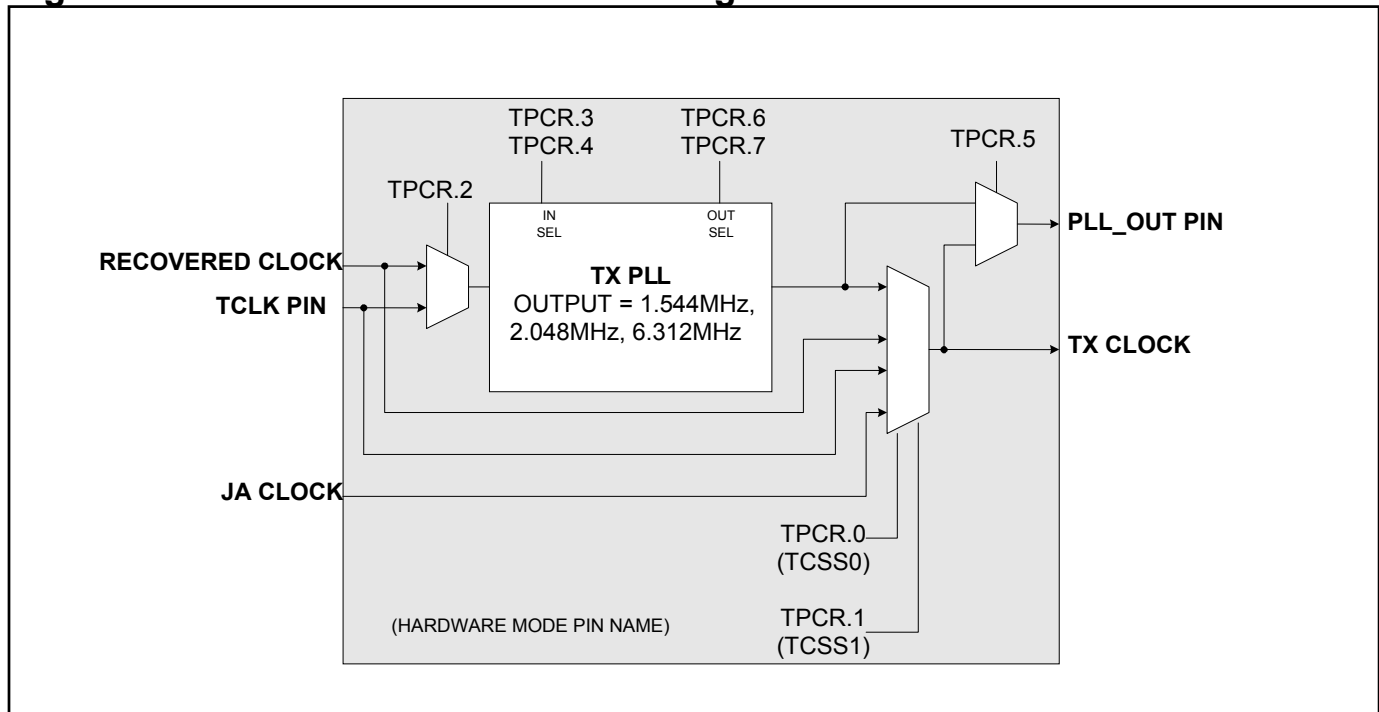
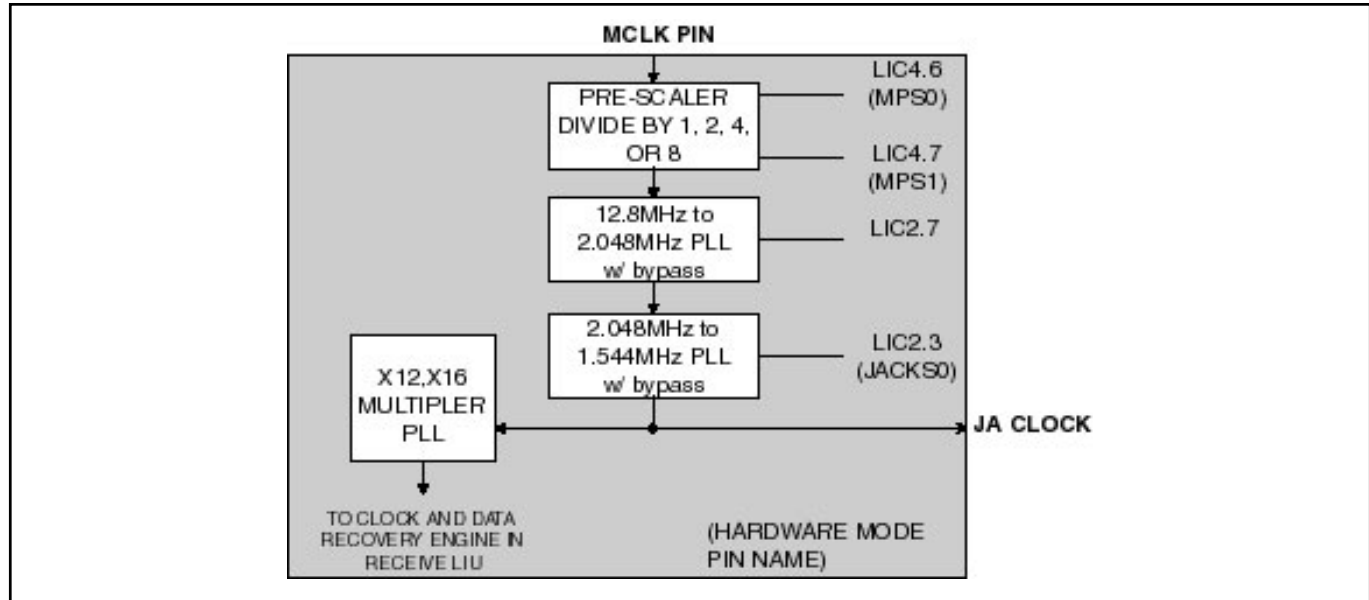
Figure 3-2. Loopback Mux Diagram (T1/E1 Modes Only)**Figure 3-3. Transmit PLL Clock Mux Diagram**

Figure 3-4. Master Clock PLL Diagram

4. PIN FUNCTION DESCRIPTION

4.1 Transmit PLL

| NAME | TYPE | FUNCTION |
|---------|------|--|
| PLL_OUT | O | Transmit PLL Output. This pin can be selected to output the 1544kHz, 2048kHz, 64kHz, or 6312kHz output from the internal TX PLL or the internal signal, TX CLOCK. See Figure 3-3 and Figure 3-4 . |
| TCLK | I | Transmit Clock Input. A 64kHz, 1.544MHz, 2.048MHz, or 6312kHz primary clock. May be selected by the TX PLL mux to either directly drive the transmit section or be converted to one of the other rates prior to driving the transmit section. See Figure 3-3 and Figure 3-4 . |

4.2 Transmit Side

| NAME | TYPE | FUNCTION |
|-------|------|---|
| TSER | I | Transmit Serial Data. Source of transmit data sampled on the falling edge of TX CLOCK (an internal signal). See Figure 3-3 , Figure 3-4 , and Figure 19-11 (transmit timing diagram). |
| TS | I/O | TSYNC. When in input mode, this pin is sampled on the falling edge of TX CLOCK (an internal signal) and a pulse at this pin will establish either frame or multiframe boundaries for the transmit side. See Figure 3-1 and Figure 19-11 . In output mode, the pin is updated on the rising edge of TX CLOCK (an internal signal) and can be programmed to output a frame or multiframe sync pulse useful for aligning data. See Figure 3-1 and Figure 19-11 . |
| TCLKO | O | Transmit Clock Output. Buffered clock that is used to clock data through the transmit-side formatter (i.e., either TCLK or RCLK). |
| TPOSO | O | Transmit Positive-Data Output. In T1 or E1 mode, updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. Can be programmed to source NRZ data via the output-data format (IOCR1.0) control bit. In 6312kHz mode, this pin is low. |
| TNEGO | O | Transmit Negative-Data Output. In T1 or E1 mode, updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. In 6312kHz mode, this pin is low. |

4.3 Receive Side

| NAME | TYPE | FUNCTION |
|------|------|---|
| RCLK | O | Receive Clock. Recovered 1.544MHz (T1), 2.048MHz (E1), or 6312kHz (G.703 Synchronization Interface). |
| RS | O | Receive Sync <i>T1/E1 Mode:</i> An extracted pulse, one RCLK wide, is output at this pin that identifies either frame (IOCR1.5 = 0) or multiframe (IOCR1.5 = 1) boundaries. If set to output frame boundaries, then through IOCR1.6, RS can also be set to output double-wide pulses on signaling frames in T1 mode. <i>6312kHz Mode:</i> This pin will be in a high-impedance state. |
| RSER | O | Receive Serial Data <i>T1/E1 Mode:</i> This is the received NRZ serial data updated on rising edges of RCLK. <i>6312kHz Mode:</i> This pin will be in a high-impedance state. |
| RLOF | O | Receive Loss Of Frame. This output can be configured to be a Loss Of Transmit Clock indicator via IOCR.4 when operating in T1 or E1 mode. <i>T1/E1 Mode:</i> Set when the receive synchronizer is searching for frame alignment (RLOF mode), or set when the signal at the TCLK pin has not transitioned for approximately 15 periods of the scaled MCLK (LOTC mode). <i>6312kHz Mode:</i> This pin will be in a high-impedance state. |
| RLOS | O | Receive Loss Of Signal <i>T1 Mode:</i> High when 192 consecutive zeros detected. <i>E1 Mode:</i> High when 255 consecutive zeros detected. <i>6312kHz Mode:</i> High when consecutive zeros detected for 65 μ s typically. |
| RAIS | O | Receive Alarm Indication Signal <i>T1 Mode:</i> Will toggle high when receive Blue Alarm is detected. <i>E1 Mode:</i> Will toggle high when receive AIS is detected. <i>6312kHz Mode:</i> This pin will be in a high-impedance state. |

4.4 Controller Interface

| NAME | TYPE | FUNCTION |
|-------------------------------------|------|---|
| $\overline{\text{INT}}$ / JACKS0 | I/O | <p>Active-Low Interrupt/Jitter Attenuator Clock Select 0</p> <p>$\overline{\text{INT}}$: Flags host controller during events, alarms, and conditions defined in the status registers. Active-low open-drain output.</p> <p>JACKS0: Hardware Mode: Jitter Attenuator Clock Select 0. Set this pin high for T1 mode operation when either a 2.048MHz, 4.096MHz, 8.192MHz or 16.382MHz signal is applied at MCLK.</p> |
| TMODE1 | I | Transmit Mode Select 1. In Hardware Mode (BIS[1:0] = 11), this bit is used to configure the transmit operating mode. |
| TMODE2 | I | Transmit Mode Select 2. In Hardware Mode (BIS[1:0] = 11), this bit is used to configure the transmit operating mode. |
| TSTRST | I | Three-State Control and Device Reset. A dual-function pin. A zero-to-one transition issues a hardware reset to the DS26503 register set. Configuration register contents are set to the default state. Leaving TSTRST high three-states all output and I/O pins (including the parallel control port). Set low for normal operation. Useful for in-board level testing. |
| BIS[1:0] | I | <p>Processor Interface Mode Select 1, 0. These bits select the processor interface mode of operation.</p> <p>BIS[1:0] : 00 = Parallel Port Mode (Multiplexed) 01 = Parallel Port Mode (Nonmultiplexed) 10 = Serial Port Mode 11 = Hardware Mode</p> |
| AD[7]/ RITD | I/O | <p>Data Bus D[7] or Address/Data Bus AD[7]/Receive Internal Termination Disable</p> <p>A[7]: In nonmultiplexed bus operation (BIS[1:0] = 01), it serves as the data bus D[7].</p> <p>AD[7]: In multiplexed bus operation (BIS[1:0] = 00), it serves as the multiplexed address/data bus AD[7].</p> <p>RITD: In Hardware Mode (BIS[1:0] = 11), internal receive termination is disabled when RITD = 1.</p> |
| AD[6]/ TITD | I/O | <p>Data Bus D[6] or Address/Data Bus AD[6]/Transmit Internal Termination Disable</p> <p>A[6]: In nonmultiplexed bus operation (BIS[1:0] = 01), it serves as the data bus D[6].</p> <p>AD[6]: In multiplexed bus operation (BIS[1:0] = 00), it serves as the multiplexed address/data bus AD[6].</p> <p>TITD: In Hardware Mode (BIS[1:0] = 11), internal transmit termination is disabled when TITD = 1.</p> |

| NAME | TYPE | FUNCTION |
|--------------------|------|--|
| AD[5]/ RMODE1 | I/O | <p>Data Bus D[5] or Address/Data Bus AD[5]/Receive Framing Mode Select Bit 1</p> <p><i>A[5]</i>: In nonmultiplexed bus operation ($BIS[1:0] = 01$), it serves as the data bus D[5].</p> <p><i>AD[5]</i>: In multiplexed bus operation ($BIS[1:0] = 00$), it serves as the multiplexed address/data bus AD[5].</p> <p><i>RMODE1</i>: In Hardware Mode ($BIS[1:0] = 11$), it selects the receive side operating mode.</p> |
| AD[4]/ RMODE0 | I/O | <p>Data Bus D[4] or Address/Data Bus AD[4]/Receive Framing Mode Select Bit 0</p> <p><i>A[4]</i>: In nonmultiplexed bus operation ($BIS[1:0] = 01$), it serves as the data bus D[4].</p> <p><i>AD[4]</i>: In multiplexed bus operation ($BIS[1:0] = 00$), it serves as the multiplexed address/data bus AD[4].</p> <p><i>RMODE0</i>: In Hardware Mode ($BIS[1:0] = 11$), it selects the receive side operating mode.</p> |
| AD[3]/TSM | I/O | <p>Data Bus D[3] or Address/Data Bus AD[3]/TS Mode Select</p> <p><i>A[3]</i>: In nonmultiplexed bus operation ($BIS[1:0] = 01$), it serves as the data bus D[3].</p> <p><i>AD[3]</i>: In multiplexed bus operation ($BIS[1:0] = 00$), it serves as the multiplexed address/data bus AD[3].</p> <p><i>TSM</i>: In Hardware Mode ($BIS[1:0] = 11$), this pin selects the function of TS. Please see the register descriptions for more detailed information.</p> |
| AD[2]/RSM/ SCLK | I/O | <p>Data Bus D[2] or Address/Data Bus AD[2]/RS Mode Select/Serial Port Clock</p> <p><i>A[2]</i>: In nonmultiplexed bus operation ($BIS[1:0] = 01$), it serves as the data bus D[2].</p> <p><i>AD[2]</i>: In multiplexed bus operation ($BIS[1:0] = 00$), it serves as the multiplexed address/data bus AD[2].</p> <p><i>RSM</i>: In Hardware Mode ($BIS[1:0] = 11$), this pin selects the function of RS. Please see the register descriptions for more detailed information.</p> <p><i>SCLK</i>: In Serial Port mode this is the serial clock input.</p> |

| NAME | TYPE | FUNCTION |
|---------------------------|------|--|
| AD[1]/ RMODE3/ MOSI | I/O | <p>Data Bus D[1] or Address/Data Bus AD[1]/Receive Mode Select 3/Master Out-Slave In</p> <p><i>A[1]</i>: In nonmultiplexed bus operation (BIS[1:0] = 01), it serves as the data bus D[1].</p> <p><i>AD[1]</i>: In multiplexed bus operation (BIS[1:0] = 00), it serves as the multiplexed address/data bus AD[1].</p> <p><i>RMODE3</i>: In Hardware Mode (BIS[1:0] = 11), this pin selects the receive side operating mode.</p> <p><i>MOSI</i>: Serial data input called Master Out-Slave In for clarity of data transfer direction.</p> |
| AD[0]/ TCSS0/ MISO | I/O | <p>Data Bus D[0] or Address/Data Bus AD[0]/Transmit Clock Source Select 0/Master In-Slave Out</p> <p><i>A[0]</i>: In nonmultiplexed bus operation (BIS[1:0] = 01), it serves as the data bus D[0].</p> <p><i>AD[0]</i>: In multiplexed bus operation (BIS[1:0] = 00), it serves as the multiplexed address/data bus AD[0].</p> <p><i>TCSS0</i>: Transmit Clock Source Select 0.</p> <p><i>MISO</i>: In serial bus mode (BIS[1:0] = 10), this pin serves as the serial data output Master In-Slave Out.</p> |
| TCSS1 | I | Transmit Clock Source Select 1 |
| A6/MPS0 | I | <p>Address Bus Bit A[6]/MCLK Prescale Select 0</p> <p><i>A6</i>: In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[6]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low.</p> <p><i>MPS0</i>: In Hardware Mode (BIS[1:0] = 11), MCLK prescale select is used to set the prescale value for the PLL.</p> |
| A5/CPOL/ TMODE0 | I | <p>Address Bus Bit A[5]/Serial Port Clock Polarity Select/Transmit Mode Select 0</p> <p><i>A5</i>: In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[5]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low.</p> <p><i>CPOL</i>: In Serial Port Mode (BIS[1:0] = 10), this pin selects the serial port clock polarity. Please see the functional timing diagrams for the Serial Port Interface for more information.</p> <p><i>TMODE0</i>: In Hardware Mode (BIS[1:0] = 11), this pin is used to configure the transmit operating mode.</p> |

| NAME | TYPE | FUNCTION |
|----------------|------|--|
| A4/CPHA/ L2 | I | <p>Address Bus Bit A[4]/Serial Port Clock Phase Select/Line Build-Out Select 2</p> <p><i>A4</i>: In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[4]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low.</p> <p><i>CPHA</i>: In Serial Port Mode (BIS[1:0] = 10), this pin selects the serial port clock phase. See the functional timing diagrams for the Serial Port Interface for more information.</p> <p><i>L2</i>: In Hardware Mode (BIS[1:0] = 11), this pin selects the line build-out value.</p> |
| A3/L1 | I | <p>Address Bus Bit A[3]/Line Build-Out Select 1</p> <p><i>A3</i>: In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[3]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low.</p> <p><i>L1</i>: In Hardware Mode (BIS[1:0] = 11), this pin selects the line build-out value.</p> |
| A2/L0 | I | <p>Address Bus Bit A[2]/Line Build-Out Select 0</p> <p><i>A2</i>: In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[2]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low.</p> <p><i>L0</i>: In Hardware Mode (BIS[1:0] = 11), this pin selects the line build-out value.</p> |
| A1/TAIS | I | <p>Address Bus Bit A[1]/Transmit AIS</p> <p><i>A1</i>: In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[1]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low.</p> <p><i>TAIS</i>: When set to a 0 and in T1/E1 operating modes, the transmitter will transmit an AIS pattern. Set to 1 for normal operation. This pin is ignored in all other operating modes.</p> |
| A0/E1TS | I | <p>Address Bus Bit A[0]/E1 Termination Select</p> <p><i>A0</i>: In nonmultiplexed bus operation (BIS[1:0] = 01), this pin serves as A[0]. In multiplexed bus operation (BIS[1:0] = 00), these pins are not used and should be tied low.</p> <p><i>E1TS</i>: In Hardware Mode (BIS[1:0] = 11), selects the E1 internal termination value (0 = 75Ω, 1 = 120Ω).</p> |

| NAME | TYPE | FUNCTION |
|---|------|--|
| BTS/HBE | I | <p>Bus Type Select/Transmit and Receive B8ZS/HDB3 Enable</p> <p><i>BTS</i>: Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the \overline{RD} (\overline{DS}), ALE (AS), and \overline{WR} (R/W) pins. If $BTS = 1$, then these pins assume the function listed in parentheses ().</p> <p><i>HBE</i>: In Hardware Mode ($BIS[1:0] = 11$), this pin enables transmit and receive B8ZS/HDB3 when in T1/E1 operating modes.</p> |
| \overline{RD} (\overline{DS})/ RMODE2 | I | <p>Read Input-Data Strobe/Receive Mode Select Bit 2</p> <p>\overline{RD} (\overline{DS}): These pins are active-low signals. DS is active high when $BIS[1:0] = 01$. See the bus timing diagrams.</p> <p><i>RMODE2</i>: In Hardware Mode ($BIS[1:0] = 11$), this pin selects the receive side operating mode.</p> |
| \overline{CS} /RLB | I | <p>Chip Select/Remote Loopback Enable</p> <p>\overline{CS}: This active-low signal must be low to read or write to the device. This signal is used for both the parallel port and the serial port modes.</p> <p><i>RLB</i>: In Hardware Mode ($BIS[1:0] = 11$), when high, remote loopback is enabled. This function is only valid when the transmit side and receive side are in the same operating mode.</p> |
| ALE (AS)/ A7/MPS1 | I | <p>Address Latch Enable (Address Strobe)/Address Bus Bit 7/MCLK Prescale Select 1</p> <p><i>ALE</i> (AS): In multiplexed bus operation ($BIS[1:0] = 00$), it serves to demultiplex the bus on a positive-going edge.</p> <p><i>A7</i>: In nonmultiplexed bus operation ($BIS[1:0] = 01$), this pin serves as A[7].</p> <p><i>MPS1</i>: In Hardware Mode ($BIS[1:0] = 11$), MCLK prescale select, used to set the prescale value for the PLL.</p> |
| \overline{WR} (R/ \overline{W})/ TMODE3 | I | <p>Write Input (Read/Write)/Transmit Mode Select 3</p> <p>\overline{WR}: In Processor Mode, this pin is the active-low write signal.</p> <p><i>TMODE3</i>: In Hardware Mode, this pin selects the transmit-side operating mode.</p> |

4.5 JTAG

| NAME | TYPE | FUNCTION |
|---------------------------|------|---|
| JTCLK | I | JTAG Clock. This clock input is typically a low frequency (less than 10MHz) 50% duty cycle clock signal. |
| JTMS | I | JTAG Mode Select (with Pullup). This input signal is used to control the JTAG controller state machine and is sampled on the rising edge of JTCLK. |
| JTDI | I | JTAG Data Input (with Pullup). This input signal is used to input data into the register that is enabled by the JTAG controller state machine and is sampled on the rising edge of JTCLK. |
| JTDO | O | JTAG Data Output. This output signal is the output of an internal scan shift register enabled by the JTAG controller state machine and is updated on the falling edge of JTCLK. The pin is in the high-impedance mode when a register is not selected or when the $\overline{\text{JTRST}}$ signal is high. The pin goes into and exits the high impedance mode after the falling edge of JTCLK. |
| $\overline{\text{JTRST}}$ | I | JTAG Reset (Active Low). This input forces the JTAG controller logic into the reset state and forces the JTDO pin into high impedance when low. This pin should be low while power is applied and set high after the power is stable. The pin can be driven high or low for normal operation, but must be high for JTAG operation. |

4.6 Line Interface

| NAME | TYPE | FUNCTION |
|-------|------|---|
| MCLK | I | Master Clock Input. A (50ppm) clock source. This clock is used internally for both clock/data recovery and for the jitter attenuator for both T1 and E1 modes. The clock rate can be 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz. When using the DS26503 in T1-only operation, a 1.544MHz (50ppm) clock source can be used. |
| RTIP | I | Receive Tip. Analog input for clock recovery circuitry. This pin connects via a 1:1 transformer to the network. See the <i>Line Interface Unit</i> section for details. |
| RRING | I | Receive Ring. Analog input for clock recovery circuitry. This pin connects via a 1:1 transformer to the network. See the <i>Line Interface Unit</i> section for details. |
| TTIP | O | Transmit Tip. Analog line-driver output. This pin connects via a 1:2 step-up transformer to the network. See the <i>Line Interface Unit</i> section for details. |
| TRING | O | Transmit Ring. Analog line-driver output. This pin connects via a 1:2 step-up transformer to the network. See the <i>Line Interface Unit</i> section for details. |
| THZE | I | Transmit High-Impedance Enable. When high, TTIP and TRING will be placed into a high-impedance state. |

4.7 Power

| NAME | TYPE | FUNCTION |
|------|------|--|
| DVDD | — | Digital Positive Supply. 3.3V \pm 5%. Should be tied to the RVDD and TVDD pins. |
| RVDD | — | Receive Analog Positive Supply. 3.3V \pm 5%. Should be tied to the DVDD and TVDD pins. |
| TVDD | — | Transmit Analog Positive Supply. 3.3V \pm 5%. Should be tied to the DVDD and RVDD pins. |
| DVSS | — | Digital Signal Ground. 0.0V. Should be tied to the RVSS and TVSS pins. |
| RVSS | — | Receive Analog Signal Ground. 0.0V. Should be tied to the DVSS and TVSS pins. |
| TVSS | — | Transmit Analog Signal Ground. 0.0V. Should be tied to the DVSS and RVSS pins. |

5. PINOUT

Table 5-1. LQFP Pinout

| PIN | TYPE | MODE | | | FUNCTION |
|--------------|------|---------------|-------------|----------|---|
| | | PARALLEL PORT | SERIAL PORT | HARDWARE | |
| 1 | I/O | AD2 | SCLK | RSM | Parallel Port Mode: Address/Data Bus Bit 2 Serial Port Mode: Serial Clock Hardware Mode: RS Mode Select |
| 2 | I/O | AD3 | — | TSM | Parallel Port Mode: Address/Data Bus Bit 3 Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: TS Mode Select |
| 3 | I/O | AD4 | — | RMODE0 | Parallel Port Mode: Address/Data Bus Bit 4 Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: Receive Mode Select 0 |
| 4 | I/O | AD5 | — | RMODE1 | Parallel Port Mode: Address/Data Bus Bit 5 Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: Receive Mode Select 1 |
| 5 | I/O | AD6 | — | TITD | Parallel Port Mode: Address/Data Bus Bit 6 Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: Transmit Internal Termination Disable |
| 6 | I/O | AD7 | — | RITD | Parallel Port Mode: Address/Data Bus Bit 7 Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: Receive Internal Termination Disable |
| 7, 24, 58 | I | DVDD | DVDD | DVDD | Digital Positive Supply |
| 8, 22, 56 | I | DVSS | DVSS | DVSS | Digital Signal Ground |
| 9 | I | A0 | — | E1TS | Parallel Port Mode: Address Bus Bit 0 Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: E1 Internal Termination Select |
| 10 | I | A1 | — | TAIS | Parallel Port Mode: Address Bus Bit 1 Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: Transmit AIS |
| 11 | I | A2 | — | L0 | Parallel Port Mode: Address Bus Bit 2 Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: Line Build-Out Select 0 |
| 12 | I | A3 | — | L1 | Parallel Port Mode: Address Bus Bit 3 Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: Line Build-Out Select 1 |
| 13 | I | A4 | CPHA | L2 | Parallel Port Mode: Address Bus Bit 4 Serial Port Mode: Serial Port Clock Phase Select Hardware Mode: Line Build-Out Select 2 |
| 14 | I | A5 | CPOL | TMODE0 | Parallel Port Mode: Address Bus Bit 5 Serial Port Mode: Serial Port Clock Polarity Select Hardware Mode: Transmit Mode Select 0 |
| 15 | I | A6 | — | MPS0 | Parallel Port Mode: Address Bus Bit 6 Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: MCLK Pre-Scaler Select 0 |
| 16 | I | ALE (AS)/A7 | — | MPS1 | Parallel Port Mode: Address Latch Enable/Address Bus Bit 7 Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: MCLK Pre-Scaler Select 1 |
| 17 | I | TCLK | TCLK | TCLK | Transmit Clock Input |

| PIN | TYPE | MODE | | | FUNCTION |
|------------|------|---------------|-------------|----------|---|
| | | PARALLEL PORT | SERIAL PORT | HARDWARE | |
| 18 | O | TCLKO | TCLKO | TCLKO | Transmit Clock Output |
| 19 | O | TNEGO | TNEGO | TNEGO | Transmit Negative-Data Output |
| 20 | O | TPOSO | TPOSO | TPOSO | Transmit Positive-Data Output |
| 21 | I | TSER | TSER | TSER | Transmit Serial Data |
| 23 | I/O | TS | TS | TS | T1/E1 Mode: Transmit Frame/Multiframe Sync |
| 25 | O | RCLK | RCLK | RCLK | Receive Clock |
| 26 | O | RS | RS | RS | T1/E1 Mode: Receive Frame/Multiframe Boundary |
| 27 | — | N.C. | N.C. | N.C. | No Connect. This pin must be left open. |
| 28 | O | RSER | RSER | RSER | Receive Serial Data |
| 29 | O | RAIS | RAIS | RAIS | Receive Alarm Indication Signal |
| 30 | O | RLOF | RLOF | RLOF | Receive Loss of Frame |
| 31 | I | — | — | TCSS1 | Parallel Port Mode: Unused, should be connected to V _{SS} . Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: Transmit Clock Source Select 1 |
| 32 | O | RLOS | RLOS | RLOS | Receive Loss Of Signal |
| 33 | I | JTMS | JTMS | JTMS | IEEE 1149.1 Test Mode Select |
| 34 | I | JTCLK | JTCLK | JTCLK | IEEE 1149.1 Test Clock Signal |
| 35 | I | JTRST | JTRST | JTRST | IEEE 1149.1 Test Reset |
| 36 | I | JTDI | JTDI | JTDI | IEEE 1149.1 Test Data Input |
| 37 | O | JTDO | JTDO | JTDO | IEEE 1149.1 Test Data Output |
| 38 | I | RVDD | RVDD | RVDD | Receive Analog Positive Supply |
| 39 | I | TSTRST | TSTRST | TSTRST | Test/Reset |
| 40, 43, 45 | I | RVSS | RVSS | RVSS | Receive Analog Signal Ground |
| 41 | I | RTIP | RTIP | RTIP | Receive Analog Tip Input |
| 42 | I | RRING | RRING | RRING | Receive Analog Ring Input |
| 44 | I | MCLK | MCLK | MCLK | Master Clock Input |
| 46 | I/O | INT | INT | JACKS0 | Parallel Port Mode: Active-Low Interrupt Serial Port Mode: Active-Low Interrupt Hardware Mode: Jitter Attenuator Clock Select 0 |
| 47 | O | PLL_OUT | PLL_OUT | PLL_OUT | Transmit PLL (TX PLL) Clock Output |
| 48 | I | — | — | TMODE2 | Parallel Port Mode: Unused, should be connected to V _{SS} . Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: Transmit Mode Select 2 |
| 49 | I | — | — | TMODE1 | Parallel Port Mode: Unused, should be connected to V _{SS} . Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: Transmit Mode Select 1 |
| 50 | I | THZE | THZE | THZE | Transmit High-Impedance Enable |
| 51 | O | TTIP | TTIP | TTIP | Transmit Analog Tip Output |
| 52 | I | TVSS | TVSS | TVSS | Transmit Analog Signal Ground |
| 53 | I | TVDD | TVDD | TVDD | Transmit Analog Positive Supply |
| 54 | O | TRING | TRING | TRING | Transmit Analog Ring Output |
| 55 | I | BTS | — | HBE | Parallel Port Mode: Bus Type Select (Motorola/Intel) Serial Port Mode: Unused, should be connected to V _{SS} . Hardware Mode: Receive and Transmit DB3/B8ZS Enable |
| 57 | I | BIS0 | BIS0 | BIS0 | Bus Interface Select Mode 0 |
| 59 | I | BIS1 | BIS1 | BIS1 | Bus Interface Select Mode 1 |

| PIN | TYPE | MODE | | | FUNCTION |
|-----|------|----------------------------------|-----------------|----------|---|
| | | PARALLEL PORT | SERIAL PORT | HARDWARE | |
| 60 | I | \overline{CS} | \overline{CS} | RLB | Parallel Port Mode: Active-Low Chip Select Serial Port Mode: Active-Low Chip Select Hardware Mode: Remote Loopback Enable |
| 61 | I | $\overline{RD} (\overline{DS})$ | — | RMODE2 | Parallel Port Mode: Active-Low Read Input (Data Strobe) Serial Port Mode: Unused, should be connected to V_{SS} . Hardware Mode: Receive Mode Select 2 |
| 62 | I | $\overline{WR} (R/\overline{W})$ | — | TMODE3 | Parallel Port Mode: Active-Low Write Input (Read/Write) Serial Port Mode: Unused, should be connected to V_{SS} . Hardware Mode: Transmit Mode Select 3 |
| 63 | I/O | AD0 | MIS0 | TCSS0 | Parallel Port Mode: Address/Data Bus Bit 0 Serial Port Mode: Serial Data Out (Master In-Slave Out) Hardware Mode: Transmit Clock Source Select 0 |
| 64 | I/O | AD1 | MOSI | RMODE3 | Parallel Port Mode: Address/Data Bus Bit 1 Serial Port Mode: Serial Data In (Master Out-Slave In) Hardware Mode: Receive Mode Select 3 |

6. HARDWARE CONTROLLER INTERFACE

In Hardware Controller mode, the parallel and serial port pins are reconfigured to provide direct access to certain functions in the port. Only a subset of the device's functionality is available in hardware mode. Each register description throughout the data sheet indicates the functions that may be controlled in hardware mode and several alarm indicators that are available in both hardware and processor mode. Also indicated are the fixed states of the functions not controllable in hardware mode.

6.1 Transmit Clock Source

Refer to [Figure 3-3](#). In Hardware Controller mode, the input to the TX PLL is always TCLK PIN. TX CLOCK is selected by the TCSS0 and TCSS1 pins, as shown in [Table 6-1](#). The PLL_OUT pin is always the same signal as select for TX CLOCK. If the user wants to slave the transmitter to the recovered clock, then the RCLK pin must be tied to the TCLK pin externally.

Table 6-1. Transmit Clock Source

| TCSS1 PIN 31 | TCSS0 PIN 63 | TRANSMIT CLOCK SOURCE |
|-----------------|-----------------|--|
| 0 | 0 | The TCLK pin is the source of transmit clock. |
| 0 | 1 | The PLL_CLK is the source of transmit clock. |
| 1 | 0 | The scaled signal present at MCLK as the transmit clock. |
| 1 | 1 | The signal present at RCLK is the transmit clock. |

6.2 Internal Termination

In Hardware Controller mode, the internal termination is automatically set according to the receive or transmit mode selected. It can be disabled via the TITD and RITD pins. If internal termination is enabled in E1 mode, the E1TS pin is use to select 75Ω or 120Ω termination. The E1TS pin applies to both transmit and receive.

Table 6-2. Internal Termination

| PIN NAME | FUNCTION |
|-----------------------|---|
| TITD PIN 5 | Transmit Internal Termination Disable. Disables the internal transmit termination. The internal transmit termination value is dependent on the state of the TMODEx pins. |
| RITD PIN 6 | Receive Internal Termination Disable. Disables the internal receive termination. The internal receive termination value is dependent on the state of the RMODEx pins. |
| E1TS PIN 9 | E1 Termination Select. Selects 120Ω or 75Ω internal termination when one of the E1 modes is selected and internal termination is enabled. IF E1 is selected for both transmit and receive, then both terminations will be the same. 0 = 75Ω 1 = 120Ω |

6.3 Line Build-Out

Table 6-3. E1 Line Build-Out

| L2 PIN 13 | L1 PIN 12 | L0 PIN 11 | APPLICATION | N (NOTE 1) | RETURN LOSS | R _t (NOTE 1) |
|--------------|--------------|--------------|-------------------------------------|---------------|----------------|----------------------------|
| 0 | 0 | 0 | 75Ω normal | 1:2 | N.M. | 0 |
| 0 | 0 | 1 | 120Ω normal | 1:2 | N.M. | 0 |
| 1 | 0 | 0 | 75Ω with high return loss (Note 2) | 1:2 | 21dB | 6.2Ω |
| 1 | 0 | 1 | 120Ω with high return loss (Note 2) | 1:2 | 21dB | 11.6Ω |
| 1 | 1 | 0 | Reserved | — | — | — |
| 1 | 1 | 1 | Reserved | — | — | — |

Table 6-4. T1 Line Build-Out

| L2 PIN 13 | L1 PIN 12 | L0 PIN 11 | APPLICATION | N (NOTE 1) | RETURN LOSS | R _t (NOTE 1) |
|--------------|--------------|--------------|-------------------------------|---------------|----------------|----------------------------|
| 0 | 0 | 0 | DSX-1 (0 to 133 feet)/0dB CSU | 1:2 | N.M. | 0 |
| 0 | 0 | 1 | DSX-1 (133 to 266 feet) | 1:2 | N.M. | 0 |
| 0 | 1 | 0 | DSX-1 (266 to 399 feet) | 1:2 | N.M. | 0 |
| 0 | 1 | 1 | DSX-1 (399 to 533 feet) | 1:2 | N.M. | 0 |
| 1 | 0 | 0 | DSX-1 (533 to 655 feet) | 1:2 | N.M. | 0 |
| 1 | 0 | 1 | Reserved | — | — | — |
| 1 | 1 | 0 | Reserved | — | — | — |
| 1 | 1 | 1 | Reserved | — | — | — |

Note 1: Transformer turns ratio.

Note 2: TTD pin must be connected high in this mode.

N.M. = not meaningful

6.4 Receiver Operating Modes

Table 6-5. Receive Path Operating Mode

| RMODE3 PIN 64 | RMODE2 PIN 61 | RMODE1 PIN 4 | RMODE0 PIN 3 | RECEIVE PATH OPERATING MODE |
|------------------|------------------|-----------------|-----------------|--|
| 0 | 0 | 0 | 0 | T1 D4 |
| 0 | 0 | 0 | 1 | T1 ESF |
| 0 | 0 | 1 | 0 | J1 D4 |
| 0 | 0 | 1 | 1 | J1 ESF |
| 0 | 1 | 0 | 0 | E1 FAS |
| 0 | 1 | 0 | 1 | E1 CAS |
| 0 | 1 | 1 | 0 | E1 CRC4 |
| 0 | 1 | 1 | 1 | E1 CAS and CRC4 |
| 1 | 0 | 0 | 0 | E1 G.703 2048kHz Synchronization Interface |
| 1 | 0 | 0 | 1 | Reserved |
| 1 | 0 | 1 | 0 | Reserved |
| 1 | 0 | 1 | 1 | 6312kHz Synchronization Interface |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

6.5 Transmitter Operating Modes

Table 6-6. Transmit Path Operating Mode

| TMODE3 PIN 62 | TMODE2 PIN 48 | TMODE1 PIN 49 | TMODE0 PIN 14 | TRANSMIT PATH OPERATING MODE |
|------------------|------------------|------------------|------------------|---|
| 0 | 0 | 0 | 0 | T1 D4 |
| 0 | 0 | 0 | 1 | T1 ESF |
| 0 | 0 | 1 | 0 | J1 D4 |
| 0 | 0 | 1 | 1 | J1 ESF |
| 0 | 1 | 0 | 0 | E1 FAS |
| 0 | 1 | 0 | 0 | E1 FAS + CAS (Note 1) |
| 0 | 1 | 0 | 1 | Reserved |
| 0 | 1 | 1 | 0 | E1 CRC4 |
| 0 | 1 | 1 | 0 | E1 CRC4 + CAS (Note 1) |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 0 | E1 G.703 2048kHz Synchronization Interface |
| 1 | 0 | 0 | 1 | Reserved |
| 1 | 0 | 1 | 0 | Reserved |
| 1 | 0 | 1 | 1 | 6312kHz Synchronization Interface (Note 2) |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

Note 1: The DS26503 does not have an internal source for CAS signaling and multiframe alignment generation. CAS signaling, and the multiframe alignment word, must be embedded in the transmit data (in the TS16 position) present on the TSER pin and frame aligned to sync signal on the TS pin.

Note 2: In addition to setting the TMODE bits to 6312kHz Synchronization Interface mode, the Transmit PLL must also be configured to transmit a 6312kHz signal through the Transmit PLL Control Register (TPCR.6 and TPCR.7).

6.6 MCLK Pre-Scaler

Table 6-7. MCLK Pre-Scaler for T1 Mode

| MPS1 PIN 16 | MPS0 PIN 15 | JACKS0 PIN 46 | MCLK (MHz) |
|----------------|----------------|------------------|---------------|
| 0 | 0 | 0 | 1.544 |
| 0 | 1 | 0 | 3.088 |
| 1 | 0 | 0 | 6.176 |
| 1 | 1 | 0 | 12.352 |
| 0 | 0 | 1 | 2.048 |
| 0 | 1 | 1 | 4.096 |
| 1 | 0 | 1 | 8.192 |
| 1 | 1 | 1 | 16.384 |

Table 6-8. MCLK Pre-Scaler for E1 Mode

| MPS1 PIN 16 | MPS0 PIN 15 | JACKS0 PIN 46 | MCLK (MHz) |
|------------------------|------------------------|--------------------------|-----------------------|
| 0 | 0 | 0 | 2.048 |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 4.096 |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 8.192 |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | 16.384 |
| 1 | 1 | 1 | Reserved |

6.7 Other Hardware Controller Mode Features

Table 6-9. Other Operational Modes

| PIN NAME | DESCRIPTION |
|---------------------|--|
| RSM PIN 1 | RS Mode Select: Selects frame or multiframe pulse at RS pin. 0 = frame mode 1 = multiframe mode |
| TSM PIN2 | TS Mode Select: In T1 or E1 operation, selects frame or multiframe mode for the TS pin. 0 = frame mode 1 = multiframe mode |
| RLB PIN 60 | Remote Loopback Enable: In this loopback, data input to the framer portion of the DS26503 will be transmitted back to the transmit portion of the LIU. Data will continue to pass through the receive side framer of the DS26503 as it would normally and the data from the transmit side formatter will be ignored. 0 = loopback disabled 1 = loopback enabled |
| TAIS PIN 10 | Transmit AIS 0 = transmit AIS alarm 1 = normal transmission |
| HBE PIN 55 | Receive and Transmit HDB3/B8ZS Enable 0 = HDB3/B8ZS disabled 1 = HDB3/B8ZS enabled |

7. PROCESSOR INTERFACE

The DS26503 is controlled via a nonmultiplexed ($BIS[1:0] = 01$) or a multiplexed ($BIS[1:0] = 00$) parallel bus. There is also a serial bus mode option, as well as a hardware mode of operation. The bus interface type is selected by BIS1 and BIS0 as shown in [Table 7-1](#).

Table 7-1. Port Mode Select

| BIS1 | BIS0 | PORT MODE |
|------|------|-------------------------------------|
| 0 | 0 | Parallel Port Mode (Multiplexed) |
| 0 | 1 | Parallel Port Mode (Nonmultiplexed) |
| 1 | 0 | Serial Port Mode (SPI) |
| 1 | 1 | Hardware Mode |

7.1 Parallel Port Functional Description

In parallel mode, the DS26503 can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parentheses (). See the timing diagrams in the *AC Electrical Characteristics* section for more details.

7.2 SPI Serial Port Interface Functional Description

A serial SPI bus interface is selected when bus select is 10 ($BIS[1:0] = 10$). In this mode, a master/slave relationship is enabled on the serial port with three signal lines (SCK, MOSI, and MISO) and a chip select (\overline{CS}), with the DS26503 acting as the slave. Port read/write timing is not related to the system read/write timing, thus allowing asynchronous, half-duplex operation. See the *AC Electrical Characteristics* section for the AC timing characteristics of the serial port.

7.2.1 Clock Phase and Polarity

Clock Phase and Polarity are selected by the CPHA and CPOL pins. The slave device should always be configured to match the bus master. See the [SPI Serial Port Mode](#) section for detailed functional timing diagrams.

7.2.2 Bit Order

The most significant bit (MSB) of each byte is transmitted first.

7.2.3 Control Byte

The bus master will transmit two control bytes following a chip select to a slave device. The MSB will be a R/\overline{W} bit (1=read, 0=write). The next 6 bits will be padded with 0s. The LSB of the first byte will be A[7]. The second control byte will be the address bits (A[6:0]) of the target register, followed by a Burst bit in the LSB position (1=Burst, 0=Non-burst).

7.2.4 Burst Mode

The last bit of the second control byte (LSB) is the Burst mode bit. When the Burst bit is enabled (set to 1) and a read operation is performed, the register address is automatically incremented after the LSB of the previous byte read to the next register address. Data will be available on the next clock edge following the LSB of the previous byte read. When the Burst bit is enabled (set to 1) and a write operation is performed, the register address will be automatically incremented to the next byte boundary following the LSB of the previous register write, and 8 more data bits will be expected on the serial bus. Burst accesses

are terminated when \overline{CS} is removed. If \overline{CS} is removed before all 8 bits of the data are read, the remaining data will be lost. If \overline{CS} is removed before all 8 bits of data are written to the part, no write access will occur and the target register will not be updated.

Note: During a Burst read access, data must be fetched internally to the part as the LSB of the previous byte is transmitted out. If this pre-fetch read access occurs to a Clear-On-Read register or a FIFO register address, and the Burst access is terminated without reading this byte out of the port, the data will be lost and/or the register cleared. Users should not terminate their Burst Read accesses at the address byte proceeding a Clear-On-Read register or a FIFO register. Data loss could occur due to the internal pre-fetch operation performed by the interface.

7.2.5 Register Writes

The register write sequence is shown in the functional timing diagrams in Section [17](#). After a \overline{CS} , the bus master transmits a write control byte containing the R/\overline{W} bit, the target register address, and the Burst bit. These two control bytes will be followed by the data byte to be written. After the first data byte, if the Burst bit is set, the DS26503 auto-increments its address counter and writes each byte received to the next higher address location. After writing address FFh, the address counter rolls over to 00h and continues to auto-increment.

7.2.6 Register Reads

The register read sequence is shown in Section [17](#). After a \overline{CS} , the bus master transmits a read control byte containing the R/\overline{W} bit, the target register address, and the Burst bit. After these two control bytes, the DS26503 responds with the requested data byte. After the first data byte, if the Burst bit is set, the DS26503 auto-increments its address counter and transmits the byte stored in the next higher address location. Note the warning mentioned above as data loss could potentially occur due to the data pre-fetch that is required to support this mode. After reading address FFh, the address counter rolls over to 00h and continues to auto-increment.

7.3 Register Map

Table 7-2. Register Map Sorted By Address

| ADDRESS | TYPE | REGISTER NAME | REGISTER ABBREVIATION |
|---------|------|-----------------------------------|-------------------------|
| 00 | R/W | Test Reset Register | TSTRREG |
| 01 | R/W | I/O Configuration Register 1 | IOCR1 |
| 02 | R/W | I/O Configuration Register 2 | IOCR2 |
| 03 | R/W | T1 Receive Control Register 1 | T1RCR1 |
| 04 | R/W | T1 Receive Control Register 2 | T1RCR2 |
| 05 | R/W | T1 Transmit Control Register 1 | T1TCR1 |
| 06 | R/W | T1 Transmit Control Register 2 | T1TCR2 |
| 07 | R/W | T1 Common Control Register | T1CCR |
| 08 | R/W | Mode Configuration Register | MCREG |
| 09 | R/W | Transmit PLL Control Register | TPCR |
| 0A | — | Reserved | — |
| 0B | — | Reserved | — |
| 0C | — | Reserved | — |
| 0D | — | Reserved | — |
| 0E | — | Reserved | — |
| 0F | — | Reserved | — |
| 10 | R | Device Identification Register | IDR |
| 11 | R | Information Register 1 | INFO1 |
| 12 | R | Information Register 2 | INFO2 |
| 13 | R | Interrupt Information Register | IIR |
| 14 | R | Status Register 1 | SR1 |
| 15 | R/W | Interrupt Mask Register 1 | IMR1 |
| 16 | R | Status Register 2 | SR2 |
| 17 | R/W | Interrupt Mask Register 2 | IMR2 |
| 18 | R | Status Register 3 | SR3 |
| 19 | R/W | Interrupt Mask Register 3 | IMR3 |
| 1A | R | Status Register 4 | SR4 |
| 1B | R/W | Interrupt Mask Register 4 | IMR4 |
| 1C | R | Information Register 3 | INFO3 |
| 1D | R/W | E1 Receive Control Register | E1RCR |
| 1E | R/W | E1 Transmit Control Register | E1TCR |
| 1F | R/W | BOC Control Register | BOCC |
| 20 | R/W | Loopback Control Register | LBCR |
| 21-2F | — | Reserved | — |
| 30 | R/W | Line Interface Control 1 | LIC1 |
| 31 | R/W | Line Interface Control 2 | LIC2 |
| 32 | R/W | Line Interface Control 3 | LIC3 |
| 33 | R/W | Line Interface Control 4 | LIC4 |
| 34 | R/W | Transmit Line Build-Out Control | TLBC |
| 35-3F | — | Reserved | — |
| 40 | R/W | Transmit Align Frame Register | TAF |
| 41 | R/W | Transmit Non-Align Frame Register | TNAF |
| 42 | R/W | Transmit Si Align Frame | TSiAF |
| 43 | R/W | Transmit Si Non-Align Frame | TSiNAF |

| ADDRESS | TYPE | REGISTER NAME | REGISTER ABBREVIATION |
|---------|------|---|------------------------|
| 44 | R/W | Transmit Remote Alarm Bits | TRA |
| 45 | R/W | Transmit Sa4 Bits | TSa4 |
| 46 | R/W | Transmit Sa5 Bits | TSa5 |
| 47 | R/W | Transmit Sa6 Bits | TSa6 |
| 48 | R/W | Transmit Sa7 Bits | TSa7 |
| 49 | R/W | Transmit Sa8 Bits | TSa8 |
| 4A | R/W | Transmit Sa Bit Control Register | TSACR |
| 4B-4F | — | Reserved | — |
| 50 | R | Receive FDL Register | RFDL |
| 51 | R/W | Transmit FDL Register | TFDL |
| 52 | R/W | Receive Facility Data Link Match Register 1 | RFDLM1 |
| 53 | R/W | Receive Facility Data Link Match Register 2 | RFDLM2 |
| 54-55 | — | Reserved | — |
| 56 | R | Receive Align Frame Register | RAF |
| 57 | R | Receive Non-Align Frame Register | RNAF |
| 58 | R | Receive Si Align Frame | RSiAF |
| 59 | R | Receive Si Non-Align Frame | RSiNAF |
| 5A | R | Receive Remote Alarm Bits | RRA |
| 5B | R | Receive Sa4 Bits | RSa4 |
| 5C | R | Receive Sa5 Bits | RSa5 |
| 5D | R | Receive Sa6 Bits | RSa6 |
| 5E | R | Receive Sa7 Bits | RSa7 |
| 5F | R | Receive Sa8 Bits | RSa8 |
| 60-EF | — | Reserved | — |
| F0 | R/W | Test Register 1 | TEST1* |
| F1 | R/W | Test Register 2 | TEST2* |
| F2 | R/W | Test Register 3 | TEST3* |
| F3 | R/W | Test Register 4 | TEST4* |
| F4 | R/W | Test Register 5 | TEST5* |
| F5 | R/W | Test Register 6 | TEST6* |
| F6 | R/W | Test Register 7 | TEST7* |
| F7 | R/W | Test Register 8 | TEST8* |
| F8 | R/W | Test Register 9 | TEST9* |
| F9 | R/W | Test Register 10 | TEST10* |
| FA | R/W | Test Register 11 | TEST11* |
| FB | R/W | Test Register 12 | TEST12* |
| FC | R/W | Test Register 13 | TEST13* |
| FD | R/W | Test Register 14 | TEST14* |
| FE | R/W | Test Register 15 | TEST15* |
| FF | R/W | Test Register 16 | TEST16* |

*TEST1 to TEST16 registers are used only by the factory.

7.3.1 Power-Up Sequence

The DS26503 contains an on-chip power-up reset function, which automatically clears the writeable register space immediately after power is supplied to the device. The user can issue a chip reset at any time. Issuing a reset will disrupt signals flowing through the DS26503 until the device is reprogrammed. The reset can be issued through hardware using the TSTRST pin or through software using the SFTRST function in the master mode register. The LIRST (LIC2.6) should be toggled from zero to one to reset the line interface circuitry. (It will take the DS26503 about 40ms to recover from the LIRST bit being toggled.)

7.3.2 Test Reset Register

Register Name: **TSTRREG**
 Register Description: **Test Reset Register**
 Register Address: **00h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-------|-------|---|---|---|--------|
| Name | — | — | TEST1 | TEST0 | — | — | — | SFTRST |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Software-Issued Reset (SFTRST). A zero-to-one transition causes the register space in the DS26503 to be cleared. A reset clears all configuration and status registers. The bit automatically clears itself when the reset has completed.

Bits 1, 2, 3, 6, 7: Unused, must be set = 0 for proper operation.

Bits 4 and 5: Test Mode Bits (TEST0, TEST1). Test modes are used to force the output pins of the DS26503 into known states. This can facilitate the checkout of assemblies during the manufacturing process and also be used to isolate devices from shared buses.

| TEST1 | TEST0 | Effect On Output Pins |
|-------|-------|--|
| 0 | 0 | Operate normally |
| 0 | 1 | Force all output pins into three-state (including all I/O pins and parallel port pins) |
| 1 | 0 | Force all output pins low (including all I/O pins except parallel port pins) |
| 1 | 1 | Force all output pins high (including all I/O pins except parallel port pins) |

7.3.3 Mode Configuration Register

Register Name: **MCREG**
 Register Description: **Mode Configuration Register**
 Register Address: **08h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|
| Name | TMODE3 | TMODE2 | TMODE1 | TMODE0 | RMODE3 | RMODE2 | RMODE1 | RMODE0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | TMODE3 PIN 62 | TMODE2 PIN 48 | TMODE1 PIN 49 | TMODE0 PIN 14 | RMODE3 PIN 64 | RMODE2 PIN 61 | RMODE1 PIN 4 | RMODE0 PIN 3 |

Bit 0 to 3: Receive Mode Configuration (RMODE[3:0]). Used to select the operating mode of the receive path for the DS26503.

| RMODE3 | RMODE2 | RMODE1 | RMODE0 | Receive Path Operating Mode |
|--------|--------|--------|--------|--|
| 0 | 0 | 0 | 0 | T1 D4 |
| 0 | 0 | 0 | 1 | T1 ESF |
| 0 | 0 | 1 | 0 | J1 D4 |
| 0 | 0 | 1 | 1 | J1 ESF |
| 0 | 1 | 0 | 0 | E1 FAS |
| 0 | 1 | 0 | 1 | E1 CAS |
| 0 | 1 | 1 | 0 | E1 CRC4 |
| 0 | 1 | 1 | 1 | E1 CAS and CRC4 |
| 1 | 0 | 0 | 0 | E1 G.703 2048kHz Synchronization Interface |
| 1 | 0 | 0 | 1 | Reserved |
| 1 | 0 | 1 | 0 | Reserved |
| 1 | 0 | 1 | 1 | 6312kHz Synchronization Interface |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

Bits 4 to 7: Transmit Mode Configuration (TMODE[3:0]). Used to select the operating mode of the transmit path for the DS26503.

| TMODE3 | TMODE2 | TMODE1 | TMODE0 | Transmit Path Operating Mode |
|--------|--------|--------|--------|---|
| 0 | 0 | 0 | 0 | T1 D4 |
| 0 | 0 | 0 | 1 | T1 ESF (Note: In this mode the TFSE (T1TCR2.6) bit should be set = 0.) |
| 0 | 0 | 1 | 0 | J1 D4 |
| 0 | 0 | 1 | 1 | J1 ESF |
| 0 | 1 | 0 | 0 | E1 FAS |
| 0 | 1 | 0 | 0 | E1 FAS + CAS (Note 1) |
| 0 | 1 | 0 | 1 | Reserved |
| 0 | 1 | 1 | 0 | E1 CRC4 |
| 0 | 1 | 1 | 0 | E1 CRC4 + CAS (Note 1) |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 0 | E1 G.703 2048 kHz Synchronization Interface |
| 1 | 0 | 0 | 1 | Reserved |
| 1 | 0 | 1 | 0 | Reserved |
| 1 | 0 | 1 | 1 | 6312kHz Synchronization Interface (Note 2) |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Reserved |

Note 1: The DS26503 does not have an internal source for CAS signaling and multiframe alignment generation. CAS signaling, and the multiframe alignment word, must be embedded in the transmit data (in the TS16 position) present on the TSER pin and frame aligned to sync signal on the TS pin.

Note 2: In addition to setting the TMODE bits to 6312kHz Synchronization Interface mode, the Transmit PLL must also be configured to transmit a 6312kHz signal through the Transmit PLL Control Register (TPCR.6 and TPCR.7)

Register Name: **TPCR**
 Register Description: **Transmit PLL Control Register**
 Register Address: **09h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|----------|-------|----------|----------|--------|-----------------|-----------------|
| Name | TPLLOFS1 | TPLLOFS0 | PLLOS | TPLLIFS1 | TPLLIFS0 | TPLLSS | TCSS1 | TCSS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | TCSS1 PIN 31 | TCSS0 PIN 63 |

For more information on all the bits in the Transmit PLL control register, refer to [Figure 3-3](#).

Bits 0 and 1: Transmit Clock (TX CLOCK) Source Select (TCSS[1:0]). These bits control the output of the TX PLL Clock Mux function. See [Figure 3-3](#).

| TCSS1 | TCSS0 | Transmit Clock (TX CLOCK) Source (See Figure 3-3) |
|-------|-------|---|
| 0 | 0 | The TCLK pin is the source of transmit clock. |
| 0 | 1 | The PLL_CLK is the source of transmit clock. |
| 1 | 0 | The scaled signal present at MCLK as the transmit clock. |
| 1 | 1 | The signal present at RCLK is the transmit clock. |

Bit 2: Transmit PLL_CLK Source Select (TPLLSS). Selects the reference signal for the TX PLL.
 0 = Use the recovered network clock. This is the same clock available at the RCLK pin (output).
 1 = Use the externally provided clock present at the TCLK pin.

Bit 3 and 4: Transmit PLL Input Frequency Select (TPLLIFS[0:1]). These bits are used to indicate the reference frequency being input to the TX PLL.

| TPLLIFS1 | TPLLIFS0 | Input Frequency |
|----------|----------|-----------------|
| 0 | 0 | 1.544MHz |
| 0 | 1 | 2.048MHz |
| 1 | 0 | — |
| 1 | 1 | 6312kHz |

Bit 5: PLL_OUT Select (PLLOS). This bit selects the source for the PLL_OUT pin. See [Figure 3-3](#).
 0 = PLL_OUT is sourced directly from the TX PLL.
 1 = PLL_OUT is the output of the TX PLL mux.

Bits 6 and 7: Transmit PLL Output Frequency Select (TPLLOFS[0:1]). These bits are used to select the TX PLL output frequency.

| TPLLOFS1 | TPLLOFS0 | Output Frequency |
|----------|----------|------------------|
| 0 | 0 | 1.544MHz |
| 0 | 1 | 2.048MHz |
| 1 | 0 | — |
| 1 | 1 | 6312kHz |

7.4 Interrupt Handling

Various alarms, conditions, and events in the DS26503 can cause interrupts. For simplicity, these are all referred to as events in this explanation. All STATUS registers can be programmed to produce interrupts. Each status register has an associated interrupt mask register. For example, SR1 (Status Register 1) has an interrupt control register called IMR1 (Interrupt Mask Register 1). Status registers are the only sources of interrupts in the DS26503. On power-up, all writeable registers are automatically cleared. Since bits in the IMRx registers have to be set = 1 to allow a particular event to cause an interrupt, no interrupts can occur until the host selects which events are to produce interrupts. Since there are potentially many sources of interrupts on the DS26503, several features are available to help sort out and identify which event is causing an interrupt. When an interrupt occurs, the host should first read the IIR register (interrupt information register) to identify which status register(s) is producing the interrupt. Once that is determined, the individual status register or registers can be examined to determine the exact source.

Once an interrupt has occurred, the interrupt handler routine should clear the IMRx registers to stop further activity on the interrupt pin. After all interrupts have been determined and processed, the interrupt handler routine should restore the state of the IMRx registers.

7.5 Status Registers

When a particular event or condition has occurred (or is still occurring in the case of conditions), the appropriate bit in a status register will be set to a one. All the status registers operate in a latched fashion, which means that if an event or condition occurs a bit is set to a one. It will remain set until the user reads that bit. An event bit will be cleared when it is read and it will not be set again until the event has occurred again. Condition bits such as RLOS, etc., will remain set if the alarm is still present.

The user will always precede a read of any of the status registers with a write. The byte written to the register will inform the DS26503 which bits the user wishes to read and have cleared. The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with the latest information. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status registers will be immediately followed by a read of the same register. This write-read scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS26503 with higher-order languages.

Status register bits are divided into two groups: condition bits and event bits. Condition bits are typically network conditions such as loss of frame, or all-ones detect. Event bits are typically markers such as the one-second timer. Each status register bit is labeled as a condition or event bit. Some of the status registers have bits for both the detection of a condition and the clearance of the condition. For example, SR2 has a bit that is set when the device goes into a loss of frame state (SR2.0, a condition bit) and a bit that is set (SR2.4, an event bit) when the loss of frame condition clears (goes in sync). Some of the status register bits (condition bits) do not have a separate bit for the “condition clear” event but rather the status bit can produce interrupts on both edges, setting, and clearing. These bits are marked as “double interrupt bits.” An interrupt will be produced when the condition occurs and when it clears.

7.6 Information Registers

Information registers operate the same as status registers except they cannot cause interrupts. INFO3 register is a read-only register and it reports the status of the E1 synchronizer in real time. INFO3 information bits are not latched, and it is not necessary to precede a read of these bits with a write.

7.7 Interrupt Information Registers

The Interrupt Information Registers provide an indication of which Status Registers (SR1 through SR4) are generating an interrupt. When an interrupt occurs, the host can read IIR to quickly identify which of the three status registers are causing the interrupt.

Register Name: **IIR**
 Register Description: **Interrupt Information Register**
 Register Address: **13h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|-----|-----|-----|-----|
| Name | — | — | — | — | SR4 | SR3 | SR2 | SR1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Status Register 1 (SR1)

0 = Status Register 1 interrupt not active.
 1 = Status Register 1 interrupt active.

Bit 1: Status Register 2 (SR2)

0 = Status Register 1 interrupt not active.
 1 = Status Register 1 interrupt active.

Bit 2: Status Register 3 (SR3)

0 = Status Register 1 interrupt not active.
 1 = Status Register 1 interrupt active.

Bit 3: Status Register 4 (SR4)

0 = Status Register 1 interrupt not active.
 1 = Status Register 1 interrupt active.

Bits 4 to 7: Unused

8. T1 FRAMER/FORMATTER CONTROL REGISTERS

The T1 framer portion of the DS26503 is configured via a set of five control registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS26503 has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two receive control registers (T1RCR1 and T1RCR2), two transmit control registers (T1TCR1 and T1TCR2), and a common control register (T1CCR). Each of these registers is described in this section.

8.1 T1 Control Registers

Register Name: **T1RCR1**
 Register Description: **T1 Receive Control Register 1**
 Register Address: **03h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-----|------|------|-------|-------|-------|--------|
| Name | — | ARC | OOF1 | OOF2 | SYNCC | SYNCT | SYNCE | RESYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Resynchronize (RESYNC). When toggled from low to high, a resynchronization of the receive side framer is initiated. Must be cleared and set again for a subsequent resync.

Bit 1: Sync Enable (SYNCE)

0 = auto resync enabled
 1 = auto resync disabled

Bit 2: Sync Time (SYNCT)

0 = qualify 10 bits
 1 = qualify 24 bits

Bit 3: Sync Criteria (SYNCC)

In D4 Framing Mode:

0 = search for Ft pattern, then search for Fs pattern
 1 = cross couple Ft and Fs pattern

In ESF Framing Mode:

0 = search for FPS pattern only
 1 = search for FPS and verify with CRC6

Bits 4 and 5: Out Of Frame Select Bits (OOF2, OOF1)

| OOF2 | OOF1 | Out Of Frame Criteria |
|------|------|-------------------------|
| 0 | 0 | 2/4 frame bits in error |
| 0 | 1 | 2/5 frame bits in error |
| 1 | 0 | 2/6 frame bits in error |
| 1 | 1 | 2/6 frame bits in error |

Bit 6: Auto Resync Criteria (ARC)

0 = resync on OOF or RLOS event
 1 = resync on OOF only

Bit 7: Unused, must be set = 0 for proper operation.

Register Name: **T1RCR2**
 Register Description: **T1 Receive Control Register 2**
 Register Address: **04h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|--------------|---|---|---|-----|-------|
| Name | — | — | RB8ZS | — | — | — | RJC | RD4YM |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | HBE PIN55 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Receive Side D4 Yellow Alarm Select (RD4YM)

0 = zeros in bit 2 of all channels

1 = a one in the S-bit position of frame 12 (J1 Yellow Alarm Mode)

Bit 1: Receive Japanese CRC6 Enable (RJC)

0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation)

1 = use Japanese standard JT-G704 CRC6 calculation

Bits 2, 3, 4, 6, 7: Unused, must be set = 0 for proper operation.

Bit 5: Receive B8ZS Enable (RB8ZS)

0 = B8ZS disabled

1 = B8ZS enabled

Register Name: **T1TCR1**
 Register Description: **T1 Transmit Control Register 1**
 Register Address: **05h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------------|------|------|---|---|---|---|------|
| Name | TJC | TFPT | TCPT | — | — | — | — | TYEL |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | RMODEx PINS | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Transmit Yellow Alarm (TYEL)

0 = do not transmit yellow alarm

1 = transmit yellow alarm

Bits 1 to 4: Unused, must be set = 0 for proper operation.

Bit 5: Transmit CRC Pass-Through (TCPT)

0 = source CRC6 bits internally

1 = CRC6 bits sampled at TSER during F-bit time

Bit 6: Transmit F-Bit Pass-Through (TFPT)

0 = F bits sourced internally

1 = F bits sampled at TSER

Bit 7: Transmit Japanese CRC6 Enable (TJC)

0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation)

1 = use Japanese standard JT-G704 CRC6 calculation

Register Name: **T1TCR2**
 Register Description: **T1 Transmit Control Register 2**
 Register Address: **06h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|------|---|-------|-------|-------|---|-------|
| Name | TB8ZS | TFSE | — | FBCT2 | FBCT1 | TD4YM | — | TB7ZS |
| Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | HBE PIN 55 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Transmit-Side Bit 7 Zero-Suppression Enable (TB7ZS)

0 = no stuffing occurs

1 = bit 7 forced to a 1 in channels with all 0s

Bits 1 and 5: Unused, must be set = 0 for proper operation.

Bit 2: Transmit-Side D4 Yellow Alarm Select (TD4YM)

0 = 0s in bit 2 of all channels

1 = a 1 in the S-bit position of frame 12

Bit 3: F-Bit Corruption Type 1 (FBCT1). A low-to-high transition of this bit causes the next three consecutive Ft (D4 framing mode) or FPS (ESF framing mode) bits to be corrupted causing the remote end to experience a loss of frame (loss of synchronization).

Bit 4: F-Bit Corruption Type 2 (FBCT2). Setting this bit high enables the corruption of one Ft (D4 framing mode) or FPS (ESF framing mode) bit in every 128 Ft or FPS bits as long as the bit remains set.

Bit 6: Transmit Fs-Bit Insertion Enable (TFSE). Only set this bit to a 1 in D4 framing applications. Must be set to 1 to source the Fs pattern from the TFDL register. In all other modes this bit must be set = 0.

0 = Fs-bit insertion disabled

1 = Fs-bit insertion enabled

Bit 7: Transmit B8ZS Enable (TB8ZS)

0 = B8ZS disabled

1 = B8ZS enabled

Register Name: **T1CCR**
 Register Description: **T1 Common Control Register**
 Register Address: **07h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---------|---------|---|-----|---|
| Name | — | — | — | TRAI-CI | TAIS-CI | — | PDE | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 0, 2, 5, 6, 7: Unused, must be set = 0 for proper operation.

Bit 1: Pulse-Density Enforcer Enable (PDE). The framer always examines the transmit and receive data streams for violations of these, which are required by ANSI T1.403: No more than 15 consecutive zeros and at least N ones in each and every time window of $8 \times (N + 1)$ bits, where N = 1 through 23. When this bit is set to one, the DS26503 forces the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, this bit should be set to zero, as B8ZS encoded data streams cannot violate the pulse-density requirements.

0 = disable transmit pulse-density enforcer

1 = enable transmit pulse-density enforcer

Bit 3: Transmit AIS-CI Enable (TAIS-CI). Setting this bit causes the AIS-CI code to be transmitted from the framer to the LIU, as defined in ANSI T1.403.

0 = do not transmit the AIS-CI code

1 = transmit the AIS-CI code

Bit 4: Transmit RAI-CI Enable (TRAI-CI). Setting this bit causes the ESF RAI-CI code to be transmitted in the FDL bit position.

0 = do not transmit the ESF RAI-CI code

1 = transmit the ESF RAI-CI code

Table 8-1. T1 Alarm Criteria

| ALARM | SET CRITERIA | CLEAR CRITERIA |
|--|--|--|
| Blue Alarm (AIS) (Note 1) | Over a 3ms window, five or fewer zeros are received | Over a 3ms window, six or more zeros are received |
| Yellow Alarm (RAI) D4 Bit-2 Mode (T1RCR2.0 = 0) D4 12th F-bit Mode (T1RCR2.0 = 1; this mode is also referred to as the “Japanese Yellow Alarm”) ESF Mode | Bit 2 of 256 consecutive channels is set to zero for at least 254 occurrences 12th framing bit is set to one for two consecutive occurrences 16 consecutive patterns of 00FF appear in the FDL | Bit 2 of 256 consecutive channels is set to zero for less than 254 occurrences 12th framing bit is set to zero for two consecutive occurrences 14 or fewer patterns of 00FF hex out of 16 possible appear in the FDL |
| Red Alarm (RLOS) (Also referred to as Loss Of Signal) | 192 consecutive zeros are received | 14 or more ones out of 112 possible bit positions are received, starting with the first one received |

Note: The definition of Blue Alarm (or Alarm Indication Signal) is an unframed, all-ones signal. Blue Alarm detectors should be able to operate properly in the presence of a $10E-3$ error rate, and they should not falsely trigger on a framed, all-ones signal. The Blue Alarm criteria in the DS26503 has been set to achieve this performance.

9. E1 FRAMER/FORMATTER CONTROL REGISTERS

The E1 framer portion of the DS26503 is configured via a set of two control registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS26503 has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There is one receive control register (E1RCR) and one transmit control register (E1TCR). There are also two information registers and a status register, as well as an interrupt mask register. Each of these registers is described in this section.

9.1 E1 Control Registers

Register Name: **E1RCR**
 Register Description: **E1 Receive Control Register**
 Register Address: **1Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-------|---------------|---|---|-----|-------|--------|
| Name | — | RLOSA | RHDB3 | — | — | FRC | SYNCE | RESYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | HBE PIN 55 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Resync (RESYNC). When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.

Bit 1: Sync Enable (SYNCE)

0 = auto resync enabled

1 = auto resync disabled

Bit 2: Frame Resync Criteria (FRC)

0 = resync if FAS received in error three consecutive times

1 = resync if FAS or bit 2 of non-FAS is received in error three consecutive times

Bits 3, 4, 7: Unused, must be set = 0 for proper operation.

Bit 5: Receive HDB3 Enable (RHDB3)

0 = HDB3 disabled

1 = HDB3 enabled

Bit 6: Receive Loss Of Signal (RLOS) Alternate Criteria (RLOSA). Defines the criteria for a Receive Loss Of Signal condition.

0 = RLOS declared upon 255 consecutive zeros (125μs)

1 = RLOS declared upon 2048 consecutive zeros (1ms)

Table 9-1. E1 Sync/Resync Criteria

| FRAME OR MULTIFRAME LEVEL | SYNC CRITERIA | RESYNC CRITERIA | ITU SPEC. |
|---------------------------|--|---|-------------------------|
| FAS | FAS present in frame N and N + 2, and FAS not present in frame N + 1 | Three consecutive incorrect FAS received Alternate: (E1RCR.2 = 1) The above criteria is met or three consecutive incorrect bit 2 of non-FAS received | G.706 4.1.1 4.1.2 |
| CRC4 | Two valid MF alignment words found within 8ms | 915 or more CRC4 code words out of 1000 received in error | G.706 4.2 and 4.3.2 |
| CAS | Valid MF alignment word found and previous time slot 16 contains code other than all zeros | Two consecutive MF alignment words received in error | G.732 5.2 |

Register Name: **E1TCR**
Register Description: **E1 Transmit Control Register**
Register Address: **1Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|---|---|------|---|---|---------------|---|
| Name | TFPT | — | — | TSiS | — | — | THDB3 | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | HBE PIN 55 | 0 |

Bits 0, 2, 3, 5, 6: Unused, must be set = 0 for proper operation.

Bit 1: Transmit HDB3 Enable (THDB3)

0 = HDB3 disabled

1 = HDB3 enabled

Bit 4: Transmit International Bit Select (TSiS)

0 = sample Si bits at TSER pin

1 = source Si bits from TAF and TNAF registers (in this mode, E1TCR1.7 must be set to 0)

Bit 7: Transmit Time Slot 0 Pass-Through (TFPT)

0 = FAS bits/Sa bits/remote alarm sourced internally from the TAF and TNAF registers

1 = FAS bits/Sa bits/remote alarm sourced from TSER

9.2 E1 Information Registers

Register Name: **INFO2**
 Register Description: **Information Register 2**
 Register Address: **12h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|-------|-------|-------|
| Name | — | — | — | — | — | CRCRC | FASRC | CASRC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: CAS Resync Criteria Met Event (CASRC). Set when two consecutive CAS MF alignment words are received in error.

Bit 1: FAS Resync Criteria Met Event (FASRC). Set when three consecutive FAS words are received in error.

Bit 2: CRC Resync Criteria Met Event (CRCRC). Set when 915/1000 codewords are received in error.

Bits 3 to 7: Unused

Register Name: **INFO3**
 Register Description: **Information Register 3 (Real Time)**
 Register Address: **1Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|-------|-------|--------|
| Name | CSC5 | CSC4 | CSC3 | CSC2 | CSC0 | FASSA | CASSA | CRC4SA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: CRC4 MF Sync Active (CRC4SA). Set while the synchronizer is searching for the CRC4 MF alignment word.

Bit 1: CAS MF Sync Active (CASSA). Set while the synchronizer is searching for the CAS MF alignment word.

Bit 2: FAS Sync Active (FASSA). Set while the synchronizer is searching for alignment at the FAS level.

Bits 3 to 7: CRC4 Sync Counter Bits (CSC0 and CSC2 to CSC5). The CRC4 sync counter increments each time the 8ms-CRC4 multiframe search times out. The counter is cleared when the framer has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling CRC4 mode. This counter is useful for determining the amount of time the framer has been searching for synchronization at the CRC4 level. ITU G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400ms, then the search should be abandoned and proper action taken. The CRC4 sync counter will rollover. CSC0 is the LSB of the 6-bit counter. (**Note:** The second LSB, CSC1, is not accessible. CSC1 is omitted to allow resolution to >400ms using 5 bits.)

Table 9-2. E1 Alarm Criteria

| ALARM | SET CRITERIA | CLEAR CRITERIA | ITU SPEC. |
|---------------|---|--|------------------|
| RLOF | An RLOF condition exists on power-up prior to initial synchronization, when a resync criteria has been met, or when a manual resync has been initiated via E1RCR.0 | | |
| RLOS | 255 or 2048 consecutive zeros received as determined by E1RCR.0 | In 255-bit times, at least 32 ones are received | G.775/G.962 |
| RRA | Bit 3 of non-align frame set to one for three consecutive occasions | Bit 3 of non-align frame set to zero for three consecutive occasions | O.162 2.1.4 |
| RUA1 | Fewer than three zeros in two frames (512 bits) | More than two zeros in two frames (512 bits) | O.162 1.6.1.2 |
| RDMA | Bit 6 of time slot 16 in frame 0 has been set for two consecutive multiframes | | |
| V52LNK | Two out of three Sa7 bits are zero | | G.965 |

Register Name: **IDR**
Register Description: **Device Identification Register**
Register Address: **10h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| Default | 0 | 0 | 0 | 1 | N | N | N | N |
| HW Mode | X | X | X | X | X | X | X | X |

Bits 0 to 3: Chip Revision Bits (ID0 to ID3). The lower four bits of the IDR are used to display the die revision of the chip. ID0 is the LSB of a decimal code that represents the chip revision.

Bits 4 to 7: Device ID (ID4 to ID7). The upper four bits of the IDR are used to display the DS26503 ID. The DS26503 ID is 0001.

Register Name: **SR2**
 Register Description: **Status Register 2**
 Register Address: **16h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|------|----------------|----------------|---------------|
| Name | RYELC | RAISC | RLOSC | RLOFC | RYEL | RAIS | RLOS | RLOF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | RAIS PIN 29 | RLOS PIN 32 | LOF PIN 30 |

Bit 0: Receive Loss of Frame Condition (RLOF). Set when the DS26503 is not synchronized to the received data stream.

Bit 1: Receive Loss Of Signal Condition (RLOS). Set when 255 (or 2048 if E1RCR.6 = 1) E1 mode or 192 T1 mode consecutive zeros have been detected. In 6312kHz Synchronization Interface Mode, this bit will be set when the signal received is out of range as defined by the G.703 Appendix II specification.

Bit 2: Receive Alarm Indication Signal (T1= Blue Alarm, E1= AIS) Condition (RAIS). Set when an unframed all-ones code is received.

Bit 3: Receive Yellow Alarm Condition (RYEL). (T1 only) Set when a yellow alarm is received.

Bit 4: Receive Loss of Frame Clear Event (RLOFC). Set when the framer achieves synchronization; will remain set until read.

Bit 5: Receive Loss Of Signal Clear Event (RLOSC). Set when loss of signal condition is no longer detected.

Bit 6: Receive Alarm Indication Signal Clear Event (RAISC). Set when the unframed all-ones condition is no longer detected.

Bit 7: Receive Yellow Alarm Clear Event (RYELC). (T1 only) Set when the yellow alarm condition is no longer detected.

Register Name: **IMR2**
 Register Description: **Interrupt Mask Register 2**
 Register Address: **17h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|------|------|------|------|
| Name | RYELC | RAISC | RLOSC | RLOFC | RYEL | RAIS | RLOS | RLOF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Receive Loss of Frame Condition (RLOF)

0 = interrupt masked

1 = interrupt enabled—interrupts on rising edge only

Bit 1: Receive Loss Of Signal Condition (RLOS)

0 = interrupt masked

1 = interrupt enabled—interrupts on rising edge only

Bit 2: Receive Alarm Indication Signal Condition (RAIS)

0 = interrupt masked

1 = interrupt enabled—interrupts on rising edge only

Bit 3: Receive Yellow Alarm Condition (RYEL)

0 = interrupt masked

1 = interrupt enabled—interrupts on rising edge only

Bit 4: Receive Loss of Frame Clear Event (RLOFC)

0 = interrupt masked

1 = interrupt enabled

Bit 5: Receive Loss Of Signal Condition Clear (RLOSC)

0 = interrupt masked

1 = interrupt enabled

Bit 6: Receive Alarm Indication Signal Clear Event (RAISC)

0 = interrupt masked

1 = interrupt enabled

Bit 7: Receive Yellow Alarm Clear Event (RYELC)

0 = interrupt masked

1 = interrupt enabled

10. I/O PIN CONFIGURATION OPTIONS

Register Name: **IOCR1**
 Register Description: **I/O Configuration Register 1**
 Register Address: **01h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-------|-----------|-------|------|-----------|------|-----|
| Name | — | RSMS2 | RSMS1 | RLOFF | TSDW | TSM | TSIO | ODF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | RSM PIN 1 | 0 | 0 | TSM PIN 2 | 0 | 0 |

Bit 0: Output Data Format (ODF)

0 = bipolar data at TPOS and TNEG
 1 = NRZ data at TPOS; TNEG = 0

Bit 1: TS I/O Select (TSIO). This bit determines whether the TS pin is an input or and output. See [Table 10-1](#).

0 = TS is an input
 1 = TS is an output

Bit 2: TS Mode Select (TSM). In T1 or E1 operation, selects frame or multiframe mode for the TS pin. In 6312kHz mode, this bit should be set = 0. See [Table 10-1](#).

0 = frame mode
 1 = multiframe mode

Bit 3: Transmit Signaling Double-Wide Sync (TSDW). In T1 mode, setting this bit = 1 and setting TSIO = 1 will cause the sync-pulse output on TS to be two clocks wide during signaling frames. In E1 or 6312kHz mode, this bit should be set = 0. See [Table 10-1](#).

0 = (T1) normal sync pulses
 1 = (T1) double-wide sync pulses during signaling frames

Bit 4: RLOF Output Function (RLOFF). In T1 or E1 receive mode this bit determines the function of the RLOF pin. In 6312kHz receive mode, this bit should be set = 0.

0 = receive loss of frame (RLOF)
 1 = loss-of-transmit clock (LOTC)

Bit 5: RS Mode Select 1(RSMS1). In T1 or E1 receive mode, this bit selects a frame or multiframe output pulse at RS pin. IOCR.6 may be used to select other function for the RS pin.

0 = frame mode
 1 = multiframe mode

Bit 6: RS Mode Select 2 (RSMS2). In T1 and E1 receive mode, this bit along with IOCR.5 selects the function of the RS pin.

T1 Mode: (when IOCR.5 set = 0)
 0 = do not pulse double-wide in signaling frames
 1 = do pulse double-wide in signaling frames
 E1 Mode: (when IOCR.5 set = 1)
 0 = RS outputs CAS multiframe boundaries
 1 = RS outputs CRC4 multiframe boundaries

Bit 7: Unused, must be set = 0 for proper operation.

Table 10-1. TS Pin Functions

| TRANSMIT MODE | IOCR.3 | IOCR.2 | IOCR.1 | TS FUNCTION |
|--------------------------|---------------|---------------|---------------|------------------------|
| T1/E1 | 0 | 0 | 0 | Frame sync input |
| T1/E1 | 0 | 0 | 1 | Frame sync output |
| T1/E1 | 0 | 1 | 0 | Multiframe sync input |
| T1/E1 | 0 | 1 | 1 | Multiframe sync output |

Table 10-2. RLOF Pin Functions

| RECEIVE MODE | IOCR.4 | RLOF PIN FUNCTION |
|-------------------------|---------------|----------------------------------|
| T1/E1 | 0 | Indicate loss of frame |
| T1/E1 | 1 | Indicates loss of transmit clock |

Register Name: **IOCR2**
 Register Description: **I/O Configuration Register 2**
 Register Address: **02h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|-------|-------|---|---|---|---|
| Name | RCLKINV | TCLKINV | RSINV | TSINV | — | — | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 0 to 3: Unused, must be set = 0 for proper operation.

Bit 4: TS Invert (TSINV)

0 = no inversion

1 = invert

Bit 5: RS Invert (RSINV)

0 = no inversion

1 = invert

Bit 6: TCLK Invert (TCLKINV)

0 = no inversion

1 = invert

Bit 7: RCLK Invert (RCLKINV)

0 = no inversion

1 = invert

11. T1 SYNCHRONIZATION STATUS MESSAGE

The DS26503 has a BOC controller to handle SSM services in T1 mode.

Table 11-1. T1 SSM Messages

| QUALITY LEVEL | DESCRIPTION | BOC CODE |
|-----------------|--|------------------|
| 1 | Stratum 1 Traceable | 0000010011111111 |
| 2 | Synchronized Traceability Unknown | 0000100011111111 |
| 3 | Stratum 2 Traceable | 0000110011111111 |
| 4 | Stratum 3 Traceable | 0001000011111111 |
| 5 | SONET Minimum Clock Traceable | 0010001011111111 |
| 6 | Stratum 4 Traceable | 0010100011111111 |
| 7 | Do Not Use For Synchronization | 0011000011111111 |
| User Assignable | Reserved For Network Synchronization Use | 0100000011111111 |

11.1 T1 Bit-Oriented Code (BOC) Controller

The DS26503 contains a BOC generator on the transmit side and a BOC detector on the receive side. The BOC function is available only in T1 mode. In typical BITS applications, the BOC controller would be used to transmit and receive Synchronization Status Messages in T1 mode over the data link.

11.2 Transmit BOC

Bits 0 through 5 in the TFDL register contain the BOC or synchronization status message to be transmitted. Setting BOCC.0 = 1 causes the transmit BOC controller to immediately begin inserting the BOC sequence into the FDL bit position. The transmit BOC controller automatically provides the abort sequence. BOC messages will be transmitted as long as BOCC.0 is set. TFSE (T1TCR2.6) must be set = 0 when using the transmit BOC function.

To transmit a BOC, use the following:

- 1) Write 6-bit code into the TFDL register.
- 2) Set SBOC bit in BOCC register = 1.

11.3 Receive BOC

The receive BOC function is enabled by setting $\text{BOCC.4} = 1$. The RFDL register will now operate as the receive BOC message and information register. The lower six bits of the RFDL register (BOC message bits) are preset to all ones. When the BOC bits change state, the BOC change of state indicator, SR3.0 will alert the host. The host will then read the RFDL register to get the BOC message. A change of state will occur when either a new BOC code has been present for time determined by the receive BOC filter bits, RBF0 and RBF1 , in the BOCC register.

To receive a BOC, use the following:

- 1) Set integration time via BOCC.1 and BOCC.2 .
- 2) Enable the receive BOC function ($\text{BOCC.4} = 1$).
- 3) Enable interrupt ($\text{IMR3.0} = 1$).
- 4) Wait for interrupt to occur.
- 5) Read the RFDL register.
- 6) The lower six bits of the RFDL register is the message.

Register Name: **BOCC**
 Register Description: **BOC Control Register**
 Register Address: **1Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-------|-----|------|------|------|
| Name | — | — | — | RBOCE | RBR | RBF1 | RBF0 | SBOC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Send BOC (SBOC). Set = 1 to transmit the BOC code placed in bits 0 to 5 of the TFDL register.

Bits 1 and 2: Receive BOC Filter Bits (RBF0, RBF1). The BOC filter sets the number of consecutive patterns that must be received without error prior to an indication of a valid message.

| RBF1 | RBF0 | CONSECUTIVE BOC CODES FOR VALID SEQUENCE IDENTIFICATION |
|------|------|---|
| 0 | 0 | None |
| 0 | 1 | 3 |
| 1 | 0 | 5 |
| 1 | 1 | 7 |

Bit 3: Receive BOC Reset (RBR). A 0-to-1 transition will reset the BOC circuitry. Must be cleared and set again for a subsequent reset.

Bit 4: Receive BOC Enable (RBOCE). Enables the receive BOC function. The RFDL register will report the received BOC code.

0 = receive BOC function disabled

1 = receive BOC function enabled. The RFDL register will report BOC messages

Bits 5, 6, 7: Unused, must be set = 0 for proper operation.

Register Name: **RFDL** (RFDL register bit usage when BOCC.4 = 1)
 Register Description: **Receive FDL Register**
 Register Address: **50h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-------|-------|-------|-------|-------|-------|
| Name | — | — | RBOC5 | RBOC4 | RBOC3 | RBOC2 | RBOC1 | RBOC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: BOC Bit 0 (RBOC0)

Bit 1: BOC Bit 1 (RBOC1)

Bit 2: BOC Bit 2 (RBOC2)

Bit 3: BOC Bit 3 (RBOC3)

Bit 4: BOC Bit 4 (RBOC4)

Bit 5: BOC Bit 5 (RBOC5)

Bits 6 and 7: This bit position is unused when BOCC.4 = 1.

Register Name: **RFDLM1, RFDLM2**
 Register Description: **Receive FDL Match Register 1**
Receive FDL Match Register 2
 Register Address: **52h, 53h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | RFDLM7 | RFDLM6 | RFDLM5 | RFDLM4 | RFDLM3 | RFDLM2 | RFDLM1 | RFDLM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Receive FDL Match Bit 0 (RFDLM0). LSB of the FDL Match Code.

Bit 1: Receive FDL Match Bit 1 (RFDLM1)

Bit 2: Receive FDL Match Bit 2 (RFDLM2)

Bit 3: Receive FDL Match Bit 3 (RFDLM3)

Bit 4: Receive FDL Match Bit 4 (RFDLM4)

Bit 5: Receive FDL Match Bit 5 (RFDLM5)

Bit 6: Receive FDL Match Bit 6 (RFDLM6)

Bit 7: Receive FDL Match Bit 7 (RFDLM7). MSB of the FDL Match Code.

Register Name: **SR3**
 Register Description: **Status Register 3**
 Register Address: **18h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|------|------|--------|-------|-------|-------|------|
| Name | RAIS-CI | LOTC | BOCC | RFDLAD | RFDLF | TFDLE | RMTCH | RBOC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Receive BOC Detector Change-of-State Event (RBOC). Set whenever the BOC detector sees a change of state to a valid BOC. The setting of this bit prompts the user to read the RFDL register.

Bit 1: Receive FDL Match Event (RMTCH). Set whenever the contents of the RFDL register matches RFDLM1 or RFDLM2.

Bit 2: TFDL Register Empty Event (TFDLE). Set when the transmit FDL buffer (TFDL) empties.

Bit 3: RFDL Register Full Event (RFDLF). Set when the receive FDL buffer (RFDL) fills to capacity.

Bit 4: RFDL Abort Detect Event (RFDLAD). Set when eight consecutive ones are received on the FDL.

Bit 5: BOC Clear Event (BOCC). Set when 30 FDL bits occur without an abort sequence.

Bit 6: Loss Of Transmit Clock Event (LOTC). Set when the signal at the TCLK pin has not transitioned for approximately 15 periods of the scaled MCLK.

Bit 7: Receive AIS-CI Event (RAIS-CI) (T1 Only). Set when the receiver detects the AIS-CI pattern as defined in ANSI T1.403.

Register Name: **IMR3**
 Register Description: **Interrupt Mask Register 3**
 Register Address: **19h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|------|------|--------|-------|-------|-------|------|
| Name | RAIS-CI | LOTC | BOCC | RFDLAD | RFDLF | TFDLE | RMTCH | RBOC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Receive BOC Detector Change-of-State Event (RBOC)

0 = interrupt masked

1 = interrupt enabled

Bit 1: Receive FDL Match Event (RMTCH)

0 = interrupt masked

1 = interrupt enabled

Bit 2: TFDL Register Empty Event (TFDLE)

0 = interrupt masked

1 = interrupt enabled

Bit 3: RFDL Register Full Event (RFDLF)

0 = interrupt masked

1 = interrupt enabled

Bit 4: RFDL Abort Detect Event (RFDLAD)

0 = interrupt masked

1 = interrupt enabled

Bit 5: BOC Clear Event (BOCC)

0 = interrupt masked

1 = interrupt enabled

Bit 6: Loss Of Transmit Clock Event (LOTC)

0 = interrupt masked

1 = interrupt enabled

Bit 7: Receive AIS-CI Event (RAIS-CI)

0 = interrupt masked

1 = interrupt enabled

Register Name: **SR4**
 Register Description: **Status Register 4**
 Register Address: **1Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|------|-----|-----|-----|------|-----|
| Name | — | RSA1 | RSA0 | TMF | TAF | RMF | RCMF | RAF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Receive Align Frame Event (RAF). (E1 only) Set every 250µs at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.

Bit 1: Receive CRC4 Multiframe Event (RCMF). (E1 only) Set on CRC4 multiframe boundaries; will continue to be set every 2ms on an arbitrary boundary if CRC4 is disabled.

Bit 2: Receive Multiframe Event (RMF)

E1 Mode: Set every 2ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.

T1 Mode: Set every 1.5ms on D4 MF boundaries or every 3ms on ESF MF boundaries.

Bit 3: Transmit Align Frame Event (TAF). (E1 only) Set every 250µs at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.

Bit 4: Transmit Multiframe Event (TMF)

E1 Mode: Set every 2ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.

T1 Mode: Set every 1.5ms on D4 MF boundaries or every 3ms on ESF MF boundaries.

Bit 5: Receive Signaling All Zeros Event (RSA0). (E1 only) Set when over a full MF, time slot 16 contains all zeros.

Bit 6: Receive Signaling All Ones Event (RSA1). (E1 only) Set when the contents of time slot 16 contains fewer than three zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.

Bit 7: Unused

Register Name: **IMR4**
 Register Description: **Interrupt Mask Register 4**
 Register Address: **1Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|------|-----|-----|-----|------|-----|
| Name | — | RSA1 | RSA0 | TMF | TAF | RMF | RCMF | RAF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Receive Align Frame Event (RAF)

0 = interrupt masked

1 = interrupt enabled

Bit 1: Receive CRC4 Multiframe Event (RCMF)

0 = interrupt masked

1 = interrupt enabled

Bit 2: Receive Multiframe Event (RMF)

0 = interrupt masked

1 = interrupt enabled

Bit 3: Transmit Align Frame Event (TAF)

0 = interrupt masked

1 = interrupt enabled

Bit 4: Transmit Multiframe Event (TMF)

0 = interrupt masked

1 = interrupt enabled

Bit 5: Receive Signaling All Zeros Event (RSA0)

0 = interrupt masked

1 = interrupt enabled

Bit 6: Receive Signaling All Ones Event (RSA1)

0 = interrupt masked

1 = interrupt enabled

Bit 7: Unused, must be set = 0 for proper operation.

Register Name: **TFDL**
 Register Description: **Transmit FDL Register**
 Register Address: **51h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TFDL7 | TFDL6 | TFDL5 | TFDL4 | TFDL3 | TFDL2 | TFDL1 | TFDL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

Note: Also used to insert *Fs* framing pattern in *D4* framing mode.

The transmit FDL register (TFDL) contains the FDL information that is to be inserted on a byte-basis into the outgoing T1 data stream. The LSB is transmitted first.

Bit 0: Transmit FDL Bit 0 (TFDL0). LSB of the transmit FDL code.

Bit 1: Transmit FDL Bit 1 (TFDL1)

Bit 2: Transmit FDL Bit 2 (TFDL2)

Bit 3: Transmit FDL Bit 3 (TFDL3)

Bit 4: Transmit FDL Bit 4 (TFDL4)

Bit 5: Transmit FDL Bit 5 (TFDL5)

Bit 6: Transmit FDL Bit 6 (TFDL6)

Bit 7: Transmit FDL Bit 7 (TFDL7). MSB of the transmit FDL code.

12. E1 SYNCHRONIZATION STATUS MESSAGE

The DS26503 provides access to both the transmit and receive Sa/Si bits. In E1, the Sa bits are used to transmit and receive the SSM. The primary method to access the Sa (and Si) bits is based on CRC4 multiframe access. An alternate method is based on double-frame access.

Table 12-1. E1 SSM Messages

| QUALITY LEVEL | DESCRIPTION | Sa BIT MESSAGE |
|---------------|--|----------------|
| 0 | Quality unknown (existing sync network) | 0000 |
| 1 | Reserved | 0001 |
| 2 | Rec. G.811 (Traceable to PRS) | 0010 |
| 3 | Reserved | 0011 |
| 4 | SSU-A (Traceable to SSU type A, see G.812) | 0100 |
| 5 | Reserved | 0101 |
| 6 | Reserved | 0110 |
| 7 | Reserved | 0111 |
| 8 | SSU-B (Traceable to SSU type B, see G.812) | 1000 |
| 9 | Reserved | 1001 |
| 10 | Reserved | 1010 |
| 11 | Synchronous Equipment Timing Source | 1011 |
| 12 | Reserved | 1100 |
| 13 | Reserved | 1101 |
| 14 | Reserved | 1110 |
| 15 | Do not use for synchronization | 01111 |

In E1 operation, SSMs are transmitted using one of the Sa bits—Sa4, Sa5, Sa6, Sa7, or Sa8. The SSM is transmitted MSB first in the first frame of the multiframe. Each multiframe will contain two SSMs, one in each sub-multiframe. An SSM is declared valid when the message in three sub-multiframes are alike.

12.1 Sa/Si Bit Access Based on CRC4 Multiframe

On the receive side, there is a set of eight registers (RSiAF, RSiNAF, RRA, RSa4 to RSa8) that report the Si and Sa bits as they are received. These registers are updated on CRC4 multiframes. A bit in status register 4 (SR4.1) indicates the multiframe boundary. The host can use the SR4.1 bit to know when to read these registers. The user has 2ms to retrieve the data before it is lost. The MSB of each register is the first received. See the following register descriptions for more details.

On the transmit side, there is also a set of eight registers (TSiAF, TSiNAF, TRA, TSa4 to TSa8) that, via the transmit Sa bit control register (TSaCR), can be programmed to insert both Si and Sa data. Data is sampled from these registers with the setting of the transmit multiframe bit in status register 2 (SR4.4). The host can use the SR4.4 bit to know when to update these registers. It has 2ms to update the data or else the old data will be retransmitted. The MSB of each register is the first bit transmitted. See the following register descriptions for details.

Register Name: **RSiAF**
 Register Description: **Receive Si Bits of the Align Frame**
 Register Address: **58h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|-------|-------|-------|
| Name | SiF0 | SiF2 | SiF4 | SiF6 | SiF8 | SiF10 | SiF12 | SiF14 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Si Bit of Frame 14(SiF14)

Bit 1: Si Bit of Frame 12(SiF12)

Bit 2: Si Bit of Frame 10(SiF10)

Bit 3: Si Bit of Frame 8(SiF8)

Bit 4: Si Bit of Frame 6(SiF6)

Bit 5: Si Bit of Frame 4(SiF4)

Bit 6: Si Bit of Frame 2(SiF2)

Bit 7: Si Bit of Frame 0(SiF0)

Register Name: **RSiNAF**
 Register Description: **Receive Si Bits of the Non-Align Frame**
 Register Address: **59h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|-------|-------|-------|
| Name | SiF1 | SiF3 | SiF5 | SiF7 | SiF9 | SiF11 | SiF13 | SiF15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Si Bit of Frame 15(SiF15)

Bit 1: Si Bit of Frame 13(SiF13)

Bit 2: Si Bit of Frame 11(SiF11)

Bit 3: Si Bit of Frame 9(SiF9)

Bit 4: Si Bit of Frame 7(SiF7)

Bit 5: Si Bit of Frame 5(SiF5)

Bit 6: Si Bit of Frame 3(SiF3)

Bit 7: Si Bit of Frame 1(SiF1)

Register Name: **RRA**
 Register Description: **Receive Remote Alarm**
 Register Address: **5Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|--------|--------|--------|
| Name | RRAF1 | RRAF3 | RRAF5 | RRAF7 | RRAF9 | RRAF11 | RRAF13 | RRAF15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Remote Alarm Bit of Frame 15(RRAF15)

Bit 1: Remote Alarm Bit of Frame 13(RRAF13)

Bit 2: Remote Alarm Bit of Frame 11(RRAF11)

Bit 3: Remote Alarm Bit of Frame 9(RRAF9)

Bit 4: Remote Alarm Bit of Frame 7(RRAF7)

Bit 5: Remote Alarm Bit of Frame 5(RRAF5)

Bit 6: Remote Alarm Bit of Frame 3(RRAF3)

Bit 7: Remote Alarm Bit of Frame 1(RRAF1)

Register Name: **RSa4**
 Register Description: **Receive Sa4 Bits**
 Register Address: **5Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | RSa4F1 | RSa4F3 | RSa4F5 | RSa4F7 | RSa4F9 | RSa4F11 | RSa4F13 | RSa4F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Sa4 Bit of Frame 15(RSa4F15)

Bit 1: Sa4 Bit of Frame 13(RSa4F13)

Bit 2: Sa4 Bit of Frame 11(RSa4F11)

Bit 3: Sa4 Bit of Frame 9(RSa4F9)

Bit 4: Sa4 Bit of Frame 7(RSa4F7)

Bit 5: Sa4 Bit of Frame 5(RSa4F5)

Bit 6: Sa4 Bit of Frame 3(RSa4F3)

Bit 7: Sa4 Bit of Frame 1(RSa4F1)

Register Name: **RSa5**
 Register Description: **Receive Sa5 Bits**
 Register Address: **5Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | RSa5F1 | RSa5F3 | RSa5F5 | RSa5F7 | RSa5F9 | RSa5F11 | RSa5F13 | RSa5F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Sa5 Bit of Frame 15(RSa5F15)

Bit 1: Sa5 Bit of Frame 13(RSa5F13)

Bit 2: Sa5 Bit of Frame 11(RSa5F11)

Bit 3: Sa5 Bit of Frame 9(RSa5F9)

Bit 4: Sa5 Bit of Frame 7(RSa5F7)

Bit 5: Sa5 Bit of Frame 5(RSa5F5)

Bit 6: Sa5 Bit of Frame 3(RSa5F3)

Bit 7: Sa5 Bit of Frame 1(RSa5F1)

Register Name: **RSa6**
 Register Description: **Receive Sa6 Bits**
 Register Address: **5Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | RSa6F1 | RSa6F3 | RSa6F5 | RSa6F7 | RSa6F9 | RSa6F11 | RSa6F13 | RSa6F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Sa6 Bit of Frame 15(RSa6F15)

Bit 1: Sa6 Bit of Frame 13(RSa6F13)

Bit 2: Sa6 Bit of Frame 11(RSa6F11)

Bit 3: Sa6 Bit of Frame 9(RSa6F9)

Bit 4: Sa6 Bit of Frame 7(RSa6F7)

Bit 5: Sa6 Bit of Frame 5(RSa6F5)

Bit 6: Sa6 Bit of Frame 3(RSa6F3)

Bit 7: Sa6 Bit of Frame 1(RSa6F1)

Register Name: **RSa7**
 Register Description: **Receive Sa7 Bits**
 Register Address: **5Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | RSa7F1 | RSa7F3 | RSa7F5 | RSa7F7 | RSa7F9 | RSa7F11 | RSa7F13 | RSa7F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Sa7 Bit of Frame 15(RSa7F15)

Bit 1: Sa7 Bit of Frame 13(RSa7F13)

Bit 2: Sa7 Bit of Frame 11(RSa7F11)

Bit 3: Sa7 Bit of Frame 9(RSa7F9)

Bit 4: Sa7 Bit of Frame 7(RSa7F7)

Bit 5: Sa7 Bit of Frame 5(RSa7F5)

Bit 6: Sa7 Bit of Frame 3(RSa7F3)

Bit 7: Sa7 Bit of Frame 1(RSa4F1)

Register Name: **RSa8**
 Register Description: **Receive Sa8 Bits**
 Register Address: **5Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | RSa8F1 | RSa8F3 | RSa8F5 | RSa8F7 | RSa8F9 | RSa8F11 | RSa8F13 | RSa8F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0/Sa8 Bit of Frame 15(RSa8F15)

Bit 1: Sa8 Bit of Frame 13(RSa8F13)

Bit 2: Sa8 Bit of Frame 11(RSa8F11)

Bit 3: Sa8 Bit of Frame 9(RSa8F9)

Bit 4: Sa8 Bit of Frame 7(RSa8F7)

Bit 5: Sa8 Bit of Frame 5(RSa8F5)

Bit 6: Sa8 Bit of Frame 3(RSa8F3)

Bit 7: Sa8 Bit of Frame 1(RSa8F1)

Register Name: **TSiAF**
 Register Description: **Transmit Si Bits of the Align Frame**
 Register Address: **42h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|--------|--------|--------|
| Name | TsiF0 | TsiF2 | TsiF4 | TsiF6 | TsiF8 | TsiF10 | TsiF12 | TsiF14 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Si Bit of Frame 14(TsiF14)

Bit 1: Si Bit of Frame 12(TsiF12)

Bit 2: Si Bit of Frame 10(TsiF10)

Bit 3: Si Bit of Frame 8(TsiF8)

Bit 4: Si Bit of Frame 6(TsiF6)

Bit 5: Si Bit of Frame 4(TsiF4)

Bit 6: Si Bit of Frame 2(TsiF2)

Bit 7: Si Bit of Frame 0(TsiF0)

Register Name: **TSiNAF**
 Register Description: **Transmit Si Bits of the Non-Align Frame**
 Register Address: **43h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|--------|--------|--------|
| Name | TsiF1 | TsiF3 | TsiF5 | TsiF7 | TsiF9 | TsiF11 | TsiF13 | TsiF15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Si Bit of Frame 15(TsiF15)

Bit 1: Si Bit of Frame 13(TsiF13)

Bit 2: Si Bit of Frame 11(TsiF11)

Bit 3: Si Bit of Frame 9(TsiF9)

Bit 4: Si Bit of Frame 7(TsiF7)

Bit 5: Si Bit of Frame 5(TsiF5)

Bit 6: Si Bit of Frame 3(TsiF3)

Bit 7: Si Bit of Frame 1(TsiF1)

Register Name: **TRA**
 Register Description: **Transmit Remote Alarm**
 Register Address: **44h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|--------|--------|--------|
| Name | TRAF1 | TRAF3 | TRAF5 | TRAF7 | TRAF9 | TRAF11 | TRAF13 | TRAF15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Remote Alarm Bit of Frame 15(TRAF15)

Bit 1: Remote Alarm Bit of Frame 13(TRAF13)

Bit 2: Remote Alarm Bit of Frame 11(TRAF11)

Bit 3: Remote Alarm Bit of Frame 9(TRAF9)

Bit 4: Remote Alarm Bit of Frame 7(TRAF7)

Bit 5: Remote Alarm Bit of Frame 5(TRAF5)

Bit 6: Remote Alarm Bit of Frame 3(TRAF3)

Bit 7: Remote Alarm Bit of Frame 1(TRAF1)

Register Name: **TSa4**
 Register Description: **Transmit Sa4 Bits**
 Register Address: **45h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | TSa4F1 | TSa4F3 | TSa4F5 | TSa4F7 | TSa4F9 | TSa4F11 | TSa4F13 | TSa4F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Sa4 Bit of Frame 15(TSa4F15)

Bit 1: Sa4 Bit of Frame 13(TSa4F13)

Bit 2: Sa4 Bit of Frame 11(TSa4F11)

Bit 3: Sa4 Bit of Frame 9(TSa4F9)

Bit 4: Sa4 Bit of Frame 7(TSa4F7)

Bit 5: Sa4 Bit of Frame 5(TSa4F5)

Bit 6: Sa4 Bit of Frame 3(TSa4F3)

Bit 7: Sa4 Bit of Frame 1(TSa4F1)

Register Name: **TSa5**
 Register Description: **Transmit Sa5 Bits**
 Register Address: **46h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | TSa5F1 | TSa5F3 | TSa5F5 | TSa5F7 | TSa5F9 | TSa5F11 | TSa5F13 | TSa5F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Sa5 Bit of Frame 15(TSa5F15)

Bit 1: Sa5 Bit of Frame 13(TSa5F13)

Bit 2: Sa5 Bit of Frame 11(TSa5F11)

Bit 3: Sa5 Bit of Frame 9(TSa5F9)

Bit 4: Sa5 Bit of Frame 7(TSa5F7)

Bit 5: Sa5 Bit of Frame 5(TSa5F5)

Bit 6: Sa5 Bit of Frame 3(TSa5F3)

Bit 7: Sa5 Bit of Frame 1(TSa5F1)

Register Name: **TSa6**
 Register Description: **Transmit Sa6 Bits**
 Register Address: **47h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | TSa6F1 | TSa6F3 | TSa6F5 | TSa6F7 | TSa6F9 | TSa6F11 | TSa6F13 | TSa6F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Sa6 Bit of Frame 15(TSa6F15)

Bit 1: Sa6 Bit of Frame 13(TSa6F13)

Bit 2: Sa6 Bit of Frame 11(TSa6F11)

Bit 3: Sa6 Bit of Frame 9(TSa6F9)

Bit 4: Sa6 Bit of Frame 7(TSa6F7)

Bit 5: Sa6 Bit of Frame 5(TSa6F5)

Bit 6: Sa6 Bit of Frame 3(TSa6F3)

Bit 7: Sa6 Bit of Frame 1(TSa6F1)

Register Name: **TSa7**
 Register Description: **Transmit Sa7 Bits**
 Register Address: **48h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | TSa7F1 | TSa7F3 | TSa7F5 | TSa7F7 | TSa7F9 | TSa7F11 | TSa7F13 | TSa7F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Sa7 Bit of Frame 15(TSa7F15)

Bit 1: Sa7 Bit of Frame 13(TSa7F13)

Bit 2: Sa7 Bit of Frame 11(TSa7F11)

Bit 3: Sa7 Bit of Frame 9(TSa7F9)

Bit 4: Sa7 Bit of Frame 7(TSa7F7)

Bit 5: Sa7 Bit of Frame 5(TSa7F5)

Bit 6: Sa7 Bit of Frame 3(TSa7F3)

Bit 7: Sa7 Bit of Frame 1(TSa4F1)

Register Name: **TSa8**
 Register Description: **Transmit Sa8 Bits**
 Register Address: **49h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | TSa8F1 | TSa8F3 | TSa8F5 | TSa8F7 | TSa8F9 | TSa8F11 | TSa8F13 | TSa8F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Sa8 Bit of Frame 15(TSa8F15)

Bit 1: Sa8 Bit of Frame 13(TSa8F13)

Bit 2: Sa8 Bit of Frame 11(TSa8F11)

Bit 3: Sa8 Bit of Frame 9(TSa8F9)

Bit 4: Sa8 Bit of Frame 7(TSa8F7)

Bit 5: Sa8 Bit of Frame 5(TSa8F5)

Bit 6: Sa8 Bit of Frame 3(TSa8F3)

Bit 7: Sa8 Bit of Frame 1(TSa8F1)

Register Name: **TSACR**
 Register Description: **Transmit Sa Bit Control Register**
 Register Address: **4Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|----|-----|-----|-----|-----|-----|
| Name | SiAF | SiNAF | RA | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Additional Bit 8 Insertion Control Bit (Sa8)

0 = do not insert data from the TSa8 register into the transmit data stream
 1 = insert data from the TSa8 register into the transmit data stream

Bit 1: Additional Bit 7 Insertion Control Bit (Sa7)

0 = do not insert data from the TSa7 register into the transmit data stream
 1 = insert data from the TSa7 register into the transmit data stream

Bit 2: Additional Bit 6 Insertion Control Bit (Sa6)

0 = do not insert data from the TSa6 register into the transmit data stream
 1 = insert data from the TSa6 register into the transmit data stream

Bit 3: Additional Bit 5 Insertion Control Bit (Sa5)

0 = do not insert data from the TSa5 register into the transmit data stream
 1 = insert data from the TSa5 register into the transmit data stream

Bit 4: Additional Bit 4 Insertion Control Bit (Sa4)

0 = do not insert data from the TSa4 register into the transmit data stream
 1 = insert data from the TSa4 register into the transmit data stream

Bit 5: Remote Alarm Insertion Control Bit (RA)

0 = do not insert data from the TRA register into the transmit data stream
 1 = insert data from the TRA register into the transmit data stream

Bit 6: International Bit in Non-Align Frame Insertion Control Bit (SiNAF)

0 = do not insert data from the TSiNAF register into the transmit data stream
 1 = insert data from the TSiNAF register into the transmit data stream

Bit 7: International Bit in Align Frame Insertion Control Bit (SiAF)

0 = do not insert data from the TSiAF register into the transmit data stream
 1 = insert data from the TSiAF register into the transmit data stream

12.2 Alternate Sa/Si Bit Access Based on Double-Frame

On the receive side, the RAF and RNAF registers will always report the data as it received in the Sa and Si bit locations. The RAF and RNAF registers are updated on align frame boundaries. The setting of the receive align frame bit in status register 4 (SR4.0) will indicate that the contents of the RAF and RNAF have been updated. The host can use the SR4.0 bit to know when to read the RAF and RNAF registers. The host has 250µs to retrieve the data before it is lost.

On the transmit side, data is sampled from the TAF and TNAF registers with the setting of the transmit align frame bit in status register 4 (SR4.3). The host can use the SR4.3 bit to know when to update the TAF and TNAF registers. It has 250µs to update the data or else the old data will be retransmitted. **If the TAF and TNAF registers are only being used to source the align frame and non-align frame-sync patterns, then the host need only write once to these registers.** Data for the Si bit can come from the Si bits of the RAF and TNAF registers, the TSiAF and TSiNAF registers, or passed through from the TSER pin.

Register Name: **RAF**
 Register Description: **Receive Align Frame Register**
 Register Address: **56h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|------|------|------|------|------|------|------|
| Name | Si | FAS6 | FAS5 | FAS4 | FAS3 | FAS2 | FAS1 | FAS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Frame Alignment Signal Bit 0 (FAS0). In normal operation this bit will be = 1.

Bit 1: Frame Alignment Signal Bit 1 (FAS1). In normal operation this bit will be = 1.

Bit 2: Frame Alignment Signal Bit 2 (FAS2). In normal operation this bit will be = 0.

Bit 3: Frame Alignment Signal Bit 3 (FAS3). In normal operation this bit will be = 1.

Bit 4: Frame Alignment Signal Bit 4 (FAS4). In normal operation this bit will be = 1.

Bit 5: Frame Alignment Signal Bit 5 (FAS5). In normal operation this bit will be = 0.

Bit 6: Frame Alignment Signal Bit 6 (FAS6). In normal operation this bit will be = 0.

Bit 7: International Bit (Si)

Register Name: **RNAF**
 Register Description: **Receive Non-Align Frame Register**
 Register Address: **57h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|-----|-----|-----|-----|-----|
| Name | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bit 0: Additional Bit 8 (Sa8)

Bit 1: Additional Bit 7 (Sa7)

Bit 2: Additional Bit 6 (Sa6)

Bit 3: Additional Bit 5 (Sa5)

Bit 4: Additional Bit 4 (Sa4)

Bit 5: Remote Alarm (A)

Bit 6: Frame Nonalignment Signal Bit (1). In normal operation this bit will be = 1.

Bit 7: International Bit (Si)

Register Name: **TAF**
 Register Description: **Transmit Align Frame Register**
 Register Address: **40h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|---|---|---|---|---|
| Name | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Default | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| HW Mode | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

Bit 0: Frame Alignment Signal Bit (1)

Bit 1: Frame Alignment Signal Bit (1)

Bit 2: Frame Alignment Signal Bit (0)

Bit 3: Frame Alignment Signal Bit (1)

Bit 4: Frame Alignment Signal Bit (1)

Bit 5: Frame Alignment Signal Bit (0)

Bit 6: Frame Alignment Signal Bit (0)

Bit 7: International Bit (Si)

Register Name: **TNAF**
Register Description: **Transmit Non-Align Frame Register**
Register Address: **41h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|-----|-----|-----|-----|-----|
| Name | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Additional Bit 8 (Sa8)

Bit 1: Additional Bit 7 (Sa7)

Bit 2: Additional Bit 6 (Sa6)

Bit 3: Additional Bit 5 (Sa5)

Bit 4: Additional Bit 4 (Sa4)

Bit 5: Remote Alarm (used to transmit the alarm A)

Bit 6: Frame Nonalignment Signal Bit (1)

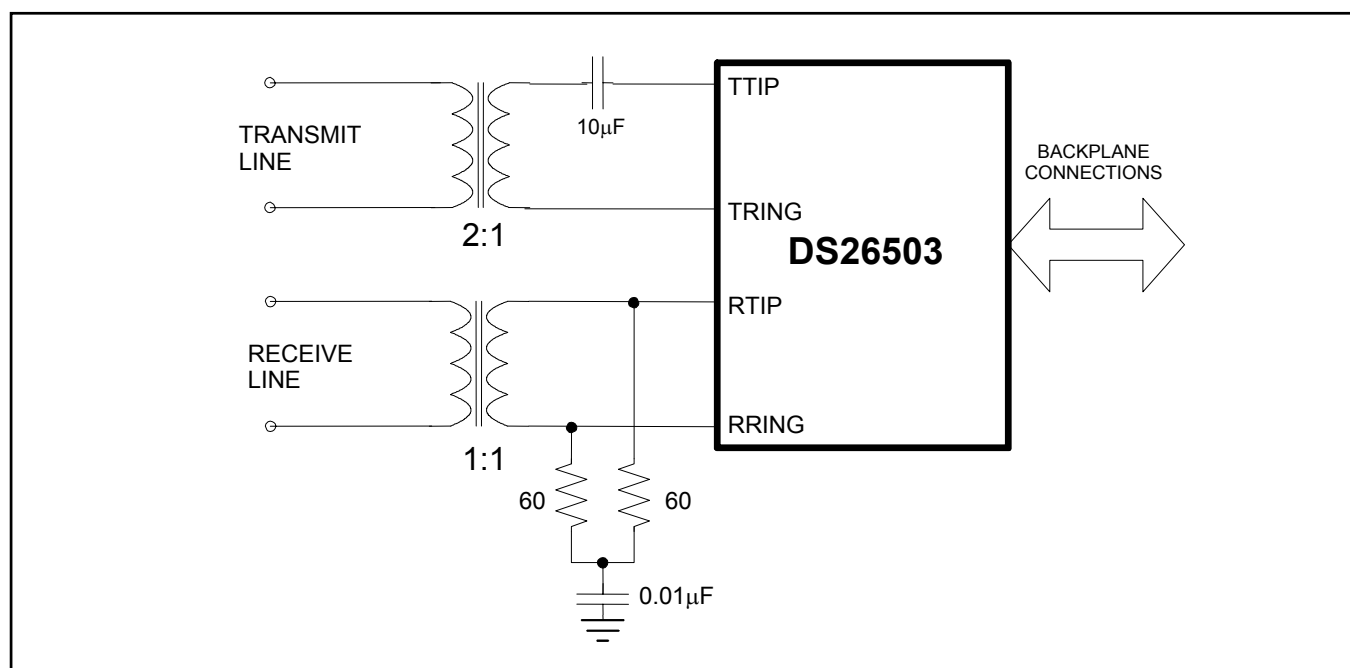
Bit 7: International Bit (Si)

13. LINE INTERFACE UNIT (LIU)

The LIU in the DS26503 contains three sections: the receiver, which handles clock and data recovery; the transmitter, which waveshapes and drives the network line; and the jitter attenuator. These three sections are controlled by the line interface control registers (LIC1–LIC4), which are described below.

The DS26503 can switch between T1 or E1 networks without changing any external components on either the transmit or receive side. [Figure 13-1](#) shows a network connection using minimal components. In this configuration the DS26503, using a fixed 120 Ω external termination, can connect to T1, J1, E1, or 6312kHz without any component change. The receiver can adjust the 120 Ω termination to 100 Ω , 110 Ω or 75 Ω . The transmitter can adjust its output impedance to provide high return loss characteristics for 75 Ω , 100 Ω , 110 Ω , and 120 Ω lines. Other components may be added to this configuration to meet safety and network protection requirements. This is covered in the *Recommended Circuits* section.

Figure 13-1. Basic Network Connection



13.1 LIU Operation

The LIU interfaces the T1, E1, and 6312kHz signals to the various types of network media through coupling transformers. The LIU transmit and receive functions are independent. For example, the receiver can be in T1 mode while the transmitter is in E1 mode. The 6312kHz transmission is an exception to the other modes. For transmission, 6312kHz is only available as a 0 to 3.3V signal on the TCLKO pin. It is not output to the TTIP and TRING pins for coupling to twisted pair. Because the G.703 specifications of the transmit pulse shape for Japanese 6312kHz are unclear, the user can externally filter this signal to generate a sine wave type of signal. However, on the receive side, 6312kHz can be input through the receive transformer to the RTIP and RRING pins.

13.2 LIU Receiver

The analog AMI/HDB3 E1 waveform or AMI/B8ZS T1 waveform is transformer-coupled into the RTIP and RRING pins of the DS26503. The user has the option to use internal termination, software selectable for 75/100/110/120 Ω application, or external termination. The LIU recovers clock and data from the analog signal and passes it through the jitter attenuation mux. (**Note:** The jitter attenuator is only available in T1 or E1 mode.) The DS26503 contains an active filter that reconstructs the analog-received signal for the nonlinear losses that occur in long-haul T1 and E1 transmission. The receiver is configurable for various T1 and E1 monitor applications. The device has a usable receive sensitivity of 0dB to -43dB for E1 and 0dB to -36dB for T1, which allows the device to operate on 0.63mm (22AWG) cables up to 2.5km (E1) and 6000ft (T1) in length.

The DS26503's LIU is designed to be fully software selectable for E1 and T1 without the need to change any external resistors for the receive-side. The receiver will allow the user to configure the DS26503 for 75 Ω , 100 Ω , 110 Ω , or 120 Ω receive termination by setting the RT0(LIC4.0), RT1(LIC4.1), and RT2(LIC4.2). When using the internal termination feature, the resistors labeled R in [Figure 13-4](#) should be 60 Ω each. If external termination is used, RT0, RT1, and RT2 should be set to zero and the resistors labeled R in [Figure 13-4](#) will need to be 37.5 Ω , 50 Ω , 55 Ω , or 60 Ω each, depending on the required termination.

There are two ranges of receive sensitivity for T1 and E1, which is selectable by the user. The EGL bit of LIC1 (LIC1.4) selects the full or limited sensitivity.

Normally, the clock that is output at the RCLK pin is the recovered clock from the waveform presented at the RTIP and RRING inputs. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to an approximate 50% duty cycle. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLK output can exhibit slightly shorter high cycles of the clock. This is due to the highly over-sampled digital clock recovery circuitry. See the *Receive AC Timing Characteristics* section for more details. When no signal is present at RTIP and RRING, a receive loss of signal (RLOS) condition will occur and the signal at RCLK will be derived from the scaled signal present on the MCLK pin.

13.2.1 Receive Level Indicator

The DS26503 will report the signal strength at RTIP and RRING in 2.5dB increments via RL3-RL0 located in the Information Register 1 (INFO1). This feature is helpful when trouble shooting line performance problems.

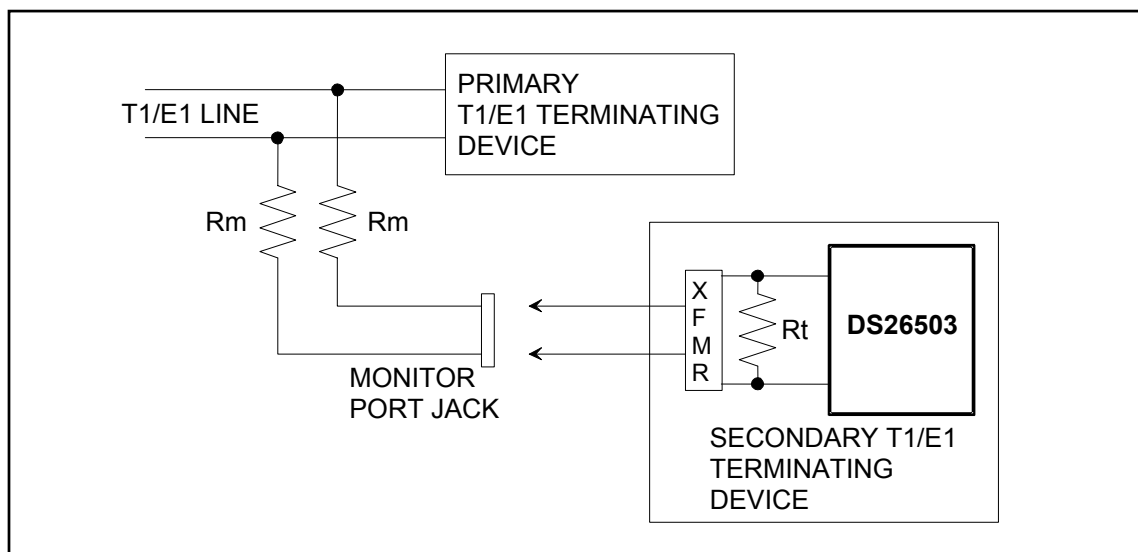
13.2.2 Receive G.703 Section 10 Synchronization Signal

The DS26503 can receive a 2.048MHz square-wave synchronization clock as specified in Section 10 of ITU G.703. To use the DS26503 in this mode, set the mode configuration bits in the Mode Configuration Register (MCREG).

13.2.3 Monitor Mode

Monitor applications in both E1 and T1 require various flat gain settings for the receive-side circuitry. The DS26503 can be programmed to support these applications via the monitor mode control bits MM1 and MM0 in the LIC3 register.

Figure 13-2. Typical Monitor Application



13.3 LIU Transmitter

The DS26503 uses a phase-lock loop along with a precision digital-to-analog converter (DAC) to create the waveforms that are transmitted onto the E1 or T1 line. The waveforms created by the DS26503 meet the latest ETSI, ITU, ANSI, and AT&T specifications. The waveform that is to be generated is set by the transmit mode bits (TMODE[3:0]) in the MCREG register, as well as the L2/L1/L0 bits in register LIC1 if applicable.

ITU specification G.703 requires an accuracy of ± 50 ppm for both T1 and E1. TR62411 and ANSI specs require an accuracy of ± 32 ppm for T1 interfaces. The transmit clock can be sourced from the recovered clock (RCLK), the pre-scaled MCLK, the TCLK pin or the TX PLL. See the TX PLL clock mux diagram in [Figure 3-3](#). Due to the nature of the design of the transmitter in the DS26503, very little jitter (less than $0.005 U_{I_{P-P}}$ broadband from 10Hz to 100kHz) is added to the jitter present on the selected transmit clock source. Also, the waveforms created are independent of the duty cycle of TCLK. The transmitter in the DS26503 couples to the transmit twisted pair (or coaxial cable in some applications) via a 1:2 step-up transformer. For the device to create the proper waveforms, the transformer used must meet the specifications listed in [Table 13-1](#). The DS26503 has the option of using software-selectable transmit termination.

The transmit line drive has two modes of operation: fixed gain or automatic gain. In the fixed gain mode, the transmitter outputs a fixed current into the network load to achieve a nominal pulse amplitude. In the automatic gain mode, the transmitter adjusts its output level to compensate for slight variances in the network load. See the *Transmit Line Build-Out Control (TLBC)* register for details.

13.3.1 Transmit Short-Circuit Detector/Limiter

The DS26503 has an automatic short-circuit limiter that limits the source current to approximately 50mA (rms) on the network side of the transformer in E1 modes of operations and 70mA (rms) on the network side of the transformer in T1 modes of operation. These values are approximate and are not guaranteed by production testing. This feature can be disabled by setting the SCLD bit (LIC2.1) = 1. TCLE (SR1.2) provides a real-time indication of when the current limiter is activated. If the current limiter is disabled, TCLE will indicate that a short-circuit condition exist. Status Register SR1.2 provides a latched version of the information, which can be used to activate an interrupt when enable via the IMR1 register. When set low, the TPD bit (LIC1.0) will power-down the transmit line driver and tri-state the TTIP and TRING pins.

13.3.2 Transmit Open-Circuit Detector

The DS26503 can also detect when the TTIP or TRING outputs are open circuited. TOCD (SR1.1) will provide a real-time indication of when an open circuit is detected. SR1 provides a latched version of the information (SR1.1), which can be used to activate an interrupt when enable via the IMR1 register. The functionality of these bits is not guaranteed by production testing.

13.3.3 Transmit BPV Error Insertion

When IBPV (LIC2.5) is transitioned from a zero to a one, the device waits for the next occurrence of three consecutive ones to insert a BPV. IBPV must be cleared and set again for another BPV error insertion.

13.3.4 Transmit G.703 Section 10 Synchronization Signal (E1 Mode)

The DS26503 can transmit the 2.048MHz square-wave synchronization clock. To transmit the 2.048MHz clock, when in E1 mode, set the mode configuration bits in the Mode Configuration Register (MCREG).

13.4 MCLK Pre-Scaler

A 2.048MHz x 2^N (where N = 0 to 3), 1.544MHz x 2^N (where N = 0 to 3), or 12.8MHz (**available in CPU interface mode only**) clock must be applied to MCLK. A pre-scaler (divide by 2, 4, or 8) and PLLs are selected to product an internal 2.048MHz or 1.544MHz clock. ITU specification G.703 requires an accuracy of ± 50 ppm for both T1 and E1. TR62411 and ANSI specs require an accuracy of ± 32 ppm for T1 interfaces. A pre-scaler divides the 16.384MHz, 12.8MHz, 8.192MHz, or 4.096MHz clock down to 2.048MHz. An on-board PLL for the jitter attenuator converts the 2.048MHz clock to a 1.544MHz rate for T1 applications. Setting JACKS0 (LIC2.3) to logic 0 bypasses this PLL.

13.5 Jitter Attenuator

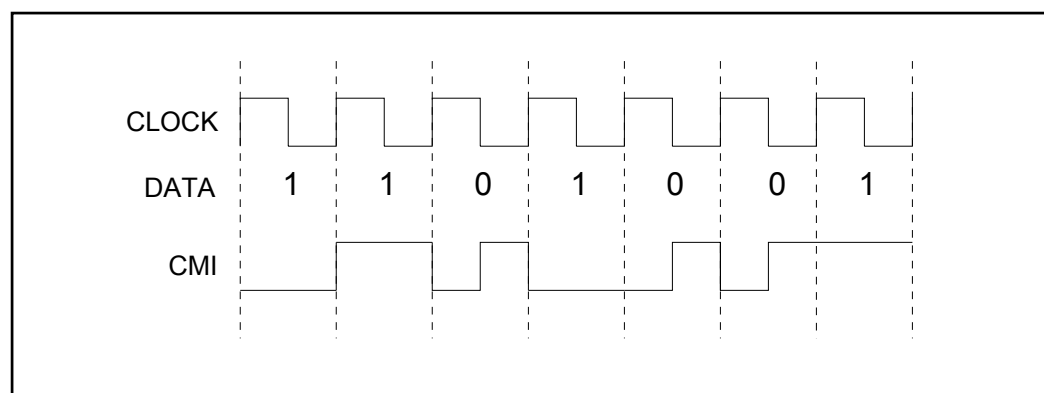
The DS26503's jitter attenuator can be set to a depth of either 32 bits or 128 bits via the JABDS bit (LIC1.2). The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay-sensitive applications. The characteristics of the attenuation are shown in [Figure 13-10](#) and [Figure 13-11](#). The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit (LIC1.3). If the part is configured for hardware mode and the jitter attenuator is enabled, it will automatically be placed in the receive path. The

the incoming jitter exceeds either 120 UI_{P-P} (buffer depth is 128 bits) or 28 UI_{P-P} (buffer depth is 32 bits), then the DS26503 will divide the internal nominal 32.768MHz (E1) or 24.704MHz (T1) clock by either 15 or 17 instead of the normal 16 to keep the buffer from overflowing. When the device divides by either 15 or 17, it also sets the Jitter Attenuator Limit Trip (JALT) bit in Status Register 1 (SR1.4).

13.6 CMI (Code Mark Inversion) Option

The DS26503 provides a CMI interface for connection to optical transports. This interface is a unipolar 1T2B type of signal. Ones are encoded as either a logical one or zero level for the full duration of the clock period. Zeros are encoded as a zero-to-one transition at the middle of the clock period.

Figure 13-3. CMI Coding



Transmit and receive CMI is enabled via LIC4.7. When this register bit is set, the TTIP pin will output CMI-coded data at normal levels. This signal can be used to directly drive an optical interface. When CMI is enabled, the user can also use HDB3/B8ZS coding. When this register bit is set, the RTIP pin will become a unipolar CMI input. The CMI signal will be processed to extract and align the clock with data.

13.7 LIU Control Registers

Register Name: **LIC1**
 Register Description: **Line Interface Control 1**
 Register Address: **30h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|--------------|--------------|-----|-----|-------|-----|-----|
| Name | L2 | L1 | L0 | EGL | JAS | JABDS | DJA | TPD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | L2 PIN 13 | L1 PIN 12 | L0 PIN 11 | 0 | 0 | 0 | 0 | 1 |

Bit 0: Transmit Power-Down (TPD)

0 = powers down the transmitter and three-states the TTIP and TRING pins
 1 = normal transmitter operation

Bit 1: Disable Jitter Attenuator (DJA)

0 = jitter attenuator enabled
 1 = jitter attenuator disabled

Bit 2: Jitter Attenuator Buffer Depth Select (JABDS)

0 = 128 bits
 1 = 32 bits (use for delay-sensitive applications)

Bit 3: Jitter Attenuator Select (JAS)

0 = place the jitter attenuator on the receive side
 1 = place the jitter attenuator on the transmit side

Bit 4: Receive Equalizer Gain Limit (EGL). This bit controls the sensitivity of the receive equalizer.

T1 Mode: 0 = -36dB (long haul)
 1 = -15dB (limited long haul)
 E1 Mode: 0 = -43dB (long haul)
 1 = -12dB (short haul)

Bits 5 to 7: Line Build-Out Select (L0 to L2). When using the internal termination, the user needs only to select 000 for 75Ω operation or 001 for 120Ω operation. This selects the proper voltage levels for 75Ω or 120Ω operation. Using TT0, TT1, and TT2 of the LICR4 register, users can then select the proper internal source termination. Line build-outs 100 and 101 are for backwards compatibility with older products only.

E1 Mode

| L2 | L1 | L0 | APPLICATION | N (NOTE 1) | RETURN LOSS | Rt (NOTE 1) |
|----|----|----|-------------------------------------|---------------|-------------|----------------|
| 0 | 0 | 0 | 75Ω normal | 1:2 | N.M. | 0 |
| 0 | 0 | 1 | 120Ω normal | 1:2 | N.M. | 0 |
| 1 | 0 | 0 | 75Ω with high return loss (Note 2) | 1:2 | 21dB | 6.2Ω |
| 1 | 0 | 1 | 120Ω with high return loss (Note 2) | 1:2 | 21dB | 11.6Ω |

Note 1: Transformer turns ratio.

Note 2: TT0, TT1, and TT2 of LIC4 register must be set to zero in this configuration.

N.M. = not meaningful

T1 Mode

| L2 | L1 | L0 | APPLICATION | N (NOTE 1) | RETURN LOSS | Rt (NOTE 1) |
|----|----|----|-------------------------------|------------|-------------|-------------|
| 0 | 0 | 0 | DSX-1 (0 to 133 feet)/0dB CSU | 1:2 | N.M. | 0 |
| 0 | 0 | 1 | DSX-1 (133 to 266 feet) | 1:2 | N.M. | 0 |
| 0 | 1 | 0 | DSX-1 (266 to 399 feet) | 1:2 | N.M. | 0 |
| 0 | 1 | 1 | DSX-1 (399 to 533 feet) | 1:2 | N.M. | 0 |
| 1 | 0 | 0 | DSX-1 (533 to 655 feet) | 1:2 | N.M. | 0 |
| 1 | 0 | 1 | Reserved | — | — | — |
| 1 | 1 | 0 | Reserved | — | — | — |
| 1 | 1 | 1 | Reserved | — | — | — |

Note 1: Transformer turns ratio.

N.M. = not meaningful

Register Name: **TLBC**
Register Description: **Transmit Line Build-Out Control**
Register Address: **34h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|-----|-----|-----|-----|-----|-----|
| Name | — | AGCE | GC5 | GC4 | GC3 | GC2 | GC1 | GC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0 to 5: Gain Control Bits 0–5 (GC0–GC5). The GC0 through GC5 bits control the gain setting for the non-automatic gain mode. Use the tables below for setting the recommended values. The LBO (line build-out) column refers to the value in the L0–L2 bits in LIC1 (Line Interface Control 1) register.

| NETWORK MODE | LB | GC5 | GC4 | GC3 | GC2 | GC1 | GC0 |
|--------------------------------|----|-----|-----|-----|-----|-----|-----|
| T1, Impedance Match Off | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| | 2 | 0 | 1 | 1 | 0 | 1 | 0 |
| | 3 | 1 | 0 | 0 | 0 | 0 | 0 |
| | 4 | 1 | 0 | 0 | 1 | 1 | 1 |
| | 5 | 1 | 0 | 0 | 1 | 1 | 1 |
| | 6 | 0 | 1 | 0 | 0 | 1 | 1 |
| T1, Impedance Match On | 7 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| | 2 | 0 | 1 | 0 | 1 | 0 | 1 |
| | 3 | 0 | 1 | 1 | 0 | 1 | 0 |
| | 4 | 1 | 0 | 0 | 0 | 1 | 0 |
| | 5 | 1 | 0 | 0 | 0 | 0 | 0 |
| E1, Impedance Match Off | 6 | 0 | 0 | 1 | 1 | 0 | 0 |
| | 7 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| E1, Impedance Match On | 4 | 1 | 0 | 1 | 0 | 1 | 0 |
| | 5 | 1 | 0 | 1 | 0 | 0 | 0 |
| E1, Impedance Match On | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

Bit 6: Automatic Gain Control Enable (AGCE)

0 = use Transmit AGC, TLBC bits 0–5 are “don’t care”

1 = do not use Transmit AGC, TLBC bits 0–5 set nominal level

Bit 7: Unused, must be set = 0 for proper operation.

Register Name: **LIC2**
 Register Description: **Line Interface Control 2**
 Register Address: **31h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|-------|------|----------------|------------------|---|------|------|
| Name | JACKS1 | LIRST | IBPV | TAIS | JACKS0 | — | SCLD | CLDS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | TAIS PIN 10 | JACKS0 PIN 46 | 0 | 0 | 0 |

Bit 0: Custom Line Driver Select (CLDS). Setting this bit to a one will redefine the operation of the transmit line driver. When this bit is set to a one and LIC1.5 = LIC1.6 = LIC1.7 = 0, then the device will generate a square wave at the TTIP and TRING outputs instead of a normal waveform. When this bit is set to a one and LIC1.5 = LIC1.6 = LIC1.7 ≠ 0, then the device will force TTIP and TRING outputs to become open-drain drivers instead of their normal push-pull operation. This bit should be set to zero for normal operation of the device.

Bit 1: Short Circuit Limit Disable (in E1 mode) (SCLD). Controls the 50mA (RMS) current limiter.

0 = enable 50mA current limiter

1 = disable 50mA current limiter

Bits 2 and 7: Unused, must be set = 0 for proper operation.

Bit 3: Jitter Attenuator Clock Select 0 (JACKS0). This bit, along with JACKS1 (LIC2.7), MPS0 (LIC4.6), and MPS1 (LIC4.7), controls the source for JA CLOCK from the MCLK pin. **Note: This bit must be configured even if the jitter attenuator is disabled.** The clock and data recovery engine also uses the JA CLOCK. Setting this bit enables the 2.048MHz to 1.544MHz conversion PLL for T1 applications. See the table in the LIC4 register description for more details on setting up the JA CLOCK source.

0 = 2.048MHz to 1.544MHz PLL bypassed

1 = 2.048MHz to 1.544MHz PLL enabled

Bit 4: Transmit Alarm Indication Signal (TAIS)

0 = transmit an unframed all-ones code

1 = transmit data normally

Bit 5: Insert BPV (IBPV). A zero-to-one transition on this bit will cause a single BPV to be inserted into the transmit data stream. Once this bit has been toggled from a zero to a one, the device waits for the next occurrence of three consecutive ones to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted.

Bit 6: Line Interface Reset (LIRST). Setting this bit from a zero to a one will initiate an internal reset that resets the clock recovery state machine and recenters the jitter attenuator. Normally this bit is only toggled on power-up. Must be cleared and set again for a subsequent reset.

Bit 7: Jitter Attenuator Clock Select 1 (JACKS1). This bit, along with JACKS0 (LIC2.3), MPS0 (LIC4.6), and MPS1 (LIC4.7), controls the source for JA CLOCK from the MCLK pin. **Note: This bit must be configured even if the jitter attenuator is disabled.** The clock and data recovery engine also uses the JA CLOCK. Setting this bit enables the 12.8MHz to 2.048MHz conversion PLL. See the table in the LIC4 register description for more details on setting up the JA CLOCK source.

0 = 12.8MHz to 2.048MHz PLL bypassed

1 = 12.8MHz to 2.048MHz PLL enabled

Register Name: **LIC3**
 Register Description: **Line Interface Control 3**
 Register Address: **32h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|---|-----|-----|---|---|------|
| Name | CMIE | CMII | — | MM1 | MM0 | — | — | TAOZ |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Transmit Alternate Ones and Zeros (TAOZ). Transmit a ...101010... pattern at TTIP and TRING.
 0 = disabled
 1 = enabled

Bits 1, 2, 5: Unused, must be set = 0 for proper operation.

Bits 3 and 4: Monitor Mode (MM0 to MM1)

| MM1 | MM0 | INTERNAL LINEAR GAIN BOOST (dB) |
|-----|-----|---------------------------------|
| 0 | 0 | Normal operation (no boost) |
| 0 | 1 | 20 |
| 1 | 0 | 26 |
| 1 | 1 | 32 |

Bit 6: CMI Invert (CMII)
 0 = CMI normal at TTIP and RTIP
 1 = invert CMI signal at TTIP and RTIP

Bit 7: CMI Enable (CMIE)
 0 = disable CMI mode
 1 = enable CMI mode

Register Name: **LIC4**
 Register Description: **Line Interface Control 4**
 Register Address: **33h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------------|----------------|-----|-----|-----|-----|-----|-----|
| Name | MPS1 | MPS0 | TT2 | TT1 | TT0 | RT2 | RT1 | RT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | MPS1 PIN 16 | MPS0 PIN 15 | — | — | — | — | — | — |

Bits 0 to 2: Receive Termination Select (RT0 to RT2)

| RT2 | RT1 | RT0 | INTERNAL RECEIVE TERMINATION CONFIGURATION |
|-----|-----|-----|---|
| 0 | 0 | 0 | Internal Receive-Side Termination Disabled |
| 0 | 0 | 1 | Internal Receive-Side 75Ω Enabled |
| 0 | 1 | 0 | Internal Receive-Side 100Ω Enabled |
| 0 | 1 | 1 | Internal Receive-Side 120Ω Enabled |
| 1 | 0 | 0 | Internal Receive-Side 110Ω Enabled |
| 1 | 0 | 1 | Internal Receive-Side Termination Disabled |
| 1 | 1 | 0 | Internal Receive-Side Termination Disabled |
| 1 | 1 | 1 | Internal Receive-Side Termination Disabled |

Bits 3 to 5: Transmit Termination Select (TT0 to TT2)

| TT2 | TT1 | TT0 | INTERNAL TRANSMIT TERMINATION CONFIGURATION |
|-----|-----|-----|--|
| 0 | 0 | 0 | Internal Transmit-Side Termination Disabled |
| 0 | 0 | 1 | Internal Transmit-Side 75Ω Enabled |
| 0 | 1 | 0 | Internal Transmit-Side 100Ω Enabled |
| 0 | 1 | 1 | Internal Transmit-Side 120Ω Enabled |
| 1 | 0 | 0 | Internal Transmit-Side 110Ω Enabled |
| 1 | 0 | 1 | Internal Transmit-Side Termination Disabled |
| 1 | 1 | 0 | Internal Transmit-Side Termination Disabled |
| 1 | 1 | 1 | Internal Transmit-Side Termination Disabled |

Bits 6 and 7: MCLK Pre-Scaler (MPS0 to MPS1) (T1 Mode)

| MCLK (MHz) | MPS1 | MPS0 | JACKS1 (LIC2.3) | JACKS0 (LIC2.7) |
|------------|------|------|-----------------|-----------------|
| 1.544 | 0 | 0 | 0 | 0 |
| 3.088 | 0 | 1 | 0 | 0 |
| 6.176 | 1 | 0 | 0 | 0 |
| 12.352 | 1 | 1 | 0 | 0 |
| 12.80 | 0 | 0 | 1 | 1 |
| 2.048 | 0 | 0 | 1 | 0 |
| 4.096 | 0 | 1 | 1 | 0 |
| 8.192 | 1 | 0 | 1 | 0 |
| 16.384 | 1 | 1 | 1 | 0 |

Bits 6 and 7: MCLK Pre-Scaler (MPS0 to MPS1) (E1 Mode)

| MCLK (MHz) | MPS1 | MPS0 | JACKS (LIC2.3) | JACKS0 (LIC2.7) |
|------------|------|------|----------------|-----------------|
| 2.048 | 0 | 0 | 0 | 0 |
| 4.096 | 0 | 1 | 0 | 0 |
| 8.192 | 1 | 0 | 0 | 0 |
| 12.80 | 0 | 0 | 0 | 1 |
| 16.384 | 1 | 1 | 0 | 0 |

Register Name: **INFO1**
 Register Description: **Information Register 1**
 Register Address: **11h**

| | | | | | | | | |
|---------|---|---|---|---|-----|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | RL3 | RL2 | RL1 | RL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bits 0 to 3: Receive Level Bits (RL0 to RL3). Real-time bits.

| RL3 | RL2 | RL1 | RL0 | RECEIVE LEVEL (dB) |
|-----|-----|-----|-----|--------------------|
| 0 | 0 | 0 | 0 | Greater than -2.5 |
| 0 | 0 | 0 | 1 | -2.5 to -5.0 |
| 0 | 0 | 1 | 0 | -5.0 to -7.5 |
| 0 | 0 | 1 | 1 | -7.5 to -10.0 |
| 0 | 1 | 0 | 0 | -10.0 to -12.5 |
| 0 | 1 | 0 | 1 | -12.5 to -15.0 |
| 0 | 1 | 1 | 0 | -15.0 to -17.5 |
| 0 | 1 | 1 | 1 | -17.5 to -20.0 |
| 1 | 0 | 0 | 0 | -20.0 to -22.5 |
| 1 | 0 | 0 | 1 | -22.5 to -25.0 |
| 1 | 0 | 1 | 0 | -25.0 to -27.5 |
| 1 | 0 | 1 | 1 | -27.5 to -30.0 |
| 1 | 1 | 0 | 0 | -30.0 to -32.5 |
| 1 | 1 | 0 | 1 | -32.5 to -35.0 |
| 1 | 1 | 1 | 0 | -35.0 to -37.5 |
| 1 | 1 | 1 | 1 | Less than -37.5 |

Bits 4 to 7: Unused

Register Name: **SR1**
 Register Description: **Status Register 1**
 Register Address: **14h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|------|---|------|------|---|
| Name | — | — | — | JALT | — | TCLE | TOCD | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bits 0, 3, 5, 6, 7: Unused, must be set = 0 for proper operation.

Bit 1: Transmit Open Circuit Detect Condition (TOCD). Set when the device detects that the TTIP and TRING outputs are open-circuited. **Note:** This function not supported in transmit 6312kHz mode and is not guaranteed by production testing.

Bit 2: Transmit Current Limit Exceeded Condition (TCLE). Set when the current limiter is activated whether the current limiter is enabled or not. This is set at approximately 50mA (RMS) on the network side of the transformer in E1 operating modes and 70mA (RMS) on the network side of the transformer in T1 operating modes. These values are approximate and are not guaranteed by production testing. **Note:** This function not supported in transmit CMI, 64kHz or 6312kHz mode.

Bit 4: Jitter Attenuator Limit Trip Event (JALT). Set when the jitter attenuator FIFO reaches to within 4 bits of its useful limit. Will be cleared when read. Useful for debugging jitter-attenuation operation.

Register Name: **IMR1**
 Register Description: **Interrupt Mask Register 1**
 Register Address: **15h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|------|---|------|------|---|
| Name | — | — | — | JALT | — | TCLE | TOCD | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | X | X | X | X | X | X | X | X |

Bits 0, 3, 5, 6, 7: Unused, must be set = 0 for proper operation.

Bit 1: Transmit Open-Circuit Detect Condition (TOCD)

0 = interrupt masked

1 = interrupt enabled—generates interrupts on rising and falling edges

Bit 2: Transmit Current Limit Exceeded Condition (TCLE)

0 = interrupt masked

1 = interrupt enabled—generates interrupts on rising and falling edges

Bit 4: Jitter Attenuator Limit Trip Event (JALT)

0 = interrupt masked

1 = interrupt enabled

13.8 Recommended Circuits

Figure 13-4. Software-Selected Termination, Metallic Protection

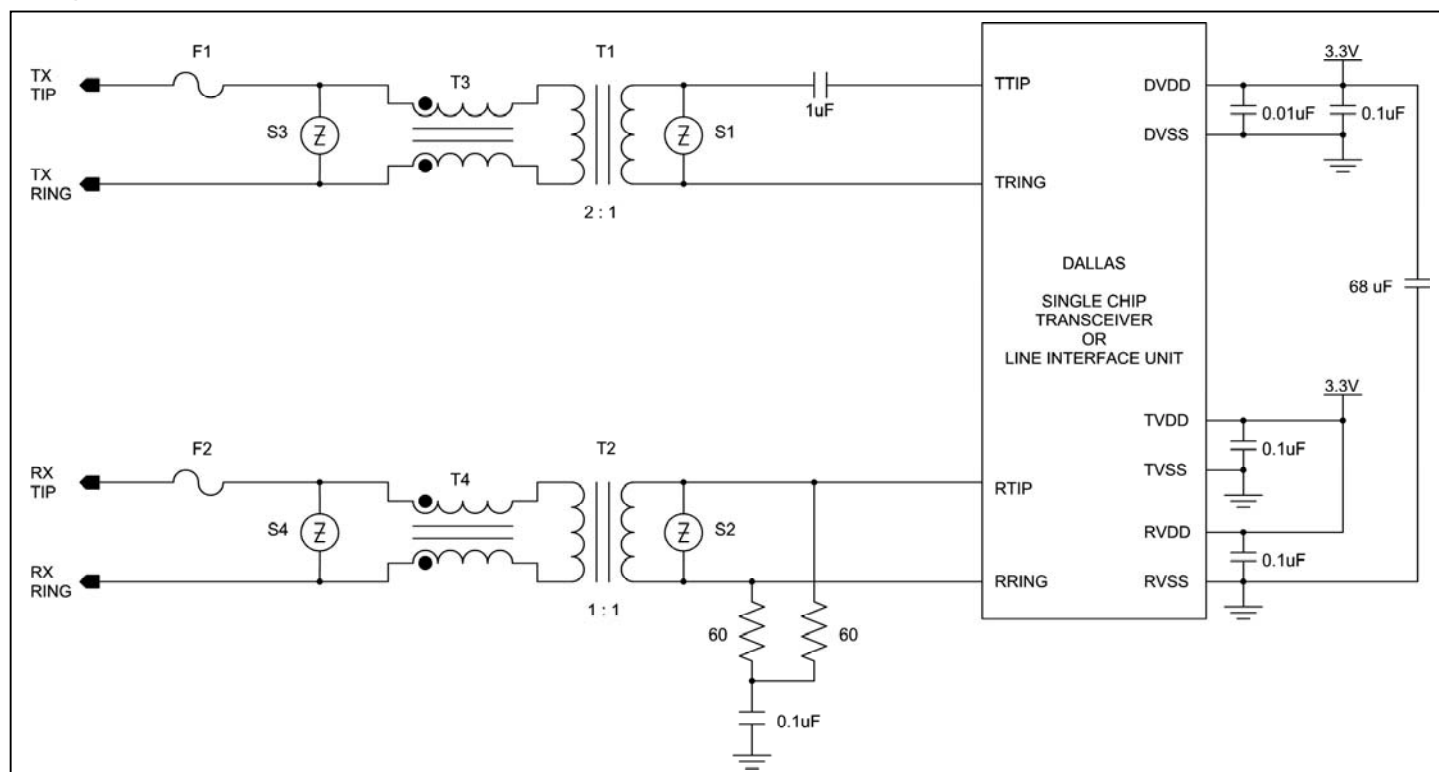


Table 13-1. Component List (Software-Selected Termination, Metallic Protection)

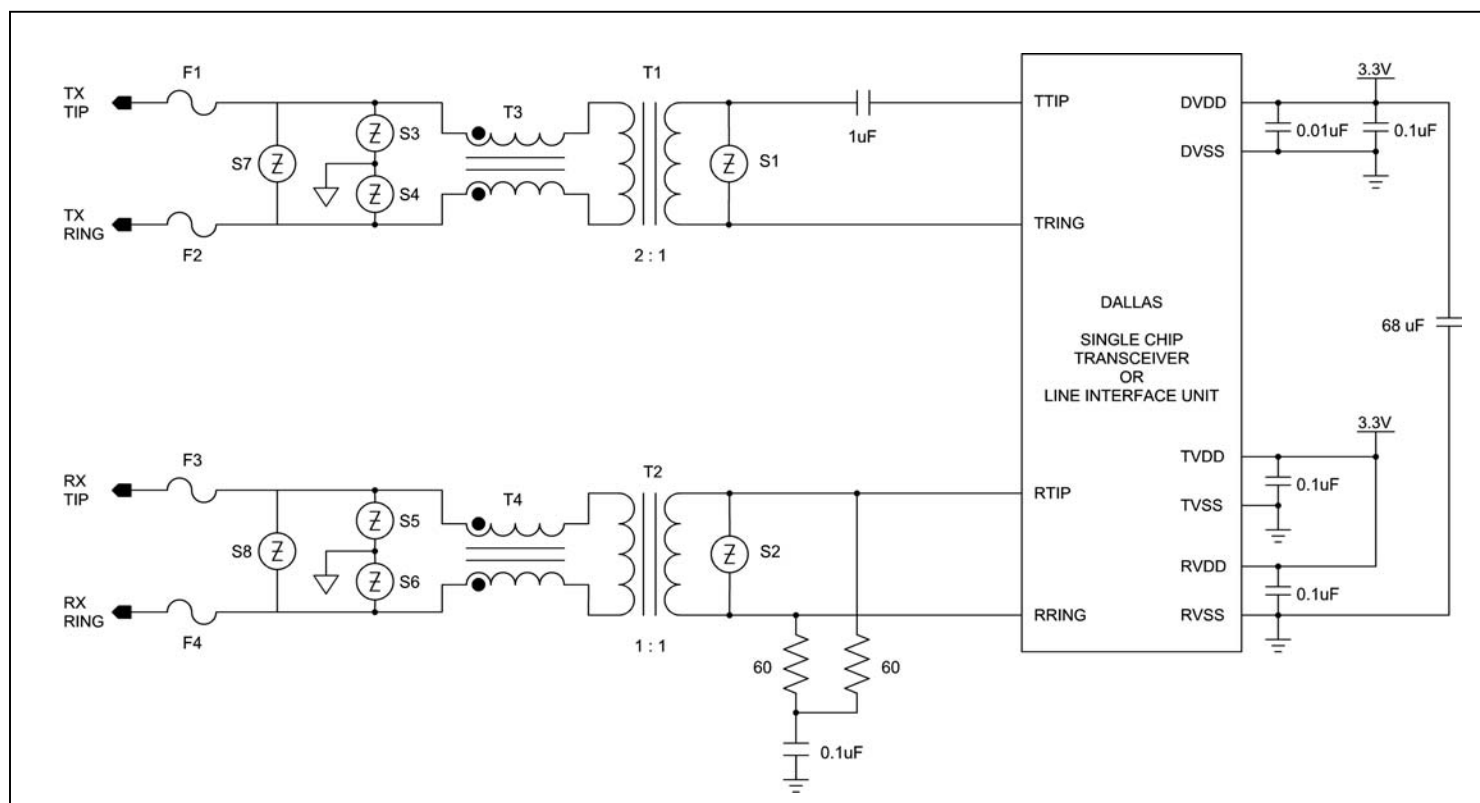
| NAME | DESCRIPTION |
|-----------|--|
| F1 and F2 | 1.25A slow blow fuse |
| S1 and S2 | 25V (max) transient suppressor |
| S3 and S4 | 77V (max) transient suppressor |
| T1 and T2 | Transformer 1:1CT and 1:136CT (5.0V, SMT) (Note 1) |
| | Transformer 1:1CT and 1:2CT (3.3V, SMT) (Note 1) |
| T3 and T4 | Dual common-mode choke (SMT) |

Note 1: T3 and T4 are optional. For more information, contact the Telecom Support Group at www.maxim-ic.com/support.

Note 2: The layout from the transformers to the network interface is critical. Traces should be at least 25 mils wide and separated from other circuit lines by at least 150 mils. The area under this portion of the circuit should not contain power planes.

Note 3: Some T1 (never in E1) applications source or sink power from the network-side center taps of the Rx/Tx transformers.

Note 4: A list of transformer part numbers and manufacturers is available by contacting www.maxim-ic.com/support.

Figure 13-5. Software-Selected Termination, Longitudinal Protection**Table 13-2. Component List (Software-Selected Termination, Longitudinal Protection)**

| NAME | DESCRIPTION |
|----------------|--|
| F1 to F4 | 1.25A slow blow fuse |
| S1 and S2 | 25V (max) transient suppressor (Note 1) |
| S3, S4, S5, S6 | 180V (max) transient suppressor (Note 1) |
| S7 and S8 | 40V (max) transient suppressor |
| T1 and T2 | Transformer 1:1CT and 1:136CT (5.0V, SMT) (Note 2) |
| | Transformer 1:1CT and 1:2CT (3.3V, SMT) (Note 2) |
| T3 and T4 | Dual common-mode choke (SMT) |

Note 1: T3 and T4 are optional. For more information, contact the Telecom Support Group at www.maxim-ic.com/support.

Note 2: A list of alternate transformer part numbers and manufacturers is available at www.maxim-ic.com/support.

Note 3: The layout from the transformers to the network interface is critical. Traces should be at least 25 mils wide and separated from other circuit lines by at least 150 mils. The area under this portion of the circuit should not contain power planes.

Note 4: Some T1 (never in E1) applications source or sink power from the network-side center taps of the Rx/Tx transformers.

Note 5: The ground trace connected to the S2/S3 pair and the S4/S5 pair should be at least 50 mils wide to conduct the extra current from a longitudinal power-cross event.

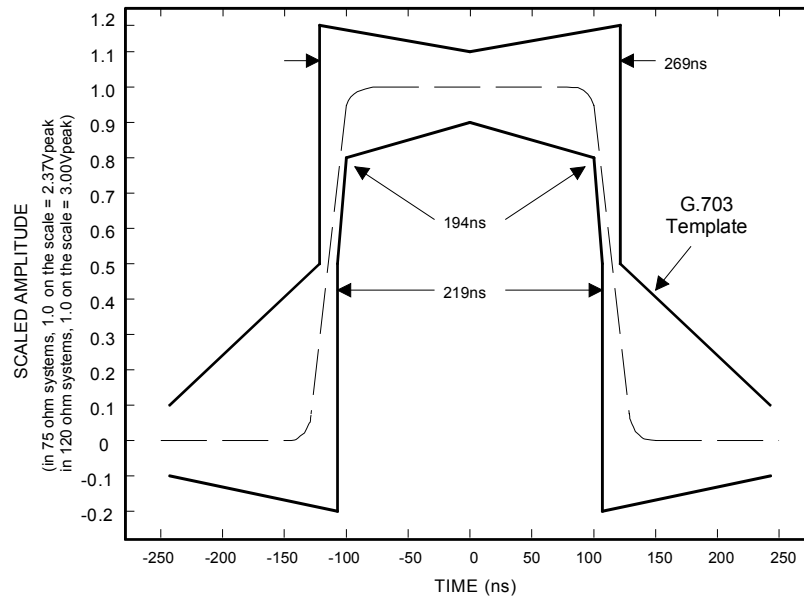
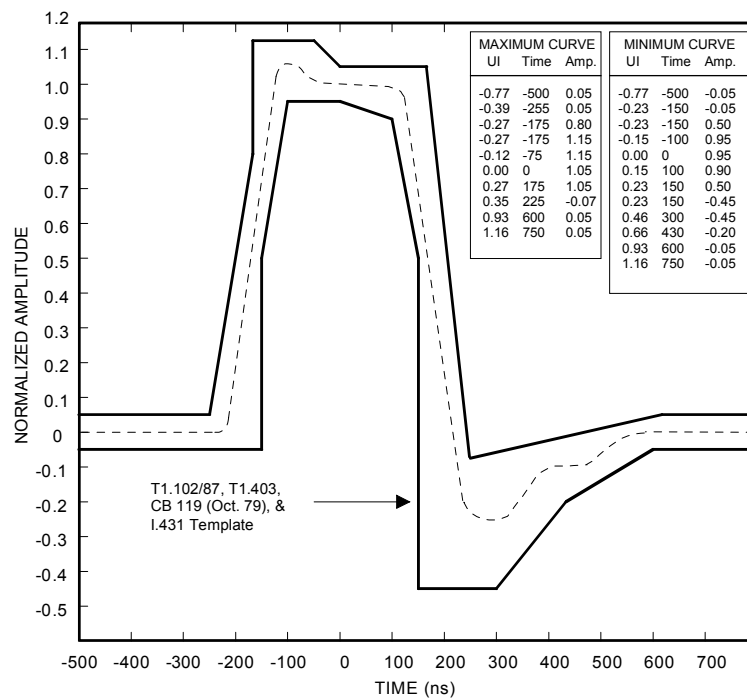
Figure 13-6. E1 Transmit Pulse Template**Figure 13-7. T1 Transmit Pulse Template**

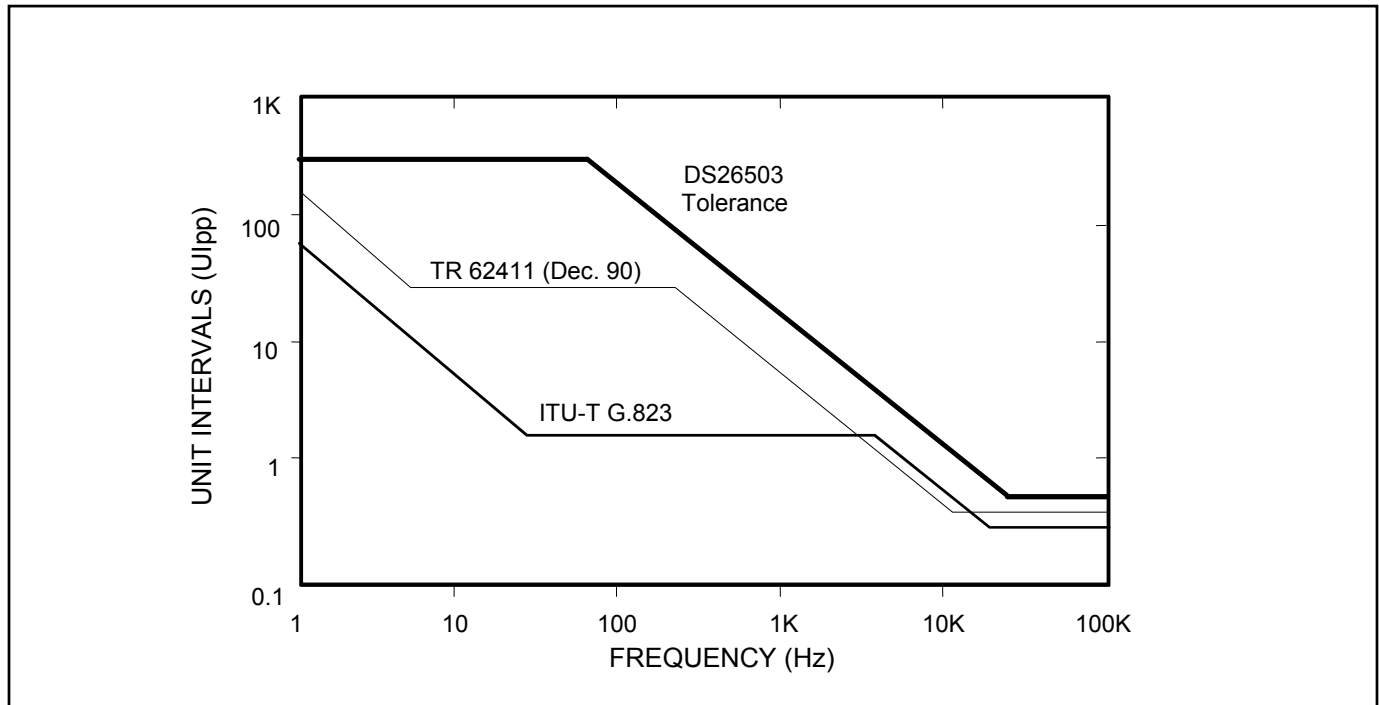
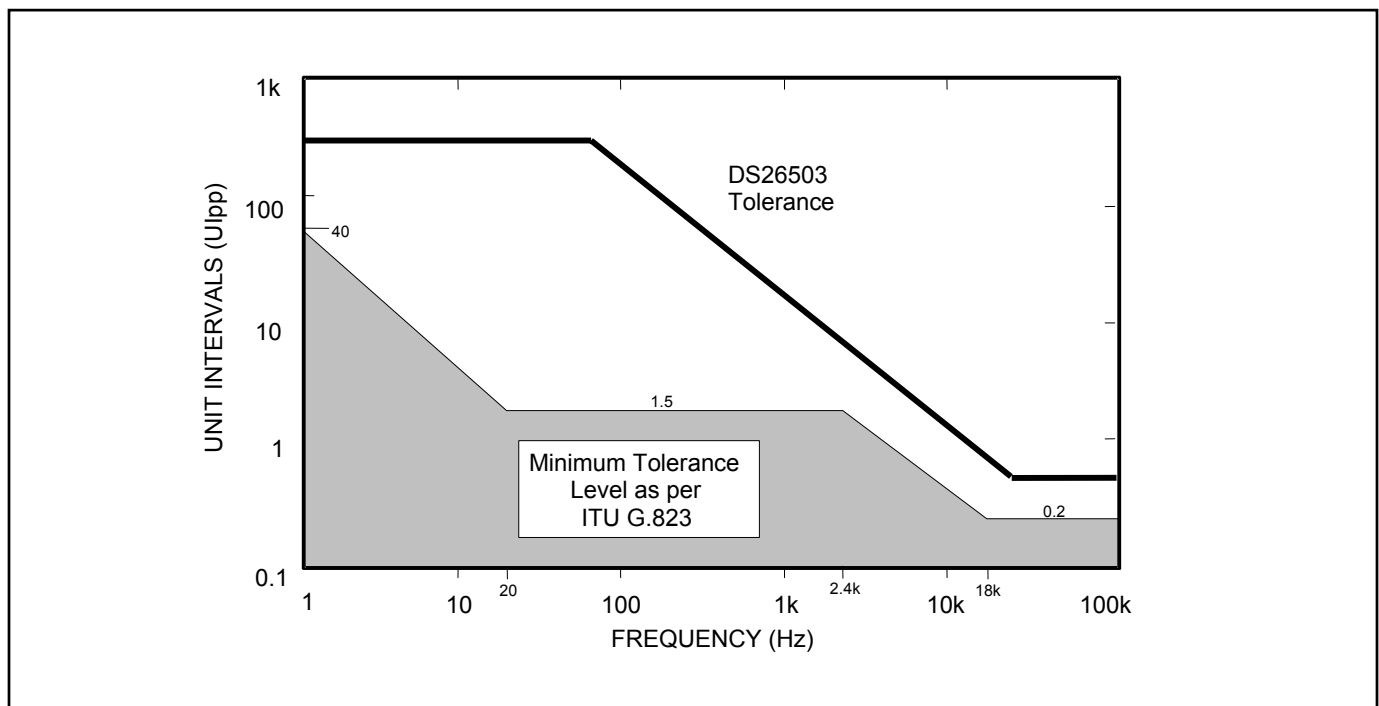
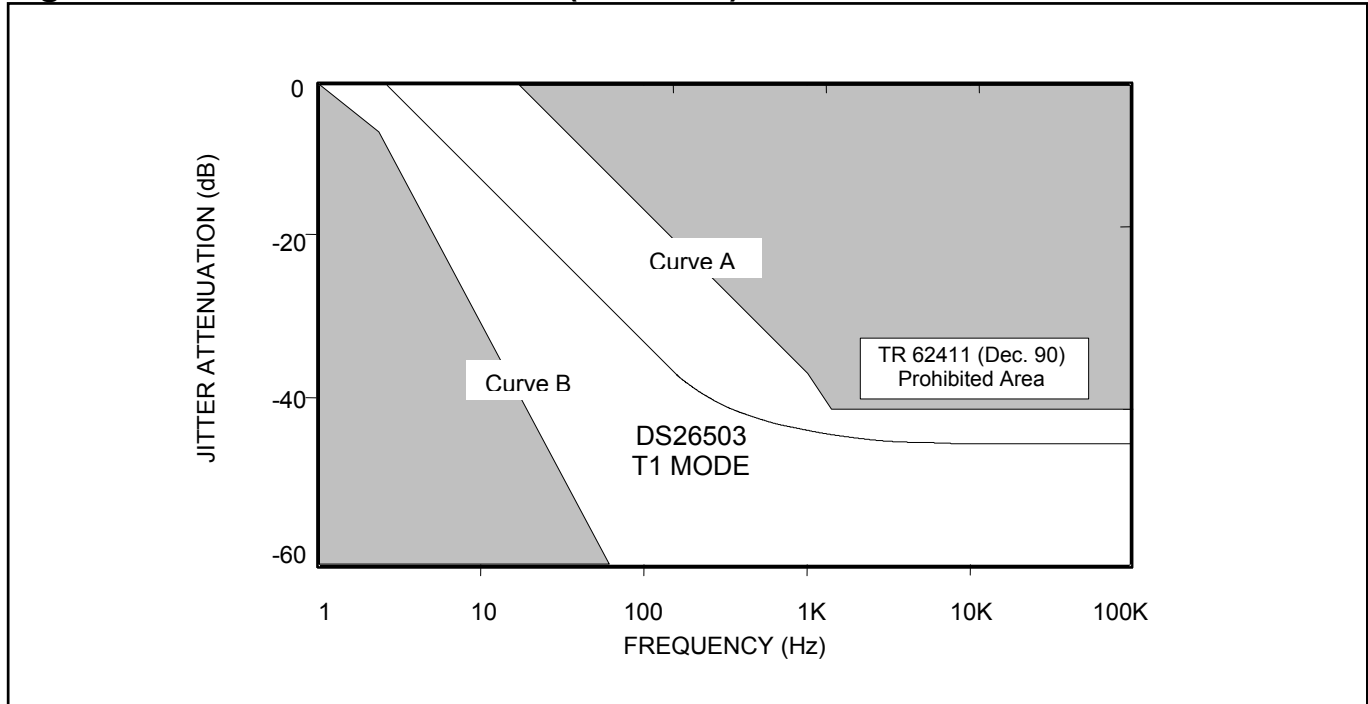
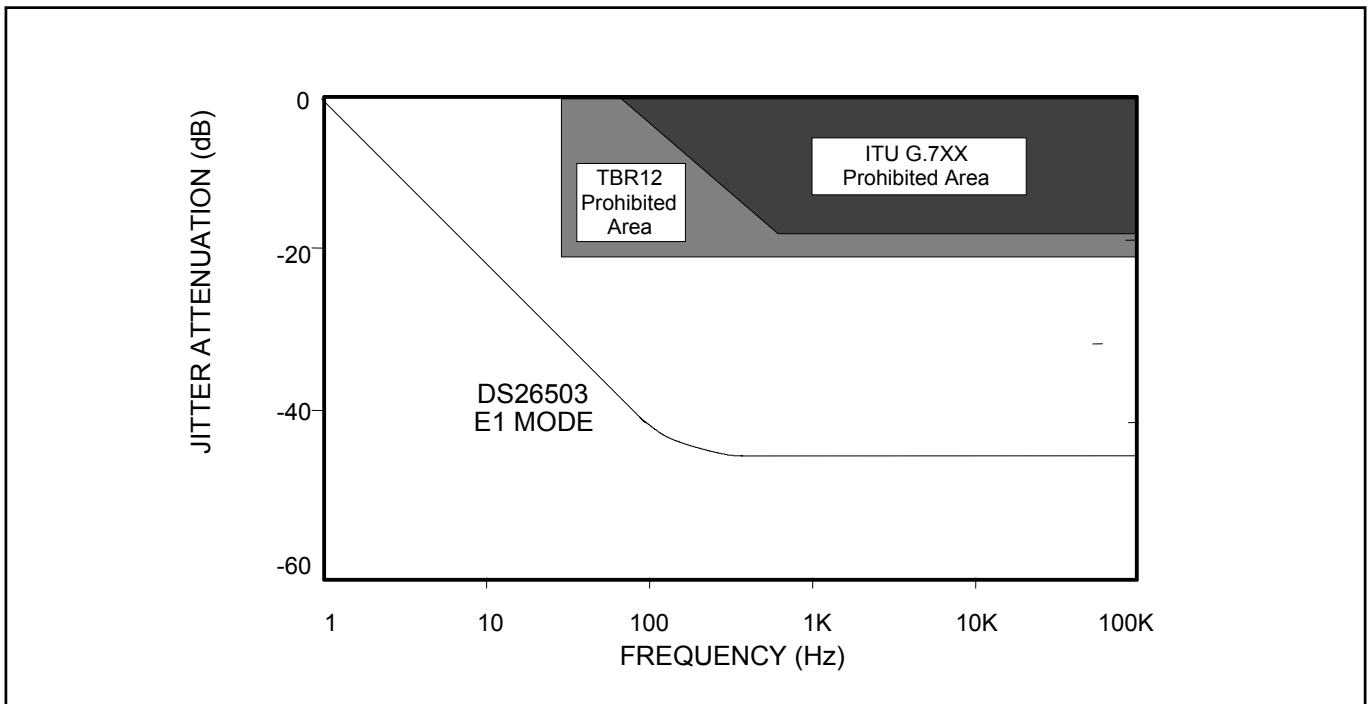
Figure 13-8. Jitter Tolerance (T1 Mode)**Figure 13-9. Jitter Tolerance (E1 Mode)**

Figure 13-10. Jitter Attenuation (T1 Mode)**Figure 13-11. Jitter Attenuation (E1 Mode)**

14. LOOPBACK CONFIGURATION

Register Name: **LBCR**
 Register Description: **Loopback Control Register**
 Register Address: **20h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|-----|---------------|---|---|
| Name | — | — | — | — | LLB | RLB | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| HW Mode | 0 | 0 | 0 | 0 | 0 | RLB PIN 60 | 0 | 0 |

Bits 0, 1, 4 to 7: Unused, must be set = 0 for proper operation.

Bit 2: Remote Loopback (RLB). In this loopback, data received at RTIP and RRING will be looped back to the transmit LIU. Received data will continue to pass through the receive side framer of the DS26503 as it would normally and the data from the transmit side formatter will be ignored.

0 = loopback disabled

1 = loopback enabled

Bit 3: Local Loopback (LLB). In this loopback, data will continue to be transmitted as normal through the transmit side of the DS26503. Data being received at RTIP and RRING will be replaced with the data being transmitted. Data in this loopback will pass through the jitter attenuator if enabled.

0 = loopback disabled

1 = loopback enabled

15. 6312kHz SYNCHRONIZATION INTERFACE

The DS26503 has a 6312kHz Synchronization Interface mode of operation that conforms with Appendix II.2 of G.703, with the exception that the DS26503 transmits a square wave as opposed to the sine wave that is defined in the G.703 specification.

15.1 Receive 6312kHz Synchronization Interface Operation

On the receive interface, a 6312kHz sine wave is accepted conforming to the input port requirements of G.703 Appendix II. Alternatively, a 6312kHz square wave will also be accepted. A 6312kHz square wave is output on RCLK in the receive direction. RS is not driven in this mode and will be three-stated.

Table 15-1. Specification of 6312kHz Clock Signal at Input Port

| | |
|-----------------|---|
| Frequency | 6312kHz |
| Signal format | Sinusoidal wave |
| Alarm condition | Alarm should not be occurred against the amplitude ranged -16dBm to +3dBm |

15.2 Transmit 6312kHz Synchronization Interface Operation

On the transmit interface, a nominally 50% duty cycle, 6312kHz square wave at standard logic levels is available from the PLL_OUT pin. In normal operation, the TCLKO pin will output the same signal. However, if remote loopback is enabled then TCLKO will be replaced with the recovered receive clock. See [Figure 3-1](#). The G.703 requirements for the 6312kHz transmitted signal are shown in [Table 15-2](#). The user must provide an external circuit to convert the TCLKO or PLL_OUT signal to the level and impedance required by G.703. The RSER and TS pins are ignored in this mode. TTIP and TRING will be three-stated in this mode.

Table 15-2. Specification of 6312kHz Clock Signal at Output Port

| | |
|--------------------|--------------------|
| Frequency | 6312kHz |
| Load impedance | 75Ω resistive |
| Transmission media | Coaxial pair cable |
| Amplitude | 0dBm ± 3dBm |

16. JTAG BOUNDARY SCAN ARCHITECTURE AND TEST ACCESS PORT

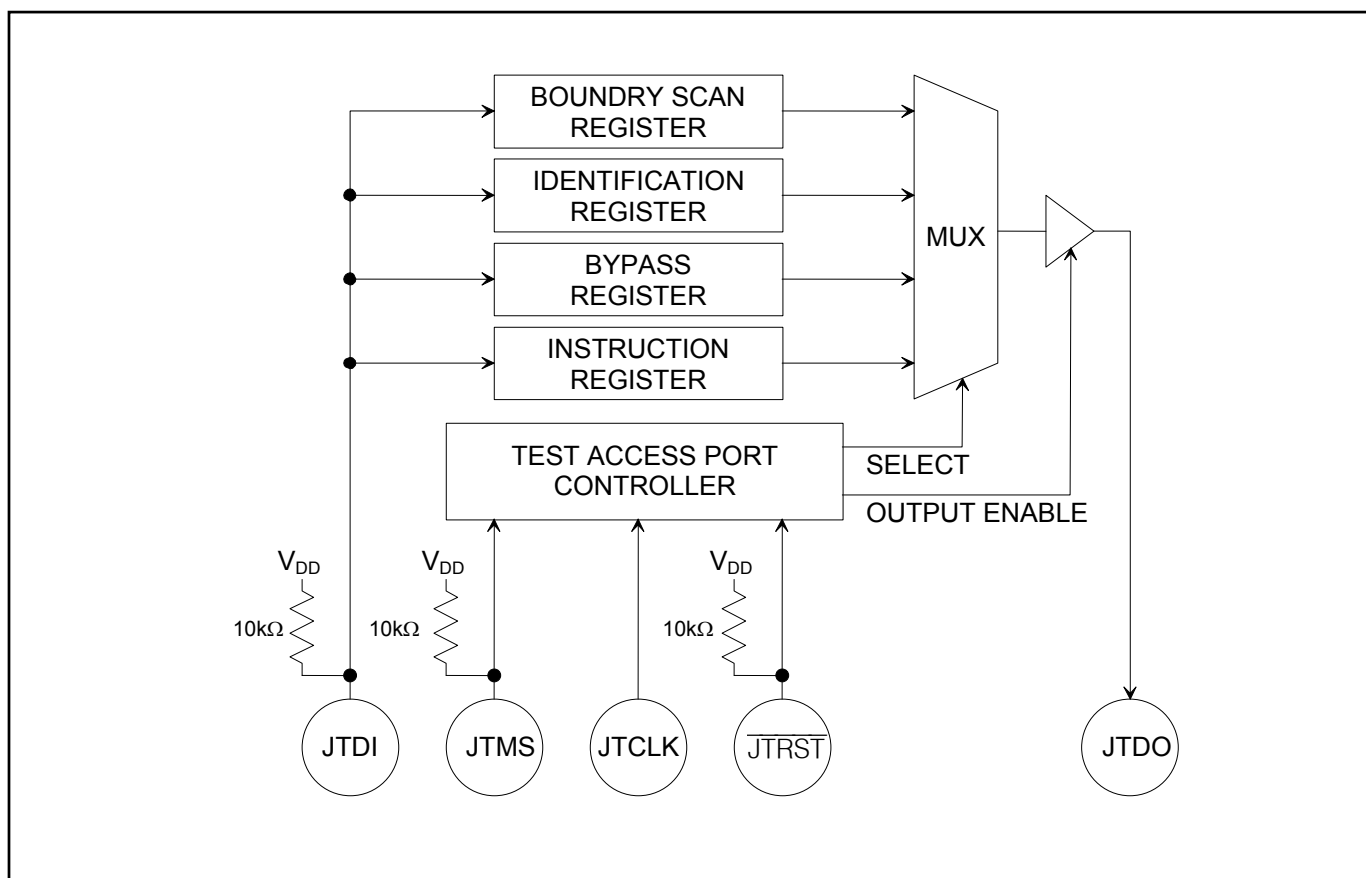
The DS26503 supports the standard IEEE 1149.1 instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. The DS26503 contains the following as required by IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

- Test Access Port (TAP)
- TAP Controller
- Instruction Register
- Bypass Register
- Boundary Scan Register
- Device Identification Register

Details on Boundary Scan Architecture and the Test Access Port can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

The Test Access Port has the necessary interface pins: $\overline{\text{JTRST}}$, JTCLK, JTMS, JTDI, and JTDO. See the pin descriptions for details.

Figure 16-1. JTAG Functional Block Diagram



TAP Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. See [Figure 16-2](#).

Test-Logic-Reset

Upon power-up, the TAP controller will be in the test-logic-reset state. The instruction register will contain the IDCODE instruction. All system logic of the device will operate normally.

Run-Test-Idle

The run-test-idle is used between scan operations or during specific tests. The instruction register and test registers will remain idle.

Select-DR-Scan

All test registers retain their previous state. With JTMS LOW, a rising edge of JTCLK moves the controller into the capture-DR state and will initiate a scan sequence. JTMS HIGH during a rising edge on JTCLK moves the controller to the select-IR-scan state.

Capture-DR

Data can be parallel-loaded into the test-data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register will remain at its current value. On the rising edge of JTCLK, the controller will go to the shift-DR state if JTMS is LOW or it will go to the exit1-DR state if JTMS is HIGH.

Shift-DR

The test-data register selected by the current instruction will be connected between JTDI and JTDO and will shift data one stage toward its serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it will maintain its previous state.

Exit1-DR

While in this state, a rising edge on JTCLK will put the controller in the update-DR state, which terminates the scanning process, if JTMS is HIGH. A rising edge on JTCLK with JTMS LOW will put the controller in the pause-DR state.

Pause-DR

Shifting of the test registers is halted while in this state. All test registers selected by the current instruction will retain their previous state. The controller will remain in this state while JTMS is LOW. A rising edge on JTCLK with JTMS HIGH will put the controller in the exit2-DR state.

Exit2-DR

A rising edge on JTCLK with JTMS HIGH while in this state will put the controller in the update-DR state and terminate the scanning process. A rising edge on JTCLK with JTMS LOW will enter the shift-DR state.

Update-DR

A falling edge on JTCLK while in the update-DR state will latch the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register.

Select-IR-Scan

All test registers retain their previous state. The instruction register will remain unchanged during this state. With JTMS LOW, a rising edge on JTCLK moves the controller into the capture-IR state and will initiate a scan sequence for the instruction register. JTMS HIGH during a rising edge on JTCLK puts the controller back into the test-logic-reset state.

Capture-IR

The capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is HIGH on the rising edge of JTCLK, the controller will enter the exit1-IR state. If JTMS is LOW on the rising edge of JTCLK, the controller will enter the shift-IR state.

Shift-IR

In this state, the shift register in the instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK toward the serial output. The parallel register as well as all test registers remain at their previous states. A rising edge on JTCLK with JTMS HIGH will move the controller to the exit1-IR state. A rising edge on JTCLK with JTMS LOW will keep the controller in the shift-IR state while moving data one stage thorough the instruction shift register.

Exit1-IR

A rising edge on JTCLK with JTMS LOW will put the controller in the pause-IR state. If JTMS is HIGH on the rising edge of JTCLK, the controller will enter the update-IR state and terminate the scanning process.

Pause-IR

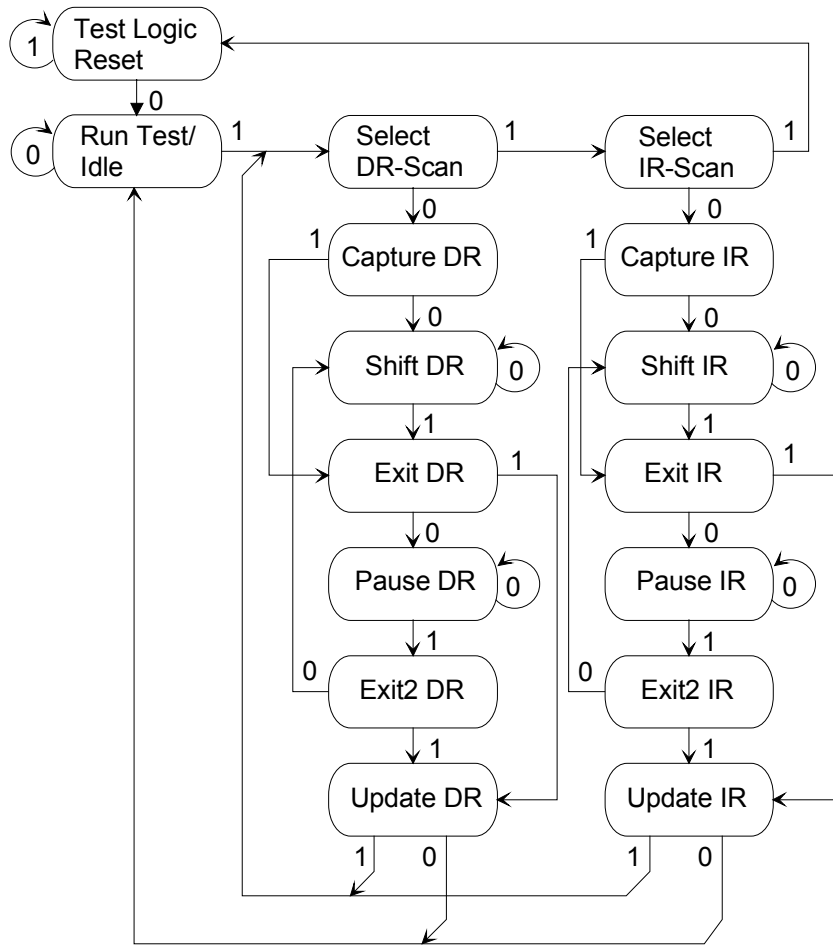
Shifting of the instruction shift register is halted temporarily. With JTMS HIGH, a rising edge on JTCLK will put the controller in the exit2-IR state. The controller will remain in the pause-IR state if JTMS is LOW during a rising edge on JTCLK.

Exit2-IR

A rising edge on JTCLK with JTMS LOW will put the controller in the update-IR state. The controller will loop back to shift-IR if JTMS is HIGH during a rising edge of JTCLK in this state.

Update-IR

The instruction code shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS LOW puts the controller in the run-test-idle state. With JTMS HIGH, the controller will enter the select-DR-scan state.

Figure 16-2. TAP Controller State Diagram

16.1 Instruction Register

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the shift-IR state, the instruction shift register will be connected between JTDI and JTDO. While in the shift-IR state, a rising edge on JTCLK with JTMS LOW will shift the data one stage toward the serial output at JTDO. A rising edge on JTCLK in the exit1-IR state or the exit2-IR state with JTMS HIGH will move the controller to the update-IR state. The falling edge of that same JTCLK will latch the data in the instruction shift register to the instruction parallel output.

Table 16-1. Instruction Codes for IEEE 1149.1 Architecture

| INSTRUCTION | SELECTED REGISTER | INSTRUCTION CODES |
|----------------|-----------------------|-------------------|
| SAMPLE/PRELOAD | Boundary Scan | 010 |
| BYPASS | Bypass | 111 |
| EXTEST | Boundary Scan | 000 |
| CLAMP | Bypass | 011 |
| HIGHZ | Bypass | 100 |
| IDCODE | Device Identification | 001 |

SAMPLE/PRELOAD

This is a mandatory instruction for the IEEE 1149.1 specification that supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device by using the capture-DR state. SAMPLE/PRELOAD also allows the device to shift data into the boundary scan register via JTDI using the shift-DR state.

BYPASS

When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the one-bit bypass test register. This allows data to pass from JTDI to JTDO not affecting the device's normal operation.

EXTEST

This allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins will be driven. The boundary scan register will be connected between JTDI and JTDO. The Capture-DR will sample all digital inputs into the boundary scan register.

CLAMP

All digital outputs of the device will output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs will not change during the CLAMP instruction.

HIGHZ

All digital outputs of the device will be placed in a high-impedance state. The BYPASS register will be connected between JTDI and JTDO.

IDCODE

When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code will be loaded into the identification register on the rising edge of JTCLK following entry into the capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO. During test-logic-reset, the identification code is forced into the instruction register's parallel output. The ID code will always have a 1 in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version [Table 16-2](#). [Table 16-3](#) lists the device ID codes.

Table 16-2. ID Code Structure

| MSB | | | LSB |
|----------------------------|-----------|-------------|-----|
| Version Contact Factory | Device ID | JEDEC | 1 |
| 4 bits | 16 bits | 00010100001 | 1 |

Table 16-3. Device ID Codes

| DEVICE | 16-BIT ID |
|---------|-----------|
| DS26503 | 0035h |

16.2 Test Registers

IEEE 1149.1 requires a minimum of two test registers: the bypass register and the boundary scan register. An optional test register has been included with the DS26503 design. This test register is the identification register and is used with the IDCODE instruction and the test-logic-reset state of the TAP controller.

16.2.1 Boundary Scan Register

This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells and is n bits in length. See for all the cell bit locations and definitions.

16.2.2 Bypass Register

This is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions that provides a short path between JTDI and JTDO.

16.2.3 Identification Register

The identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the test-logic-reset state.

Table 16-4. Boundary Scan Control Bits

| CELL # | NAME | TYPE | CONTROL CELL |
|--------|------------|--------------|--------------|
| 0 | AD1 | Output3 | 1 |
| 1 | AD1_7_CTRL | Controlr | |
| 2 | AD0 | Output3 | 3 |
| 3 | AD0_CTRL | Controlr | |
| 4 | WR_RW | observe_only | |
| 5 | RD_DS | observe_only | |
| 6 | CS | observe_only | |
| 7 | BIS1 | observe_only | |
| 8 | BIS0 | observe_only | |
| 9 | BTS | observe_only | |
| 10 | THZE | observe_only | |
| 11 | TMODE1 | observe_only | |
| 12 | TMODE2 | observe_only | |
| 13 | PLL_CLK | observe_only | |
| 14 | INT | Output3 | 15 |
| 15 | INT_CTRL | Controlr | |
| 16 | TSTRST | observe_only | |
| 17 | RLOS | observe_only | |
| 18 | TCSS1 | observe_only | |
| 19 | RLOF | observe_only | |
| 20 | RAIS | observe_only | |
| 21 | RSER | observe_only | |
| 22 | OUT_400HZ* | observe_only | |
| 23 | RS | observe_only | |
| 24 | RCLK | observe_only | |
| 25 | TS | Output3 | 26 |
| 26 | TS_CTRL | Controlr | |
| 27 | TSER | observe_only | |
| 28 | TPOSO | observe_only | |

| CELL # | NAME | TYPE | CONTROL CELL |
|--------|--------|--------------|--------------|
| 29 | TNEGO | observe_only | |
| 30 | TCLKO | observe_only | |
| 31 | TCLK | observe_only | |
| 32 | ALE_A7 | observe_only | |
| 33 | A6 | observe_only | |
| 34 | A5 | observe_only | |
| 35 | A4 | observe_only | |
| 36 | A3 | observe_only | |
| 37 | A2 | observe_only | |
| 38 | A1 | observe_only | |
| 39 | A0 | observe_only | |
| 40 | AD7 | Output3 | 1 |
| 41 | AD6 | Output3 | 1 |
| 42 | AD5 | Output3 | 1 |
| 43 | AD4 | Output3 | 1 |
| 44 | AD3 | Output3 | 1 |
| 45 | AD2 | Output3 | 1 |

** This pin is not bonded out on the DS26503 package, however, it must be accounted for in the chain.*

17. FUNCTIONAL TIMING DIAGRAMS

17.1 Processor Interface

17.1.1 Parallel Port Mode

See the *AC Timing* section.

17.1.2 SPI Serial Port Mode

Figure 17-1. SPI Serial Port Access, Read Mode, CPOL = 0, CPHA = 0

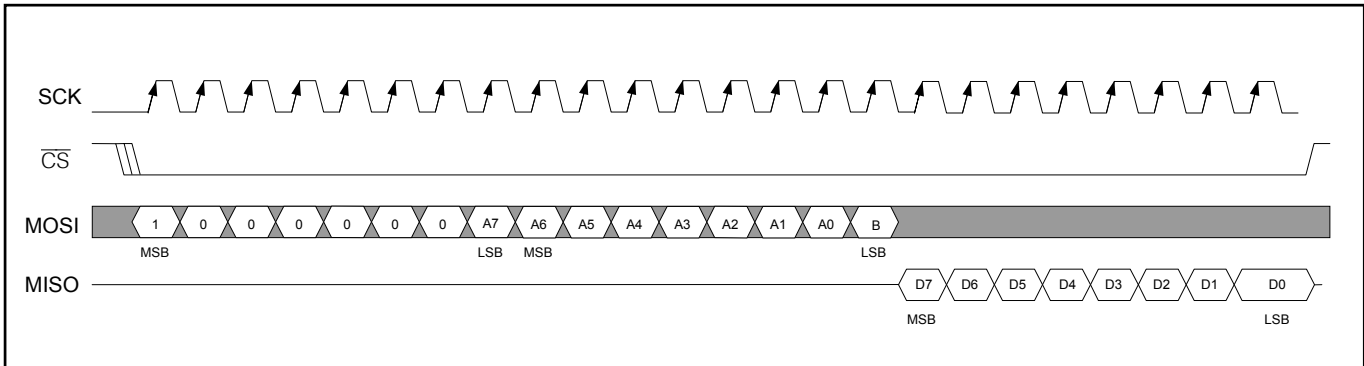


Figure 17-2. SPI Serial Port Access, Read Mode, CPOL = 1, CPHA = 0

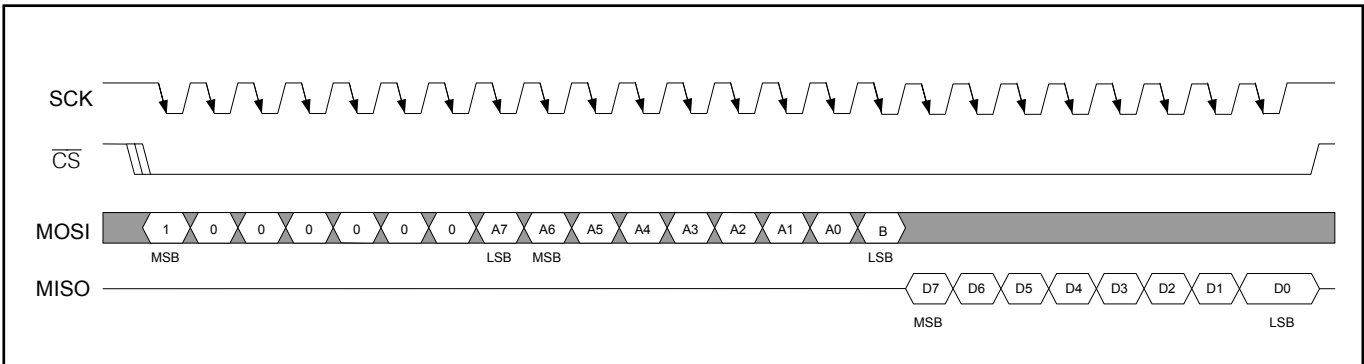


Figure 17-3. SPI Serial Port Access, Read Mode, CPOL = 0, CPHA = 1

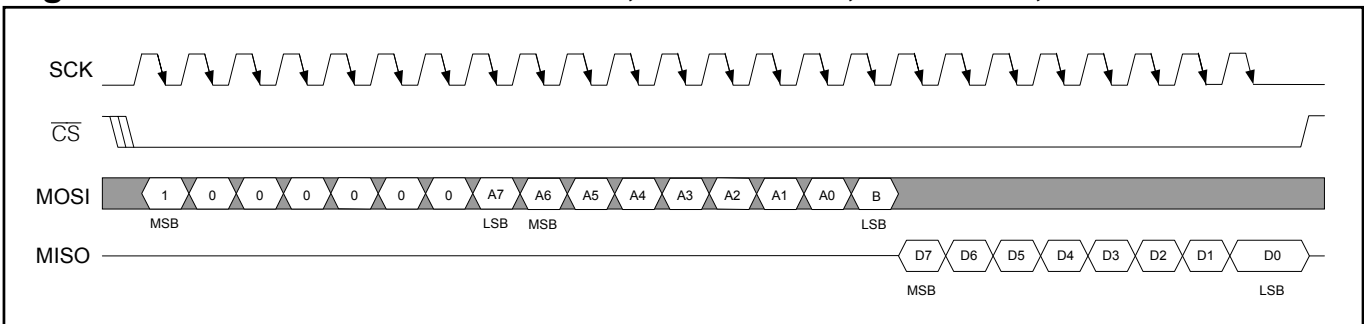


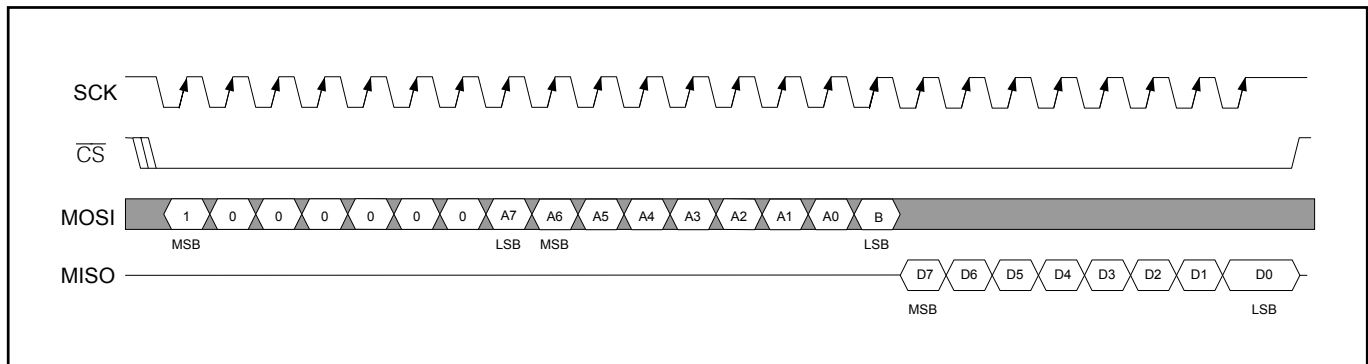
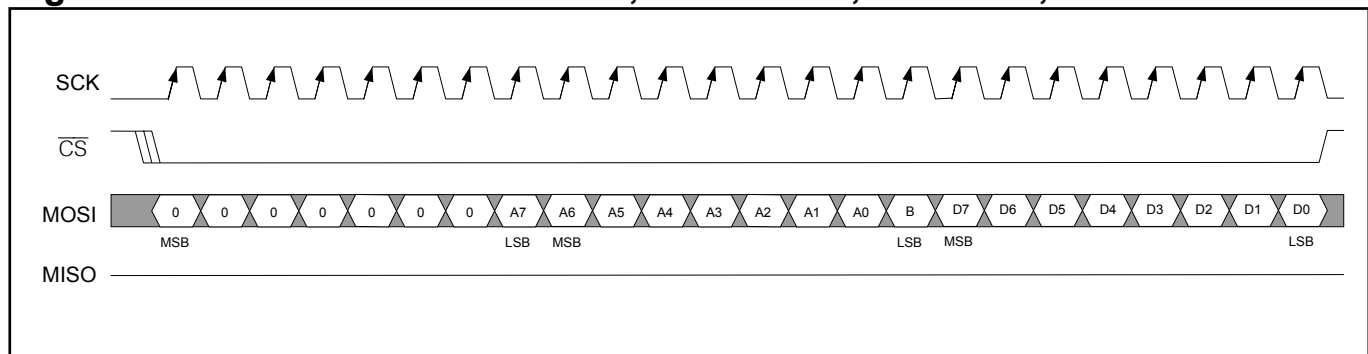
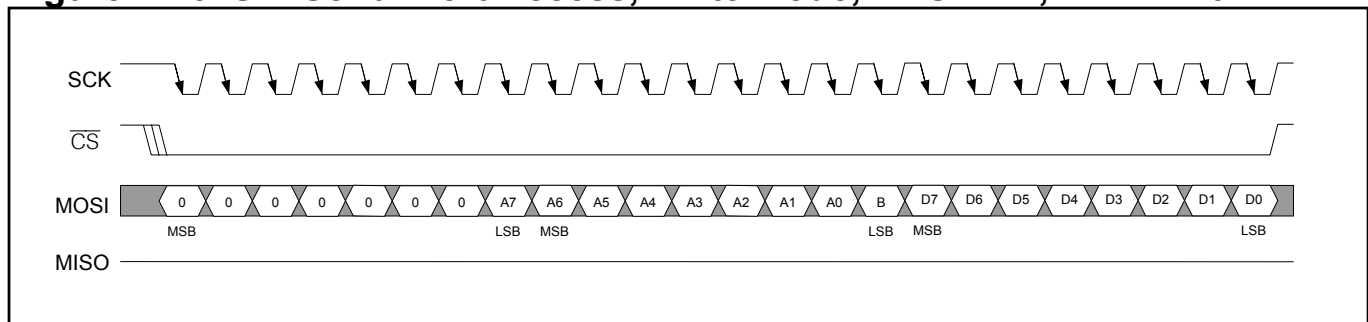
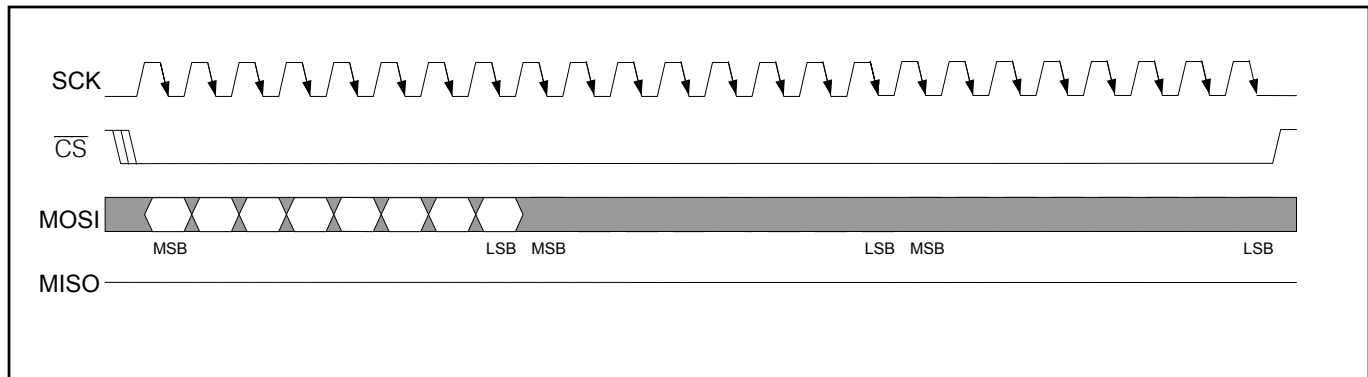
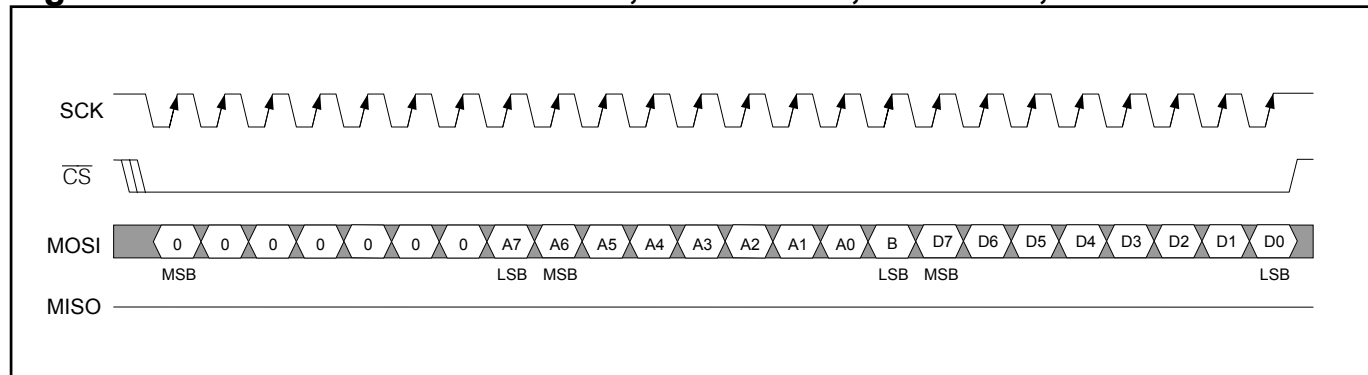
Figure 17-4. SPI Serial Port Access, Read Mode, CPOL = 1, CPHA = 1**Figure 17-5. SPI Serial Port Access, Write Mode, CPOL = 0, CPHA = 0****Figure 17-6. SPI Serial Port Access, Write Mode, CPOL = 1, CPHA = 0**

Figure 17-7. SPI Serial Port Access, Write Mode, CPOL = 0, CPHA = 1**Figure 17-8. SPI Serial Port Access, Write Mode, CPOL = 1, CPHA = 1**

18. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground.....-1.0V to +6.0V
 Operating Temperature Range for DS26503L.....0°C to +70°C
 Operating Temperature Range for DS26503LN.....-40°C to +85°C (**Note 1**)
 Storage Temperature Range.....-55°C to +125°C
 Soldering Temperature.....See IPC/JEDEC J-STD-20 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

Note 1: Specifications to -40°C are guaranteed by design (GBD) and not production tested.

Table 18-1. Thermal Characteristics

| PARAMETER | MIN | TYP | MAX | NOTES |
|---|-------|-----------|--------|-------|
| Ambient Temperature | -40°C | | +85°C | 2 |
| Junction Temperature | | | +125°C | |
| Theta-JA (θ_{JA}) in Still Air | | +46.3°C/W | | 3 |

Table 18-2. Theta-JA (θ_{JA}) vs. Airflow

| FORCED AIR (meters per second) | THETA-JA (θ_{JA}) |
|-----------------------------------|----------------------------|
| 0 | +45.3°C/W |
| 1 | +37.2°C/W |
| 2.5 | +34.4°C/W |

Note 2: The package is mounted on a four-layer JEDEC standard test board.

Note 3: Theta-JA (θ_{JA}) is the junction-to-ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board.

Table 18-3. Recommended DC Operating Conditions

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ for DS26503L; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for DS26503LN.)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|-----------|----------|-------|-----|-------|-------|-------|
| Logic 1 | V_{IH} | 2.0 | | 5.5 | V | 4 |
| Logic 0 | V_{IL} | -0.3 | | +0.8 | V | 4 |
| Supply | V_{DD} | 3.135 | 3.3 | 3.465 | V | 5 |

Note 4: Guaranteed by design (GBD).

Note 5: Applies to RVDD, TVDD, and DVDD.

Table 18-4. Capacitance

($T_A = +25^\circ\text{C}$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|--------------------|-----------|-----|-----|-----|-------|-------|
| Input Capacitance | C_{IN} | | 5 | | pF | |
| Output Capacitance | C_{OUT} | | 7 | | pF | |

Table 18-5. DC Characteristics

($V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ for DS26503L; $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS26503LN.)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|-----------------------|----------|------|-----|------|---------|-------|
| Supply Current | I_{DD} | | 85 | 150 | mA | |
| Input Leakage | I_{IL} | -1.0 | | +1.0 | μA | 6 |
| Output Leakage | I_{LO} | | | 1.0 | μA | 7 |
| Output Current (2.4V) | I_{OH} | -1.0 | | | mA | |
| Output Current (0.4V) | I_{OL} | +4.0 | | | mA | |

Note 6: $0.0V < V_{IN} < V_{DD}$

Note 7: Applied to \overline{INT} when three-stated.

19. AC TIMING PARAMETERS AND DIAGRAMS

Capacitive test loads are 40pF for bus signals and 20pF for all others.

19.1 Multiplexed Bus

Table 19-1. AC Characteristics, Multiplexed Parallel Port

($V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ for DS26503L; $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS26503LN.) (Note 1, [Figure 19-1](#), [Figure 19-2](#), and [Figure 19-3](#))

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|------------|-----|-----|-----|-------|-------|
| Cycle Time | t_{CYC} | 200 | | | ns | |
| Pulse Width, \overline{DS} Low or \overline{RD} High | PW_{EL} | 100 | | | ns | |
| Pulse Width, \overline{DS} High or \overline{RD} Low | PW_{EH} | 100 | | | ns | |
| Input Rise/Fall Times | t_R, t_F | | | 20 | ns | |
| R/ \overline{W} Hold Time | t_{RWH} | 10 | | | ns | |
| R/ \overline{W} Setup Time Before \overline{DS} High | t_{RWS} | 50 | | | ns | |
| \overline{CS} Setup Time Before \overline{DS} , \overline{WR} , or \overline{RD} Active | t_{CS} | 20 | | | ns | |
| \overline{CS} Hold Time | t_{CH} | 0 | | | ns | |
| Read-Data Hold Time | t_{DHR} | 10 | | 50 | ns | |
| Write-Data Hold Time | t_{DHW} | 5 | | | ns | |
| Muxed Address Valid to AS or ALE Fall | t_{ASL} | 15 | | | ns | |
| Muxed Address Hold Time | t_{AHL} | 10 | | | ns | |
| Delay Time \overline{DS} , \overline{WR} , or \overline{RD} to AS or ALE Rise | t_{ASD} | 20 | | | ns | |
| Pulse Width AS or ALE High | PW_{ASH} | 30 | | | ns | |
| Delay Time, AS or ALE to \overline{DS} , \overline{WR} , or \overline{RD} | t_{ASED} | 10 | | | ns | |
| Output Data Delay Time from \overline{DS} or \overline{RD} | t_{DDR} | | | 80 | ns | |
| Data Setup Time | t_{DSW} | 50 | | | ns | |

Note 1: The timing parameters listed in this table are guaranteed by design (GBD).

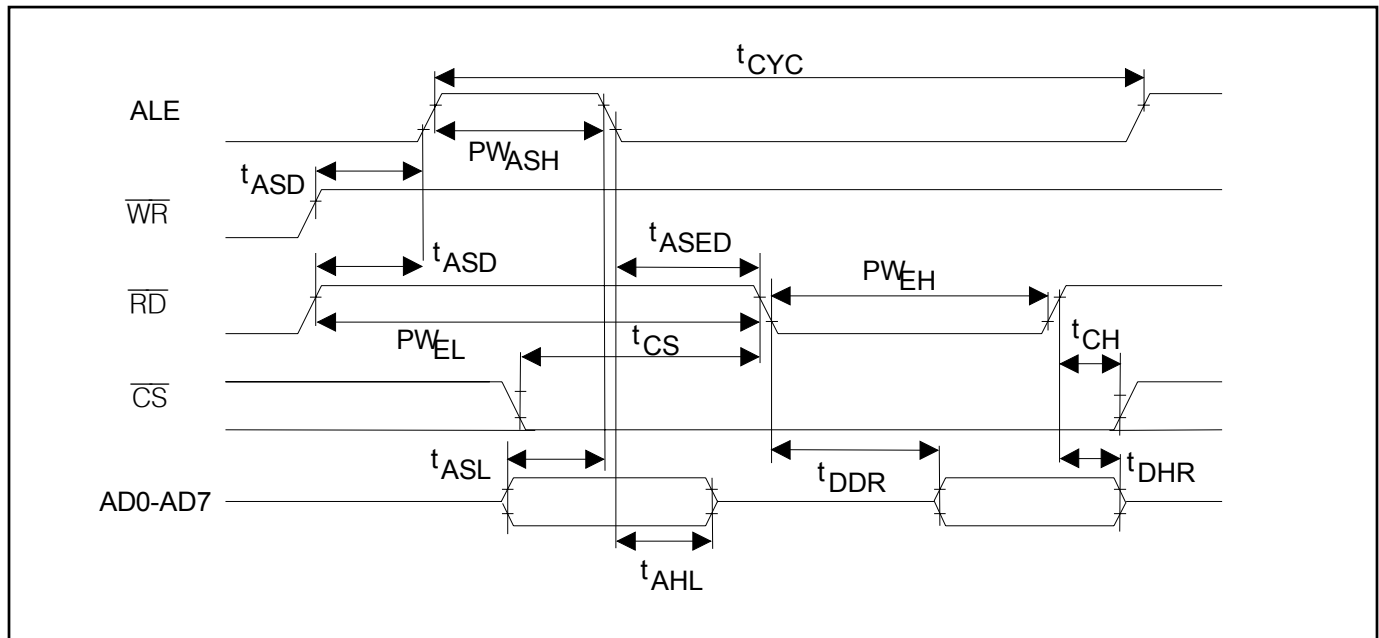
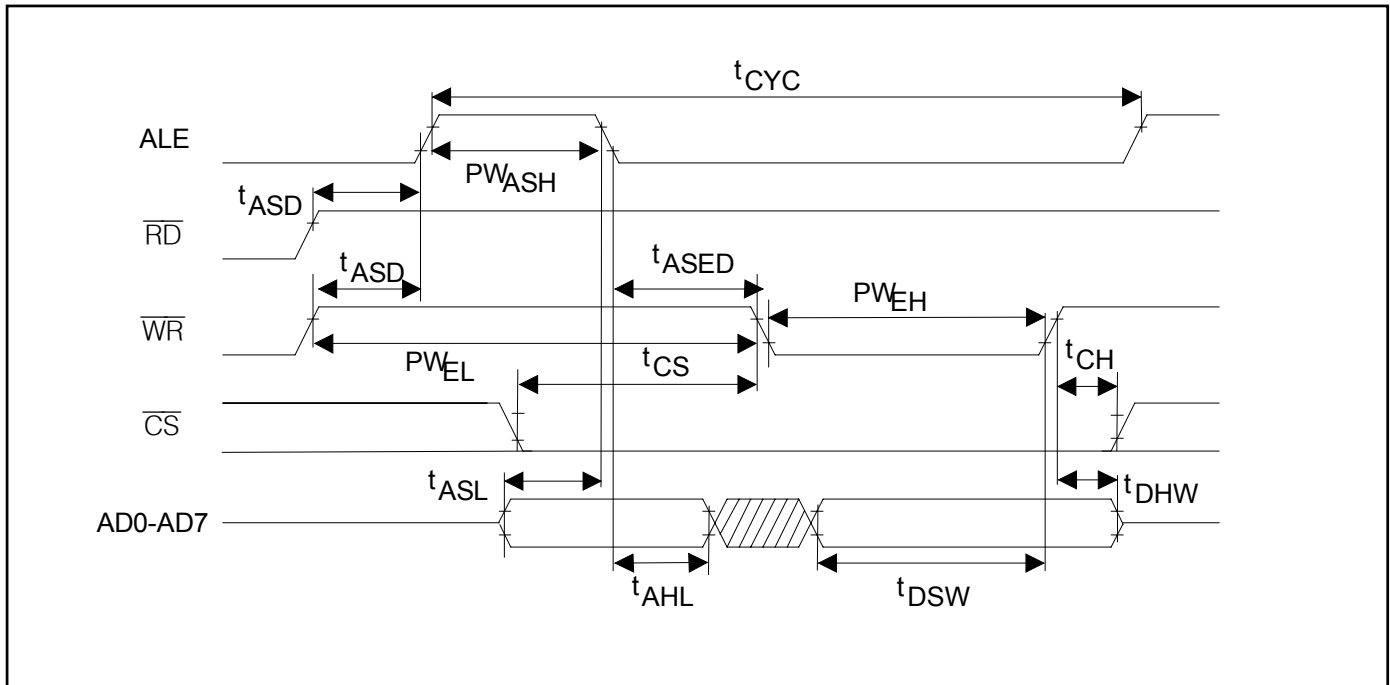
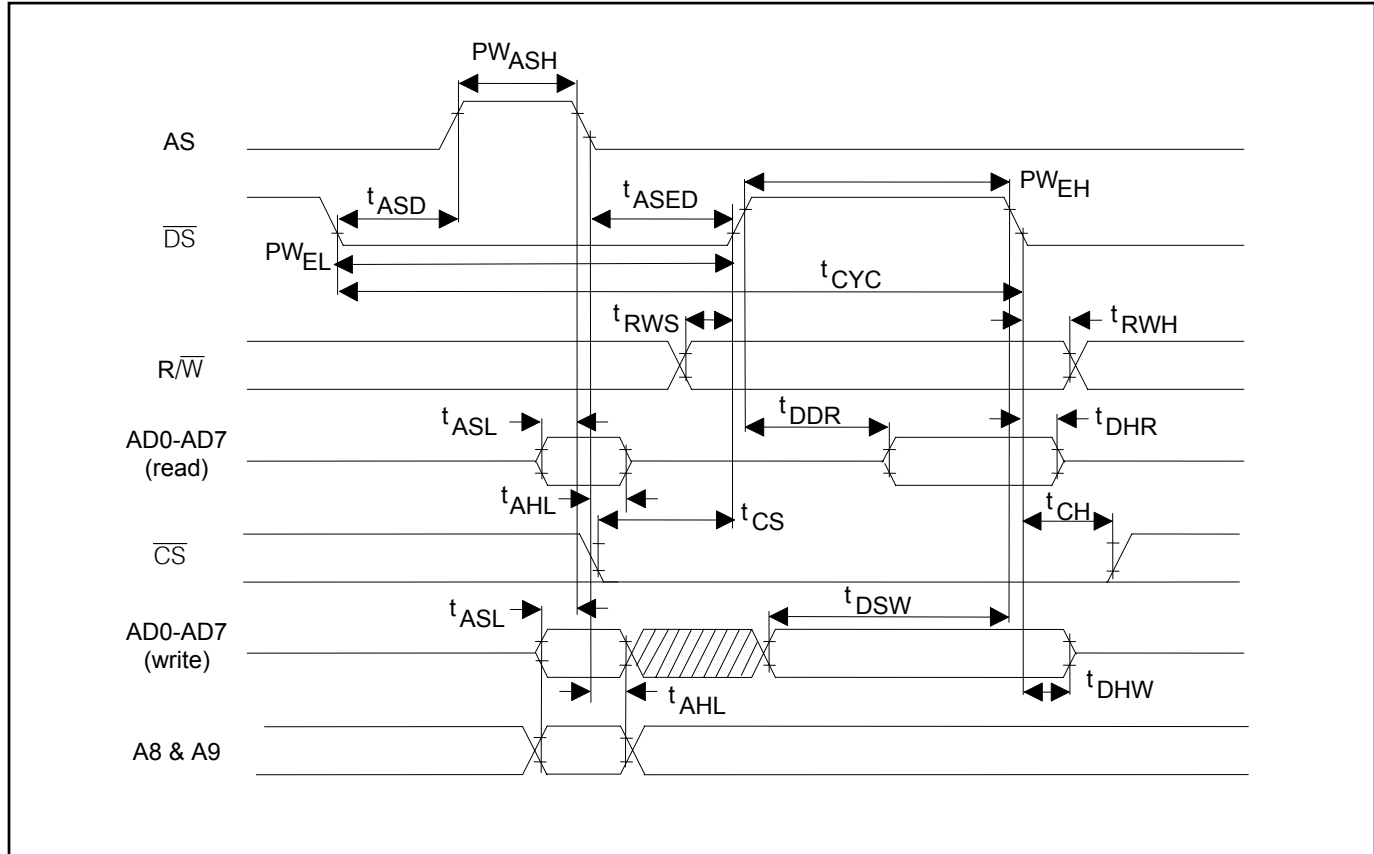
Figure 19-1. Intel Bus Read Timing (BTS = 0 / BIS[1:0] = 00)**Figure 19-2. Intel Bus Write Timing (BTS = 0 / BIS[1:0] = 00)**

Figure 19-3. Motorola Bus Timing (BTS = 1 / BIS[1:0] = 00)

19.2 Nonmultiplexed Bus

Table 19-2. AC Characteristics, Non-Mux Parallel Port

($V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ for DS26503L; $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS26503LN.) (Note 1, [Figure 19-4](#), [Figure 19-5](#), [Figure 19-6](#), and [Figure 19-7](#))

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|--------|-----|-----|-----|-------|-------|
| Setup Time for A0 to A7, Valid to \overline{CS} Active | t1 | 0 | | | ns | |
| Setup Time for \overline{CS} Active to Either \overline{RD} , \overline{WR} , or \overline{DS} Active | t2 | 0 | | | ns | |
| Delay Time from Either \overline{RD} or \overline{DS} Active to Data Valid | t3 | | | 75 | ns | |
| Hold Time from Either \overline{RD} , \overline{WR} , or \overline{DS} Inactive to \overline{CS} Inactive | t4 | 0 | | | ns | |
| Hold Time from \overline{CS} Inactive to Data Bus Three-State | t5 | 5 | | 20 | ns | |
| Wait Time from Either \overline{WR} or \overline{DS} Activate to Latch Data | t6 | 75 | | | ns | |
| Data Setup Time to Either \overline{WR} or \overline{DS} Inactive | t7 | 10 | | | ns | |
| Data Hold Time from Either \overline{WR} or \overline{DS} Inactive | t8 | 10 | | | ns | |
| Address Hold from Either \overline{WR} or \overline{DS} Inactive | t9 | 10 | | | ns | |

Note 1: The timing parameters listed in this table are guaranteed by design (GBD).

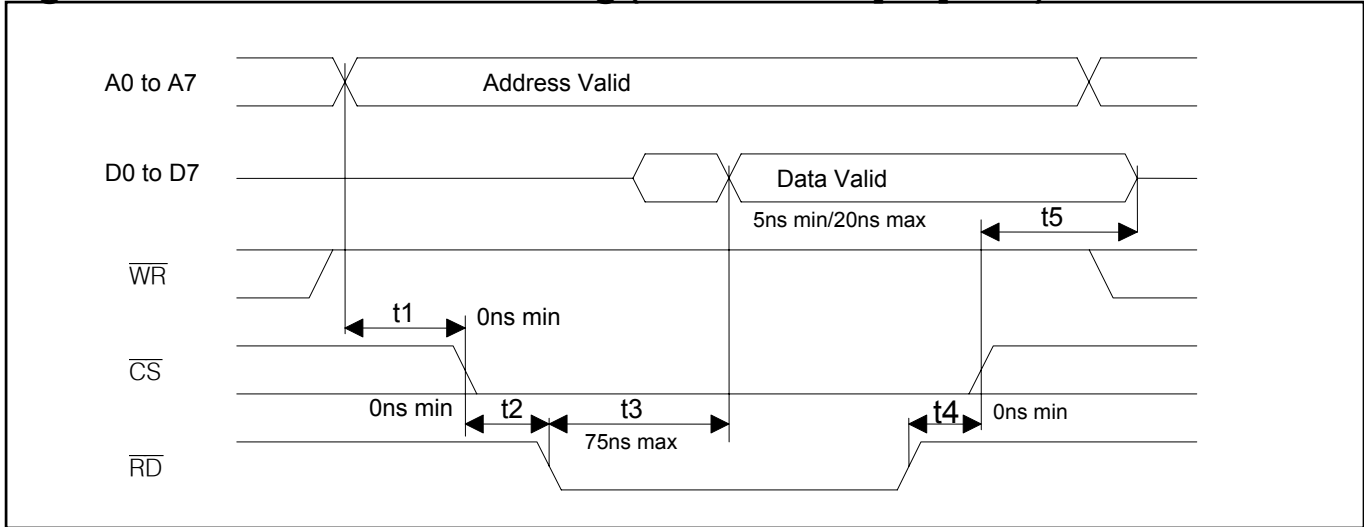
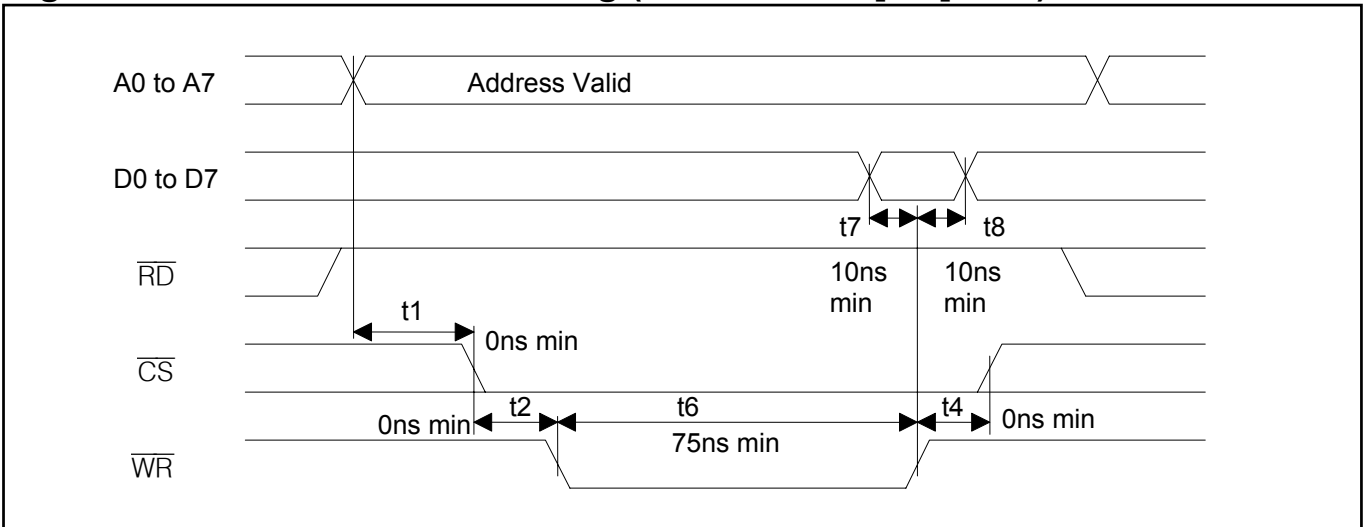
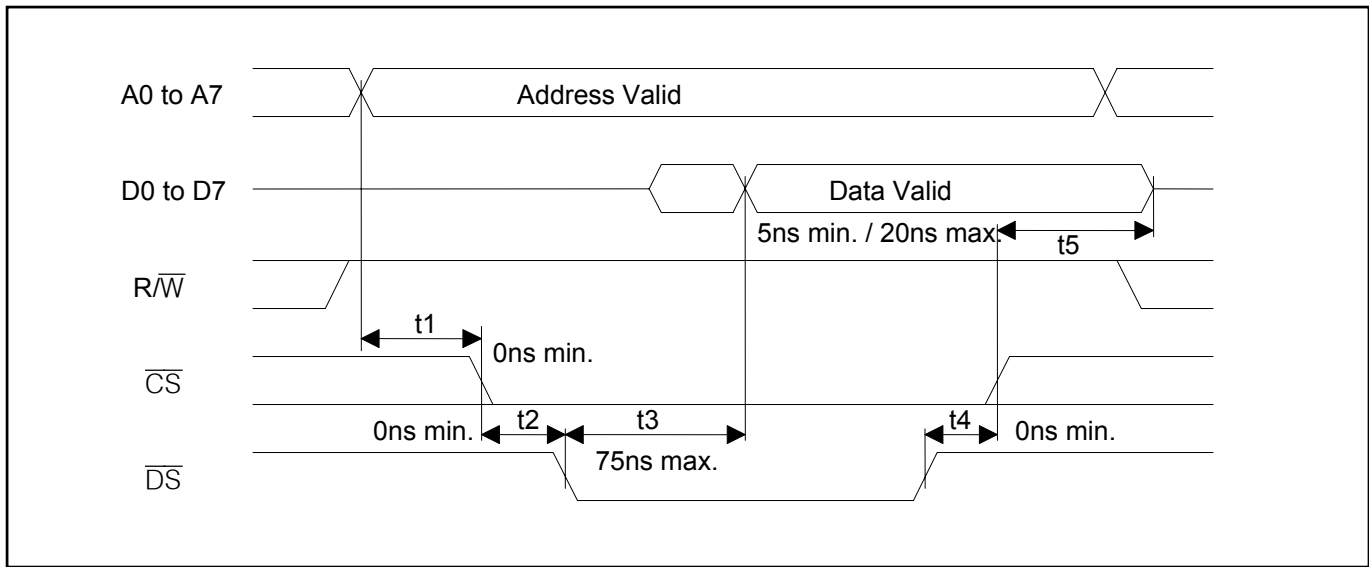
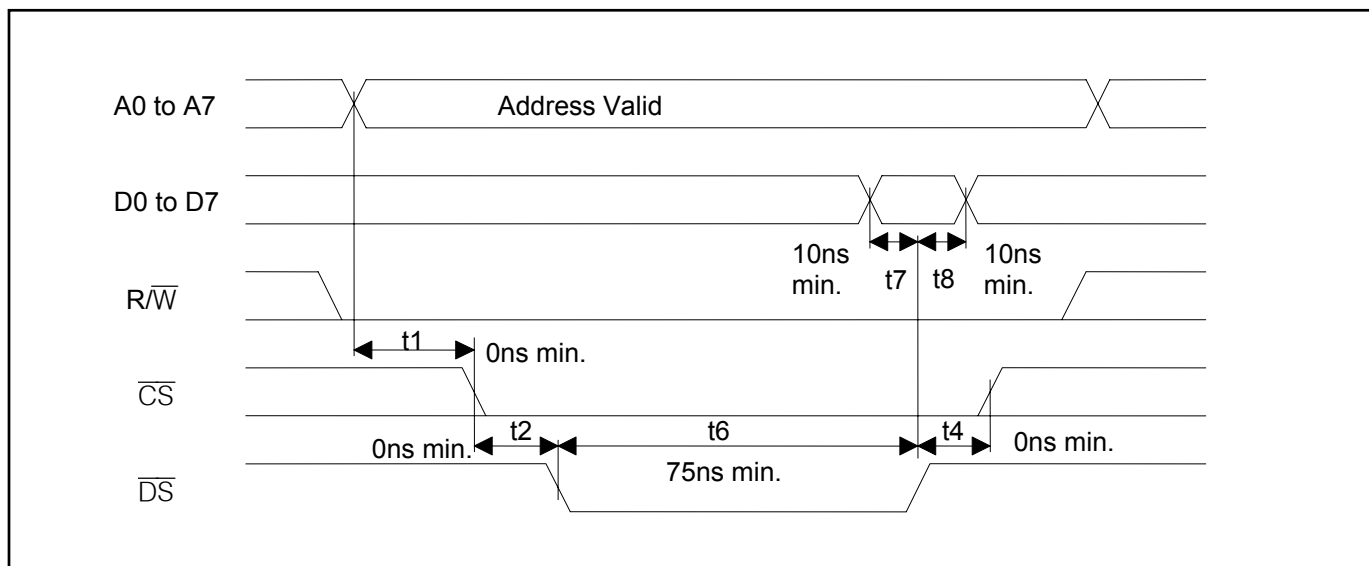
Figure 19-4. Intel Bus Read Timing (BTS = 0 / BIS[1:0] = 01)**Figure 19-5. Intel Bus Write Timing (BTS = 0 / BIS[1:0] = 01)**

Figure 19-6. Motorola Bus Read Timing (BTS = 1 / BIS[1:0] = 01)**Figure 19-7. Motorola Bus Write Timing (BTS = 1 / BIS[1:0] = 01)**

19.3 Serial Bus

Table 19-3. AC Characteristics, Serial Bus

($V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ for DS26503L; $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS26503LN.) (Note 1, [Figure 19-8](#) and [Figure 19-9](#))

| DIAGRAM NUMBER (NOTE 2) | CHARACTERISTIC (NOTE 3) | | SYMBOL | MIN | MAX | UNITS |
|-------------------------------|--|----------|---------------|-----|-----|-------|
| | Operating Frequency Slave | | $f_{BUS(S)}$ | | 10 | MHz |
| 1 | Cycle Time: Slave | | $t_{CYC(S)}$ | 100 | | ns |
| 2 | Enable Lead Time | | $t_{LEAD(S)}$ | 15 | | ns |
| 3 | Enable Lag Time | | $t_{LAG(S)}$ | 15 | | ns |
| 4 | Clock (CLK) High Time Slave | | $t_{CLKH(S)}$ | 50 | | ns |
| 5 | Clock (CLK) Low Time Slave | | $t_{CLKL(S)}$ | 50 | | ns |
| 6 | Data Setup Time (inputs) Slave | | $t_{SU(S)}$ | 5 | | ns |
| 7 | Data Hold Time (inputs) Slave | | $t_{H(S)}$ | 15 | | ns |
| 8 | Access Time, Slave (Note 4) | CPHA = 0 | $t_{A(CP0)}$ | 0 | 40 | ns |
| | | CPHA = 1 | $t_{A(CP1)}$ | 0 | 20 | |
| 9 | Disable Time, Slave (Note 5) | | $t_{DIS(S)}$ | | 25 | ns |
| 10 | Data Valid Time, After Enable Edge Slave (Note 6) | | $t_{V(S)}$ | | 40 | ns |
| 11 | Data Hold Time, Outputs, After Enable Edge Slave | | $t_{HD(S)}$ | 5 | | ns |

Note 1: The timing parameters listed in this table are guaranteed by design (GBD).

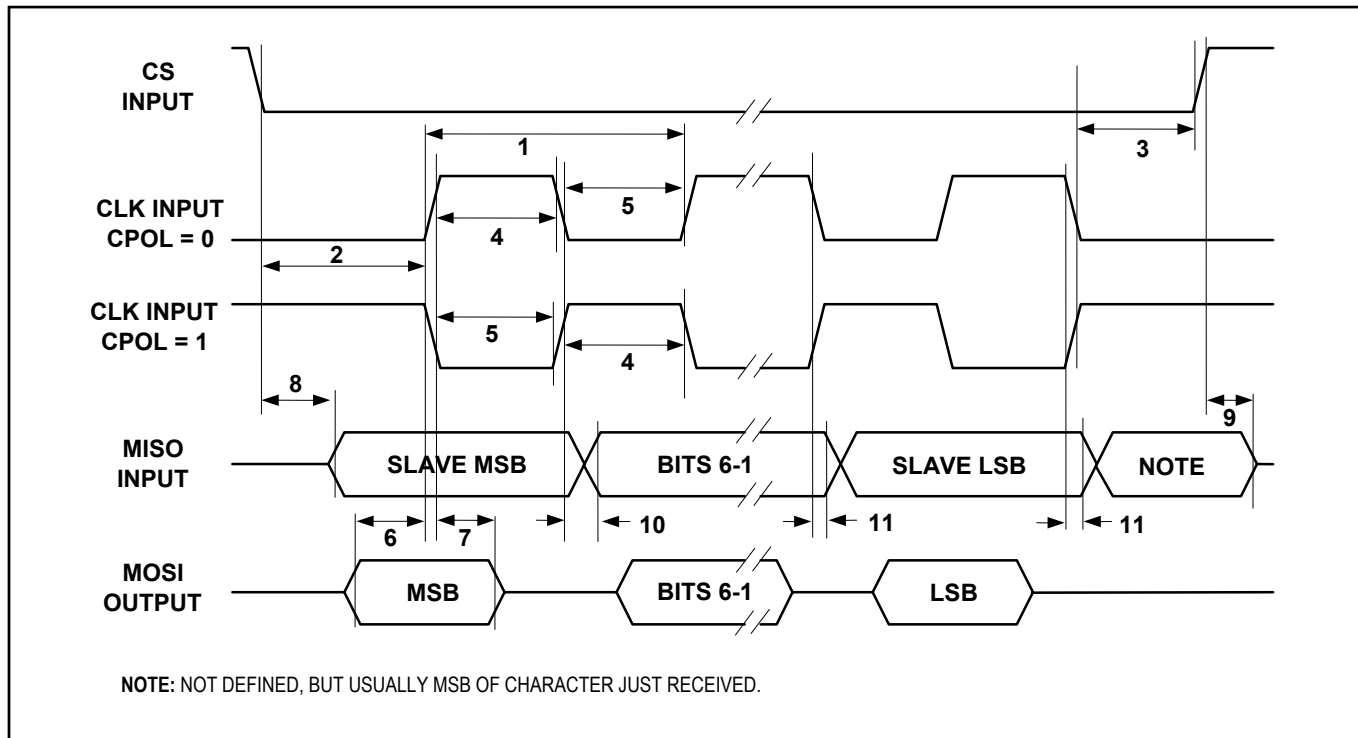
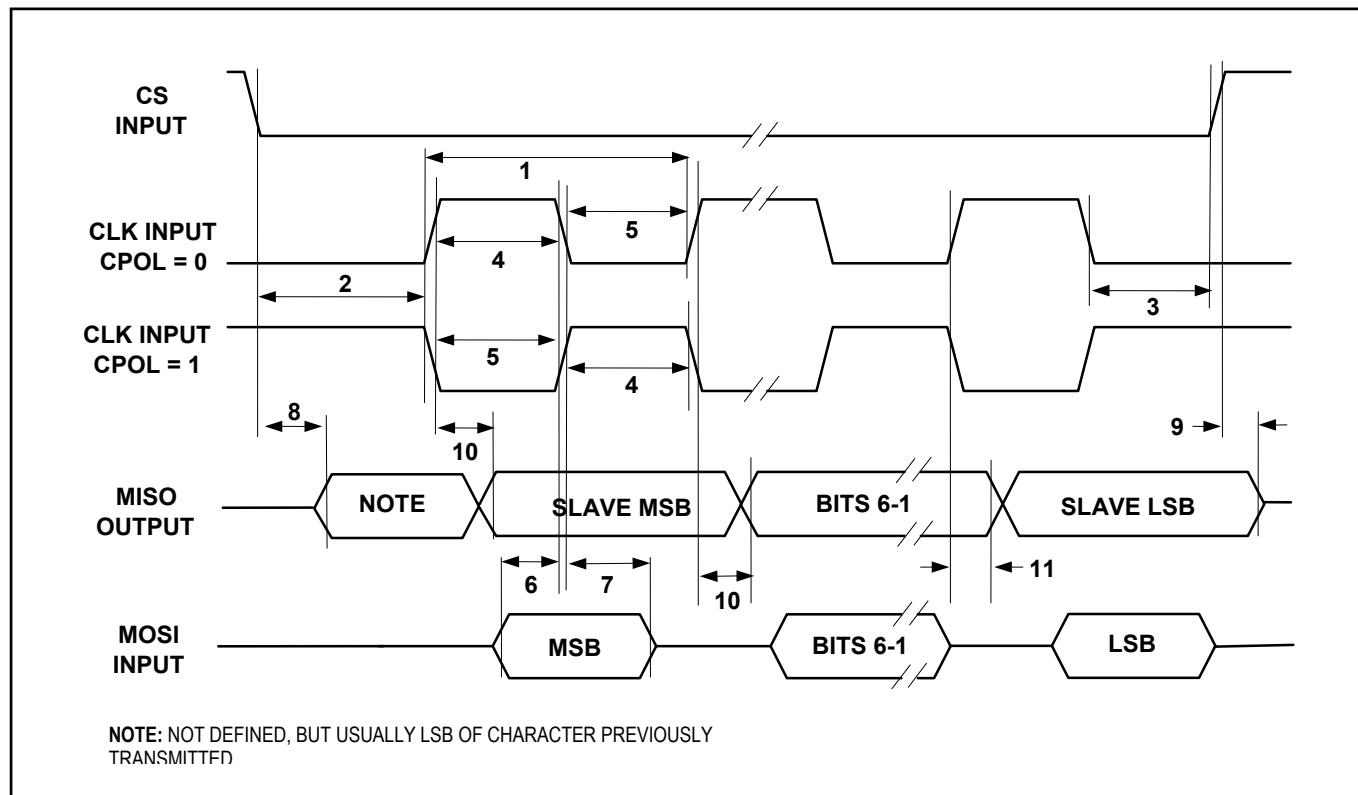
Note 2: Numbers refer to dimensions in the following [Figure 19-8](#) and [Figure 19-9](#).

Note 3: All timing is shown with respect to 20% V_{DD} and 70% V_{DD} , unless otherwise noted. 100pF load on all SPI pins.

Note 4: Time to data active from high-impedance state.

Note 5: Hold time to high-impedance state.

Note 6: With 100pF on all SPI pins.

Figure 19-8. SPI Interface Timing Diagram, CPHA = 0, BIS[1:0] = 10**Figure 19-9. SPI Interface Timing Diagram, CPHA = 1, BIS[1:0] = 10**

19.4 Receive Side AC Characteristics

Table 19-4. Receive Side AC Characteristics

($V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ for DS26503L; $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS26503LN.) (Note 1, [Figure 19-10](#))

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|--------------------|----------|-----|-------|-----|-------|-------|
| RCLK Period | t_{CP} | | 488 | | ns | 2 |
| | | | 648 | | | 3 |
| | | | 158.4 | | | 4 |
| RCLK Pulse Width | t_{CH} | 200 | | | ns | 5 |
| | t_{CL} | 200 | | | | |
| RCLK Pulse Width | t_{CH} | 150 | | | ns | 6 |
| | t_{CL} | 150 | | | | |
| RCLK to RSER Delay | t_{D1} | | | 20 | ns | |
| RCLK to RS Delay | t_{D2} | | | 50 | ns | |

Note 1: The timing parameters listed in this table are guaranteed by design (GBD).

Note 2: E1 mode.

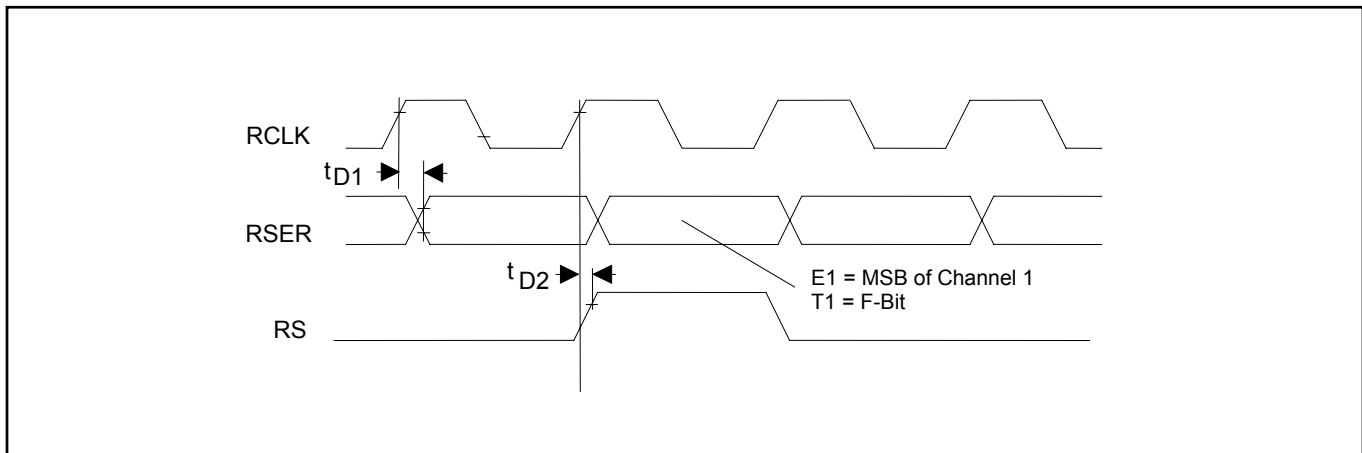
Note 3: T1 or J1 mode.

Note 4: 6312kHz mode.

Note 5: Jitter attenuator enabled in the receive path.

Note 6: Jitter attenuator disabled or enabled in the transmit path.

Figure 19-10. Receive Timing, T1/E1



19.5 Transmit Side AC Characteristics

Table 19-5. Transmit Side AC Characteristics

($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$.) (Note 1 and [Figure 19-11](#))

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------------|------------|-----|-------|-----|-------|-------|
| TCLK Period | t_{CP} | | 488 | | ns | 2 |
| | | | 648 | | ns | 3 |
| | | | 158.4 | | ns | 4 |
| TCLK Pulse Width | t_{CH} | 75 | | | ns | |
| | t_{CL} | 75 | | | ns | |
| TCLK Rise and Fall Times | t_R, t_F | | | 25 | ns | |
| TX CLOCK Setup to TSER, TS | t_{SU} | 20 | | | ns | 5, 6 |
| Delay TX CLOCK to TS | t_{D2} | | | 50 | ns | 6, 7 |
| Delay TCLK to PLL_OUT, TX CLOCK | t_{D3} | | | 20 | ns | 6, 8 |
| Delay TCLKO to TPOSO and TNEG0 | t_{DD} | | | 50 | ns | |

Note 1: The timing parameters listed in this table are guaranteed by design (GBD).

Note 2: E1 mode.

Note 3: T1 or J1 mode.

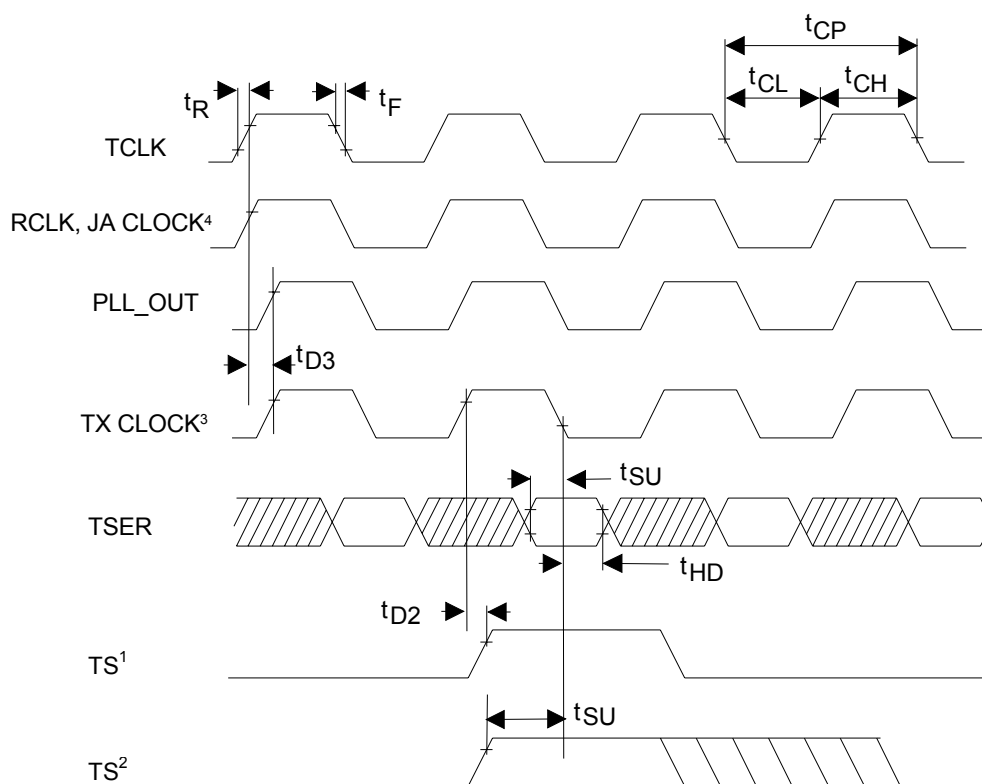
Note 4: 6312kHz mode.

Note 5: TS in input mode.

Note 6: TX CLOCK is an internal signal.

Note 7: TS in output mode.

Note 8: TX CLOCK is an internal signal that samples TSER and TS when TS is in input mode.

Figure 19-11. Transmit Timing, T1/E1

(REFER TO THE TRANSMIT PLL BLOCK DIAGRAM, [Figure 3-3](#).)

NOTE 1: TS IN OUTPUT MODE.

NOTE 2: TS IN INPUT MODE.

NOTE 3: TX CLOCK IS THE INTERNAL CLOCK THAT DRIVES THE TRANSMIT SECTION. THE SOURCE OF THIS SIGNAL DEPENDS ON THE CONFIGURATION OF THE TRANSMIT PLL. IF TX CLOCK IS GENERATED BY THE TRANSMIT PLL (CONVERSION FROM ANOTHER CLOCK RATE) THEN THE USER SHOULD OUTPUT THAT SIGNAL ON THE PLL_OUT PIN AND USE THAT SIGNAL TO REFERENCE TSER AND TS IF TS IS IN THE INPUT MODE.

NOTE 4: RCLK (THE RECOVERED LINE CLOCK) AND JA CLOCK (AN INTERNAL CLOCK DERIVED FROM MCLK) MAY BE SELECTED AS THE SOURCE FOR THE TRANSMIT PLL OR USED UNCONVERTED FOR TX CLOCK.

20. REVISION HISTORY

| REVISION | DESCRIPTION |
|----------|--|
| 070904 | New product release. |
| 032405 | Updated Table 2-1 and Table 2-2. Replaced the older recommended LIU circuits in Section 13.8 with newer versions (Figure 13-4 and Figure 13-5, Table 13-1 and Table 13-2). Modified the value of t_{DD} in Table 19-5. Added timing information to Table 19-5 and updated Figure 19-11. |
| 081105 | Corrected the bit order for the TCPR register. Bits 6 and 7 were reversed. Bits 3 and 4 were reversed. Corrected the polarity of the TAIS pin description for hardware mode operation (pages 18 and 28). The register control bit description for LIC2.4 is correct. Added thermal values to Table 18-2. |
| 101805 | Changed Section 13.4 to read “ 2.048×2^N (where $N = 1$ to 3)” instead of “ $2.048 \times N$ (where $N = 1$ to 4).” Edited Figure 3-4 to show 12.8MHz clock option and added references throughout relevant sections of the document. Added JACKS1 bit to LIC2.7—This feature is available in Rev B1 and later. |
| 022806 | Clarified the open circuit and short circuit wording in Sections 13.3.1 and 13.3.2 and SR1 bits 1 and 2. |
| 053107 | (Page 48) Removed reference to E1RCR and E1TCR bit 3 (this bit functionality has been moved to the MCREG). |
| 100507 | (Pages 108–109) In the <i>Absolute Maximum Ratings</i> (Section 18), added <i>Note 1: Specifications at -40 °C are guaranteed by design GBD and not production tested.</i> to Operating Temp Range for DS26503LN. Renumbered notes for Table 18-1 to Table 18-5. |
| 121707 | (Page 16) Clarified RITD and TITD descriptions. (Page 19) For E1TS description, changed $0 = 120\Omega$ and $1 = 75\Omega$ to $0 = 75\Omega$ and $1 = 120\Omega$. (Page 82) Corrected Note 2 in the LIC1[7:5] register description to include TT2 along with TT0 and TT1. |

21. PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information.)

64-Pin LQFP ([56-G4019-001](#))

