# Up Converter Mixer with Fractional-N Frequency Synthesizer and VCO

# AK1575

## 1. Overview

AK1575 is the up-converter mixer with fractional-N frequency synthesizer and integrated VCO. AK1575 is targeted at the application that requires a high linearity performance in frequency conversion. The mixer block is comprised of the differential input and the differential output. Input frequency range is from 20MHz to 1000MHz and output frequency range is from 690MHz to 4000MHz. The current consumption and the analog performance can be adjusted by a resistance connected to BIAS pin. The power supply voltage of mixer covers 4.75 to 5.25V.

The local signal output frequency range is from 262.5MHz to 4400MHz generated by internal VCO, synthesizer and divider. Not only a local signal is supplied to an internal mixer, but also can be taken to outside. A power supply voltage range of VCO/synthesizer is 2.7V to 3.6V or 4.75V to 5.25V.
The CPU interface is 24bit serial data and its voltage is ranging from 2.7V to 5.25V

## 2. Features

General

- RF output frequency Range: 690MHz to 4.0GHz
- IF input frequency Range: 20MHz to 1000MHz
- LO frequency Range: 262.5MHz to 4.4GHz
- Supply Voltage : 4.75V to 5.25 V (Mixer)
  2.7 to 3.6V / 4.75 to 5.25V (Synthesizer /VCO)
- Current Consumption: 150mA typ.
- Package: 32pin QFN (0.5mm pitch, 5mm × 5mm × 0.85mm)
- Operating Temperature : -40°C ~ 85°C

Synthesizer/VCO

- Normalized Phase Noise: -218dBc/Hz
- Phase Noise: -111dBc/Hz @100kHz $f_o$=2.1GHz

Mixer ($f_{rf}$=2GHz)

- Conversion Gain: -1.5dB typ.
- Input 3rd orders intercept point: +24dBm typ.
- Noise Figure: 13dB typ.

Application

Microwave Radio Link
Cellular BTS / Repeater

# 3. Table of Content


1. Overview 1
2. Features 1
3. Table of Content 2
4. Block Diagram and Function 3
5. Pin function Description and Assignment 4
6. Absolute Maximum Rating 6
7. Recommended Operating Range 7
8. Electrical Characteristics 7
9. Block Functional Descriptions 11
10. Loop filter /Charge Pump 12
11. Register Map 13
12. Lock Detect 22
13. Frequency Setup 25
14. Fast Lock mode 26
15. VCO 27
16. Power up Sequence 28
17. Typical Evaluation Board Schematic 29
18. Interface Circuit 31
19. Outer Dimensions 33
20. Marking 34

## 4. Block Diagram and Function

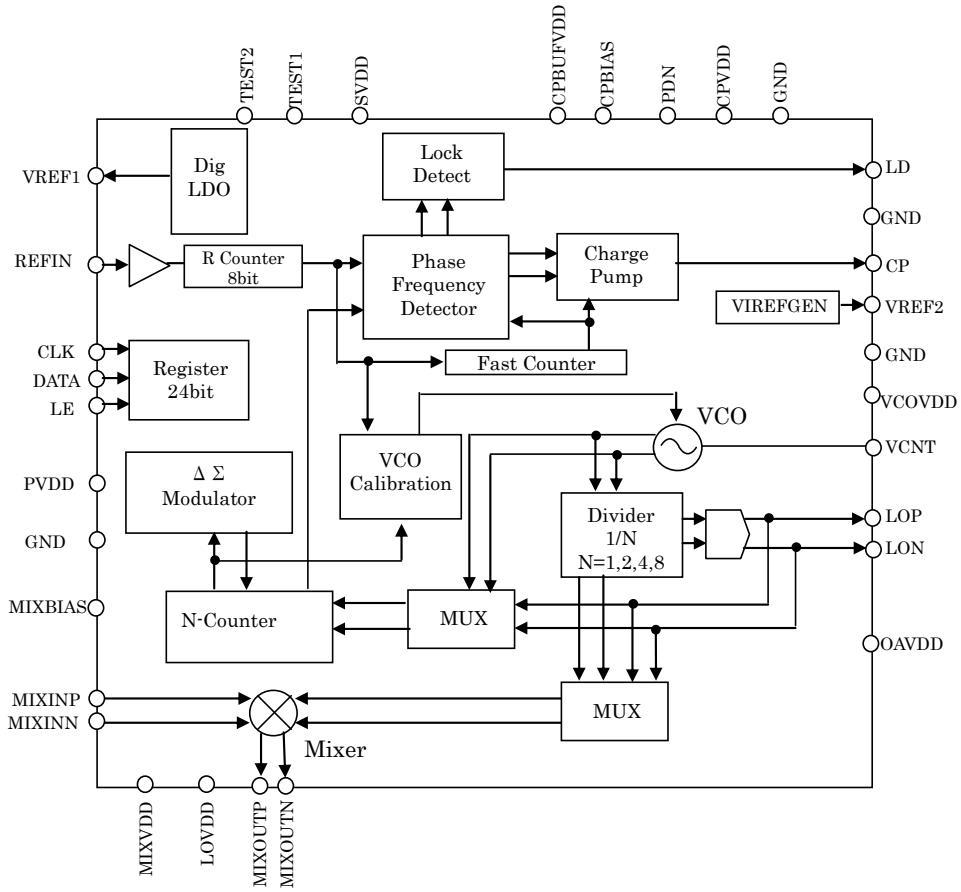



**Fig. 1 Block diagram**

### Block function description

| Block | Function |
|---|---|
| Mixer | Frequency Mixer which converts RF signal to IF signal |
| N divider | Frequency divider which divides the signal of VCO and pass it to phase frequency detector |
| ΔΣ Modulator | Control the modulus of N divider and realize fractional dividing |
| R counter | Frequency divider which divides the signal of reference clock and pass it to phase frequency detector |
| PFD (Phase Frequency Detector) | Detect a phase difference between the divided VCO signal and comparison frequency, and then drive the charge pump |
| Charge Pump | Output the electric charge according to the phase difference detected by PFD |
| VCO | The voltage controlled oscillator divided into three bands |

## 5. Pin function Description and Assignment

### 1. Pin Functions

| No | Name | I/O | Pin function | Power Down | Remarks |
|---|---|---|---|---|---|
| 1 | VREF1 | AO | Connecting a capacitor to the ground plane | | |
| 2 | PVDD | P | Synthesizer Power Supply | | |
| 3 | GND | G | | | |
| 4 | MIXBIAS | AI | Connecting a resistor to the ground plane | | |
| 5 | MIXINN | AI | Mixer Input | | |
| 6 | MIXINP | AI | Mixer complementary Input | | |
| 7 | MIXVDD | P | Mixer Power Supply | | |
| 8 | LOVDD | P | Mixer Local Power Supply | | |
| 9 | MIXOUTP | AO | Mixer Output | | Open collector |
| 10 | MIXOUTN | AO | Mixer complementary Output | | Open collector |
| 11 | PDN | DI | Power Control<br>A logic low on this pin powers down the device | | Schmidt trigger input |
| 12 | LE | DI | Load Enable | | Schmidt trigger input |
| 13 | CLK | DI | Serial Clock Input | | Schmidt trigger input |
| 14 | DATA | DI | Serial Data Input | | Schmidt trigger input |
| 15 | LD | DO | Lock Detect Output | LOW | |
| 16 | SVDD | P | Interface Power Supply | | |
| 17 | LOP | AIO | Local complementary Input / Output | | |
| 18 | LON | AIO | Local Input / Output | | |
| 19 | OAVDD | P | Local Output Amplifier Power Supply | | |
| 20 | GND | G | | | |
| 21 | VCNT | AI | Control Input to VCO | | |
| 22 | VREF2 | AO | Connecting a capacitor to the ground plane | | |
| 23 | GND | G | | | |
| 24 | VCOVDD | P | VCO Power Supply | | |
| 25 | CPBIAS | AI | Connecting a resistor to the ground plane | | |
| 26 | CP | AO | Charge Pump Output | Tri-State | |
| 27 | GND | G | | | |
| 28 | CPVDD | P | Charge Pump Power Supply | | |
| 29 | CPBUFVDD | P | Charge Pump Pre-Buffer Power Supply | | |

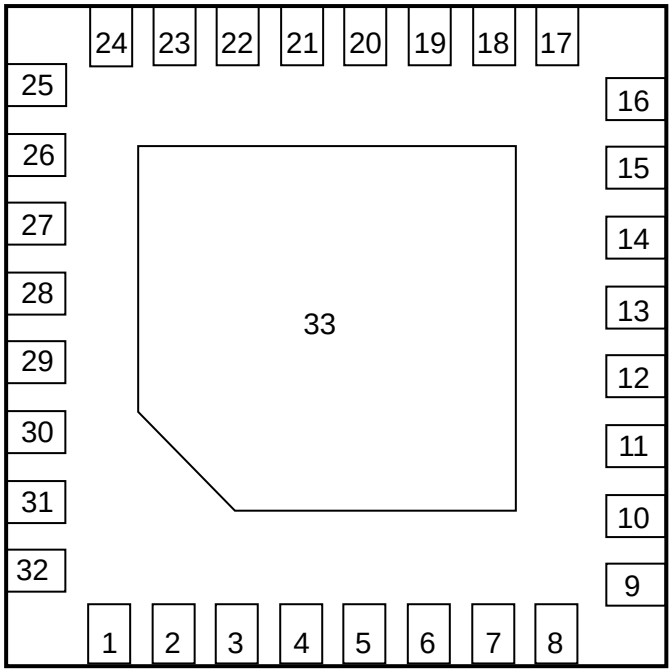
| No | Name | I/O | Pin function | Power Down | Remarks |
|---|---|---|---|---|---|
| 30 | TEST1 | DI | Test enable<br>A logic low on this pin test mode the device. | | Pull Down<br>Schmidt trigger input |
| 31 | TEST2 | DI | Test enable<br>A logic low on this pin test mode the device. | | Pull Down<br>Schmidt trigger input |
| 32 | REFIN | AI | Reference Input | | |

Note 1) The exposed pad at the center of the backside should be connected to ground.

The following table shows the meaning of abbreviations used in the "I/O" column above.

| | | | |
|---|---|---|---|
| AI:Analog input pin | AO:Analog output pin | AIO:Analog I/O pin | DI:Digital input pin |
| DO:Digital output pin | P: Power supply pin | G:Ground pin | |

**2. Pin Assignments**




**32pin QFN (0.5mm pitch, 5mm x 5mm)**

**Fig. 2 Package Pin Layout (Top View)**

## 6. Absolute Maximum Rating

| Parameter | Symbol | Min. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Supply Voltage | VDD1 | -0.3 | 5.5 | V | Note1, Note2 |
| | VDD2 | -0.3 | 5.5 | V | Note 3 |
| | VDD3 | -0.3 | 5.5 | V | Note4 |
| Ground Level | VSS | 0 | 0 | V | Note5 |
| Maximum RF Input Level | RFPOW | | 12 | dBm | Note6 |
| Maximum Lo Input Level | LOPOW | | 12 | dBm | Note7 |
| Analog Input Voltage | VAIN | VSS-0.3 | VDD3+0.3 | V | Note1, Note8 |
| Digital Input Voltage1 | VDIN1 | VSS-0.3 | VDD1+0.3 | V | Note1, Note9 |
| Digital Input Voltage 2 | VDIN2 | VSS-0.3 | VDD3+0.3 | V | Note1, Note10 |
| Input Current | IIN | -10 | 10 | mA | |
| Storage Temperature | Tstg | -55 | 125 | °C | |

Note1 All voltage reference ground Level: 0V

Note2 Applied to the [SVDD] pin

Note3 Applied to the [MIXVDD] and [LOVDD] pins

Note4 Applied to the [CPVDD], [CPBUFVDD], [PVDD], [VCOVDD] and [OAVDD] pins

Note5 Applied to the All [GND] pins

Note6 Applied to the [MIXINP] and [MIXINN] pins

Note7 Applied to the [LOP] and [LON] pins

Note8 Applied to the [VCNT] and [REFIN] pins

Note9 Applied to the [CLK], [DATA], [LE] and [PDN] pins

Note10 Applied to the [TEST1] and [TEST2] pins

Exceeding these maximum ratings may result in damage to the AK1575. Normal operation is not guaranteed at these extremes.

## 7. Recommended Operating Range

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Operating Temperature | Ta | -40 | | 85 | °C | |
| Supply Voltage | VDD1 | 2.7 | 3.0 | 5.25 | V | |
| | VDD2 | 4.75 | 5 | 5.25 | V | |
| | VDD3 | 2.7 | 3 | 3.6 | V | |
| | | 4.75 | 5 | 5.25 | V | |

Note1 Applied to the [SVDD] pin

Note2 Applied to the [MIXVDD] and [LOVDD] pins

Note3 Applied to the [CPVDD], [CPBUFVDD], [PVDD], [VCOVDD] and [OAVDD] pins

## 8. Electrical Characteristics

**1. Digital DC Characteristics**

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| High level input voltage | Vih | | 0.8×VDD1 | | | V | Note 1) |
| Low level input voltage | Vil | | | | 0.2×VDD1 | V | Note 1) |
| High level input current 1 | Iih1 | Vih = VDD1=5.25V | -1 | | 1 | μA | Note 1) |
| High level input current 2 | Iih2 | Vih = VDD2=5.25V | 27 | 53 | 106 | μA | Note 2) |
| Low level input current | Iil | Vil = 0V, VDD1=5.25V | -1 | | 1 | μA | Note 1) |
| High level output voltage | Voh | Ioh = -500μA | VDD1-0.4 | | | V | Note 3) |
| Low level output voltage | Vol | Iol = 500μA | | | 0.4 | V | Note 3) |

Note1 Applied to the [CLK], [DATA], [LE], and [PDN] pins

Note2 Applied to the [TEST1] and [TEST2] pins

Note3 Applied to the [LD] pin

## 2. Serial Interface Timing

<Write-In Timing>

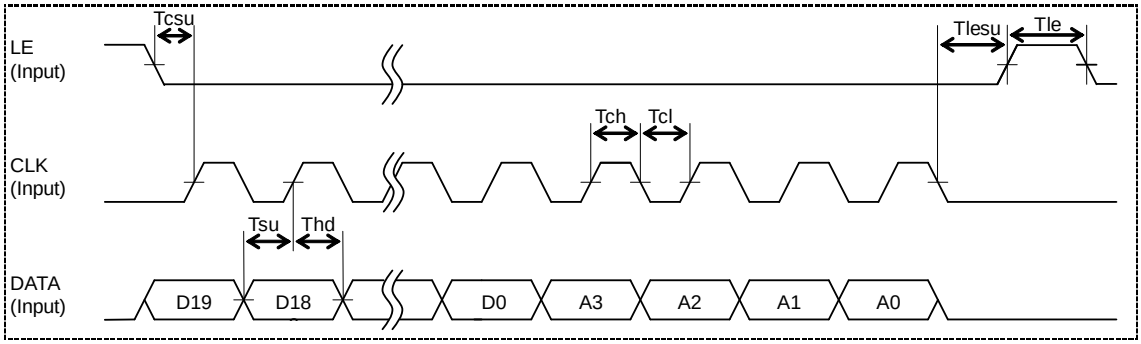



**Fig.3 Serial Interface Timing**

**Serial Interface Timing**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Clock L level hold time | Tcl | 25 | | | ns | |
| Clock H level hold time | Tch | 25 | | | ns | |
| Clock setup time | Tcsu | 10 | | | ns | |
| Data setup time | Tsu | 10 | | | ns | |
| Data hold time | Thd | 10 | | | ns | |
| LE setup time | Tlesu | 10 | | | ns | |
| LE pulse width | Tle | 25 | | | ns | |

### 3. Analog Circuit Characteristics

VDD1=2.7~5.25V, VDD2=4.75~5.25V, VDD3=2.7~3.6V or 4.75~5.25V, -40℃＜Ta＜85℃, CPBIAS=27kohm, MIXBIAS=33kohm, IF input frequency=200MHz, Internal VCO using unless otherwise specified.

| Item | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| RF Frequency Range | 690 | | 4000 | MHz | |
| IF Frequency Range | 20 | | 1000 | MHz | |
| Internal LO Frequency Range | 262.5 | | 4400 | MHz | |
| LO Input Level 1 | -5 | 0 | +5 | dBm | {MODE}=2,differential input or {MODE}=3 |
| LO Input Level 2 | -5 | | +1 | dBm | {MODE}=2, single input |
| LO Output Level @1GHz | | 6 | | dBm | {LOLV}=3 |
| | | 3 | | dBm | {LOLV}=2 |
| | | 0 | | dBm | {LOLV}=1 |
| | | -6 | | dBm | {LOLV}=0 |
| **Mixer** | | | | | |
| Mixer Input impedance | | 50 | | Ω | with matching circuit |
| Mixer Output impedance | | 200 | | Ω | with matching circuit |
| Current Adjusting resistance | 22 | 33 | 56 | kΩ | Connect to [MIXBIAS] pin |
| RFOUT=2GHz | | | | | |
| Conversion Gain | -4.5 | -1.5 | 1.5 | dB | |
| RF P1dB | 7 | 10 | | dBm | |
| IIP2 | | 70 | | dBm | |
| IIP3 | 20 | 24 | | dBm | guaranteed by design |
| NF | | 13 | 17 | dB | guaranteed by design |
| Local Leakage LO-to-RF | | -50 | | dBm | Use internal VCO |
| | | -50 | | dBc | Use external Local |
| Local Leakage LO-to-IF | | -80 | | dBm | Use internal VCO |
| | | -70 | | dBc | Use external Local |
| RFOUT=1GHz | | | | | |
| NF | | 11 | | dB | |
| RFOUT=4GHz | | | | | |
| NF | | 16 | | dB | |

| Item | | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| **REFIN characteristics** | | | | | | |
| Input Sensitivity | | 0.4 | | 2 | Vpp | |
| Input Frequency | | 10 | | 300 | MHz | |
| **Phase Frequency Detector** | | | | | | |
| PFD frequency | | 1.2 | | 40 | MHz | |
| **Charge Pump** | | | | | | |
| CP Maximum current | | | 2400 | | μA | |
| CP Minimum current | | | 300 | | μA | |
| Icp TRI-STATE leak current | | | 1 | | nA | Ta=25°C |
| CP Output Range | | 0.5 | | VDD3 -0.5 | V | |
| CP current adjusting resistance | | 22 | 27 | 33 | kΩ | Connect to [CPBIAS] pin |
| Normalized Phase Noise | | | -218 | | dBc/Hz | |
| **VCO** | | | | | | |
| Operating Frequency Range | | 2100 | | 3000 | MHz | VCO1 |
| | | 3000 | | 3400 | MHz | VCO2 |
| | | 3400 | | 4400 | MHz | VCO3 |
| VCO sensitivity | | | fv×0.02 | | MHz/V | fv: Oscillation Frequency |
| Phase Noise @2.1GHz | 10kHz offset | | -85 | | dBc/Hz | |
| | 100kHz offset | | -111 | | dBc/Hz | |
| | 1MHz offset | | -132 | | dBc/Hz | |
| | 10MHz offset | | -152 | | dBc/Hz | |

| Item | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| **Current Consumption** | | | | | |
| IDD1 | | 1 | 2 | mA | [PDN]="L" |
| IDD2 | | 140 | 200 | mA | [PDN]="H",{MIXEN}=1, {MODE}=0,{DIV}=0 |
| IDD3 | | 150 | 210 | mA | [PDN]="H",{MIXEN}=1, {MODE}=0,{DIV}≥2 |
| IDD4 | | 190 | 270 | mA | [PDN]="H",{MIXEN}=1, {MODE}=1,{DIV}≥2 |

# 9. Block Functional Descriptions

## ・ Operation Mode

AK1575 operation is controlled as follows by the [PDN] pin and registers.

| Function | Pin | Registers | | | Operating state | | | |
|---|---|---|---|---|---|---|---|---|
| | [PDN] | {MIXEN} | MODE[1] | MODE[2] | Mixer | Synthesizer | VCO | Local Out |
| StandBy1 | ”L” | X | X | X | OFF | OFF | OFF | OFF |
| Prohibited | ”H” | 0 | 0 | 0 | OFF | ON | ON | OFF |
| Func1 | ”H” | 0 | 0 | 1 | OFF | ON | ON | Output |
| Func2 | ”H” | 0 | 1 | 0 | OFF | ON | OFF | Input |
| StandBy2 | ”H” | 0 | 1 | 1 | OFF | OFF | OFF | OFF |
| Func3 | ”H” | 1 | 0 | 0 | ON | ON | ON | OFF |
| Func4 | ”H” | 1 | 0 | 1 | ON | ON | ON | Output |
| Func5 | ”H” | 1 | 1 | 0 | ON | ON | OFF | Input |
| Func6 | ”H” | 1 | 1 | 1 | ON | OFF | OFF | Input |

StandBy1:Stand-by mode. Current consumption is minimized. It is available to write to the registers.

Func1: VCO and Synthesizer are active and Local signal outputs from [LOP] and [LON] pins.

Func2:Only Synthesizer is active. PLL operation is available with the external VCO.

StandBy2: Stand-by mode. Current consumption is minimized. It is available to write to the registers.

Func3: VCO, Synthesizer and Mixer are active.

Func4: VCO, Synthesizer and Mixer are active and Local signal outputs from [LOP] and [LON] pins.

Func5: Synthesizer and Mixer are active. PLL operation is available with the external VCO.

Func6: Only Mixer is active. A local signal needs to be input from [LOP] and [LON] pins.

## 10. Loop filter /Charge Pump

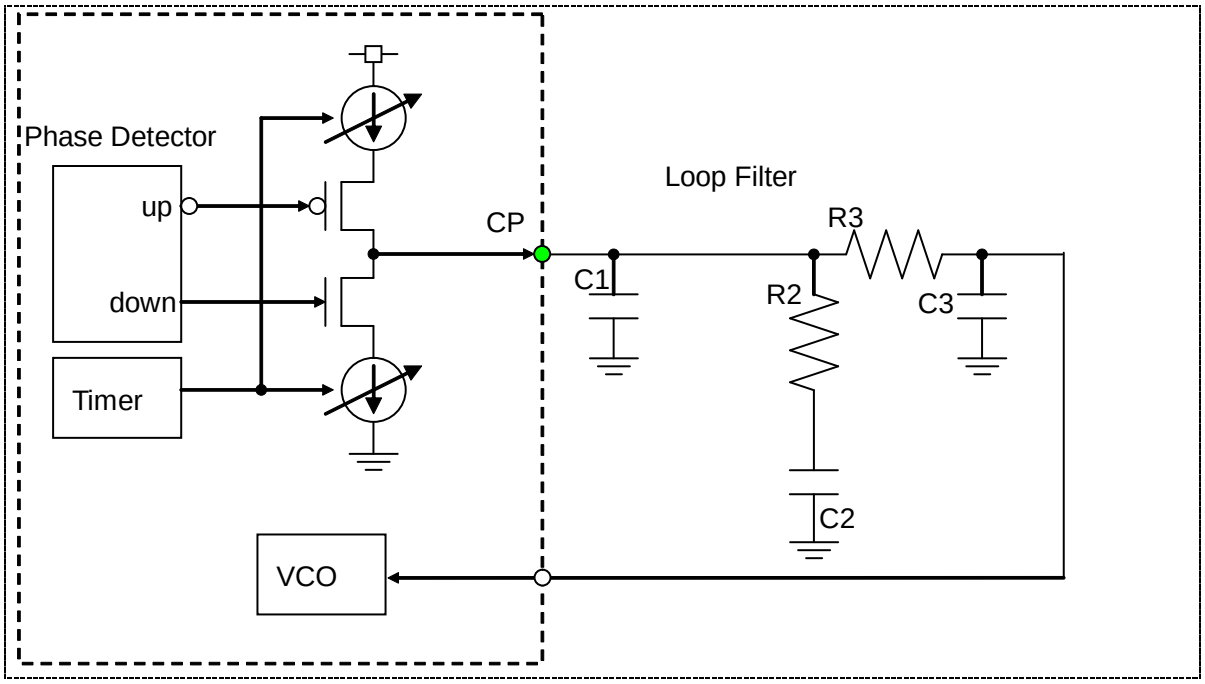



**Fig.4 Loop Filter Schematic**

## 11. Register Map

| Name | Data | Address | | | |
|---|---|---|---|---|---|
| Freq1 | D19 - D0 | 0 | 0 | 0 | 1 |
| Freq2 | | 0 | 0 | 1 | 0 |
| Freq3 | | 0 | 0 | 1 | 1 |
| Function | | 0 | 1 | 0 | 0 |

| Name | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Freq1 | 0 | 0 | 0 | VCO [1] | VCO [0] | DIV [1] | DIV [0] | 0 | INT [11] | INT [10] | INT [9] | INT [8] | INT [7] | INT [6] | INT [5] | INT [4] | INT [3] | INT [2] | INT [1] | INT [0] | 0x01 |
| Freq2 | 0 | CP1 [2] | CP1 [1] | CP1 [0] | 0 | CP2 [2] | CP2 [1] | CP2 [0] | FRAC [11] | FRAC [10] | FRAC [9] | FRAC [8] | FRAC [7] | FRAC [6] | FRAC [5] | FRAC [4] | FRAC [3] | FRAC [2] | FRAC [1] | FRAC [0] | 0x02 |
| Freq3 | R [7] | R [6] | R [5] | R [4] | R [3] | R [2] | R [1] | R [0] | MOD [11] | MOD [10] | MOD [9] | MOD [8] | MOD [7] | MOD [6] | MOD [5] | MOD [4] | MOD [3] | MOD [2] | MOD [1] | MOD [0] | 0x03 |
| Function | CALTM [3] | CALTM [2] | CALTM [1] | CALTM [0] | 0 | LDCNT SEL | LD | MTLD | FAST EN | FAST [3] | FAST [2] | FAST [1] | FAST [0] | CP HIZ | DSM ON | MIX EN | MODE [1] | MODE [0] | LOLV [1] | LOLV [0] | 0x04 |

**Notes for writing into registers**

1) The setting of <Address 0x02> and <Address 0x03> is reflected to each circuit when writing to <Address 0x01>.
2) <Address 0x04> behavior is reflected by itself.

When AK1575 powers on, the initial registers value is not defined. It is required to write the data in all addresses in order to commit it.

## < Address0x01:Freq1 >

**D [16:15]**

**VCO[1:0] : Select VCO**

In accordance with the used frequency, select the VCO.

| VCO[1:0]<br>Dec | VCO oscillating range<br>Frequency |
|---|---|
| 0 | 2.1GHz～3.0GHz |
| 1 | 3.0GHz～3.4GHz |
| 2 | 3.4GHz～4.4GHZ |
| 3 | prohibited |

**D [14:13]**

**DIV[1:0] : LoDivider**

In accordance with the used frequency, select the division number.

| DIV[1:0]<br>Dec | LoDivider<br>Divide Number |
|---|---|
| 0 | No divide |
| 1 | 2 divide |
| 2 | 4 divide |
| 3 | 8 divide |

**D [11:0]**

**INT[11:0] : NDivider**

N divider divided number.

The allowed range is 35 to 4091.

## < Address0x02:Freq2 >

**D [18: 16]**

**CP1[2:0] : Set the charge pump current for normal status**

**D [14:12]**

**CP2[2:0] : Set the charge pump current for fast lock**

CP1 is the charge pump current setting of the normal mode.

CP2 is the charge pump current setting of the fast lock mode

Charge pump current is determined by the following formula.

Charge pump current [A] = Icp_min [A] × (CP1 or CP2 setting value+1)

Icp_min [A] = 8.1 / R [ohm]

R: the resistance value which is connected to [CPBIAS] pin

Charge pump current (typ) unit : μA

| CP1[2:0] | R | | |
|---|---|---|---|
| CP2[2:0] | 33kΩ | 27kΩ | 22kΩ |
| 0 | 245 | 300 | 368 |
| 1 | 491 | 600 | 736 |
| 2 | 736 | 900 | 1105 |
| 3 | 982 | 1200 | 1473 |
| 4 | 1227 | 1500 | 1841 |
| 5 | 1473 | 1800 | 2209 |
| 6 | 1718 | 2100 | 2577 |
| 7 | 1964 | 2400 | 2945 |

**D [11:0]**

**FRAC[11:0]:Fractional Numerator determination**

Set the Numerator of Fractional divider.

The allowed range is from 0 to (MOD[11:0] -1).

## < Address0x03:Freq3 >

**D[19:12]**

**R [7:0]: 8bit Reference Counter**

**Maximum PFD frequency is 40MHz**

| R[13:0] | Divide Ratio |
|---|---|
| 0 | Prohibited |
| 1 | 1 |
| 2 | 2 |
| 3 | 3 |
| 4 | 4 |
| • | • |
| • | • |
| • | • |
| 253 | 253 |
| 254 | 254 |
| 255 | 255 |

**D [11:0]**

**MOD[11:0]:Fractional Denominator determination**

Set the denominator of Fractional divider.

The allowed range is from 2 to 4095.

## < Address0x04: function >

**D[19:16]**

**CALTM [3:0]: Set the calibration precision of VCO**

The register {CALTM [3:0]} determines the calibration precision and time for VCO. When {CALTM [3:0]} is larger, the calibration precision increases, but the required time becomes long as trade-off. The value calculated by the following formula is recommended to get enough calibration precision. However, {CALTM [3:0]} should be set between from 1 to 11. 0 and over 11 is prohibited.

$\{CALTM[3:0]\} \geqq \log_2(F_{PFD}/20000)$

$F_{PFD}$ : PFD frequency

The calibration time can be estimated as following calculation;

Calibration time = $1 / F_{PFD} \times \{(6 + 2\text{^}\{CALTM[3:0]\}) \times 8 + 3\}$

**D [14]**

**LDCNTSEL: Lock Detect Precision**

Set the counter value for digital lock detect.

| LDCNTSEL | Function | |
|---|---|---|
| 0 | 15 times Count | unlocked to locked |
| | 3 times Count | locked to unlocked |
| 1 | 31 times Count | unlocked to locked |
| | 7 times Count | locked to unlocked |

**D [13]**

**LD: Lock detect function**

Set the lock detect function.

0: Digital lock detect

1: Analog lock detect

**D [12]**

**MTLD: Local signal mute**

0: Don't mute local signal in unlock state.

1: Mute local signal in unlock state.

※Please use {MTLD} =0 at the time of {LD}=1.

Please use {MTLD}=1 at the time of {MODE}=1

**D [11]**

**FASTEN : Fast Lock mode setting**

Enable / disable fast lock mode.

0: Disable fast lock mode

1: Enable fast lock mode

Please refer to "14. Fast lock mode" for details.

**D[10:7]**

**FAST [3:0] : Fast lock timer setting**

Set the count number of fast lock timer.

Count Number = 511 + FAST[3:0] × 512

| TIMER[3:0] | Count Number |
|---|---|
| 0 | 511 |
| 1 | 1023 |
| 2 | 1535 |
| 3 | 2047 |
| 4 | 2559 |
| 5 | 3071 |
| 6 | 3583 |
| 7 | 4095 |
| 8 | 4607 |
| 9 | 5119 |
| 10 | 5631 |
| 11 | 6143 |
| 12 | 6655 |
| 13 | 7167 |
| 14 | 7679 |
| 15 | 8191 |

**D [6]**

**CPHIZ: Charge Pump TRI-STATE**

Set the charge pump output in Tri-State.

0: Normal

1: Tri-State

**D [5]**

**DSMON:** ΔΣ-modulator activation

In Integer-N setting, set the ΔΣ-modulator to active.

0: ΔΣ-modulator inactive

1: ΔΣ-modulator active

**D [4]**

**MIXEN: Mixer Enable**

0: Stand-by

1: Enable

**D [3:2]**

**MODE [1:0]: Local operation mode**

Set the operation of Synthesizer, VCO and LOP/LON pins.

| MODE[1:0] | Local Operating MODE |
|---|---|
| 0 | Internal Synthesizer and VCO are active. |
| 1 | Internal Synthesizer and VCO are active and the local signal outputs from LOP/LON pins. |
| 2 | The mode operating external VCO with internal synthesizer. |
| 3 | The mode using an external local signal. |

**D [1:0]**

**LOLV [1:0]: Local output power**

At the state of {MODE [1:0]} =1, set the power of the local signal output from LOP/LON pins.

| LOLV[1:0] | LOP, LON output power [dBm] |
|---|---|
| 0 | -6 |
| 1 | 0 |
| 2 | 3 |
| 3 | 6 |

## 12. Lock Detect

Lock detect output can be selected by {LD} in D [13] of <Address0x04>. When {LD} is set to "1", the [LD] pin outputs a phase comparison result which is from phase detector directly. (This is called "analog lock detect".) When {LD} is set to "0", the output is the lock detect signal according to the on-chip logic. (This is called "digital lock detect".)

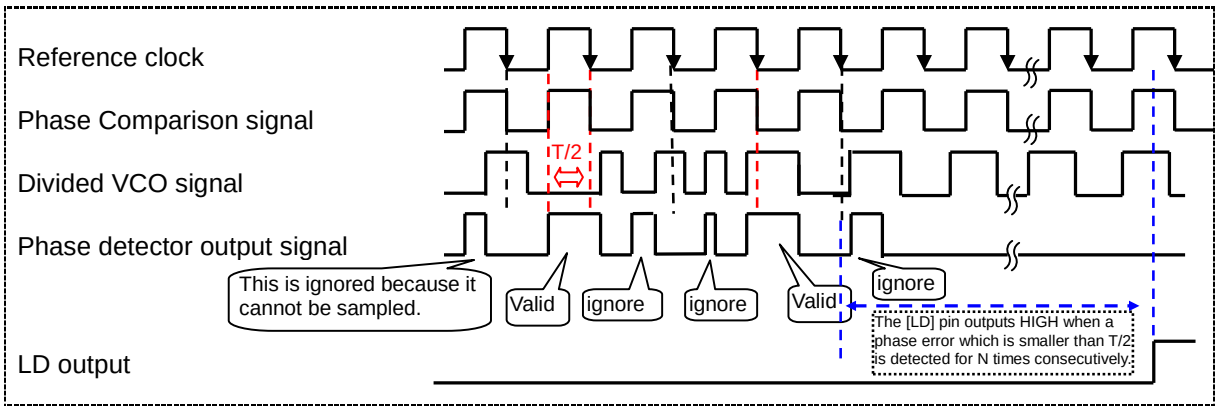
The digital lock detect can be done as following:

The [LD] pin is in unlocked state (which outputs "L") when a frequency setup is made.

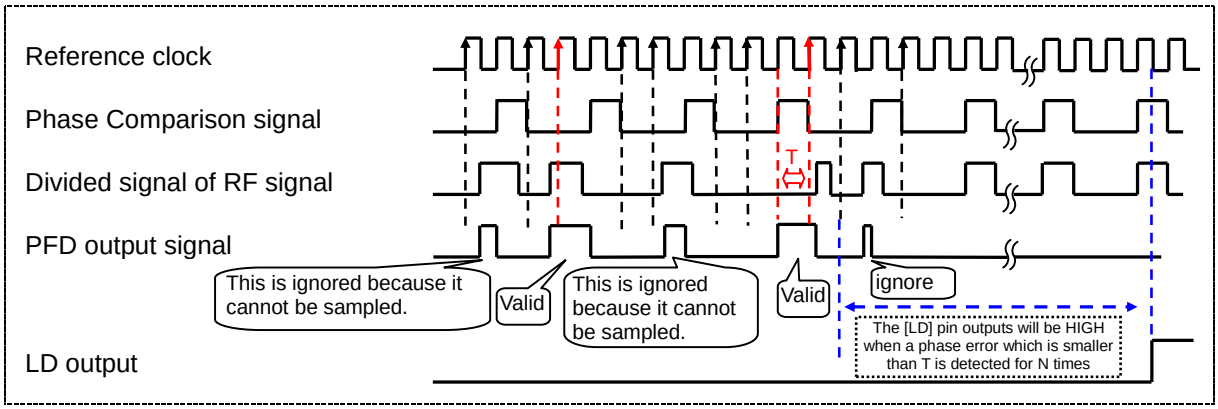
In the digital lock detect, the [LD] pin outputs "H" (which means the locked state) when a phase error smaller than a cycle of [REFIN] clock (T) is detected for N times consecutively. When a phase error larger than T is detected for N times consecutively while the [LD] pin outputs "H", then the [LD] pin outputs "L" (which means the unlocked state). The counter value N can be set by {LDCNTSEL} in D [14] of <Address0x04>. The N is different between "unlocked to locked" and "locked to unlocked".

| {LDCNTSEL} | unlocked to locked | locked to unlocked |
|---|---|---|
| 0 | N=15 | N=3 |
| 1 | N=31 | N=7 |

The lock detect signal is shown below

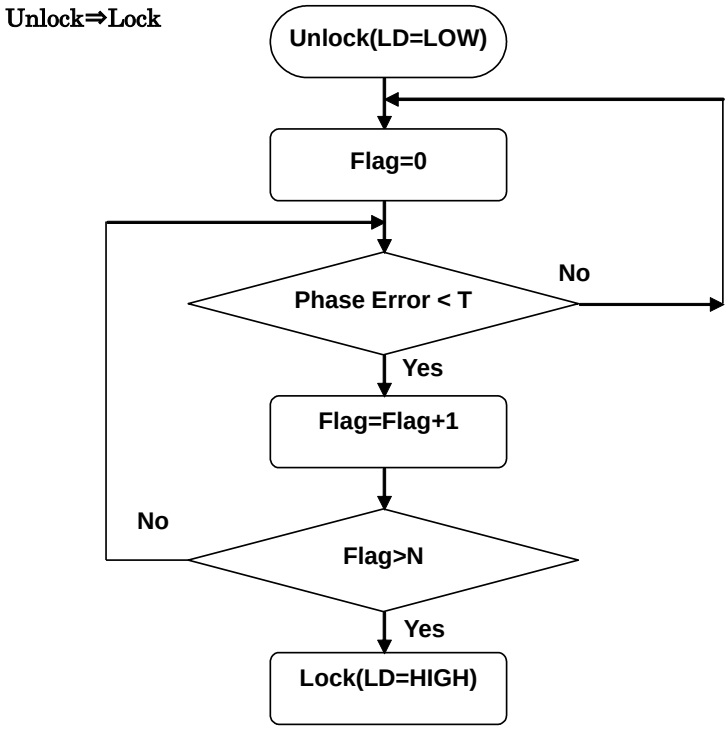



Case of "R = 1"

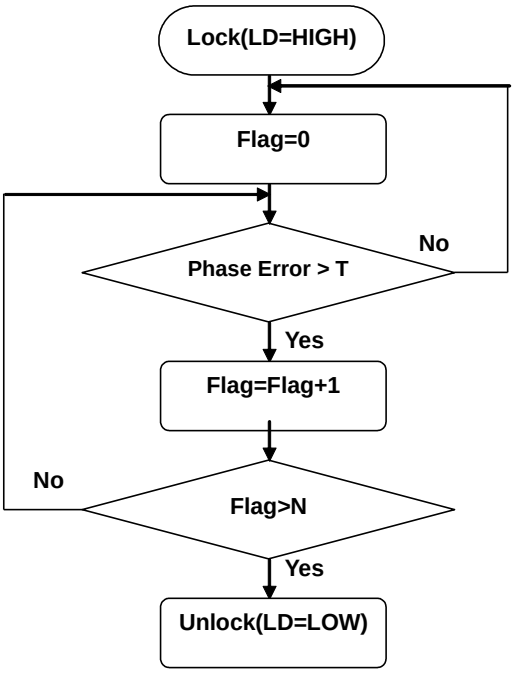



Case of “R > 1”

**Fig6. .Digital Lock Detect Operations**



Lock⇒unlock


Lock(LD=HIGH)
Flag=0
Phase Error > T
No
Yes
Flag=Flag+1
No
Flag>N
Yes
Unlock(LD=LOW)

## 13. Frequency Setup

The following formula is used to calculate the frequency setting for the AK1575.

Frequency setting ＝Ref Frequency × (INT+FRAC/MOD)

| | |
|---|---|
| Ref Frequency | : PFD fequency |
| INT | : Integer divide Number (Refer to <Address 0x01> : INT[11:0]) |
| FRAC | : Numenator setting number (Refer to <Address 0x02> : FRAC[11:0]) |
| MOD | : Denominator setting number (Refer to <Address 0x03> : MOD[11:0]) |

Set in the range of 35 to 4091 for INT[11:0].

Set in the range of 0 to (MOD-1) for FRAC[11:0]

Set in the range of 2 to 4095 for MOD[11:0]

○ Example

To complete Ref Frequency=19.2MHz, Frequency setting=2460.1MHz, set as follows

INT = 128

FRAC = 25

MOD = 192

Frequency setting = 19.2MHz × (128 + (25 / 192)) = 2460.1MHz

By writing <Address 0x01, 0x02, 0x03>, frequency is set. When <Address 0x01> is written, the setting of <Address 0x03> and <Addresses 0x02> is reflected in the internal circuit. At the time of the writing of <Address 0x01>, it is necessary for a synthesizer block to be powered on. The writing of <Address 0x01> as a trigger, frequency setting and VCO calibration are carried out, and fast lock counter starts operation. To set frequency definitely, <Address 0x01> should be written in the state that {MODE [1:0]} in <Address 0x04> is 0 or 1 or 2 and [PDN] pin is “H”.

## 14. Fast Lock mode

The fast lock mode becomes effective when set {FASTEN} of <Address 0x04> to"1".

○Fast Lock Mode

When writing in <Address0x01> with {FASTEN}=1, Fast Lock Up mode starts after calibration. The Fast Lock Up mode is valid only during the time period set by the timer according to the counter value in {FAST [3:0]} in <Address0x04>, and the charge pump current is set to the value specified by {CP2}. When the specified time period elapses, the Fast Lock Up mode operation is switched to the normal operation, and the charge pump current returns to {CP1} setting

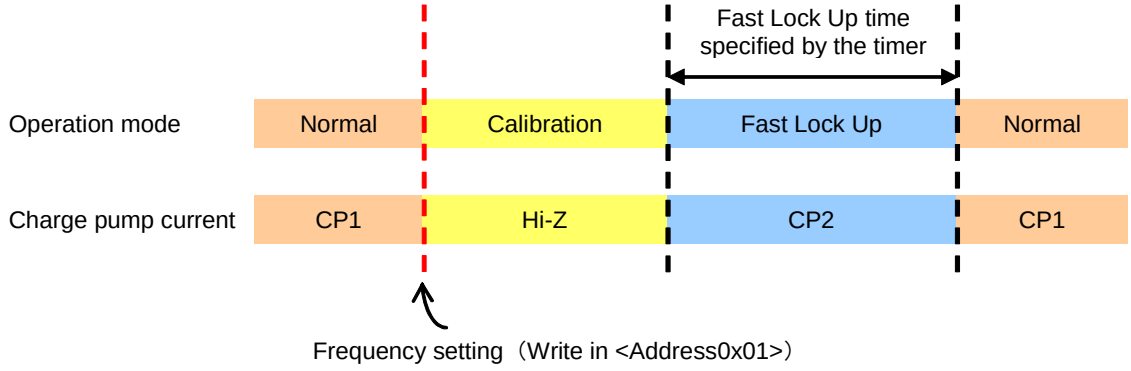



Fig.7. **Fast Lock up Mode Timing Chart**

○Timer period

{FAST [3:0]} in <Address0x04> is used to set the time period for this mode. The following formula is used to calculate the time period

Counter Value =511＋FAST[3:0] × 512

## 15. VCO

Calibration

AK1575 has three VCO core in uses several overlapping bands to allow low Phase Noise, low VCO sensitivity ($K_{VCO}$) and wide frequency range. The selection which VCO should be used can be done by the register {VCO[1:0]} in <Address 0x01>. Moreover, the correct band is chosen automatically at frequency setting, which is called calibration.

The calibration starts when <Address0x01> are written in the condition that {MODE[1]} in <Address 0x04>="0" and [PDN] pin="H". During the calibration, $V_{TUNE}$ of VCO is disconnected from the output of the loop filter and connected to an internal reference voltage. The charge pump output is disabled.

The internal bias must be stable so that the calibration is done correctly. Therefore, it is necessary to wait 500μsec at least until <Address0x01> writing after [PDN] rises up.

The register {CALTM [3:0]} determines the calibration time. When {CALTM [3:0]} is larger, the calibration precision increases, but the required time becomes long as a trade-off. The value calculated by the following formula is recommended to get enough calibration precision. However, {CALTM [3:0]} should be set at from 1 to 11. 0 and over 11 is prohibited.

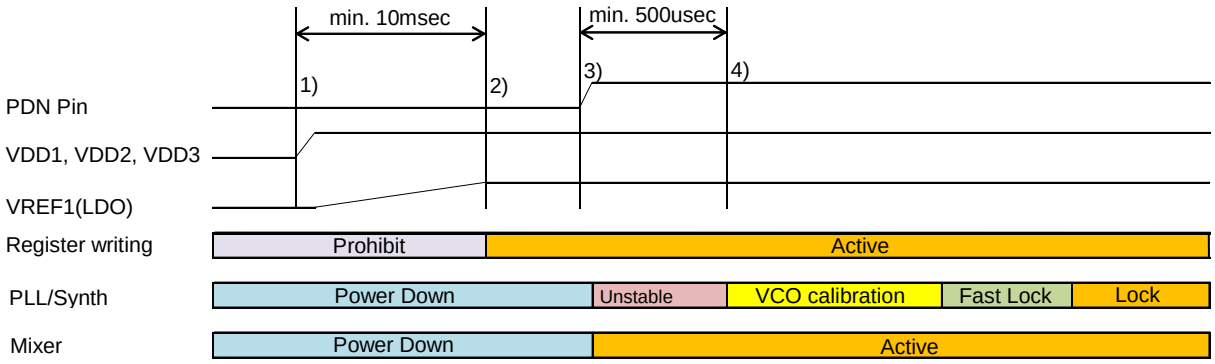
$$\{CALTM[3:0]\} \geq \log_2(F_{PFD} / 20000)$$

$F_{PFD}$ : PFD frequency

The calibration time can be estimated as following calculation;

$$\text{Calibration time} = 1 / F_{PFD} \times \{(6 + 2\text{^} \{CALTM [3:0]\}) \times 8 + 3\}$$

## 16. Power up Sequence




1) Set [PDN] pin to "L" and turn on power supplies (VDD1/VDD2/VDD3)
2) The stabilization time for [VREF1] (LDO) is 10msec. After LDO is stabilized, write the data to the registers of <Address 0x01, 0x02, 0x03, 0x04>
3) Set [PDN] pin to "H". In this state, the internal circuits are in an operating state, but PLL/Synth is unstable yet.
4) The stabilization time of internal BIAS circuits is 500usec. After BIAS circuit is stabilized, write the data to <Address 0x01>. VCO calibration starts and PLL status will be locked. Refer to 14.Fast Lock Mode and 15.VCO contents regarding fast Lock mode and VCO calibration.

Note1) The initial register values are not defined. Therefore, it is required to write the data in all addresses of the register.

Note2) The stabilization time for LDO is required more than 10ms.

## 17. Typical Evaluation Board Schematic

1.Evaluation Board schematic and the list of external parts

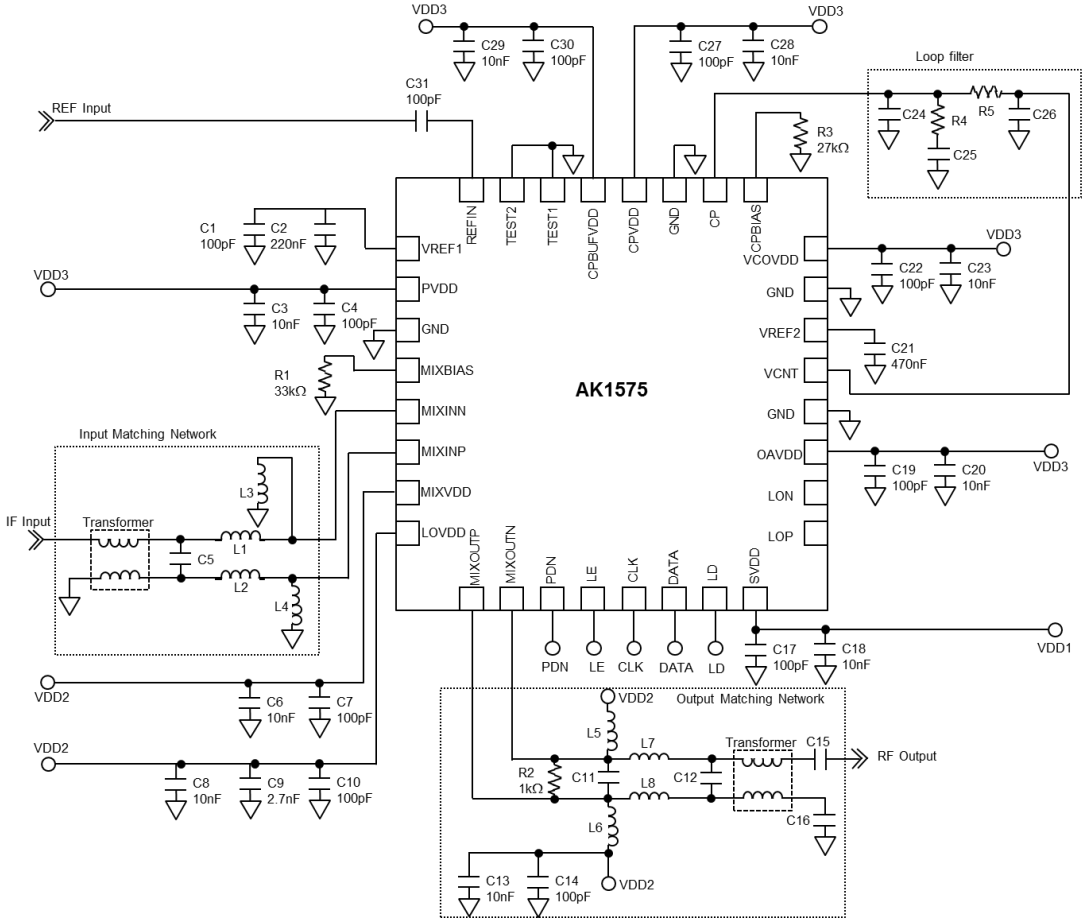



**Fig.9. Typical Evaluation Board Schematic**

| Ref. | Value | Ref. | Value | Ref. | Value | Ref. | Value | Ref. | Value |
|---|---|---|---|---|---|---|---|---|---|
| C1 | 100pF | C10 | 100pF | C19 | 100pF | C28 | 10nF | L6 | Matching |
| C2 | 220nF | C11 | Matching | C20 | 10nF | C29 | 10nF | L7 | Matching |
| C3 | 10nF | C12 | Matching | C21 | 470nF | C30 | 100pF | L8 | Matching |
| C4 | 100pF | C13 | 10nF | C22 | 100pF | C31 | 100pF | R1 | 33kΩ |
| C5 | Matching | C14 | 100pF | C23 | 10nF | L1 | Matching | R2 | 1kΩ |
| C6 | 10nF | C15 | Matching | C24 | Loop Filter | L2 | Matching | R3 | 27kΩ |
| C7 | 100pF | C16 | Matching | C25 | Loop Filter | L3 | Matching | R4 | Loop Filter |
| C8 | 10nF | C17 | 100pF | C26 | Loop Filter | L4 | Matching | R5 | Loop Filter |
| C9 | 2.7nF | C18 | 10nF | C27 | 100pF | L5 | Matching | | |

Note1) Exposed Pad at the center of the backside is should be connected to ground.
Note2) [TEST1] and [TEST2] pins should be connected to ground.

2. External circuit to input the external Local signal to [LOP] and [LON] pins.

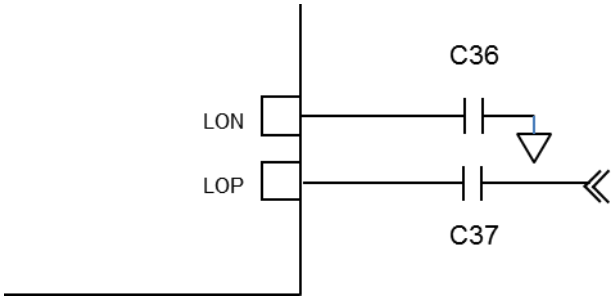



**Fig 7 Circuit for local input**

| Ref | Value |
|---|---|
| C36 | 100pF |
| C37 | 100pF |

3. External circuit to output the internal local signal from [LOP] and [LON] pins

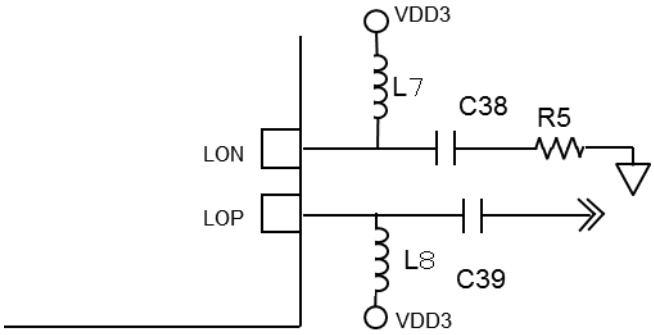
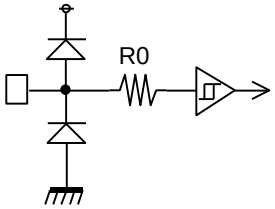
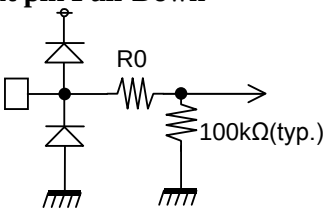
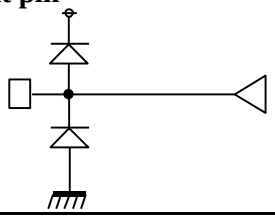
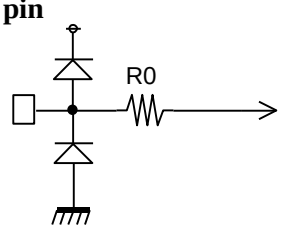


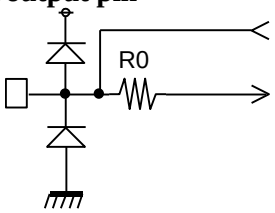
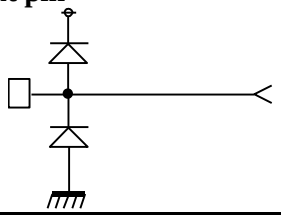
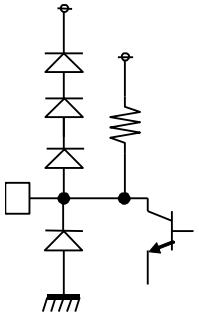
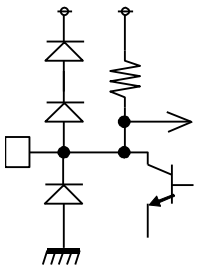
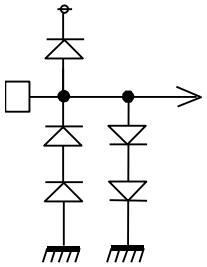

**Fig 8 Circuit for local output**

Example of the external components for this mode

| Ref | Value |
|---|---|
| C38 | 100pF |
| C39 | 100pF |
| L7 | 180nH |
| L8 | 180nH |
| R5 | 50Ω |

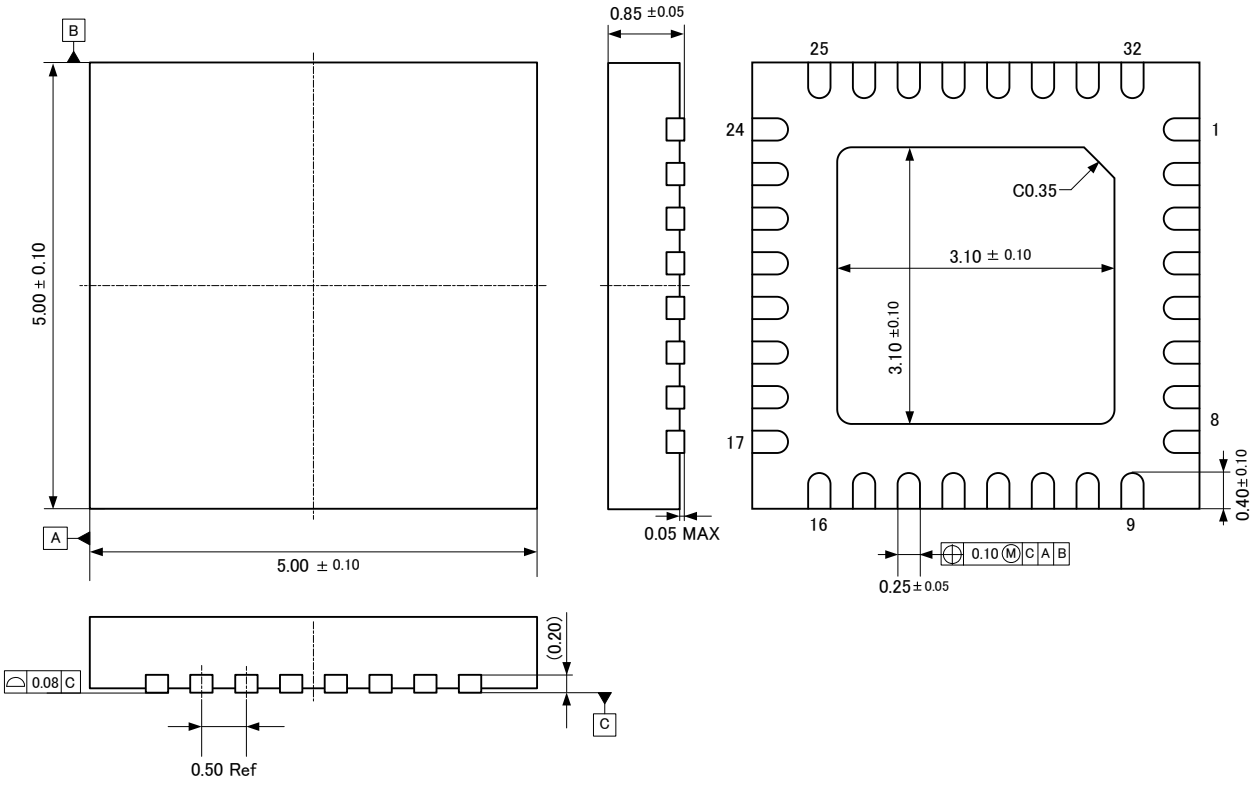
## 18. Interface Circuit

| Pin No. | Name | I/O | R0 (Ω) (typ.) | Cur (μA) | Function |
|---|---|---|---|---|---|
| 11 | PDN | DI | 300 | | **Digital input pin**   |
| 12 | LE | DI | 300 | | |
| 13 | CLK | DI | 300 | | |
| 14 | DATA | DI | 300 | | |
| | | | | | |
| 30 | TEST1 | DI | 300 | | **Digital input pin Pull-Down**   |
| 31 | TEST2 | DI | 300 | | |
| 15 | LD | DO | | | **Digital Output pin**  |
| 21 | VCNT | I | 100 | | **Analog input pin**   |
| 32 | REFIN | I | 300 | | |

| Pin No. | Name | I/O | R0 (Ω) (typ.) | Cur (μA) | Function |
|---|---|---|---|---|---|
| 1 | VREF1 | AO | 300 | | **Analog input/output pin**   |
| 4 | MIXBIAS | AO | 300 | | |
| 22 | VREF2 | AI | 300 | | |
| 25 | CPBIAS | AI | 300 | | |
| | | | | | |
| 23 | CP | O | | | **Analog output pin**  |
| | | | | | |
| 9 | MIXOUTN | O | | | **RF open collector output pin**  |
| 10 | MIXOUTP | O | | | |
| | | | | | |
| 17 | LOP | IO | | | **RF open collector input/output pin**  |
| 18 | LON | IO | | | |
| | | | | | |
| 5 | MIXINN | IO | | | **RF input pin**  |
| 6 | MIXINP | IO | | | |
| | | | | | |

## 19. Outer Dimensions

QFN32-5X5-0.50

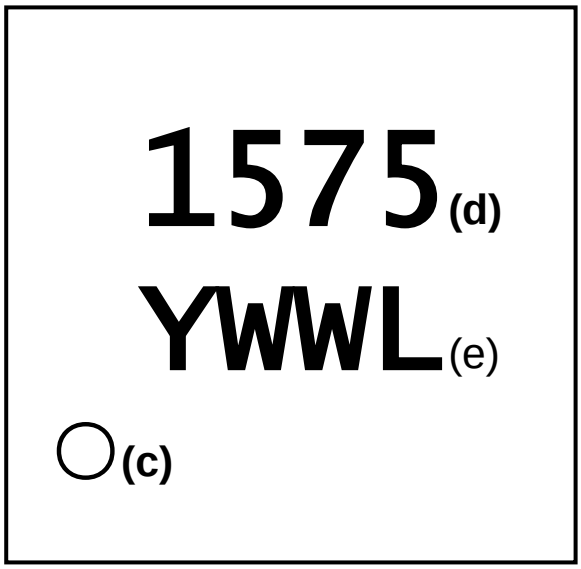



Note) The exposed pad at the center of the backside should be connected to ground.

## 20. Marking

(a) Style : QFN
(b) Number of pins : 32
(c) 1 pin marking: : ○
(d) Product number : 1575
(e) Date code : YWWL (4 digits)

Y:Lower 1 digit of calendar year (Year 2013 → 3, 2014 → 4 ...)
WW: Week
L: Lot identification, given to each product lot which is made in a week
→ LOT ID is given in alphabetical order (A, B, C…).



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