

# Multifunctional Ignition and Injector Driver

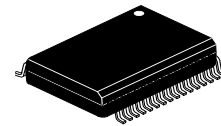
The 33812 is an engine control analog power IC intended for motorcycle and other single/dual cylinder small engine control applications. The IC consists of three integrated low-side drivers, one pre-driver, a +5.0 V, voltage pre-regulator, an MCU watchdog circuit, an ISO 9141 K-Line interface, and a parallel interface for MCU communication. The three low-side drivers are provided for driving a fuel injector, a lamp or LED, and a relay or other load. The pre-driver is intended to drive either an Insulated Gate Bipolar Transistor (IGBT) or a bipolar Darlington transistor to control an ignition coil. This device is powered by SMARTMOS technology.

## Features:

- Designed to operate over the range of  $\sim 4.7\text{ V} \leq V_{\text{PWR}} \leq 36\text{ V}$
- Fuel injector driver - Current Limit - 4.0 A typical
- Ignition pre-driver can drive IGBT or Darlington bipolar junction transistors
- Ignition pre-driver has independent high and low-side outputs
- Relay driver - current limit - 4.0 A typical
- Lamp driver- current limit - 1.5 A typical
- All external outputs protected against short to battery, overcurrent
- Ignition and other drivers protected against overtemperature
- Interfaces directly to MCU using 5.0 V parallel interface
- VCC voltage pre-regulator provides +5.0 V power for the MCU
- MCU Power On RESET generator
- MCU watchdog timer circuit with parallel refresh/time setting line
- Independent fault annunciation outputs for ignition, injector and relay drivers
- ISO-9141 K-Line transceiver for communicating diagnostic messages

33812

SMALL ENGINE CONTROL IC



EK Pb-FREE SUFFIX  
98ASA10556D  
32 Pin SOICW EP

## Applications:

- Single cylinder engine control
- Dual cylinder engine control

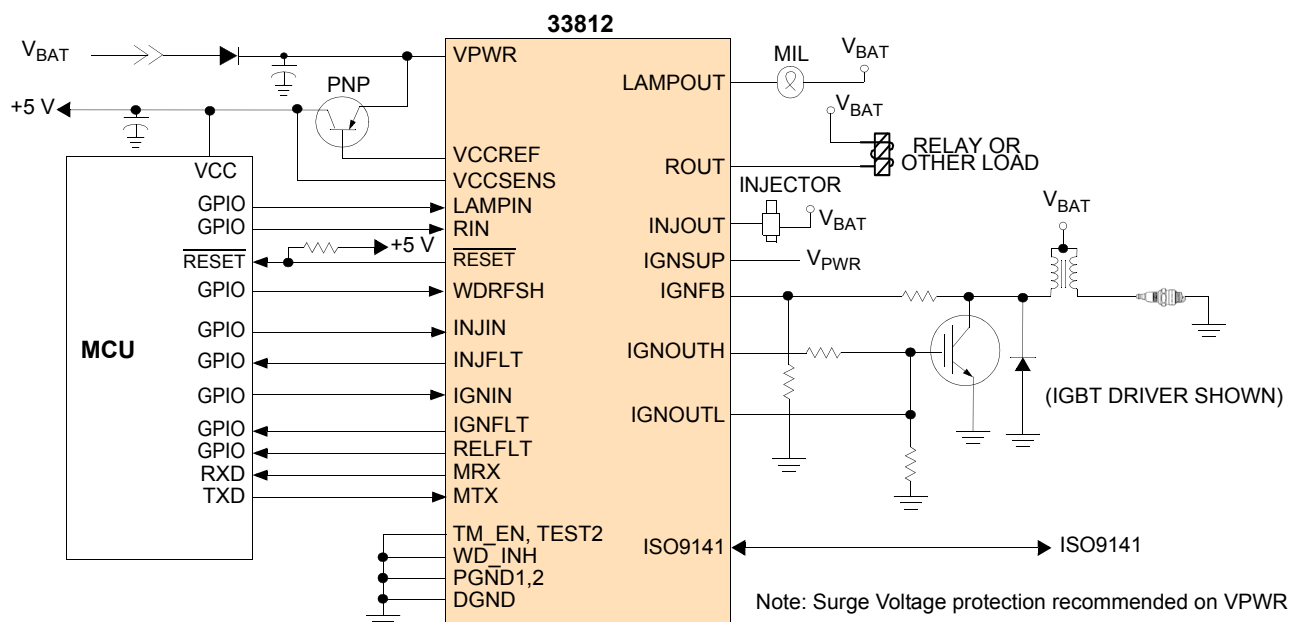


Figure 1. Simplified application diagram

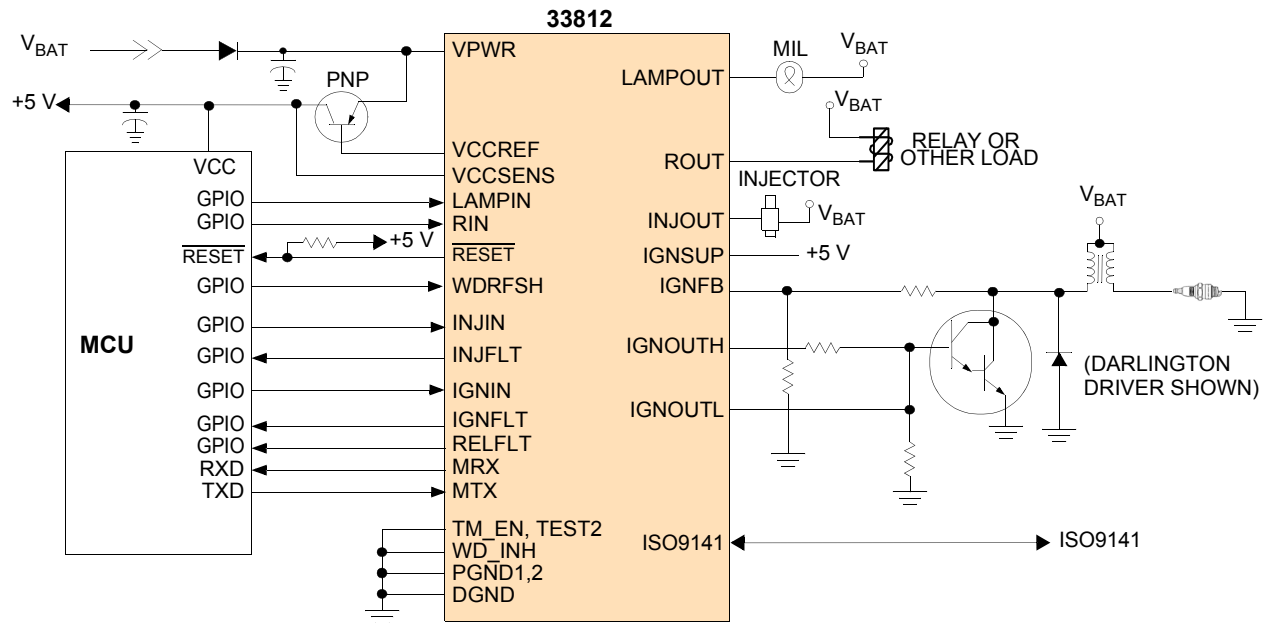


Figure 2. Simplified application diagram (Darlington mode)

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# 1 Orderable parts

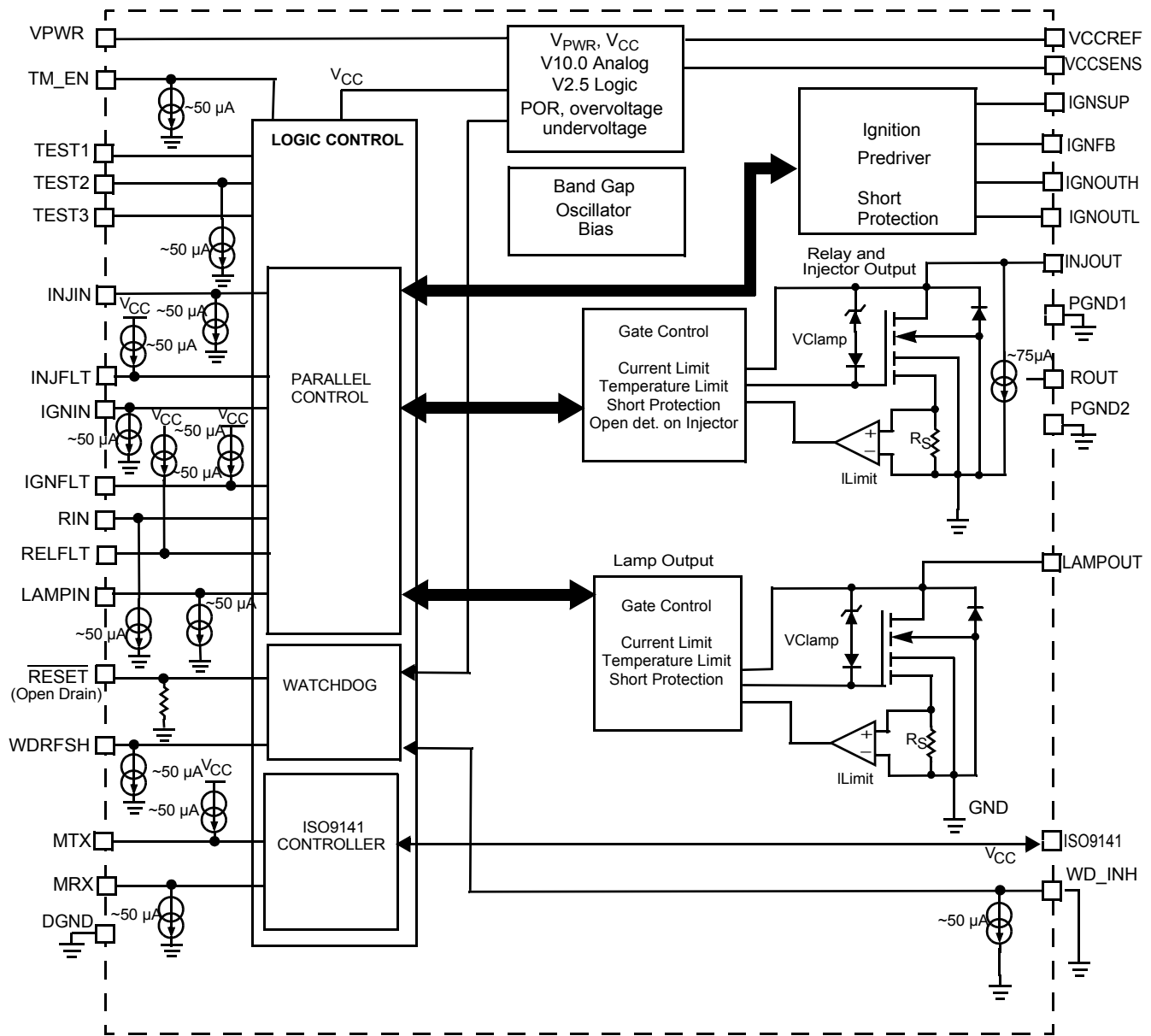
Table 1. Orderable part variations

| Part number | Temperature (T <sub>A</sub> ) | Package                      | Notes |
|-------------|-------------------------------|------------------------------|-------|
| MC33812EK   | -40 °C to 125 °C              | 98ASA10556D, 32-pin SOICW-EP | (1)   |

Notes

1. For Tape and Reel, add an R2 suffix to the part number.

## 2 Internal block diagram



\*Note: Pull-up and pull-down current sources are ~50 µA unless otherwise noted

Figure 3. Simplified internal block diagram

## 3 Pin connections

### 3.1 Pinout diagram

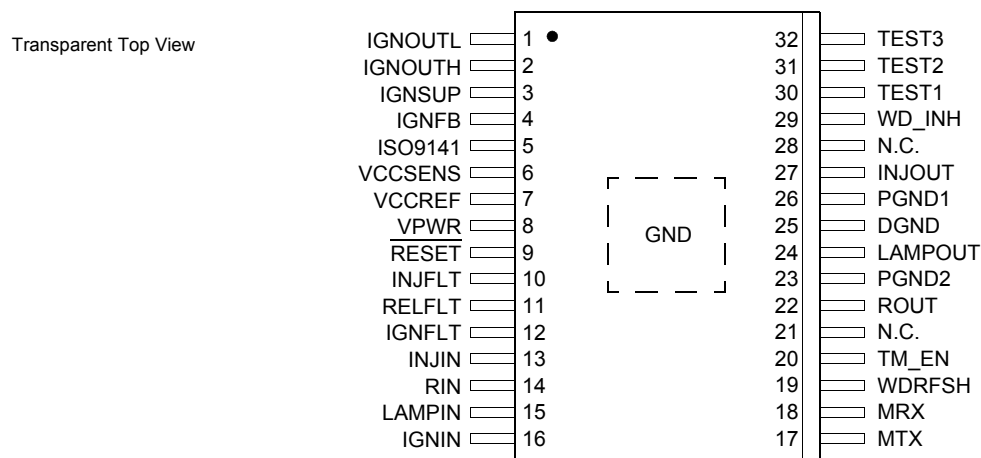


Figure 4. Pin connections

Table 2. Pin definitions

| Pin | Pin name | Pin function | Formal name                                     | Description  |
|-----|----------|--------------|---|--|
| 1   | IGNOUTL  | Output       | Ignition Output Low                             | Low-side output to drive Gate/Base of IGBT/Bipolar Darlington  |
| 2   | IGNOUTH  | Output       | Ignition Output High                            | High-side output to drive Gate/Base of IGBT/Bipolar Darlington   |
| 3   | IGNSUP   | Input        | Ignition Output Supply                          | Tie to +5.0 V for Darlington, tie to the $V_{PWR}$ supply for IGBT output device   |
| 4   | IGNFB    | Input        | Feedback from Source                            | Voltage feedback from source of Ignition driver transistor through 10:1 voltage divider  |
| 5   | ISO9141  | Input/Output | ISO9141 K-Line Bidirectional Serial Data Signal | The ISO9141 pin is $V_{PWR}$ level IN/OUT signal connected to external ECU Tester using ISO9141 protocol. The output is open drain and the Input is a ratiometric $V_{PWR}$ level threshold comparator |
| 6   | VCCSENS  | Input        | Voltage Sense from VCC                          | Feedback to internal $V_{CC}$ regulator from external pass transistor  |
| 7   | VCCREF   | Output       | VCC Reference Base drive                        | Base drive voltage for external PNP pass transistor  |
| 8   | VPWR     | Supply Input | Main Voltage Supply Input                       | VPWR is the main voltage supply Input for the device. Connected to +12 volt battery (It should have reverse battery protection and transient suppression)  |
| 9   | RESET    | Output       | Reset Output to MCU                             | Logic Level Reset signal used to reset the MCU when the watchdog circuit times out, during undervoltage conditions on VCC and for initial power up and power down                                      |
| 10  | INJFLT   | Output       | Injector Fault                                  | Logic Level output to MCU indicating any fault in the injector circuit   |
| 11  | RELFLT   | Output       | Relay Fault                                     | Logic Level output to MCU indicating any fault in the relay circuit  |
| 12  | IGNFLT   | Output       | Ignition Fault                                  | Logic Level output to MCU indicating any fault in the ignition circuit   |
| 13  | INJIN    | Input        | Injector Parallel Input                         | Logic Level input from the MCU to control the injector driver output   |
| 14  | RIN      | Input        | Relay Parallel Input                            | Logic Level Parallel input to activate RELAY output, ROUT  |
| 15  | LAMPIN   | Input        | LAMP Parallel Input                             | Logic Level Parallel input to activate the malfunction indicator lamp output, LAMP   |
| 16  | IGNIN    | Input        | Ignition Parallel Input                         | Logic Level Input from MCU controlling the ignition coil current flow and spark.   |
| 17  | MTX      | Input        | ISO9141 MCU Data Input                          | Input logic level ISO9141 data from the MCU to the ISO9141 IN/OUT pin  |
| 18  | MRX      | Output       | Low-side Driver Output                          | Output logic level ISO9141 data to the MCU from the ISO9141 IN/OUT pin   |
| 19  | WDRFSH   | Input        | Watchdog Refresh                                | Logic level input from MCU to refresh the watchdog circuit to prevent RESET  |
| 20  | TM_EN    | Input        | Test Mode Enable                                | Used by NXP test engineering, tie to Gnd in operation  |

**Table 2. Pin definitions**

| Pin | Pin name | Pin function | Formal name            | Description   |
|-----|----------|--------------|------------------------|---|
| 21  | N.C.     | Unused       | -----                  | Unused pin, leave open  |
| 22  | ROUT     | Output       | Relay Driver Output    | Low-side relay driver output driven by parallel input RIN                                       |
| 23  | PGND2    | Ground       | Power Ground 2         | Ground for RELAY driver output  |
| 24  | LAMPOUT  | Output       | Warning Lamp Output    | Low-side driver output for MIL (warning lamp) driven by parallel input LAMPIN                   |
| 25  | DGND     | Ground       | Supply Ground          | Tied to ground plane, used for ground for all low power signals                                 |
| 26  | PGND1    | Ground       | Power Ground 1         | Ground for INJOUT injector driver output  |
| 27  | INJOUT   | Output       | Injector Driver Output | Low-side driver output for Injector driven by parallel input INJIN                              |
| 28  | N.C.     | Unused       | -----                  | Unused pin, leave open  |
| 29  | WD_INH   | Input        | Watch Dog Inhibit      | Normally tied to GND, if tied high through a pull-up, it inhibits RESET from a watchdog timeout |
| 30  | TEST1    | Input        | Test 1                 | MUST be tied to GND   |
| 31  | TEST2    | Input        | Test 2                 | MUST be tied to GND   |
| 32  | TEST3    | Input        | Test 3                 | MUST leave OPEN   |
| EP  | GND      | Ground       | Substrate Ground       | Should be tied to DGND  |

## 4 Electrical characteristics

### 4.1 Maximum ratings

**Table 3. Maximum ratings**

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol   | Rating  | Value  | Unit            | Notes |
|--|---|--|-----------------|-------|
| V <sub>PWR</sub>   | VPWR Supply Voltage   | -0.3 to 45   | V <sub>DC</sub> | (2)   |
| V <sub>IL</sub>  | Logic Input Voltage (MTX, INJIN, IGNIN, WDRFSH, LAMPIN, RIN)  | -0.3 to V <sub>CC</sub>  | V <sub>DC</sub> |       |
| V <sub>INJOUT</sub><br>V <sub>RELOUT</sub>                                       | Injector and RELAY Low-side Driver Drain Voltage (V <sub>INJOUT</sub> )   | -0.3 to V <sub>CLAMP_INJ</sub><br>-0.3 to V <sub>CLAMP_REL</sub> | V <sub>DC</sub> |       |
| LAMP <sub>OUT</sub>  | Lamp Low-side Driver Drain Voltage (LAMP <sub>OUT</sub> )   | -0.3 to V <sub>CLAMP_LAMP</sub>                                  | V <sub>DC</sub> |       |
| E <sub>CLAMP_INJ_SP</sub><br>E <sub>CLAMP_REL_SP</sub>                           | Output Clamp Energy (INJOUT and ROUT) (Single Pulse)<br>T <sub>JUNCTION</sub> = 150 °C, I <sub>OUT</sub> = 1.5 A  | 100  | mJ              |       |
| E <sub>CLAMP_INJ_CP</sub><br>E <sub>CLAMP_REL_CP</sub>                           | Output Clamp Energy (INJOUT and ROUT) (Continuous operation)<br>T <sub>JUNCTION</sub> = 125 °C, I <sub>OUT</sub> = 1.0 A, (Max. frequency is 70 Hz, Maximum Duty Cycle 90%) | 100  | mJ              |       |
| I <sub>OCC_MAX</sub>   | Output Continuous Current (INJOUT and ROUT) T <sub>JUNCTION</sub> = 150 °C  | 2.0  | A               |       |
| E <sub>CLAMP_LAMP_SP</sub>   | Output Clamp Energy (LAMP <sub>OUT</sub> ) (Single Pulse) - T <sub>JUNCTION</sub> = 150 °C, I <sub>OUT</sub> = 0.5 A  | 35   | mJ              |       |
| V <sub>ESD1</sub><br>V <sub>ESD2</sub><br>V <sub>ESD3</sub><br>V <sub>ESD4</sub> | ESD Voltage<br>• Human Body Model<br>• Machine Model<br>• Charge Device Model (Corner pins)<br>• Charge Device Model  | ±2000<br>±200<br>±750<br>±500                                    | V               | (3)   |

#### THERMAL RATINGS

|  |  |  |      |          |
|--|--|--|------|----------|
| T <sub>A</sub><br>T <sub>J</sub><br>T <sub>C</sub>       | Operating Temperature<br>• Ambient<br>• Junction<br>• Case                               | -40 to 125<br>-40 to 150<br>-40 to 125 | °C   |          |
| T <sub>STG</sub>   | Storage Temperature  | -55 to 150                             | °C   |          |
| P <sub>D</sub>   | Power Dissipation (T <sub>A</sub> = 25°C)  | 1.7                                    | W    | (6)      |
| T <sub>SOLDER</sub>                                      | Peak Package Reflow Temperature During Solder Mounting                                   | Note 5                                 | °C   | (4), (5) |
| R <sub>θJA</sub><br>R <sub>θJL</sub><br>R <sub>θJC</sub> | Thermal Resistance<br>• Junction-to-Ambient<br>• Junction- to-Lead<br>• Junction-to-Flag | 75<br>8.0<br>1.2                       | °C/W |          |

#### Notes

- Exceeding these limits may cause malfunction or permanent damage to the device.
- ESD testing is performed in accordance with the Human Body Model (HBM) (C<sub>ZAP</sub> = 100 pF, R<sub>ZAP</sub> = 1500 Ω), the Machine Model (MM) (C<sub>ZAP</sub> = 200 pF, R<sub>ZAP</sub> = 0 Ω), and the Charge Device Model (CDM), Robotic (C<sub>ZAP</sub> = 4.0 pF).
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.nxp.com](http://www.nxp.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx)], and review parametrics.
- This parameter is guaranteed by design, but is not production tested.



## 4.2 Static electrical characteristics

**Table 4. Static electrical characteristics**

Characteristics noted under conditions of  $7.0\text{ V} \leq V_{\text{PWR}} \leq 18\text{ V}$ ,  $-40\text{ }^{\circ}\text{C} \leq T_{\text{C}} \leq 125\text{ }^{\circ}\text{C}$ , unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with  $V_{\text{PWR}} = 14\text{ V}$ ,  $T_{\text{A}} = 25\text{ }^{\circ}\text{C}$ .

| Symbol  | Characteristic  | Min.        | Typ.             | Max.          | Unit          | Notes |
|---|---|-------------|------------------|---------------|---------------|-------|
| <b>POWER INPUT (VPWR)</b>   |   |             |                  |               |               |       |
| $V_{\text{PWR(FO)}}$<br>$V_{\text{PWR(FP)}}$  | Supply Voltage (measured at VPWR pin)<br>• Fully Operational<br>• Full Parameter Specification  | 4.7<br>7.0  | –<br>–           | 36<br>18      | V             | (7)   |
| $I_{\text{VPWR(ON)}}$   | Supply Current - All Outputs Disabled (Normal Mode)   | –           | 10.0             | 14.0          | mA            |       |
| $V_{\text{PWR(OV)}}$  | $V_{\text{PWR}}$ Overvoltage Shutdown Threshold Voltage   | 36.5        | 39               | 42            | V             | (8)   |
| $V_{\text{PWR(OV-HYS)}}$  | $V_{\text{PWR}}$ Overvoltage Shutdown Hysteresis Voltage  | 0.5         | 1.5              | 3.0           | V             |       |
| $V_{\text{PWR(UV)}}$  | $V_{\text{PWR}}$ Undervoltage Shutdown Threshold Voltage  | 3.0         | 3.7              | 4.4           | V             | (8)   |
| $V_{\text{PWR(UV-HYS)}}$  | $V_{\text{PWR}}$ Undervoltage Shutdown Hysteresis Voltage   | 100         | 200              | 300           | mV            |       |
| <b>VOLTAGE REGULATOR OUTPUTS (VCCREF, VCCSENS)</b>  |   |             |                  |               |               |       |
| $V_{\text{SENS}}$   | VCCSENS (VCC) Output Voltage (measured with external output PNP (FZT753 typical) transistor and 500 $\Omega$ Load on VCCSENS)   | 4.9         | 5.0              | 5.1           | V             |       |
| $I_{\text{VCCREF}}$   | VCCREF Output Current   | –           | -5.0             | –             | mA            | (9)   |
| $I_{\text{VCCCL}}$  | VCCREF Current Limit  | 5.0         | 15               | 20            | mA            |       |
| $V_{\text{OCE}}$  | Output Capacitance External (ceramic, low ESR recommended)  | 2.2         | –                | –             | $\mu\text{F}$ |       |
| $I_{\text{VCCSENS}}$  | VCCSENS Input Current   | –           | 50               | 1000          | $\mu\text{A}$ |       |
| $\text{REG}_{\text{LINE\_VCC}}$   | Line Regulation (external output PNP transistor and 500 $\Omega$ Load on VCCSENS)   | –           | 2                | 25            | mV            |       |
| $\text{REG}_{\text{LOAD\_VCC}}$   | Load Regulation (external output PNP transistor and 500 $\Omega$ Load on VCCSENS)   | –           | 2                | 25            | mV            |       |
| $V_{\text{DROPOUT}}$  | Dropout Voltage (Minimal Input/Output Voltage at full load)   | –           | 46               | 200           | mV            |       |
| $\text{RESET}_{\text{UV\_VCC}}$   | $V_{\text{CC}}$ Undervoltage $\overline{\text{RESET}}$ Threshold Voltage  | 4.5         | 4.7              | 4.9           | V             |       |
| <b>LOW-SIDE DRIVER (INJOUT AND ROUT)</b>  |   |             |                  |               |               |       |
| $V_{\text{OUT(FLT-TH)}}$  | Output Fault Detection Voltage Threshold<br>Outputs programmed OFF (Open Load, Injector/Relay)<br>Outputs programmed ON (Short to Battery)  | 2.0         | 2.5              | 3.0           | V             | (10)  |
| $I_{\text{(OFF)OCO}}$   | Output OFF Open Load Detection Current (Injector/Relay)<br>• $V_{\text{DRAIN}} = 18\text{ V}$ , Outputs Programmed OFF  | 40          | 75               | 150           | $\mu\text{A}$ |       |
| $R_{\text{DS(ON)-INJ/REL}}$<br>$R_{\text{DS(ON)-INJ/REL}}$<br>$R_{\text{DS(ON)-INJ/REL}}$ | Drain-to-Source ON Resistance<br>• $I_{\text{OUT}} = 1.0\text{ A}$ , $T_{\text{J}} = 125^{\circ}\text{C}$ , $V_{\text{PWR}} = 14\text{ V}$<br>• $I_{\text{OUT}} = 1.0\text{ A}$ , $T_{\text{J}} = 25^{\circ}\text{C}$ , $V_{\text{PWR}} = 14\text{ V}$<br>• $I_{\text{OUT}} = 1.0\text{ A}$ , $T_{\text{J}} = -40^{\circ}\text{C}$ , $V_{\text{PWR}} = 14\text{ V}$ | –<br>–<br>– | –<br>0.25<br>0.2 | 0.4<br>–<br>– | $\Omega$      |       |
| $I_{\text{OUT(LIM)-INJ/REL}}$   | Output Self Limiting Current  | 3.0         | –                | 6.0           | A             |       |
| $V_{\text{CLAMP\_INJ/REL}}$   | Output Clamp Voltage - $I_{\text{D}} = 20\text{ mA}$  | 48          | 53               | 58            | V             |       |

**Notes**

- Overvoltage thresholds minimum and maximum include hysteresis
- Undervoltage thresholds minimum and maximum include hysteresis, for disabling outputs only,  $\overline{\text{RESET}}$  based on  $V_{\text{CC}}$  undervoltage
- This parameter is guaranteed by design, however is not production tested.
- Output fault detect thresholds are the same for output open and shorts.

**Table 4. Static electrical characteristics (continued)**

Characteristics noted under conditions of  $7.0\text{ V} \leq V_{PWR} \leq 18\text{ V}$ ,  $-40\text{ }^{\circ}\text{C} \leq T_C \leq 125\text{ }^{\circ}\text{C}$ , unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with  $V_{PWR} = 14\text{ V}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ .

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|--------|----------------|------|------|------|------|-------|
|--------|----------------|------|------|------|------|-------|

**LOW-SIDE DRIVER (INJOUT AND ROUT) (CONTINUED)**

|                        |  |     |    |     |                    |      |
|------------------------|--|-----|----|-----|--------------------|------|
| $I_{OUT(LKG)-INJ}$     | Output Leakage Current (INJOUT)<br>• $V_{DRAIN} = 24\text{ V}$ , (Note: open load detection current can't be disabled) | –   | –  | 1.0 | mA                 |      |
| $I_{OUT(LKG)-REL}$     | Output Leakage Current (ROUT)<br>• $V_{DRAIN} = 24\text{ V}$ , (Note: open load detection current can't be disabled)   | –   | –  | 1.0 | mA                 |      |
| $T_{LIM-INJ/REL}$      | Overtemperature Shutdown   | 155 | –  | 190 | $^{\circ}\text{C}$ | (11) |
| $T_{LIM(HYS)-INJ/REL}$ | Overtemperature Shutdown Hysteresis  | 5.0 | 10 | 15  | $^{\circ}\text{C}$ | (11) |

**LOW-SIDE DRIVER (LAMP OUT)**

|                        |  |     |     |     |                    |      |
|------------------------|--|-----|-----|-----|--------------------|------|
| $R_{DS(on)LAMP}$       | Drain-to-Source ON Resistance<br>• $I_{OUT} = 300\text{ mA}$ , $T_J = 150\text{ }^{\circ}\text{C}$ , $V_{PWR} = 14\text{ V}$ | –   | –   | 1.0 | $\Omega$           |      |
| $I_{OUT(LIM)-LAMP}$    | Output Self Limiting Current   | 1.0 | –   | 2.5 | A                  |      |
| $V_{CLAMP-LAMP}$       | Output Clamp Voltage - $I_D = 20\text{ mA}$  | 48  | 53  | 58  | V                  |      |
| $I_{OUT(LKG)-LAMP}$    | Output Leakage Current<br>• $V_{DRAIN} = 24\text{ V}$ , (Note: no open load detection current)                               | –   | –   | 20  | $\mu\text{A}$      | (11) |
| $V_{OUT(FLT-TH)-LAMP}$ | Output Fault Detection Voltage Threshold<br>Outputs programmed ON (short to battery)   | 2.0 | 2.5 | 3.0 | V                  | (11) |
| $T_{LIM-LAMP}$         | Overtemperature Shutdown   | 155 | –   | 190 | $^{\circ}\text{C}$ | (11) |
| $T_{LIM(HYS)-LAMP}$    | Overtemperature Shutdown Hysteresis  | 5.0 | 10  | 15  | $^{\circ}\text{C}$ | (11) |

**IGNITION (IGBT/DARLINGTON) DRIVER PARAMETERS (IGNOUTL, IGNOUTH, IGNFB, IGNSUP)**

|  |  |        |                  |                                 |                    |      |
|--|--|--------|------------------|---------------------------------|--------------------|------|
| $R_{DS\_L(on)}$                          | Drain-to-Source ON Resistance<br>(IGNOUTL Output, Gate/Base Drive Turn Off Resistance)   | 150    | 300              | 400                             | $\Omega$           |      |
| $R_{DS\_H(on)}$                          | Drain-to-Source ON Resistance<br>(IGNSUP to IGNOUTH Output, Gate/Base Drive Turn On Resistance)  | –      | 70               | 90                              | $\Omega$           |      |
| $I_{GATEDRIVE\_H}$                       | Ignition Output High Source Current (IGNOUTH)  | 40     | 50               | –                               | mA                 |      |
| $PD\_IGNOUTH$                            | Ignition Output High (IGNOUTH) Device Power Dissipation  | –      | –                | 300                             | mW                 | (12) |
| $V_{IGNFB\_OUT(FLT-TH)}$                 | Output Fault Detection Voltage Threshold<br>(At IGNFB pin, not at input of 10:1 Voltage Divider)<br>Output programmed OFF (Open Load)<br>Output programmed ON (Short to Battery) | 100    | 250              | 400                             | mV                 | (13) |
| $I_{FBX(FLT-SNS)}$                       | Feedback Sense Current (FBX Input Current), $FBX = 2.0\text{ V}$ , Output Programmed OFF   | –      | –                | 1.0                             | $\mu\text{A}$      |      |
| $V_{IGNSUP\_IGBT}$<br>$V_{IGNSUP\_DARL}$ | IGNSUP Voltage for:<br>• IGBT<br>• Darlington  | –<br>– | $V_{PWR}$<br>5.0 | $V_{PWR\_MAX}$<br>$V_{CC\_MAX}$ | V                  | (13) |
| $T_{LIM-IGNOUTH,L}$                      | Overtemperature Shutdown on IGNOUTH and IGNOUTL  | 155    | –                | 190                             | $^{\circ}\text{C}$ | (13) |
| $T_{LIM(HYS)-IGNOUTH,L}$                 | Overtemperature Shutdown Hysteresis on IGNOUTH and IGNOUTL   | 5.0    | 10               | 15                              | $^{\circ}\text{C}$ | (13) |

**Notes**

11. This parameter is guaranteed by design, however is not production tested.
12. These parameters are guaranteed by design.
13. This parameter is guaranteed by design, however it is not production tested.

**Table 4. Static electrical characteristics (continued)**

Characteristics noted under conditions of  $7.0\text{ V} \leq V_{\text{PWR}} \leq 18\text{ V}$ ,  $-40\text{ }^{\circ}\text{C} \leq T_{\text{C}} \leq 125\text{ }^{\circ}\text{C}$ , unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with  $V_{\text{PWR}} = 14\text{ V}$ ,  $T_{\text{A}} = 25\text{ }^{\circ}\text{C}$ .

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|--------|----------------|------|------|------|------|-------|
|--------|----------------|------|------|------|------|-------|

**ISO9141 TRANSCEIVER PARAMETERS (ISO9141)**

|                        |   |                              |     |                             |    |      |
|------------------------|---|------------------------------|-----|-----------------------------|----|------|
| $V_{\text{IL\_ISO}}$   | Input Low Voltage at ISO I/O pin              | –                            | –   | $0.3 \times V_{\text{PWR}}$ | V  |      |
| $V_{\text{IH\_ISO}}$   | Input High Voltage at ISO I/O pin             | $0.7 \times V_{\text{PWR}}$  | –   | –                           | V  |      |
| $V_{\text{HYST\_ISO}}$ | Input Hysteresis at ISO I/O pin               | $0.15 \times V_{\text{PWR}}$ | –   | –                           |    |      |
| $V_{\text{OL\_ISO}}$   | Output Low Voltage at ISO I/O pin             | –                            | –   | $0.2 \times V_{\text{PWR}}$ | V  |      |
| $V_{\text{OH\_ISO}}$   | Output High Voltage at ISO I/O pin            | $0.8 \times V_{\text{PWR}}$  | –   | –                           | V  |      |
| $I_{\text{LIM\_ISO}}$  | Output Current Limit at ISO I/O pin (MTX = 0) | 50                           | 100 | 150                         | mA |      |
| $C_{\text{L\_ISO}}$    | Load Capacitance at ISO I/O pin               | 0.01                         | 3.0 | 10                          | nF | (14) |

**DIGITAL OUTPUTS (MRX, IGNFLT, RELFLT, INJFLT)**

|                 |   |                            |   |                            |   |  |
|-----------------|---|----------------------------|---|----------------------------|---|--|
| $V_{\text{OH}}$ | Output Logic High Voltage Level (at $I_{\text{OH}} = 1.0\text{ mA}$ load) | $0.8 \times V_{\text{CC}}$ | – | $V_{\text{CC}} + 0.2$      | V |  |
| $V_{\text{OL}}$ | Output Logic Low Voltage Level (at $I_{\text{OL}} = 1.0\text{ mA}$ load)  | GND                        | – | $0.1 \times V_{\text{CC}}$ | V |  |

**DIGITAL OUTPUT (RESET)**

|                    |   |     |   |     |            |  |
|--------------------|---|-----|---|-----|------------|--|
| $R_{\text{RESET}}$ | Resistance of Internal pull-down resistor on open drain RESET pin | 100 | – | 500 | k $\Omega$ |  |
|--------------------|---|-----|---|-----|------------|--|

**DIGITAL INPUTS (MTX, INJIN, IGNIN, LAMPIN, WDRFSH, RIN, WD\_INH)**

|                        |   |                            |     |                            |               |      |
|------------------------|---|----------------------------|-----|----------------------------|---------------|------|
| $V_{\text{IH}}$        | Input Logic High Voltage Thresholds                             | $0.7 \times V_{\text{CC}}$ | –   | $V_{\text{CC}} + 0.3$      | V             |      |
| $V_{\text{IL}}$        | Input Logic Low Voltage Thresholds                              | GND - 0.3                  | –   | $0.2 \times V_{\text{CC}}$ | V             |      |
| $V_{\text{IHYS}}$      | Input Logic Voltage Hysteresis                                  | 0.5                        | –   | 1.5                        | V             |      |
| $C_{\text{IN}}$        | Input Logic Capacitance   | –                          | –   | 20                         | pF            | (15) |
| $I_{\text{LOGIC\_PD}}$ | Input Logic Pull-down Current (all except MTX) - 0.8 V to 5.0 V | 30                         | 50  | 100                        | $\mu\text{A}$ |      |
| $I_{\text{LOGIC\_PU}}$ | Input Logic Pull-up Current (MTX only) - 0.8 V to 5.0 V         | -30                        | -50 | -100                       | $\mu\text{A}$ |      |

**Notes**

14. This parameter is guaranteed by design, however it is not production tested.
15. These parameters are guaranteed by design.

## 4.3 Dynamic electrical characteristics

**Table 5. Dynamic electrical characteristics**

Characteristics noted under conditions of  $7.0\text{ V} \leq V_{\text{PWR}} \leq 18\text{ V}$ ,  $-40\text{ }^{\circ}\text{C} \leq T_{\text{C}} \leq 125\text{ }^{\circ}\text{C}$ , unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with  $V_{\text{PWR}} = 14\text{ V}$ ,  $T_{\text{A}} = 25\text{ }^{\circ}\text{C}$ .

| Symbol                             | Characteristic  | Min. | Typ. | Max. | Unit             | Notes |
|------------------------------------|---|------|------|------|------------------|-------|
| <b>POWER INPUT</b>                 |   |      |      |      |                  |       |
| $t_{\text{UV}}$                    | Required Low State Duration on VPWR for Undervoltage Detect<br>$V_{\text{PWR}} \leq V_{\text{PWR\_UV}}$ | 1.0  | –    | –    | $\mu\text{s}$    | (16)  |
| <b>WATCHDOG TIMER</b>              |   |      |      |      |                  |       |
| $\text{WD}_{\text{MAX}}$           | Maximum Time Value Watchdog can be loaded with  | –    | –    | 10   | s                |       |
| $\text{WD}_{\text{LOAD}}$          | Maximum WDRFSH Pulse Width to load full Watchdog time value   | –    | –    | 1.0  | ms               |       |
| $\text{WDRFSH}_{\text{MIN}}$       | Minimum Pulse Width on WDRFSH to refresh Watchdog timer   | 1.0  | –    | –    | $\mu\text{s}$    |       |
| $\text{WD}_{\text{RESET}}$         | Reset Pulse Width when Watchdog times out   | 100  | –    | –    | $\mu\text{s}$    |       |
| <b>ISO9141 TRANSCEIVER</b>         |   |      |      |      |                  |       |
| $\text{ISO}_{\text{BR}}$           | Typical ISO9141 Data Rate   | –    | 10   | –    | kbps             | (16)  |
| $t_{\text{TXDF}}$                  | Turn OFF Delay MTX Input to ISO Output  | –    | –    | 2.0  | $\mu\text{s}$    |       |
| $t_{\text{RXDF}}, t_{\text{RXDR}}$ | Turn ON/OFF Delay ISO Input to MRX Output   | –    | –    | 1.0  | $\mu\text{s}$    |       |
| $t_{\text{RXR}}, t_{\text{RXF}}$   | Rise and Fall Time MRX Output (measured from 10% to 90%)  | –    | –    | 1.0  | $\mu\text{s}$    |       |
| $t_{\text{TXR}}, t_{\text{TXF}}$   | Maximum Rise and Fall Time MTX Input (measured from 10% to 90%)   | –    | –    | 1.0  | $\mu\text{s}$    | (16)  |
| <b>LAMP DRIVER</b>                 |   |      |      |      |                  |       |
| $t_{\text{OC(BLANK)}}$             | Inrush Current Blanking Time (LAMP-OUT only)  | 5.0  | 7.0  | 9.0  | ms               |       |
| $t_{\text{RETRY\_LAMP}}$           | LAMP-OUT, Automatic Retry Timer During Short to Battery Fault Condition                                 | 7.0  | 10   | 13   | ms               |       |
| <b>DIGITAL LOGIC OUTPUTS</b>       |   |      |      |      |                  |       |
| $t_{\text{R(DLO)}}$                | INJFLT, IGNFLT Output Signal Rise Time  | –    | 100  | 200  | ns               | (16)  |
| $t_{\text{F(DLO)}}$                | INJFLT, IGNFLT Output Signal Fall Time  | –    | 100  | 200  | ns               | (16)  |
| <b>INJECTOR AND RELAY DRIVER</b>   |   |      |      |      |                  |       |
| $t_{\text{SC}}$                    | Output ON Current Limit Fault Filter Timer  | 30   | 60   | 90   | $\mu\text{s}$    |       |
| $t_{\text{(OFF)OC}}$               | Output OFF Open Circuit Fault Filter Timer (INJECTOR and RELAY Driver)                                  | 100  | –    | 400  | $\mu\text{s}$    |       |
| $t_{\text{SR(RISE)}}$              | Output Slew Rate - Rise - $Z_{\text{LOAD}} = 14\text{ }\Omega$ , $V_{\text{LOAD}} = 14\text{ V}$        | 1.0  | 5.0  | 10   | V/ $\mu\text{s}$ |       |
| $t_{\text{SR(FALL)}}$              | Output Slew Rate - Fall - $Z_{\text{LOAD}} = 14\text{ }\Omega$ , $V_{\text{LOAD}} = 14\text{ V}$        | 1.0  | 5.0  | 10   | V/ $\mu\text{s}$ |       |
| <b>IGNITION PRE-DRIVER</b>         |   |      |      |      |                  |       |
| $t_{\text{(OFF)OC}}$               | Output OFF Open Circuit Fault Filter Timer  | 100  | –    | 400  | $\mu\text{s}$    |       |
| $t_{\text{(ON)(SC)}}$              | Output ON Short-circuit to Battery Fault Detection Timer  | 30   | 60   | 90   | $\mu\text{s}$    |       |

**Notes**

16. This parameter is guaranteed by design, however is not production tested.

## 5 Functional description

### 5.1 Functional pin description

#### 5.1.1 Supply input (VPWR)

The VPWR pin is battery input to the 33812 IC. A POR/LVI sub-circuit monitors this input's voltage level. The VPWR pin requires external reverse battery and transient protection.

#### 5.1.2 Output (VCCREF)

The VCCREF output pin is used to drive an external 5.0 V regulator PNP bipolar pass transistor.

#### 5.1.3 Input (VCCSENS)

The VCCSENS pin is used to monitor the +5.0 Volts from the external pass transistor's output. A POR is performed when the voltage on the VCCSENS pin goes from 0 to VCC.

#### 5.1.4 Digital ground (DGND)

The DGND pin provides ground reference for the digital inputs and outputs. The  $V_{CC}$  supply is referenced to the DGND pin.

#### 5.1.5 PGND1 and PGND2

The PGNDx pins provide power additional ground reference for the power outputs, ROUT, LAMPOUT, and INJOUT. The  $V_{PWR}$  supply is referenced to the PGND pins.

#### 5.1.6 Injector input (INJIN)

The INJIN pin is the parallel input controlling the Injector output, INJOUT. The INJIN pin is a logic level input with built-in pull-down to ground to prevent accidental actuation of the injector if the connection to the pin is lost.

#### 5.1.7 Injector and relay driver output (INJOUT/ROUT)

The INJOUT and ROUT output pins are the injector driver and relay driver outputs for the fuel Injector and the relay this IC supports. The relay driver and injector drivers are identical in operation and features. The injector driver output is controlled by the parallel input (INJIN) and the relay driver output is controlled by the parallel input (RIN). The injector and relay outputs are turned off during  $V_{PWR}$  overvoltage and undervoltage events. Open circuit (during off state), short to battery (during on state), and overtemperature faults are detected and annunciated as a logic high on the INJFLT and RELFLT lines. Overcurrent is limited by the current limiting circuitry, but is not annunciated unless the overcurrent is due to a short to battery. For either driver, when a fault condition is detected, the driver turns off, and when the fault condition clears, it tries to turn on again, if the input line goes low and then high.

#### 5.1.8 Lamp driver output (LAMPOUT)

The LAMPOUT output pin is the lamp driver, a low-side driver capable of driving an incandescent lamp. The current limit blanking time is set to allow the driver to handle the inrush current of a cold lamp filament. The LAMPOUT output is controlled by the parallel input pin (LAMPIN). The LAMPOUT low-side driver is protected against overtemperature, and short to battery. Unlike the Injector driver, when a fault condition is detected, the LAMPOUT driver turns off, but when the fault condition clears, it turns on again, while the input line, LAMPIN is high.

### 5.1.9 Pre-driver output, with feedback and supply voltage input (IGNSUP, IGNOUTL, IGNOUTH, IGNFB)

The IGNOUTL and IGNOUTH output pins are the low-side and high-side output pins of the Ignition pre-driver. They are used to drive either an IGBT or a Darlington BJT to control the ignition coil current to produce a spark. The choice of output device, IGBT or Darlington Bipolar Junction Transistor, is indicated by the choice of supply voltage on the IGNSUP pin.

When driving a Darlington bipolar transistor, the IGNSUP line must be tied to the +5.0 V supply. When driving an IGBT, the IGNSUP may be tied to a protected voltage source (e.g.  $V_{PWR}$ ) greater than +5.0 V to achieve the necessary gate drive voltage required by the IGBT. The high-side output device current limits if the circuit is forced to supply currents greater than the maximum indicated.

The IGNOUTL and IGNOUTH lines are controlled by the parallel input (IGNIN). The IGNOUT(L,H) outputs and the associated feedback pin, IGNFB, provide short to battery protection for the external driver transistor. A 10:1 voltage divider must be used on the feedback pin to prevent >400 Volt Ignition Coil flyback voltage from damaging the IC.

Open circuit (off state), short to battery (on state), and temperature limit threshold exceeded on the pre-driver stage are detected on the output, and all annunciated as a logic high on the IGNFLT line. There is no individual annunciation of these three fault conditions. The IGNFLT line goes high when any of the three fault conditions are present. If an overcurrent /short to battery fault condition, as defined by a  $V_{DS}$  greater than the  $V_{IGNFB\_OUT(FLT-TH)}$  is detected, the IGNOUTH or IGNOUTL turns off and does not turn on again until the fault condition has cleared and the IGNIN input line goes low and then high.

### 5.1.10 Outputs (INJFLT, RELFLT, IGNFLT)

The INJFLT, RELFLT and IGNFLT pins are the logic level outputs indicating when a fault condition has been detected on the INJOUT, ROUT or IGNOUT pins. These pins are normally low and go high when a fault is detected. Toggling the respective input pin clears the respective fault pin if the fault has been cleared.

### 5.1.11 K-Line communication (MTX, MRX, ISO9141)

These three pins are used to provide an ISO914, K-line communication link for the MCU to provide diagnostic support for the system. MRX is the +5.0 V logic level serial output line to the MCU. MTX is the +5.0 V logic level serial input to the IC from the MCU. The ISO9141 pin is a bidirectional line, consistent with the ISO9141 specification for signalling to and from the MCU.

### 5.1.12 Reset (RESET)

The  $\overline{\text{RESET}}$  pin is an open drain output. Without power on the circuit,  $\overline{\text{RESET}}$  is held low by an internal pull-down resistor. When power is applied to the circuit and the voltage on the  $V_{CC\_SENSE}$  pin reaches the lower voltage threshold, (5.0 volts - 2% = 4.9 V) the  $\overline{\text{RESET}}$  pin remains at a low level (open drain FET turned on) for a period of time equal to the value  $WD_{\text{RESET}}$ . After this time period, the  $\overline{\text{RESET}}$  pin then goes high and stays high until a watchdog  $\overline{\text{RESET}}$  is generated, or an undervoltage event on VCC occurs. The watchdog time and refresh features are controlled via the WDRFSH line.

### 5.1.13 Reload and Refresh time (WDRFSH)

The WDRFSH pin is an input supplied by an MCU output to set up the initial reload time,  $WD_{\text{RELOAD}}$ , and to refresh the watchdog timer. See the description of the watchdog timer for information on how to use this pin.

### 5.1.14 Watchdog Inhibit (WD\_INH)

The WD\_INH, watchdog inhibit pin, is normally tied to ground. If desired, during software development, it can be lifted from the ground pad and pulled high through an external pull-up resistor. When high, WD\_INH prevents the watchdog timer from causing a  $\overline{\text{RESET}}$  because of a watchdog timeout. The WD\_INH should not be connected to an MCU I/O pin or left floating in normal operation.

### 5.1.15 Test pins (TEST1, TEST2, and TEST3)

These three pins are used only by NXP test engineering during the production testing of the 33812. They are not to be used for any application purpose and must be handled as specified in the pinout section of this document.

## 6 Functional device operation

### 6.1 Operational modes

The 33812 has two states of operation, Normal state and Reset state.

#### 6.1.1 Reset state

Applying  $V_{PWR}$  to the device generates a Power On RESET (POR) placing the device in the RESET state. The Power On RESET circuit incorporates a timer to prevent high frequency transients from causing an erroneous POR. An undervoltage condition on VCC also places the device in the RESET state causing a RESET pulse to be generated on the RESET line. All RESETs pre-load the watchdog timer with the maximum time value,  $WD_{MAX}$ . The Watchdog begins counting on the rising edge of the pulse.

#### 6.1.2 NORMAL state

The NORMAL State is entered after the RESET line goes high. Control register settings from RESET are as follows:

- All Outputs Off
- Watchdog timer loaded with the  $WD_{MAX}$  time value

#### 6.1.3 Power supply

The 33812 is designed to operate from 4.5 V to 36 V on the VPWR pin. The VPWR pin supplies power to all internal regulators, analog and logic circuit blocks. The VCCREF output pin controls an external PNP bipolar transistor, such that the collector is driven to +5.0 V  $\pm 2\%$ . The VCCSENS input pin, connected to the collector of the PNP, is used to monitor the output voltage and provides the feedback to regulate the PNP collector to +5.0 V.

### 6.2 Injector driver operation

The open drain low-side driver (LSD) INJOUT is designed to control a fuel injector. The injector driver is controlled through the logic level parallel input pin, INJIN. When INJIN is high, the INJOUT pin is pulled to ground, turning on the fuel injector. When INJIN is low, the injector pulls the INJOUT output to VBAT and the injector is turned off. The INJOUT driver includes off state open load detection and its output device is protected against overcurrent, short to battery, overtemperature, inductive flyback overvoltage, and  $V_{PWR}$  overvoltage.

#### 6.2.1 INJOUT output protection features

##### 6.2.1.1 Overcurrent ( $I_{OUT-LIM}$ )

The Injector Driver protection scheme uses three separate protection schemes to prevent damage to the output device. The first protection scheme is deployed when an overcurrent event occurs. In this case, the current limiting circuitry attempts to limit the maximum current flow to the specified  $I_{LIM-INJ}$  value.

##### 6.2.1.2 Short to battery

The second protection scheme is invoked when the overcurrent fault is due to a hard short to battery. In this case, the protection circuitry, after the short detection filter time, turn off the output driver. The output does not try to turn on again until the INJIN input goes low and then high again. A short to battery is reported as a high logic level on the INJFLT line.

### 6.2.1.3 Temperature limit ( $T_{LIM}$ )

The third protection scheme deals with the junction temperature of the output device. Any time the maximum temperature limit on the output device is exceeded ( $T_{LIM}$ ), the device shuts down until the junction temperature falls below this maximum temperature minus the hysteresis temperature value. The  $T_{LIM}$  hysteresis value is  $T_{LIM(HYST)}$ .

The maximum temperature ( $T_{LIM}$ ) protection scheme controls the output device regardless of the state of the INJIN input. The device is unable to be activated until the junction temperature falls below this maximum temperature minus the hysteresis temperature value. An overtemperature fault is also reported as a high logic level on the INJFLT line.

### 6.2.1.4 Overvoltage ( $V_{CLAMP-INJ}$ and $V_{PWR(OV)}$ )

The injector driver is also protected against two types of overvoltage conditions:

- When the  $V_{PWR}$  supply exceeds the  $V_{PWR(OV)}$  threshold, the INJOUT output turns off and stays off until the overvoltage condition abates and the INJIN input pin toggles low and then high again.
- The output device controls inductive flyback voltages by an active clamping network that limits the voltage across the output device to  $V_{CLAMP-INJ}$  volts.

## 6.2.2 INJOUT fault detection features

### 6.2.2.1 Off state, Open load detection

An open load on the injector driver is detected by the voltage level on the drain of the output device in the off state. Internal to the device is a pull-down current source. In the event of an open injector the drain voltage is pulled low. When the voltage crosses the open load detection threshold, an open load is detected. The open load fault detect threshold is set internally and is not programmable. The open load fault is reported as a high logic level on the INJFLT line.

### 6.2.2.2 On state, Shorted load detection

The INJOUT driver is capable of detecting a shorted injector load (short to battery) in the on state. A shorted load fault is reported when the drain pin voltage is greater than the preset short threshold voltage. The shorted load fault detect threshold is set internally and is not programmable. The shorted load fault is reported as a high logic level on the INJFLT line.

### 6.2.2.3 Clearing the INJFLT line

When the INJFLT line goes high for any of the following reasons, while the INJIN line is high (on state):

- Short to battery
- Overtemperature
- Overvoltage
- Open load

The INJFLT line remains high until the INJIN line goes to a low logic level and then returns high (rising edge).



## 6.3 Ignition pre-driver operation

The Ignition pre-driver output is controlled by the logic level input IGNIN. When IGNIN is high the IGNOUTH pin is pulled high to IGNSUP. When the IGNIN pin is low, the IGNOUTL line is pulled to ground turning off the driver Darlington or IGBT. The IGNOUT pre-driver protects the output device against overcurrent, short to battery, and VPWR overvoltage.

### 6.3.1 IGNOUT output protection features

#### 6.3.1.1 Overcurrent and short to battery ( $I_{LIM}$ )

The Ignition Pre-driver protection scheme senses overcurrent in the driver device by monitoring the voltage at the IGNFB pin. Since this pin is protected by a 10:1 voltage divider, the overcurrent threshold voltage is set internally to 1/10 of the voltage expected on the drain or collector of the output device in an overcurrent situation. Since the Ignition output device is external to the 33812, a short to battery is the same as an overcurrent fault. An overcurrent fault or short to battery is reported as a high logic level on the IGNFLT line.

#### 6.3.1.2 Temperature limit ( $T_{LIM}$ )

Since the Ignition output device is external to the 33812, there is no overtemperature protection provided.

### 6.3.2 IGNOUT fault detection features

#### 6.3.2.1 Off state, Open load detection

An open load on the ignition driver external device is detected by the voltage level on the drain or collector of the output device in the off state (through a 10:1 voltage divider). In the event of an open ignition coil the drain/collector voltage is pulled low. When the voltage crosses the open load detection threshold, an open load is detected. The open load fault detect threshold is set internally and is not programmable. An open load fault is reported as a high logic level on the IGNFLT line.

#### 6.3.2.2 Overvoltage ( $V_{PWR(OV)}$ )

The Ignition pre-driver is also protected against an overvoltage condition:

When the VPWR supply exceeds the  $V_{PWR(OV)}$  threshold, the IGNOUTL and IGNOUTH outputs turn off and stays off until the overvoltage condition clears and the next rising edge of the IGNIN input pin.

#### 6.3.2.3 Clearing the IGNFLT line

When the IGNFLT line goes high for any of the following reasons, while the IGNIN line is high (on state):

- Short to battery
- Overvoltage
- Overtemperature of the IGNOUTL and IGNOUTH transistors
- Open load

The IGNFLT line remains high until the IGNIN line goes to the low logic level and then returns high.

## 6.4 Relay driver operation

The Relay Driver (ROUT) is a low-side driver controlled by the logic level RIN input pin. When RIN is high, the ROUT pin is pulled to ground, turning on an external relay or other device. When RIN is low, the relay coil pulls the ROUT output to  $V_{BAT}$ , and the relay is turned off. The ROUT driver includes off state open load detection and its output device is protected against overcurrent, short to battery, overtemperature, inductive flyback overvoltage, and VPWR overvoltage. The relay driver is functionally and electrically identical to the Injector driver and can be used as a second Injector driver, for two cylinder applications, as long as maximum power dissipation considerations are observed.

## 6.4.1 ROUT protection features

### 6.4.1.1 Overcurrent ( $I_{OUT-LIM\ ROUT}$ )

The ROUT Driver protection scheme uses three separate protection schemes to prevent damage to the output device. The first protection scheme is deployed when an overcurrent event occurs. In this case, the current limiting circuitry attempts to limit the maximum current flow to the specified  $I_{OUT\ LIM-REL}$  value.

### 6.4.1.2 Short to battery

The second protection scheme is invoked when the overcurrent fault is due to a hard short to battery. In this case, the protection circuitry, after the short detection filter time, turns off the output driver. The output does not try to turn on again until the RIN input goes low and then high again. A short to battery is reported as a high logic level on the RELFLT line.

### 6.4.1.3 Temperature limit ( $T_{LIM}$ )

The third protection scheme deals with the junction temperature of the output device. Any time the maximum temperature limit on the output device is exceeded ( $T_{LIM}$ ), the device shuts down until the junction temperature falls below this maximum temperature minus the hysteresis temperature value. The  $T_{LIM}$  hysteresis value is  $T_{LIM(HYST)}$ .

The maximum temperature ( $T_{LIM}$ ) protection scheme controls the output device regardless of the state of the RIN input. The device is unable to be activated until the junction temperature falls below this maximum temperature minus the hysteresis temperature value. An overtemperature fault is also reported as a high logic level on the RELFLT line.

### 6.4.1.4 Overvoltage ( $V_{CLAMP-REL}$ and $V_{PWR(OV)}$ )

The relay driver is also protected against two types of overvoltage conditions:

- When the VPWR supply exceeds the  $V_{PWR(OV)}$  threshold, the ROUT output turns off and stays off until the overvoltage condition abates and the RN input pin toggles low and then high again.
- The output device is protected against inductive flyback voltages greater than  $V_{CLAMP-REL}$  by an active clamping network that limits the voltage across the output device to  $V_{CLAMP-REL}$  volts.

## 6.4.2 ROUT fault detection features

### 6.4.2.1 Off state, open load detection

An open load on the relay driver is detected by the voltage level on the drain of the output device in the off state. Internal to the device is a pull-down current source. In the event of an open injector, the drain voltage is pulled low. When the voltage crosses the open load detection threshold, an open load is detected. The open load fault detect threshold is set internally and is not programmable. The open load fault is reported as a high logic level on the RELFLT line.

### 6.4.2.2 On state, Shorted load detection

The ROUT driver is capable of detecting a shorted load (short to battery) in the on state. A shorted load fault is reported when the drain pin voltage is greater than the preset short threshold voltage. The shorted load fault detect threshold is set internally and is not programmable. The shorted load fault is reported as a high logic level on the RELFLT line.

### 6.4.2.3 Clearing the RELFLT line

When the RELFLT line goes high for any of the following reasons, while the RIN line is high (on state):

- Short to battery
- Overtemperature
- Overvoltage
- Open load

The RELFLT line remains high until the RIN line goes to a low logic level and then returns high (rising edge).

## 6.5 Lamp driver operation

The Lamp Driver is a low side driver controlled by the logic level LAMPIN input pin. When LAMPIN is high, the LAMP pin is pulled to ground, turning on an external bulb or LED. When LAMPIN is low, the bulb or LED pulls the LAMP output to  $V_{BAT}$ , and the lamp is turned off.

### 6.5.1 LAMPOUT protection features

#### 6.5.1.1 Overcurrent ( $I_{OUT-LIM-LAMP}$ )

The LAMPOUT Driver protection scheme uses three separate protection schemes to prevent damage to the output device. The first protection scheme is deployed when an overcurrent event occurs. In this case, the current limiting circuitry attempts to limit the maximum current flow to the specified  $I_{OUT-LIM-LAMP}$  value.

#### 6.5.1.2 Short to battery

The second protection scheme is invoked when the overcurrent fault is due to a hard short to battery. In this case, the protection circuitry, after the short detection filter time, turns off the output driver. There is an internal retry timer to try to turn on again if the fault clears. There is no annunciation of any LAMPOUT faults.

#### 6.5.1.3 Temperature limit ( $T_{LIM}$ )

The third protection scheme deals with the junction temperature of the output device. Any time the maximum temperature limit on the output device is exceeded ( $T_{LIM}$ ), the device shuts down until the junction temperature falls below this maximum temperature minus the hysteresis temperature value. The  $T_{LIM}$  hysteresis value is  $T_{LIM(HYST)}$ . The maximum temperature ( $T_{LIM}$ ) protection scheme controls the output device regardless of the state of the LAMPIN input. The device is unable to be activated until the junction temperature falls below this maximum temperature minus the hysteresis temperature value.

## 6.6 LAMPOUT fault detection features

### 6.6.1 Off state, Open load detection

Since there is no way to annunciate an open load fault for the lamp output driver, no open load fault detection is performed by the 33812.

### 6.6.2 On state, Shorted load detection

Even though there is no way to annunciate a shorted load fault for the lamp output driver, shorted fault detection is performed by the 33812 as part of the protection for the output FET. The LAMPOUT driver also has an overcurrent blanking time of  $t_{OC(BLANK)}$  to allow for incandescent lamp inrush current

## 6.7 Over/undervoltage shutdown strategy

The behavior of the outputs after an overvoltage or undervoltage event on VPWR is listed in [Table 6](#).

**Table 6. Overvoltage/undervoltage truth table**

| Output  | State Before OV or UV | State When Returning From Overvoltage | State When Returning From Undervoltage |
|---------|-----------------------|---------------------------------------|--|
| INJOUT  | X                     | OFF                                   | OFF                                    |
| IGNOUT  | X                     | OFF                                   | OFF                                    |
| ROUT    | OFF                   | OFF                                   | OFF                                    |
| ROUT    | ON                    | ON                                    | OFF                                    |
| LAMPOUT | OFF                   | OFF                                   | OFF                                    |
| LAMPOUT | ON                    | ON                                    | OFF                                    |

## 6.8 Watchdog timer operation

The purpose of the watchdog timer is to provide a  $\overline{\text{RESET}}$  to the MCU whenever the MCU is locked up in a loop or otherwise hung up, perhaps by executing erroneous code, such as a HALT instruction. The watchdog timer is initialized by a power on RESET or a RESET occurring after a fault such as an undervoltage event on VCC.

Whenever the watchdog timer is refreshed, it is always reloaded with the value  $\text{WD}_{\text{RELOAD}}$ , which initially has a value of  $\text{WD}_{\text{MAX}}$  seconds. Whenever a RESET occurs, the  $\text{WD}_{\text{RELOAD}}$  value is set to  $\text{WD}_{\text{MAX}}$  seconds and the watchdog timer is re-loaded with this value. When the RESET pulse returns high, and, if the WDRFSH line is low, the watchdog timer starts counting. If the watchdog timer reaches the  $\text{WD}_{\text{MAX}}$  value before the next rising edge on the WDRFSH line, the watchdog circuit generates a  $\overline{\text{RESET}}$  pulse to the MCU and reload itself with the maximum time value of  $\text{WD}_{\text{RELOAD}}$ , which has been set back to  $\text{WD}_{\text{MAX}}$  seconds.

In normal operation, the MCU issues a WDRFSH pulse, periodically, which re-loads the watchdog timer with the  $\text{WD}_{\text{RELOAD}}$  value and starts the counting again, thus avoiding a watchdog timer generated  $\overline{\text{RESET}}$  pulse. When the watchdog timer is refreshed by a WDRFSH pulse, before the watchdog timer reaches the programmed value, the refresh prevents a  $\overline{\text{RESET}}$  pulse from being issued to the MCU.

### 6.8.1 Loading the Watchdog timer and $\text{WD}_{\text{RELOAD}}$

Aside from the  $\overline{\text{RESET}}$  case, which always loads the  $\text{WD}_{\text{RELOAD}}$  value and the watchdog timer with the maximum time value,  $\text{WD}_{\text{MAX}}$ , there is an additional way that the watchdog timer and the value  $\text{WD}_{\text{RELOAD}}$  can be re-loaded. During initialization, if the WDRFSH pulse width is greater than  $\text{WD}_{\text{LOAD}}$ , both the watchdog timer and the value  $\text{WD}_{\text{RELOAD}}$  loads with a timer count value, corresponding to the width of the pulse present on the WDRFSH input. Once this value is set, no further setting of the  $\text{WD}_{\text{LOAD}}$  value is possible until a RESET is performed.

Once the WDRFSH input goes low, the watchdog timer begins incrementing again, counting up to the new value loaded into the reload register. The watchdog must be refreshed by another pulse on the WDRFSH line, before the watchdog timer counts up to the reload value, or else a RESET pulse is generated and sent to the MCU.

If the WDRFSH line is ever kept high for longer than  $\text{WD}_{\text{RELOAD}}$  seconds, the watchdog issues an immediate  $\overline{\text{RESET}}$  to the MCU. Upon receiving a RESET input from the 33812, the MCU should always be programmed to bring the WDRFSH line low to avoid being locked in a “deadly embrace” condition where the MCU and 33812 alternate back and forth between the RESET and Normal states.

### 6.8.2 Disabling the Watchdog timer

If the  $\text{WD}_{\text{INH}}$  line is pulled high through a pull-up resistor of 10 K or less, (i.e. not tied to ground), the watchdog timer is inhibited from issuing a  $\overline{\text{RESET}}$  to the MCU, while the line is held in this state. This “watchdog Inhibited” state should only be used during software testing and development to avoid being concerned about an inadvertent watchdog RESET.

## 6.8.2.1 Watchdog timing diagrams

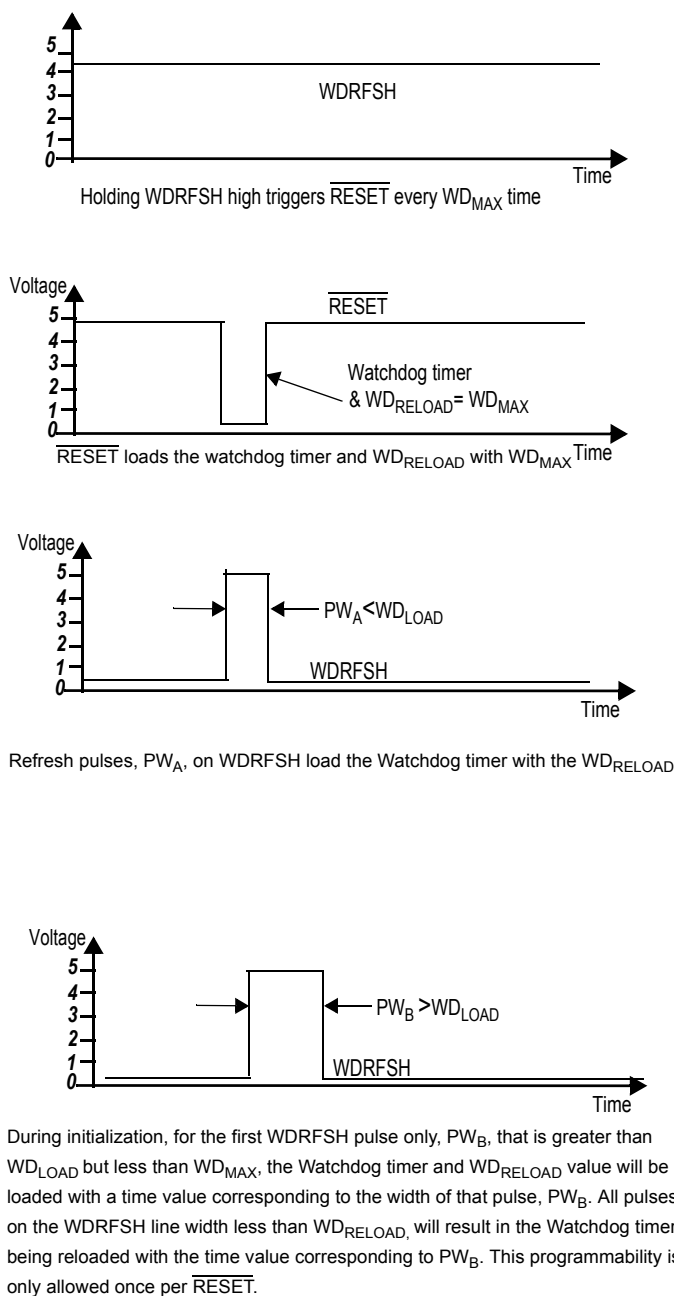


Figure 5. Watchdog loaded with  $\text{WD}_{\text{MAX}}$

## **6.9 ISO-9141 transceiver operation**

### **6.9.1 Bus I/O pin (ISO9141)**

This I/O pin represents the single-wire bus transmitter and receiver.

### **6.9.2 Transmitter characteristics**

The ISO-9141 bus transmitter is a low-side MOSFET with internal overcurrent thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated so no external pull-up components are required for the application in a slave node. Voltage can go from -18 V to 40 V without current supplied from any other source than the pull-up resistance. The ISO9141 pin exhibits no reverse current from the ISO9141 bus line to VPWR, even in the event of GND shift or VPWR disconnection. The transmitter has one slew rate (normal slew rate)

### **6.9.3 Receiver characteristics**

The receiver thresholds are ratiometric with the VPWR supply pin.

## 7 Typical applications

### 7.1 Low-voltage operation

During a low voltage condition ( $4.5\text{ V} < V_{\text{PWR}} < 9.0\text{ V}$ ) the device operates as described in the functional description, however, certain parameters listed in the tables may be out of specification. Fault condition annunciation is not guaranteed below the minimum parametric operating voltage.

### 7.2 Low-side injector driver voltage clamp

The Injector output of the 33812 incorporates an internal voltage clamp to provide fast turn OFF and transient protection. Each clamp independently limits the drain-to-source voltage to  $V_{\text{CLAMP\_INJ}}$ . The total energy clamped ( $E_J$ ) can be calculated by multiplying the peak current ( $I_{\text{PEAK}}$ ) times the clamp voltage ( $V_{\text{CL}}$ ) times the Time ( $\tau$ ) all divided by 2 (see [Figure 6](#)). Characterization of the output clamp, using a repetitive pulse method at 1.0 A, indicates the maximum energy to be 100 mJ at 125 °C junction temperature per output

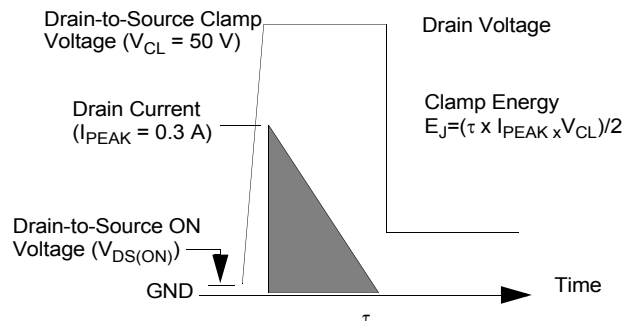


Figure 6. Output Voltage Clamping

#### 7.2.1 Reverse battery and transient protection

The 33812 device requires external reverse battery protection on the VPWR pin. All outputs consist of a power MOSFET with an integral substrate diode. During a reverse battery condition, current flows through the load via the substrate diode. Under this condition, load devices turn on. If reverse battery protection for the loads is required, a diode must be placed in series with the load. Good automotive engineering practices recommend the use of transient voltage suppression on the VPWR line. A TVS device and adequate capacitive decoupling are necessary for a robust design.

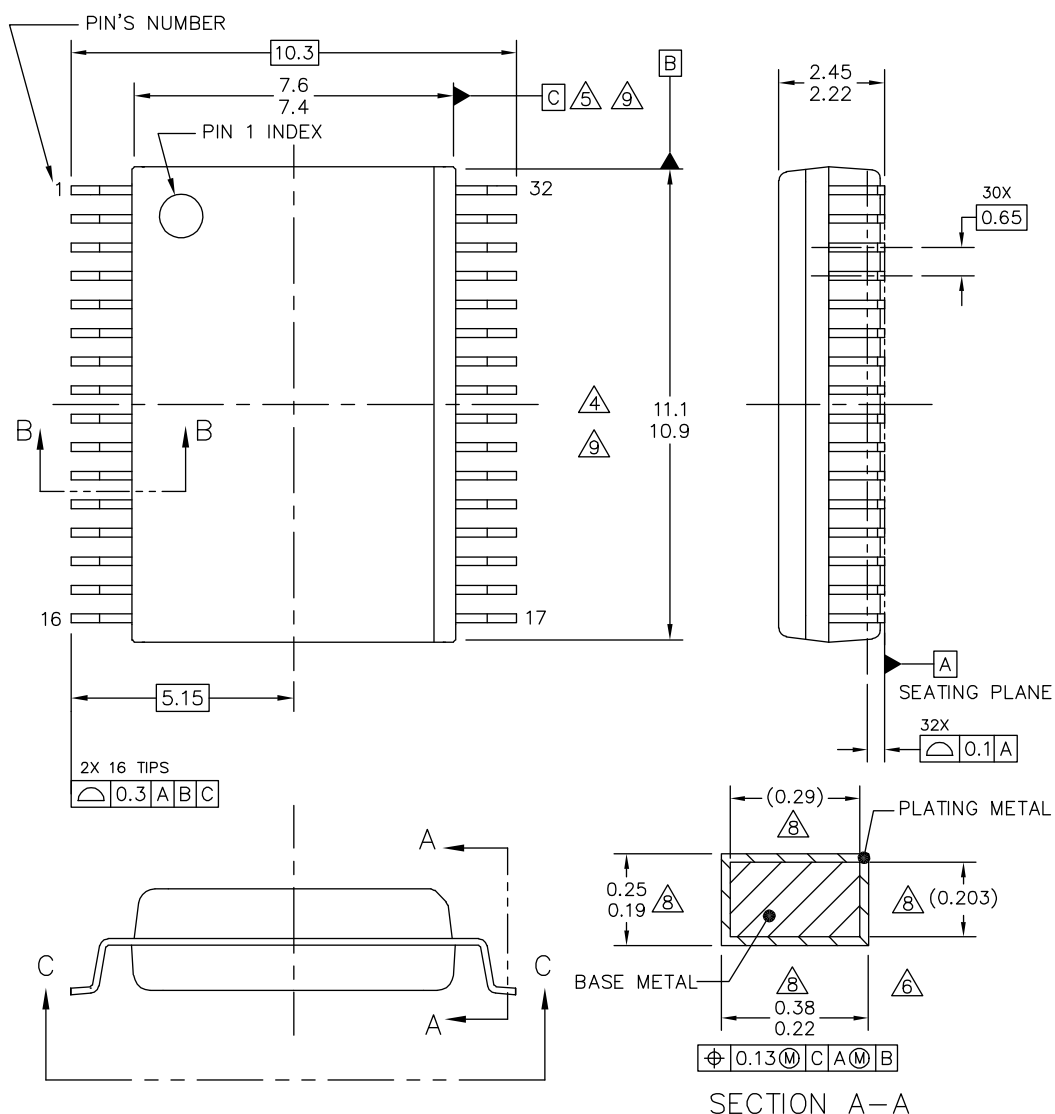
# 8 Packaging

## 8.1 Package dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to [www.nxp.com](http://www.nxp.com) and perform a keyword search for the drawing's document number.

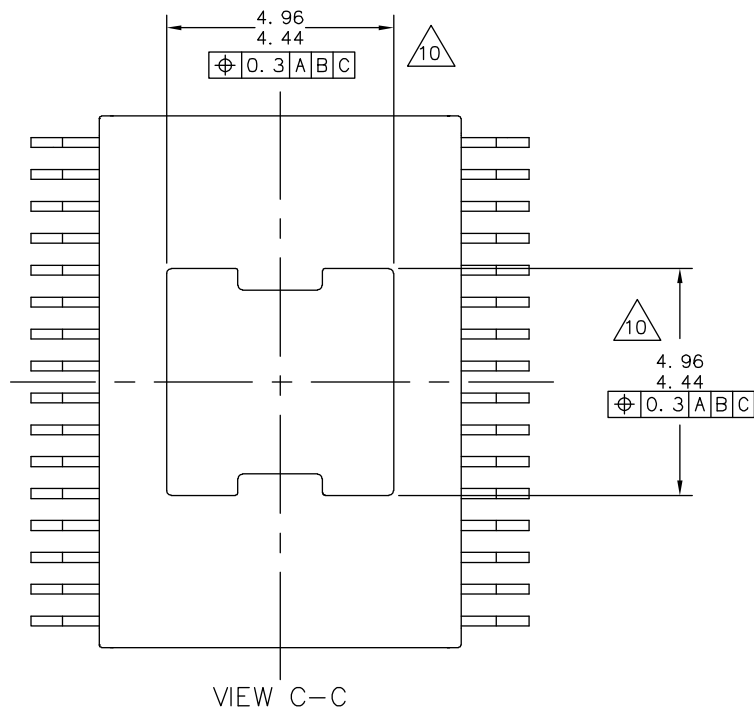
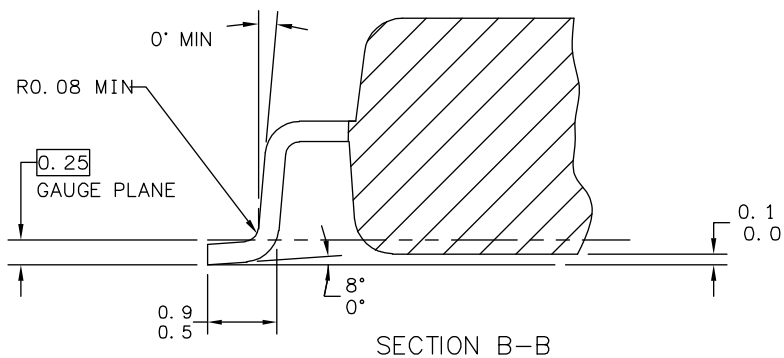
**Table 7. Package drawing information**

| Package     | Suffix | Package outline drawing number |
|-------------|--------|--------------------------------|
| 32 SOICW-EP | EK     | 98ASA10556D                    |



|  |                           |                            |
|--|---------------------------|----------------------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.                    | <b>MECHANICAL OUTLINE</b> | PRINT VERSION NOT TO SCALE |
| TITLE: 32LD SOIC W/B, 0.65 PITCH<br>4.7 X 4.7 EXPOSED PAD,<br>CASE-OUTLINE | DOCUMENT NO: 98ASA10556D  | REV: D                     |
|  | CASE NUMBER: 1454-04      | 20 JUN 2008                |
|  | STANDARD: NON-JEDEC       |                            |





|  |                           |                            |
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|  | CASE NUMBER: 1454-04      | 20 JUN 2008                |
|  | STANDARD: NON-JEDEC       |                            |

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSION RANGES DEFINE THE PRIMARY KEEP-OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.34mm FROM MAXIMUM EXPOSED PAD SIZE

|  |                          |                    |  |                            |  |
|--|--------------------------|--------------------|--|----------------------------|--|
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| TITLE: 32LD SOIC W/B, 0.65 PITCH<br>4.7 X 4.7 EXPOSED PAD,<br>CASE-OUTLINE | DOCUMENT NO: 98ASA10556D |                    |  | REV: D                     |  |
|  | CASE NUMBER: 1454-04     |                    |  | 20 JUN 2008                |  |
|  | STANDARD: NON-JEDEC      |                    |  |                            |  |

## 9 Revision history

| Revision | Date   | Description of changes   |
|----------|--------|--|
| 4.0      | 7/2009 | <ul style="list-style-type: none"><li>Initial release</li></ul>  |
| 5.0      | 7/2010 | <ul style="list-style-type: none"><li>Changed Part Number from PCZ33812AEK/R2 to MCZ33812AEK/R2</li></ul>  |
|          | 4/2013 | <ul style="list-style-type: none"><li>No technical changes. Revised back page. Updated document properties</li><li>Added SMARTMOS sentence to first paragraph</li></ul>                                    |
| 6.0      | 4/2016 | <ul style="list-style-type: none"><li>PN consolidation: MCZ33812EK &amp; MCZ33812AEK are consolidated in one device MC33812EK as per DM 17148</li><li>Updated data sheet document form and style</li></ul> |

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