M27256
256K (32K x 8) UV ERASABLE PROM

Military

- **Military Temperature Range: −55°C to +125°C (T_C)**
- **Software Carrier Capability**
- **200, 250, 350 ns Access Times**
- **Two-Line Control**
- **int$_e$ligent Identifier™ Mode — Automated Programming Operations**
- **Industry Standard Pinout . . . JEDEC Approved**
- **Low Power — 125 mA max. Active — 50 mA max. Standby**
- **int$_e$ligent Programming™ Algorithm — Fastest EPROM Programming**

The Intel M27256 is a 5V only, 262, 144-bit ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM). Organized as 32K words by 8 bits, individual bytes are accessed in 200 ns. This is compatible with high performance microprocessors, such as the Intel 8 MHz M80186, allowing full speed operation without the addition of performance-degrading WAIT states. The M27256 is also directly compatible with Intel's M8051 family of microcontrollers.

The M27256 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the M27256's high density, cost effective EPROM storage, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems.

The M27256's large storage capability of 32K bytes enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a M27256 EPROM directly on a system's memory bus. This would permit immediate microprocessor access and execution of software and eliminate the need for time consuming disk accesses and downloads.

Several advanced features have been designed into the M27256 that allow for fast and reliable programming — the int$_e$ligent identifier™ mode and the int$_e$ligent Programming™ Algorithm. Programming equipment that takes advantage of these innovations will electronically identify the M27256 and then rapidly program it using an efficient programming method.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMS. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The M27256 is manufactured using Intel's advanced HMOS* II-E technology.

*HMOS is a patented process of Intel Corporation.

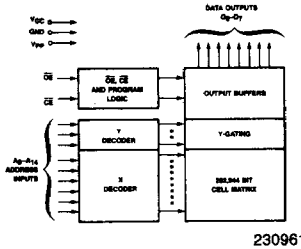

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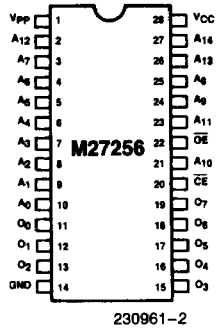
Figure 1. Block Diagram

Pin Names

A_0–A_{14}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs



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LCC

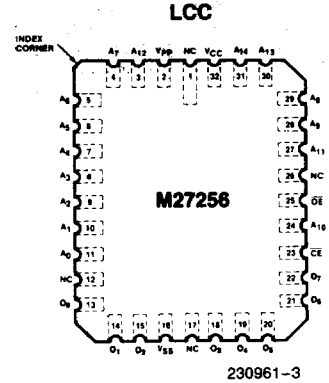

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Figure 2. Pin Configurations

January 1990
Order Number: 230961-004

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias ..... −55°C to +125°C

Storage Temperature ..... −65°C to +150°C

All Input or Output Voltages with Respect to Ground ..... +6.25V to −0.6V

Voltage on Pin 24 with Respect to Ground ..... +13.5V to −0.6V

V_{PP} Supply Voltage with Respect to Ground ..... +13.0V to −0.6V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

READ OPERATION

D.C. CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Limits			Units	Comments
		Min	Typ(3)	Max		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.5V
I_{PP1}[2]	V_{PP} Current Read/Standby			5	mA	V_{PP} = 5.5V
I_{CC1}[2]	V_{CC} Current Standby		20	50	mA	$\overline{CE}$ = V_{IH}
I_{CC2}[2]	V_{CC} Current Active		45	125	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
V_{IL}[5]	Input Low Voltage	−0.1		+0.8	V	
V_{IH}[5]	Input High Voltage	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

See notes on next page.

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A.C. CHARACTERISTICS (Over Specified Operating Conditions)

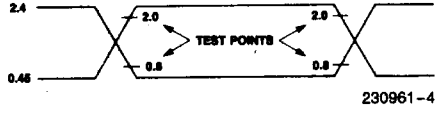
Symbol	Parameter	M27256-20		M27256-25		M27256-35		Units	Comments
		Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		200		250		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		200		250		350	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay	0	75		100		130	ns	$\overline{CE} = V_{IL}$
t_{DF}(4)	$\overline{OE}$ High to Output Float	0	55	0	60	0	110	ns	$\overline{CE} = V_{IL}$
t_{OH}(4)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_C = +25°C$ and nominal supply voltages.
4. Output Float is defined as the point where data is no longer driven.
5. These values apply to D.C. test conditions only. The A.C. values are $V_{IL} = 0.45V$ max, $V_{IH} = 2.4V$ min.

CAPACITANCE $T_C = +25°C, f = 1$ MHz

Symbol	Parameter	Typ(1)	Max	Units	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. TESTING INPUT, OUTPUT WAVEFORM



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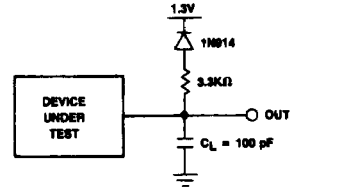
A.C. Testing: Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



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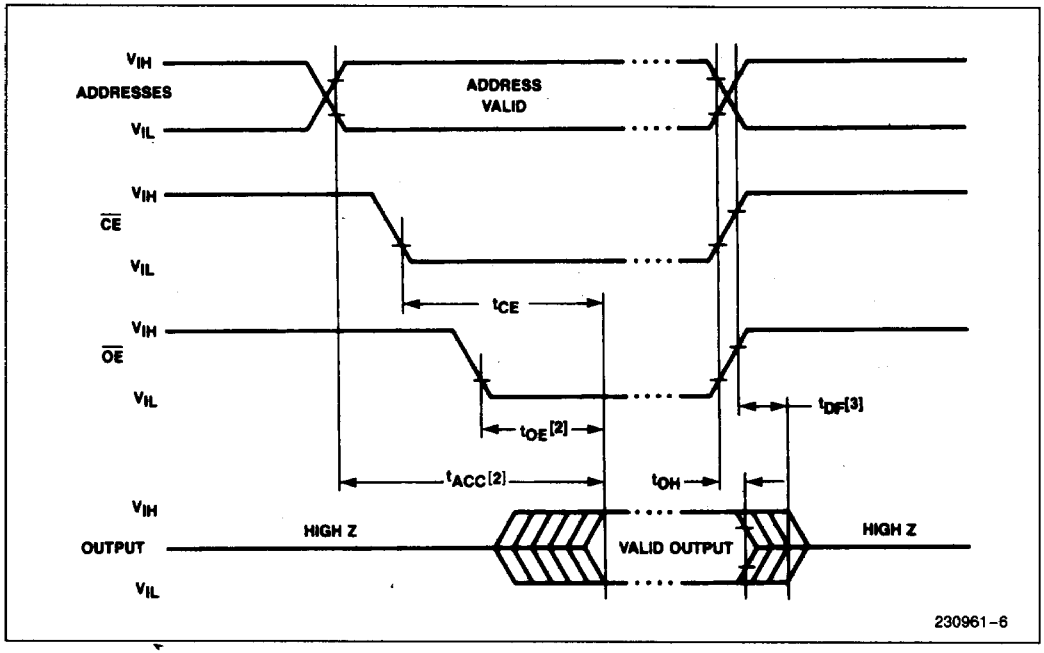
$C_L = 100$ pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



NOTES:
1. Typical values are for T_C = 25°C and nominal supply voltages.
2. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
3. Output float is defined as the point where data is no longer driven.

DEVICE OPERATION

The eight modes of operation of the M27256 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for int$_e$ligent identifier mode.

Table 1. Operating Modes

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A_9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
int$_e$ligent Programming	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Optional Verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
int$_e$ligent Identifier	V_{IL}	V_{IL}	V_H	V_{CC}	V_{CC}	Code

NOTES:
1. X can be V_{IH} or V_{IL}
2. V_H = 12.0V ±0.5V

Read Mode

The M27256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The M27256 has a standby mode which reduces the maximum active current from 125 mA to 50. The M27256 is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ (pin 20) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) should be made a common connection to all devices in the array connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

System Considerations

The power switching characteristics of HMOS* II-E EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

Programming

Caution: Exceeding 13.0V on pin 1 (V_{PP}) will permanently damage the M27256.

Initially, and after each erasure, all bits of the M27256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M27256 is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

int$_e$ligent Programming™ Algorithm

The M72756 int$_e$ligent Programming Algorithm rapidly programs Intel M27256 EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of five minutes. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27256 int$_e$ligent Programming Algorithm is shown in Figure 3.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one-millisecond pulses applied to a particular M27256 location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

Program Inhibit

Programming of multiple M27256s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other M27256s from being programmed. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel M27256s may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with V_{PP} at 12.5V will program the selected M27256.

Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} at 12.5V.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the M27256.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the Intel M27256, these two identifier bytes are given in Table 2. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (O_7) defined as the parity bit.

ERASURE CHARACTERISTICS

The erasure characteristics of the M27256 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical M27256 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27256 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the M27256 window to prevent unintentional erasure.

The recommended erasure procedure for the M27256 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The M27256 should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an M27256 can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the M27256 to high intensity UV light for long periods may cause permanent damage.

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Table 2. M27256 int$_e$ligent Identifier™ Bytes

Pins / Identifier	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	0	0	1	89
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

NOTES:
1. A_9 = 12.0V ±0.5V
2. A_1–A_8, A_{10}–A_{13}, $\overline{CE}$, $\overline{OE}$ = V_{IL}
3. A_{14} = V_{IH} or V_{IL}

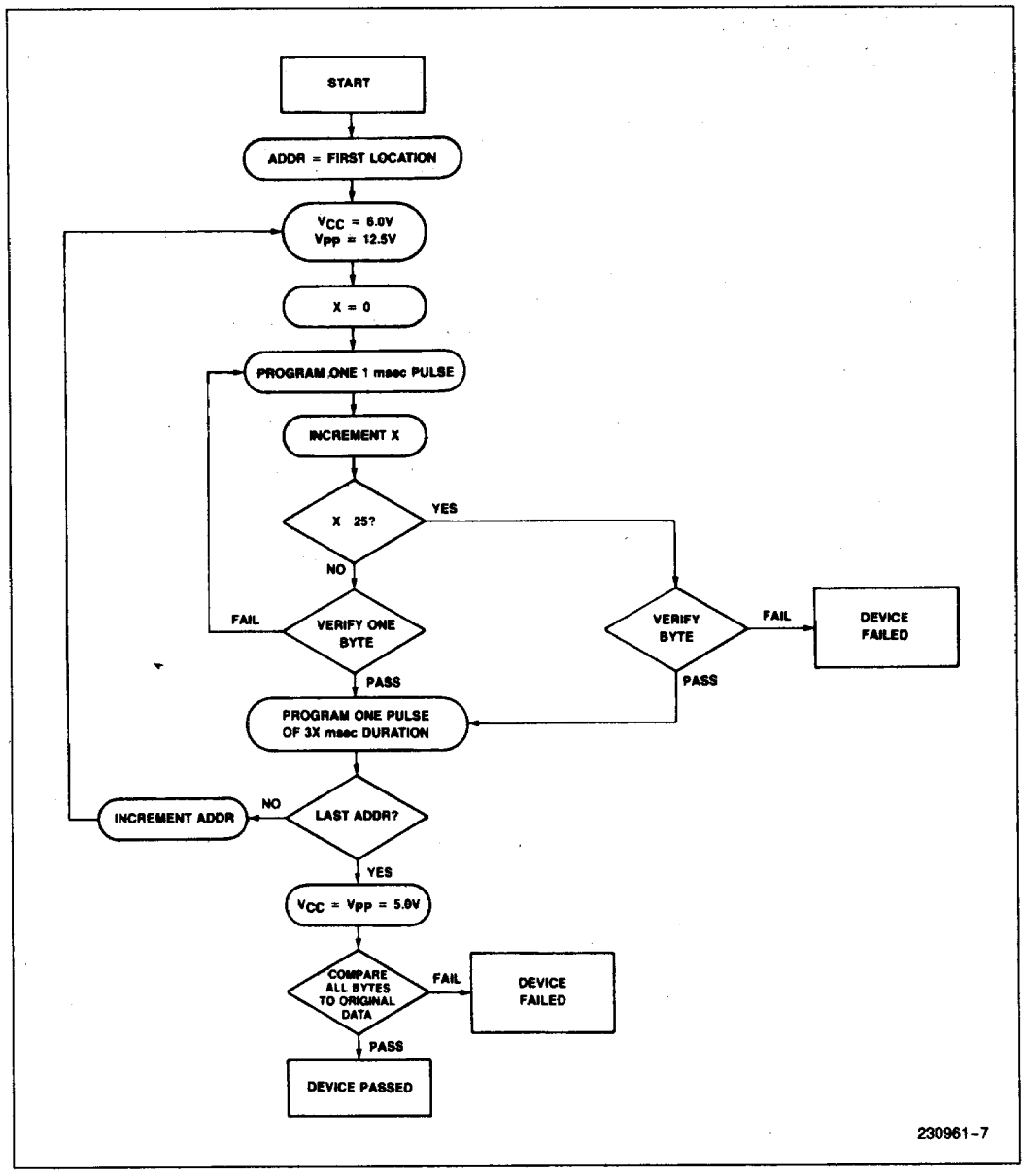

Figure 3. M27256 int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

D.C. PROGRAMMING CHARACTERISTICS

T_C = 25 ±5°C, V_{CC} = 6.0V ±0.25V, V_{PP} = 12.5V ±0.3V

Symbol	Parameter	Limits			Comments (Note 1)
		Min	Max	Unit	
I_{IL}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC} − 1	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4		V	I_{OH} = −400 μA
I_{CC2}	V_{CC} Supply Current (Program & Verify)		100	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	

NOTE:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

A.C. PROGRAMMING CHARACTERISTICS

T_C = 25 ±5°C, V_{CC} = 6.0V ±0.25V, V_{PP} = 12.5V ±0.3V

Symbol	Parameter	Limits			Comments (Note 1)
		Min	Max	Unit	
t_{AS}	Address Setup Time	2		μs	
t_{OES}	$\overline{OE}$ Setup Time	2		μs	
t_{DS}	Data Setup Time	2		μs	
t_{AH}	Address Hold Time	0		μs	
t_{DH}	Data Hold Time	2		μs	
t_{DFP}(4)	Output Enable to Output Float Delay	0	130	ns	
t_{VPS}	V_{PP} Setup Time	2		μs	
t_{VCS}	V_{CC} Setup Time	2		μs	
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.05	ms	(Note 3)
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85	78.75	ms	(Note 2)
t_{OE}	Data Valid from $\overline{OE}$		150	ns	

***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1 ms ±5%.
4. Output Float is defined as the point where data is no longer driven.

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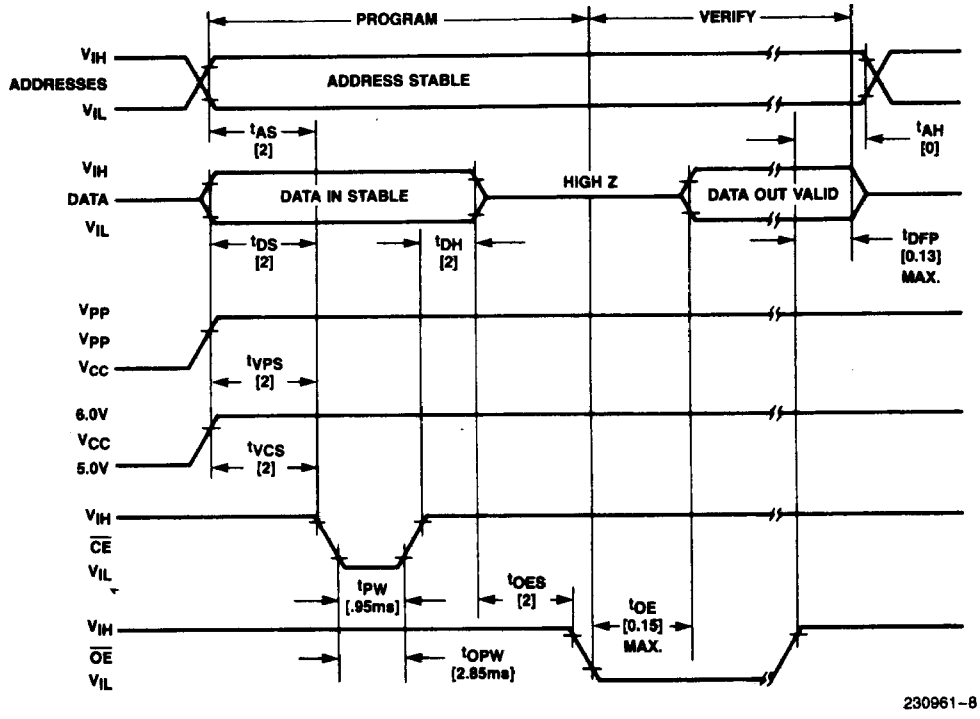
intelligent Programming™ WAVEFORMS



NOTES:
1. All times shown in [ ] are minimum and in μs unless otherwise specified.
2. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
3. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
4. When programming the M27256 a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.