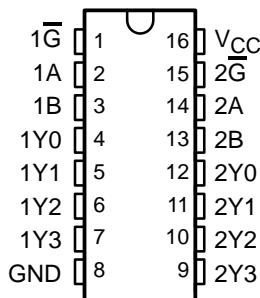
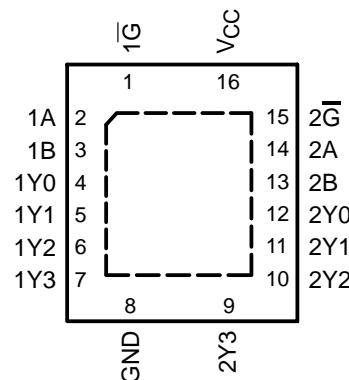


- Operating Range 2-V to 5.5-V  $V_{CC}$
- Designed Specifically for High-Speed Memory Decoders and Data-Transmission Systems
- Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

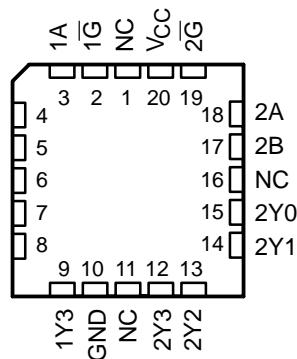
SN54AHC139 . . . J OR W PACKAGE  
SN74AHC139 . . . D, DB, DGV, N, NS  
OR PW PACKAGE  
(TOP VIEW)



SN74AHC139 . . . RGY PACKAGE  
(TOP VIEW)



SN54AHC139 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'AHC139 devices are dual 2-line to 4-line decoders/demultiplexers designed for 2-V to 5.5-V  $V_{CC}$  operation. These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

## ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AHC139RGYR	HA139
	PDIP – N	Tube	SN74AHC139N	SN74AHC139N
	SOIC – D	Tube	SN74AHC139D	AHC139
		Tape and reel	SN74AHC139DR	
	SOP – NS	Tape and reel	SN74AHC139NSR	AHC139
	SSOP – DB	Tape and reel	SN74AHC139DBR	HA139
	TSSOP – PW	Tube	SN74AHC139PW	HA139
		Tape and reel	SN74AHC139PWR	
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHC139DGVR	HA139
	CDIP – J	Tube	SNJ54AHC139J	SNJ54AHC139J
	CFP – W	Tube	SNJ54AHC139W	SNJ54AHC139W
	LCCC – FK	Tube	SNJ54AHC139FK	SNJ54AHC139FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN54AHC139, SN74AHC139 DUAL 2-LINE TO 4-LINE DECODERS/DEMULITPLEXERS

SCLS259K – DECEMBER 1995 – REVISED MARCH 2003

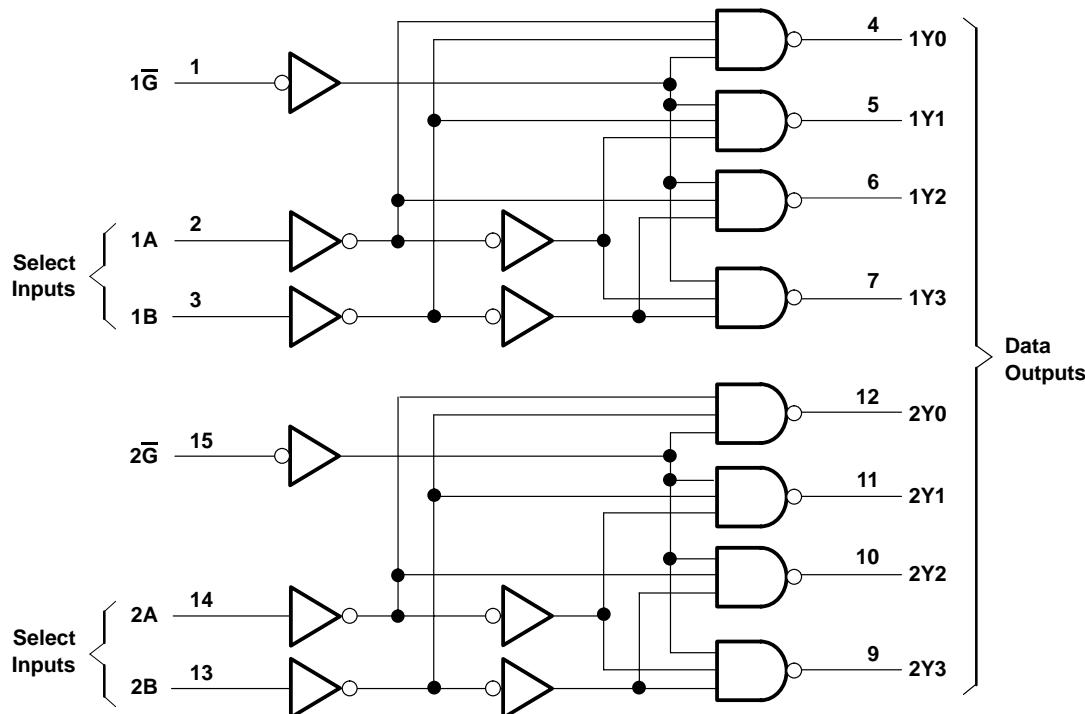
## description/ordering information (continued)

The active-low enable ( $\bar{G}$ ) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

FUNCTION TABLE  
(each decoder/demultiplexer)

$\bar{G}$	INPUTS		OUTPUTS			
	B	A	Y <sub>0</sub>	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

## logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.  
3. The package thermal impedance is calculated in accordance with JESD 51-5.

**recommended operating conditions (see Note 4)**

				SN54AHC139	SN74AHC139	UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V		1.5	1.5	V
		V <sub>CC</sub> = 3 V		2.1	2.1	
		V <sub>CC</sub> = 5.5 V		3.85	3.85	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	0.5	V
		V <sub>CC</sub> = 3 V		0.9	0.9	
		V <sub>CC</sub> = 5.5 V		1.65	1.65	
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50	-50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		-4	-4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V		-8	-8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		4	4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V		8	8	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		100	100	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		20	20	
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**PRODUCT PREVIEW** information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



# SN54AHC139, SN74AHC139 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SCLS259K – DECEMBER 1995 – REVISED MARCH 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC139	SN74AHC139	UNIT	
			MIN	TYP	MAX	MIN	MAX		
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.9	2		1.9	1.9	V	
		3 V	2.9	3		2.9	2.9		
		4.5 V	4.4	4.5		4.4	4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48	2.48		
		4.5 V	3.94			3.8	3.8		
	I <sub>OL</sub> = 50 µA	2 V		0.1		0.1	0.1		
V <sub>OL</sub>		3 V		0.1		0.1	0.1		
		4.5 V		0.1		0.1	0.1		
		I <sub>OL</sub> = 4 mA	3 V		0.36	0.5	0.44		
I <sub>OL</sub> = 8 mA	4.5 V		0.36		0.5	0.44			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		±0.1		±1*	±1	µA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		4		40	40	µA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	2	10			10	pF	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHC139	SN74AHC139	UNIT	
				MIN	TYP	MAX	MIN	MAX		
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	7.2**	11**		1**	13**	1	13
t <sub>PHL</sub>				7.2**	11**		1**	13**	1	13
t <sub>PLH</sub>	G	Y	C <sub>L</sub> = 15 pF	6.4**	9.2**		1**	11**	1	11
t <sub>PHL</sub>				6.4**	9.2**		1**	11**	1	11
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	9.7	14.5		1	16.5	1	16.5
t <sub>PHL</sub>				9.7	14.5		1	16.5	1	16.5
t <sub>PLH</sub>	G	Y	C <sub>L</sub> = 50 pF	8.9	12.7		1	14.5	1	14.5
t <sub>PHL</sub>				8.9	12.7		1	14.5	1	14.5

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHC139	SN74AHC139	UNIT	
				MIN	TYP	MAX	MIN	MAX		
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	5**	7.2**		1**	8.5**	1	8.5
t <sub>PHL</sub>				5**	7.2**		1**	8.5**	1	8.5
t <sub>PLH</sub>	G	Y	C <sub>L</sub> = 15 pF	4.4**	6.3**		1**	7.5**	1	7.5
t <sub>PHL</sub>				4.4**	6.3**		1**	7.5**	1	7.5
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	6.5	9.2		1	10.5	1	10.5
t <sub>PHL</sub>				6.5	9.2		1	10.5	1	10.5
t <sub>PLH</sub>	G	Y	C <sub>L</sub> = 50 pF	5.9	8.3		1	9.5	1	9.5
t <sub>PHL</sub>				5.9	8.3		1	9.5	1	9.5

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

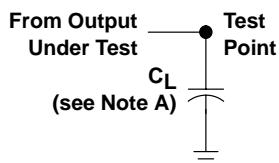


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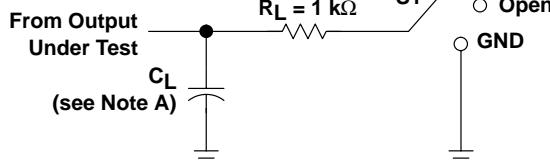
operating characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1$ MHz	13	pF

### PARAMETER MEASUREMENT INFORMATION

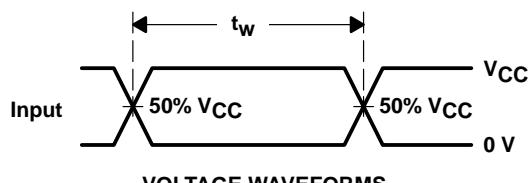


LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

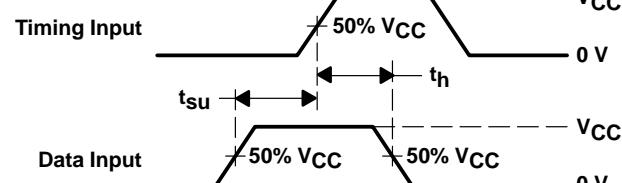


LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS

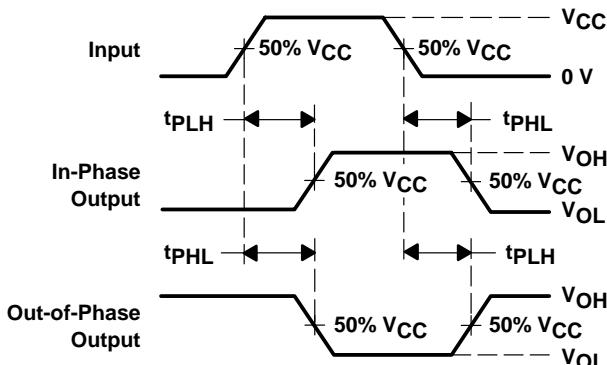
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND
Open Drain	$V_{CC}$



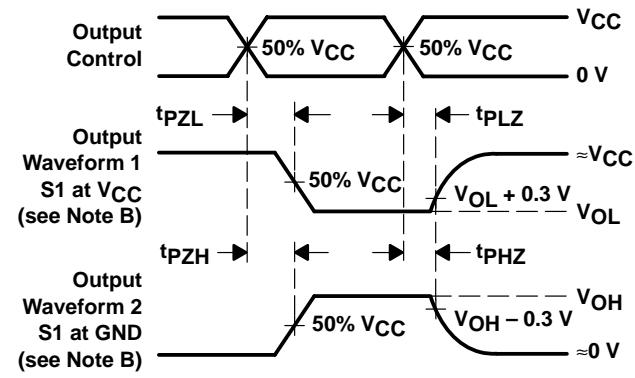
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
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Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>
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	Optical Networking <a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
	Security <a href="http://www.ti.com/security">www.ti.com/security</a>
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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AHC139D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DBLE	OBsolete	SSOP	DB	16		TBD	Call TI	Call TI
SN74AHC139DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHC139NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHC139NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139PWLE	OBsolete	TSSOP	PW	16		TBD	Call TI	Call TI
SN74AHC139PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC139RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
no Sb/Br)								
SN74AHC139RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

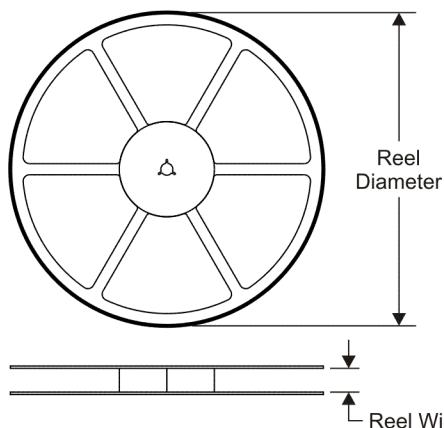
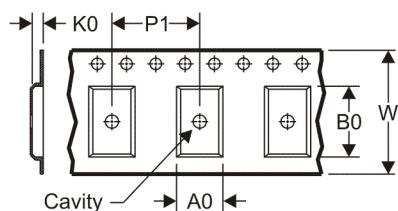
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

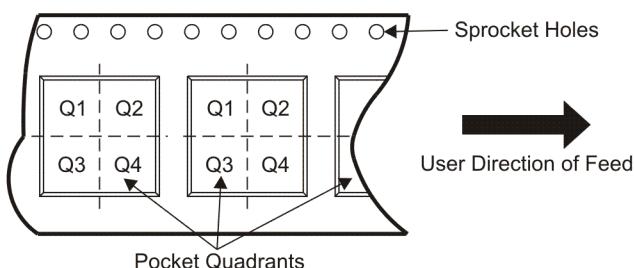
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC139DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHC139DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC139DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC139NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC139PWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74AHC139RGYR	VQFN	RGY	16	3000	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

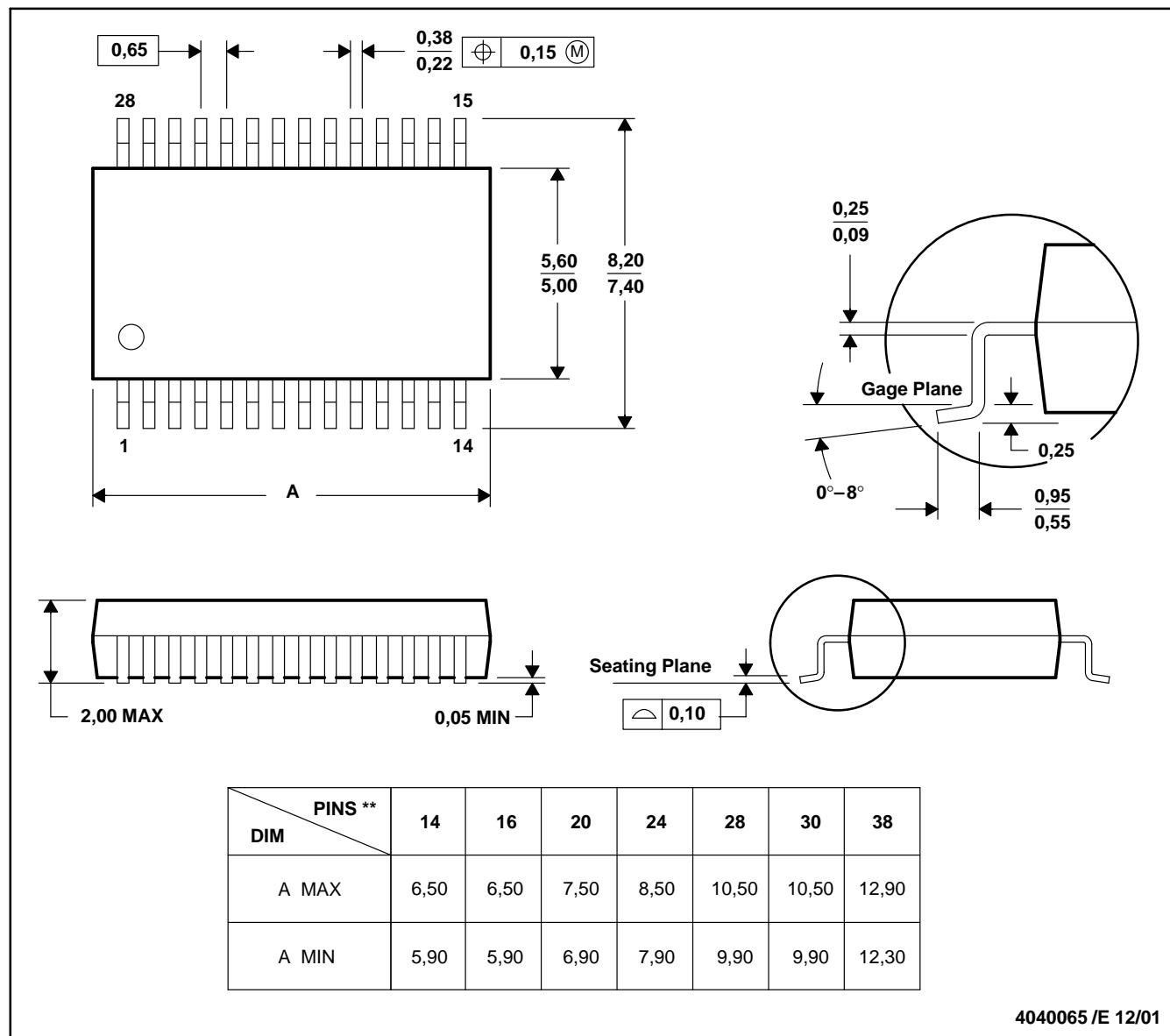

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC139DBR	SSOP	DB	16	2000	346.0	346.0	33.0
SN74AHC139DGVR	TVSOP	DGV	16	2000	346.0	346.0	29.0
SN74AHC139DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74AHC139NSR	SO	NS	16	2000	346.0	346.0	33.0
SN74AHC139PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
SN74AHC139RGYR	VQFN	RGY	16	3000	190.5	212.7	31.8

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



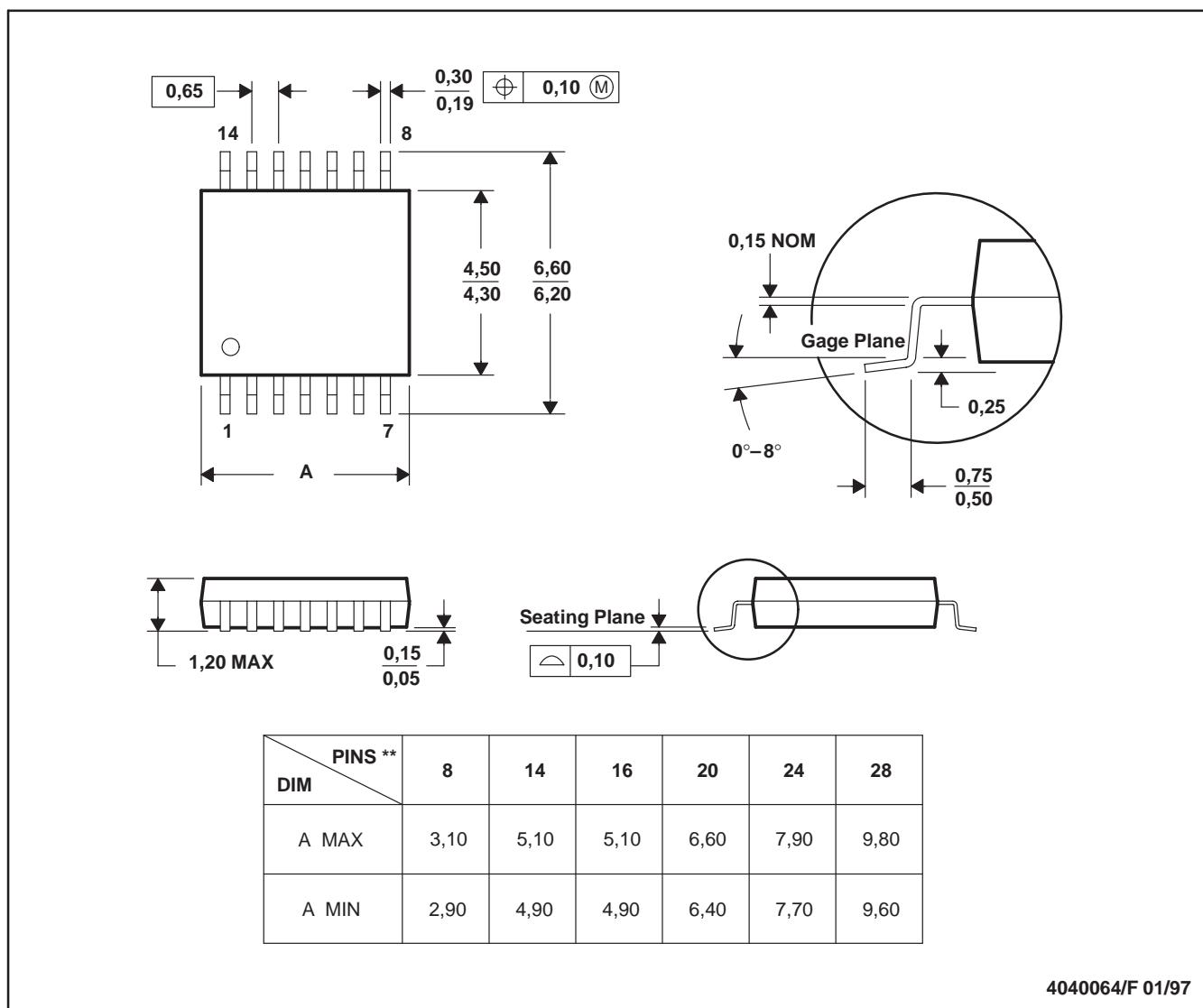
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



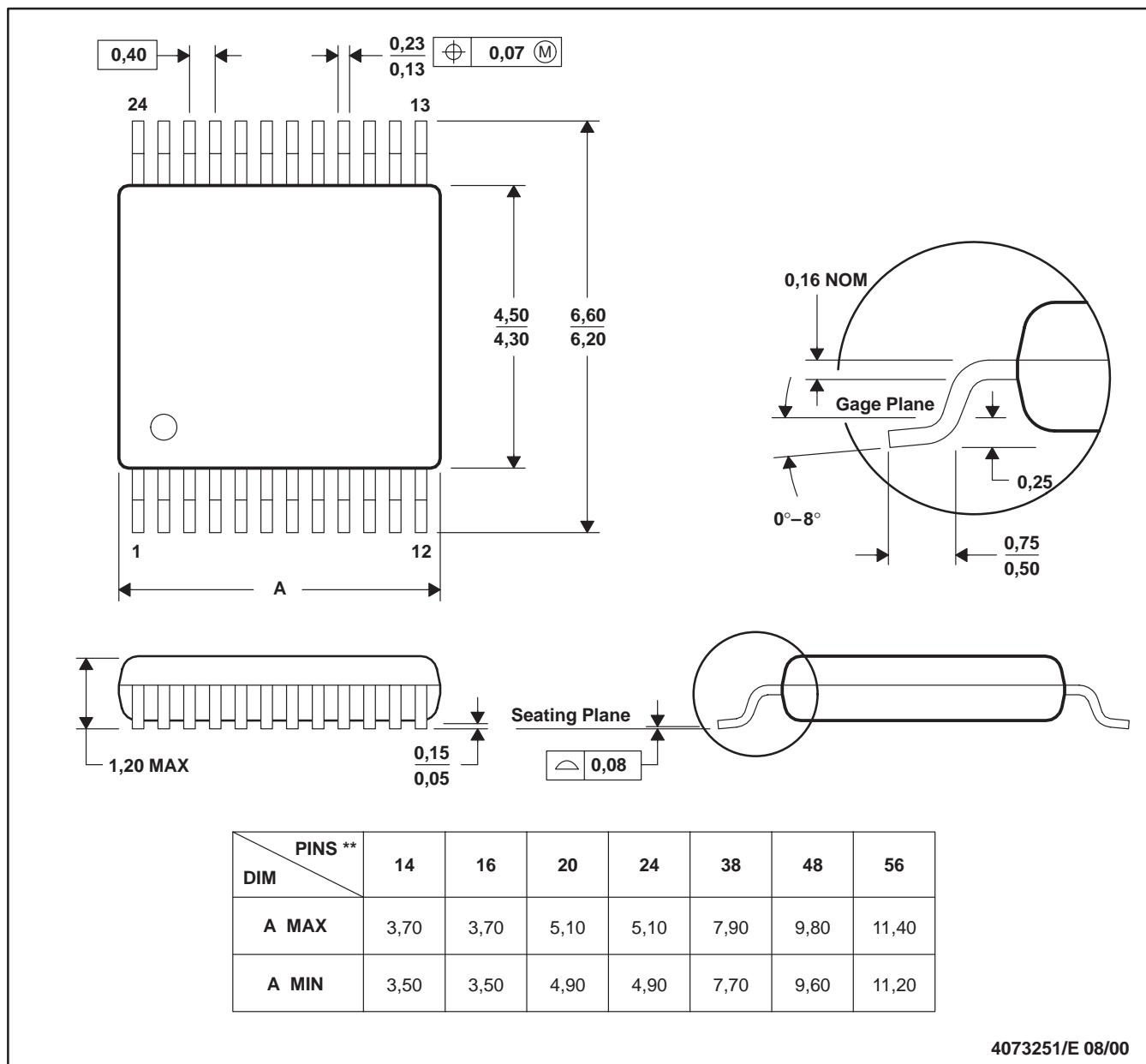
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

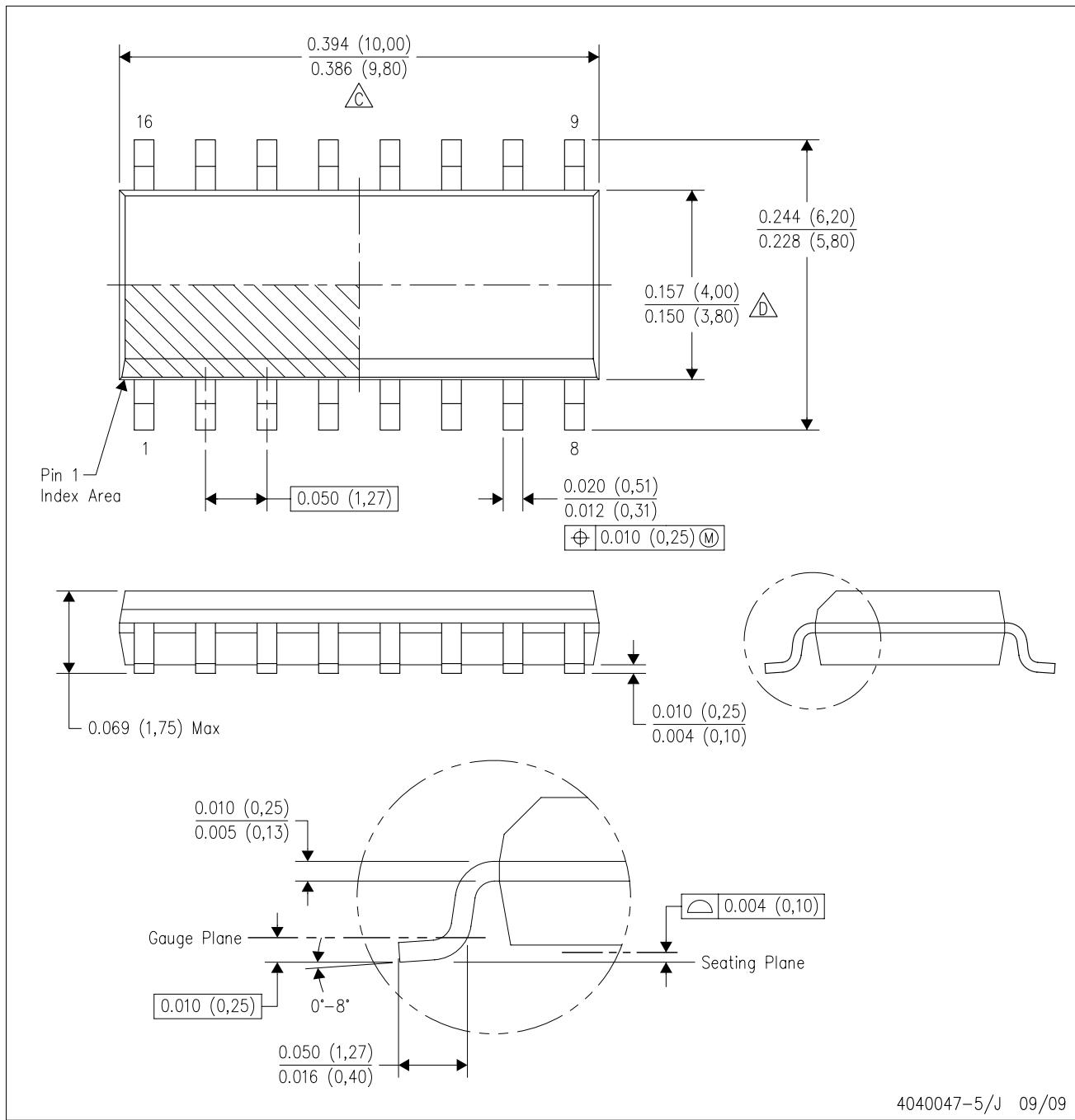
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-5/J 09/09

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

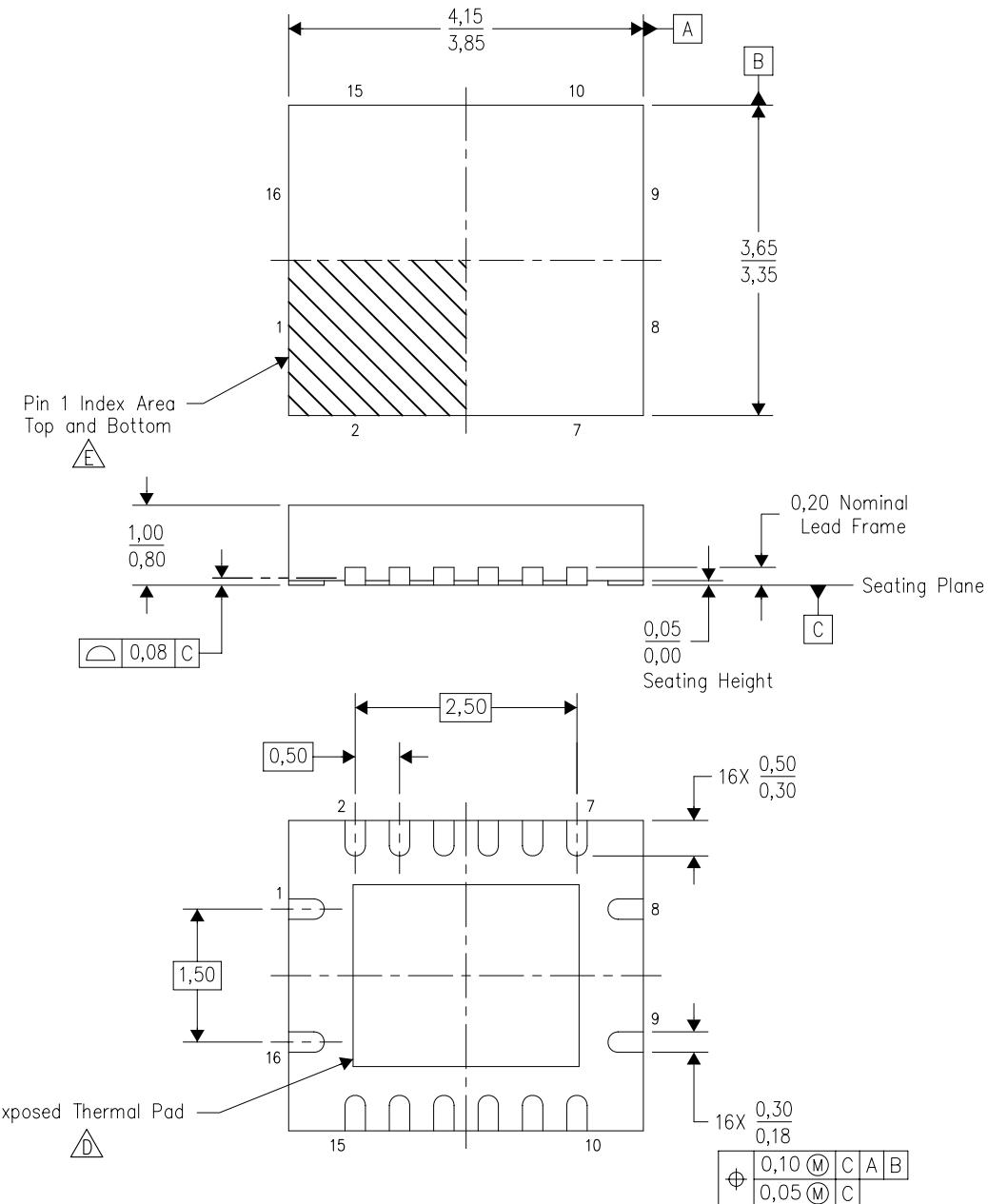
 Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.  
E. Reference JEDEC MS-012 variation AC.

E. Reference JEDEC MS-012 variation AC.

## MECHANICAL DATA

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



### Bottom View

4203539-3/H 06/2009

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No-Lead) package configuration.

 The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

 See the Product Data Sheet for details regarding the exposed thermal pad dimensions.  
Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.  
The Pin 1 identifiers are either a molded, marked or metal feature.

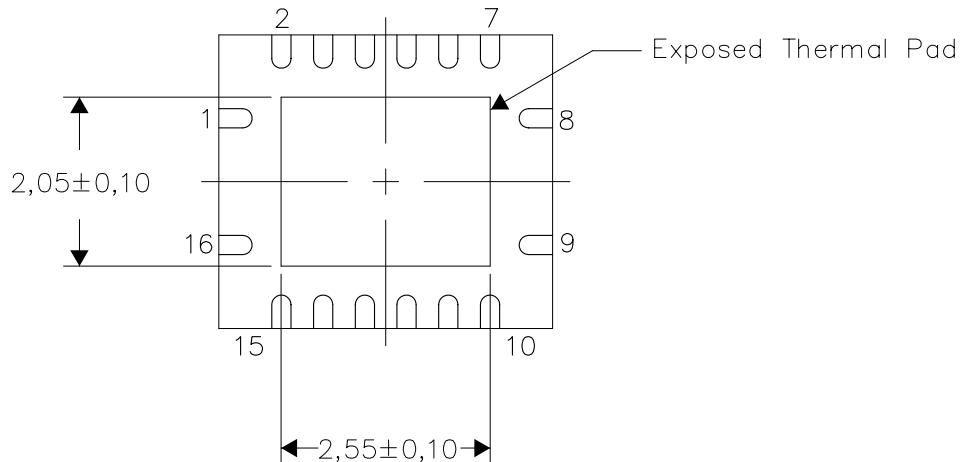
F. Package complies to JEDEC MO-241 variation BB

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

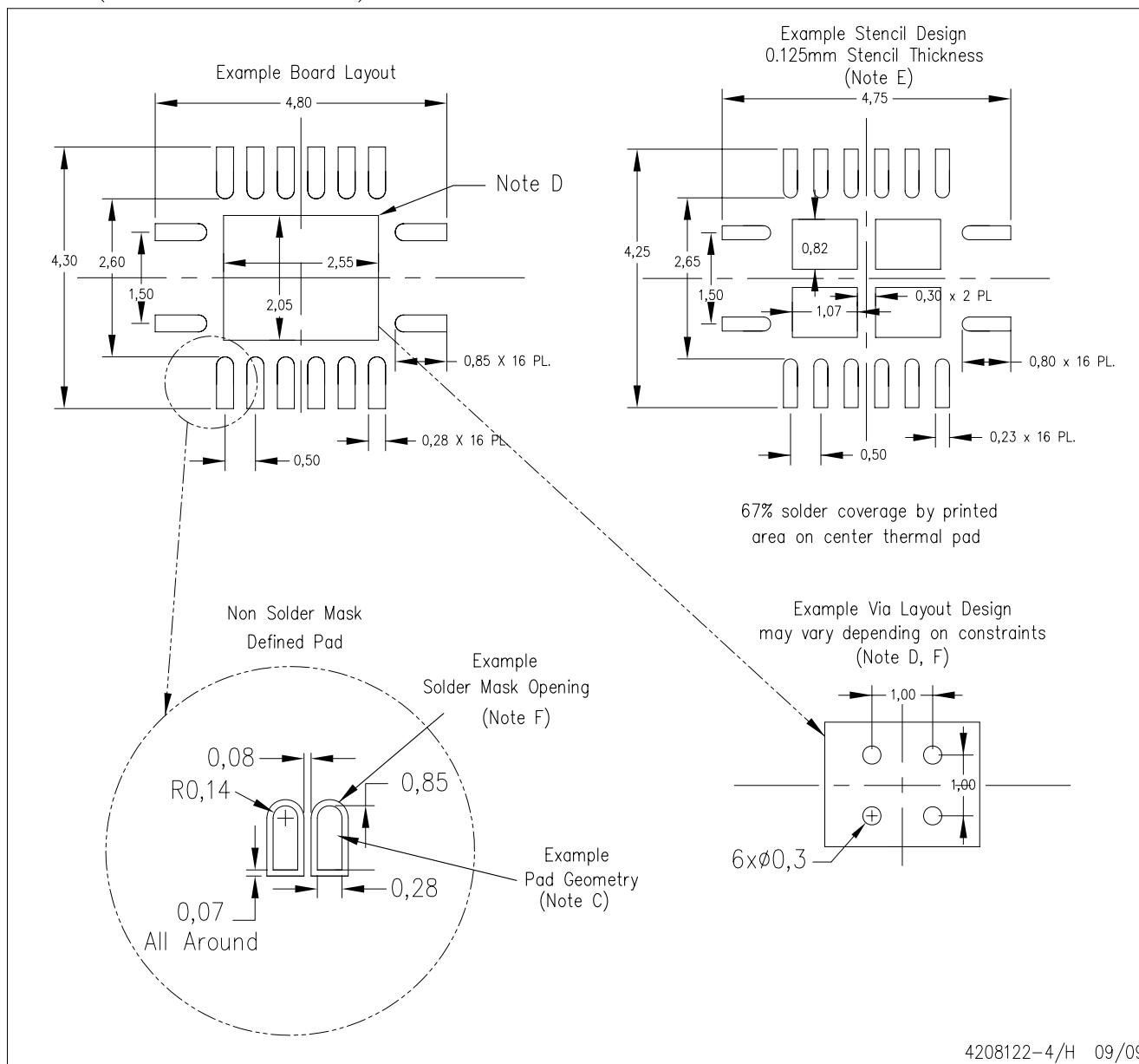


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

## RGY (R-PVQFN-N16)



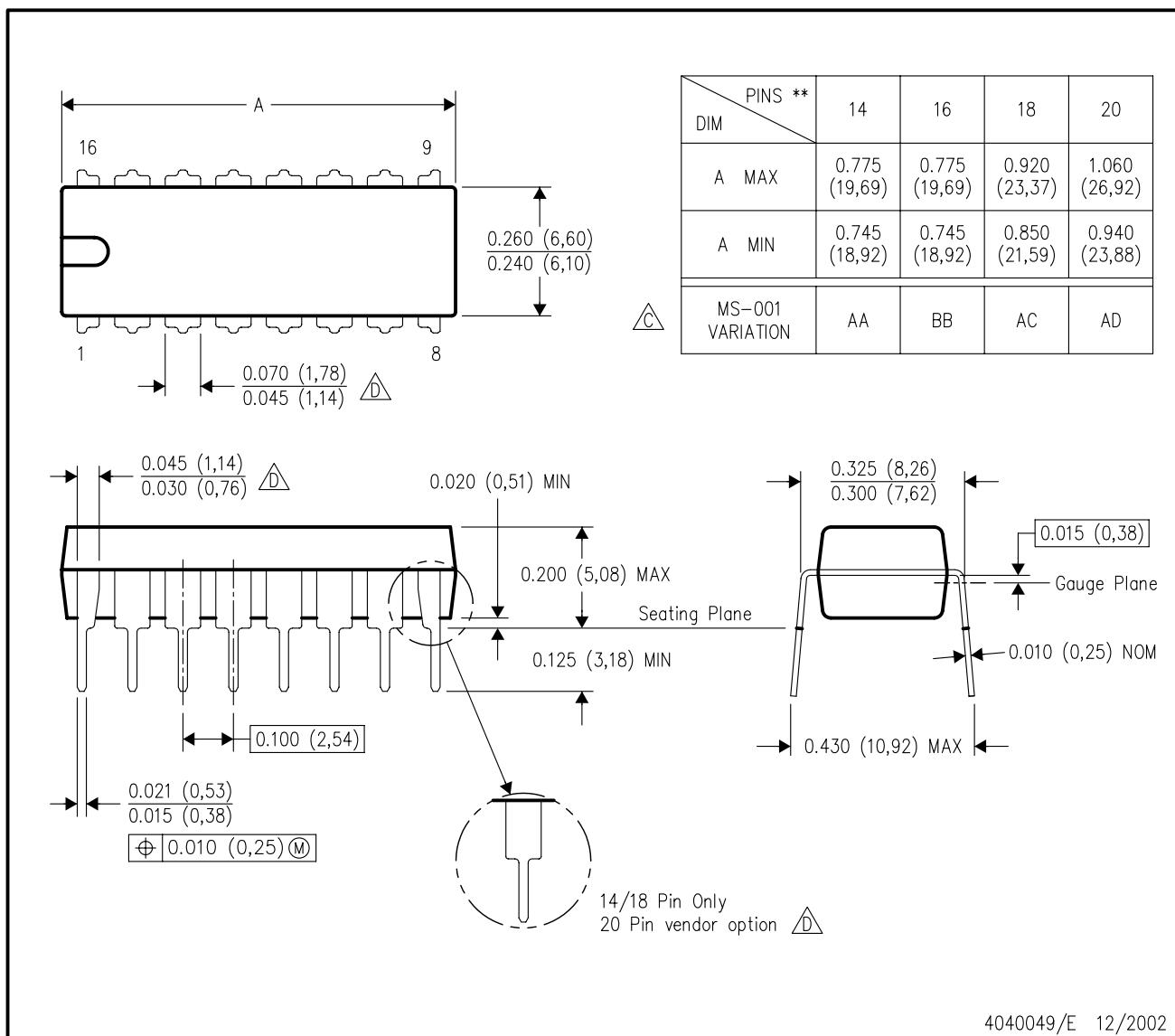
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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