

74LVC2245A

Octal transceiver with direction pin, 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

Rev. 5 — 4 November 2011

Product data sheet

1. General description

The 74LVC2245A is a octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

A send/receive (DIR) input controls direction, and an output enable ($\overline{OE}$) input makes easy cascading possible. Pin $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

It is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The device is designed with 30 Ω series termination resistors in both HIGH and LOW output stages to reduce line noise.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices as translators in mixed 3.3 V and 5 V applications.

2. Features and benefits

- 5 V tolerant inputs/outputs, for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Integrated 30 Ω termination resistors
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

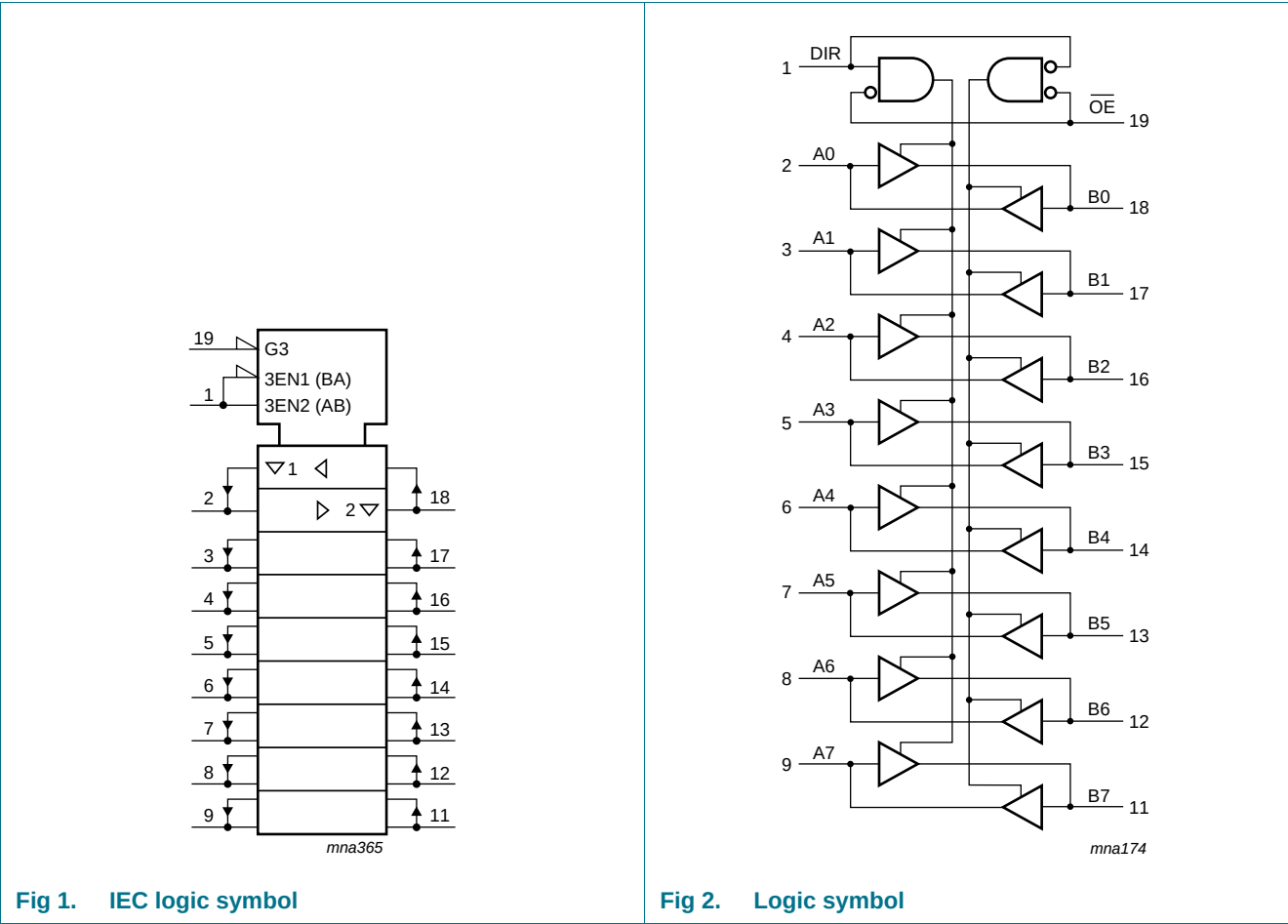


3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC2245AD	−40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC2245ADB	−40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVC2245APW	−40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVC2245ABQ	−40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram



5. Pinning information

5.1 Pinning

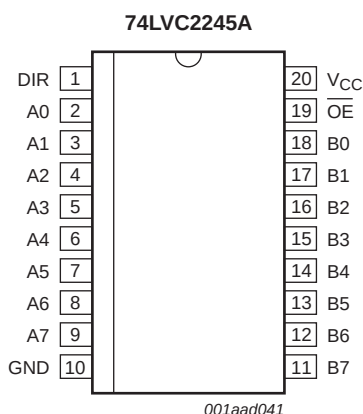
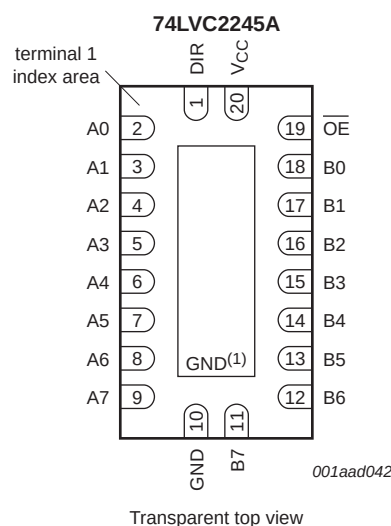


Fig 3. Pin configuration SO20 and (T)SSOP20



- (1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 4. Pin configuration DHVQFN20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control input
A[0:7]	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B[0:7]	18, 17, 16, 15, 14, 13, 12, 11	data input/output
OE	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Functional table

Input		Input/output	
OE	DIR	An	Bn
LOW	LOW	A = B	input
LOW	HIGH	input	B = A
HIGH	don't care	Z (high-impedance OFF-state)	Z (high-impedance OFF-state)

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
V_O	output voltage	output HIGH or LOW state	[2] -0.5	$V_{CC} + 0.5$	V
		output 3-state	[2] -0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	$^{\circ}\text{C}$
P_{tot}	total power dissipation	$T_{amb} = -40$ $^{\circ}\text{C}$ to $+125$ $^{\circ}\text{C}$	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO20 packages: above 70 $^{\circ}\text{C}$ derate linearly with 8 mW/K.

For (T)SSOP20 packages: above 60 $^{\circ}\text{C}$ derate linearly with 5.5 mW/K.

For DHVQFN20 packages: above 60 $^{\circ}\text{C}$ derate linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	0	-	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = –100 μ A; V _{CC} = 1.65 V to 3.6 V	V _{CC} – 0.2	V _{CC}	-	V _{CC} – 0.3	-	V
		I _O = –2 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = –4 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = –6 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = –9 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = –12 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μ A; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 2 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 4 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 6 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 12 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μ A
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND;	-	±0.1	±5	-	±20	μ A
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	±0.1	±10	-	±20	μ A
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	μ A
Δ I _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} – 0.6 V; I _O = 0 A	-	5	500	-	5000	μ A
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	4.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	T _{amb} = –40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	An to Bn; Bn to An; see Figure 5 ^[2]						
		V _{CC} = 1.2 V	-	26	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.8	7.5	17.1	1.8	18.0	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	3.9	8.4	1.5	9.4	ns
		V _{CC} = 2.7 V	1.5	3.9	7.3	1.5	9.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.3	6.3	1.5	8.0	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An or Bn; see Figure 6 ^[2]						
		V _{CC} = 1.2 V	-	28	-	-	-	ns
		V _{CC} = 1.65 V	2.5	9.5	18.8	2.5	21.0	ns
		V _{CC} = 2.3 V to 2.7 V	2.1	5.3	10.3	2.1	11.5	ns
		V _{CC} = 2.7 V	1.5	5.4	9.5	1.5	12.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	4.2	8.2	1.5	10.5	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An or Bn; see Figure 6 ^[2]						
		V _{CC} = 1.2 V	-	12.0	-	-	-	ns
		V _{CC} = 1.65 V	3.0	5.0	10.2	3.0	11.0	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.8	5.8	1.0	6.3	ns
		V _{CC} = 2.7 V	1.5	3.6	6.9	1.5	9.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.7	3.3	5.9	1.7	7.5	ns
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V ^[3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ^[4]						
		V _{CC} = 1.65 V to 1.95 V	-	7.7	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	11.3	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	14.4	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz, f_o = output frequency in MHz,

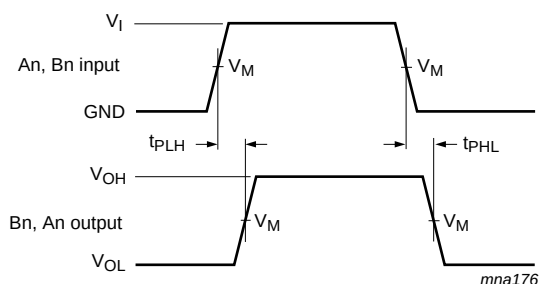
C_L = output load capacitance in pF,

V_{CC} = supply voltage in Volts,

N = number of inputs switching,

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. AC waveforms

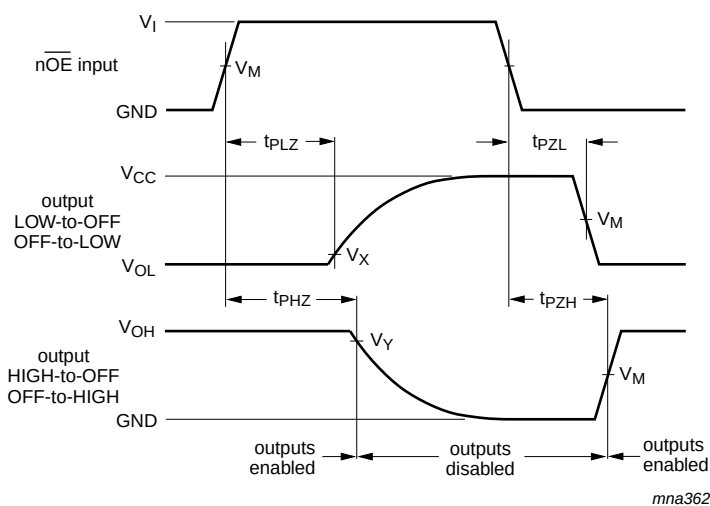


$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$.

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. The inputs An, Bn to outputs Bn, An propagation delays



$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$.

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$.

$V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$;

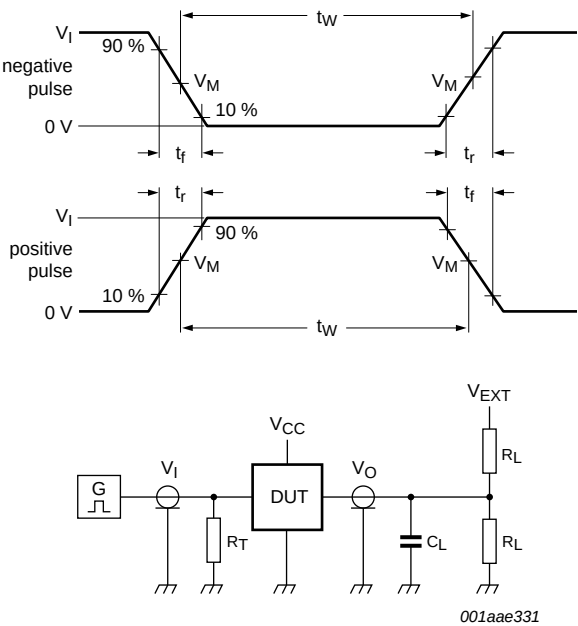
$V_X = V_{OL} + 0.15 \text{ V}$ at $V_{CC} < 2.7 \text{ V}$.

$V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$;

$V_Y = V_{OH} - 0.15 \text{ V}$ at $V_{CC} < 2.7 \text{ V}$.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. 3-state enable and disable times



Test data is given in [Table 8](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 7. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm SOT163-1

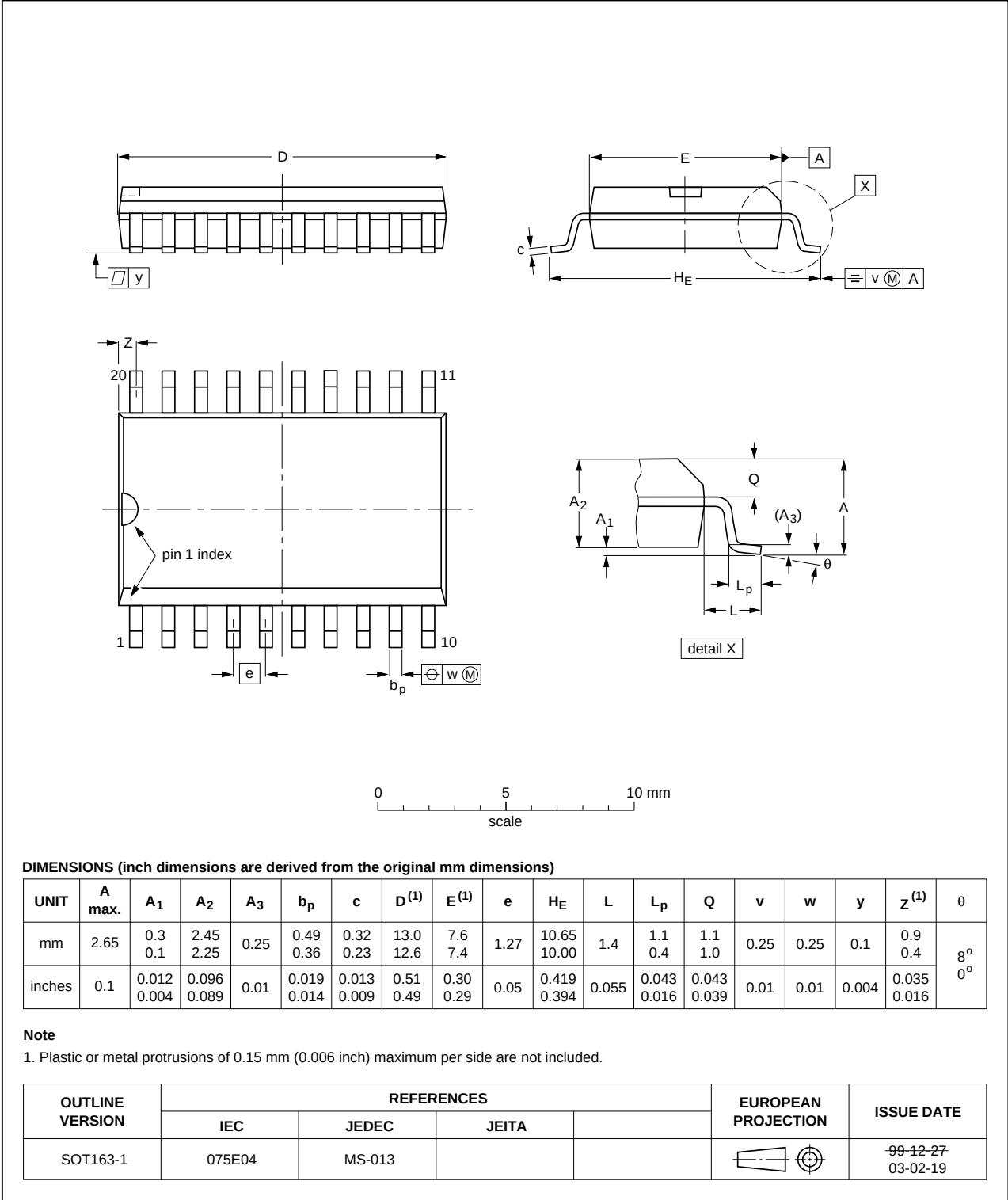
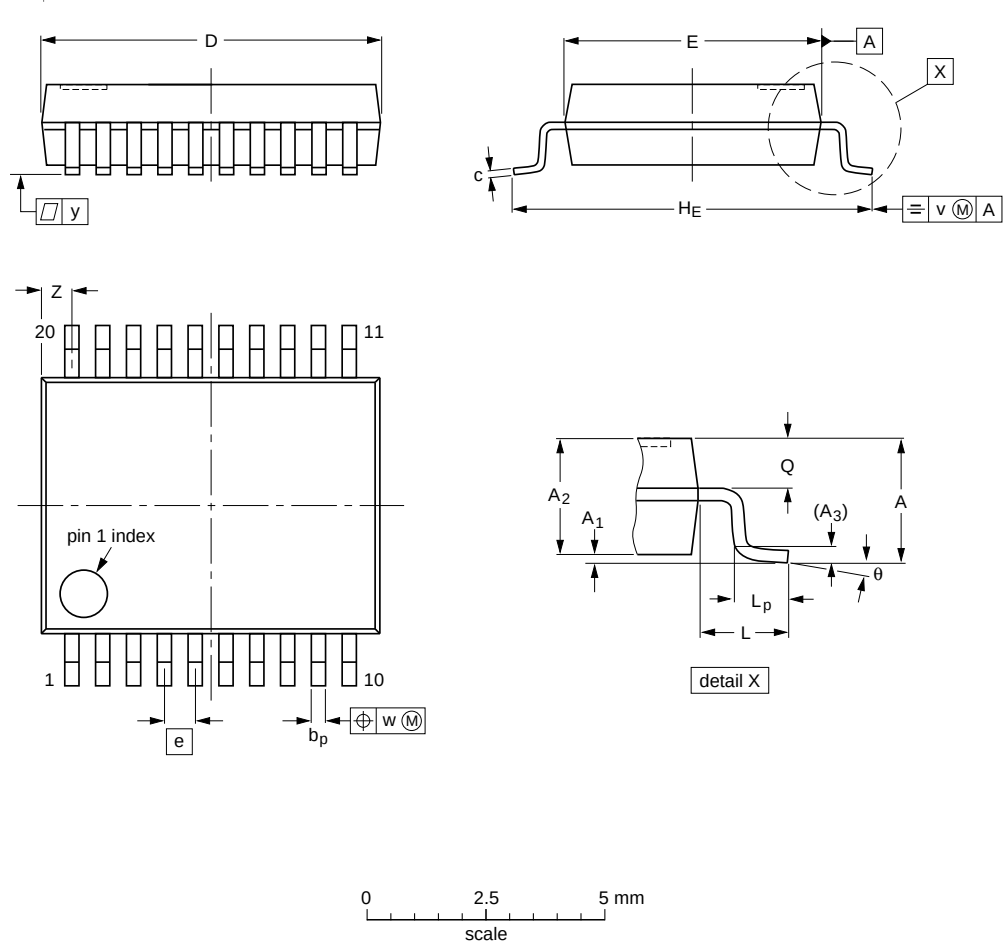


Fig 8. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				99-12-27 03-02-19

Fig 9. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

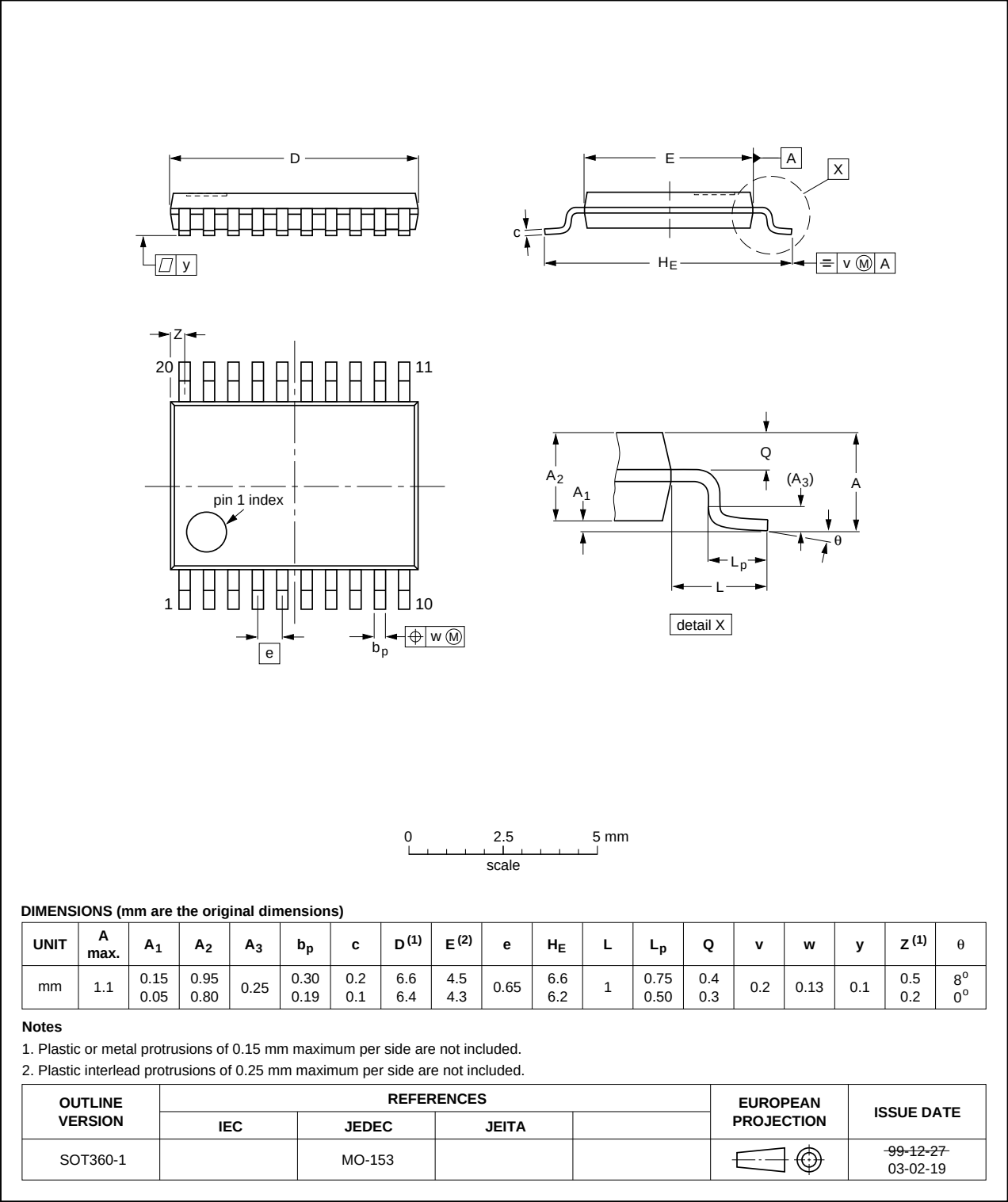


Fig 10. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

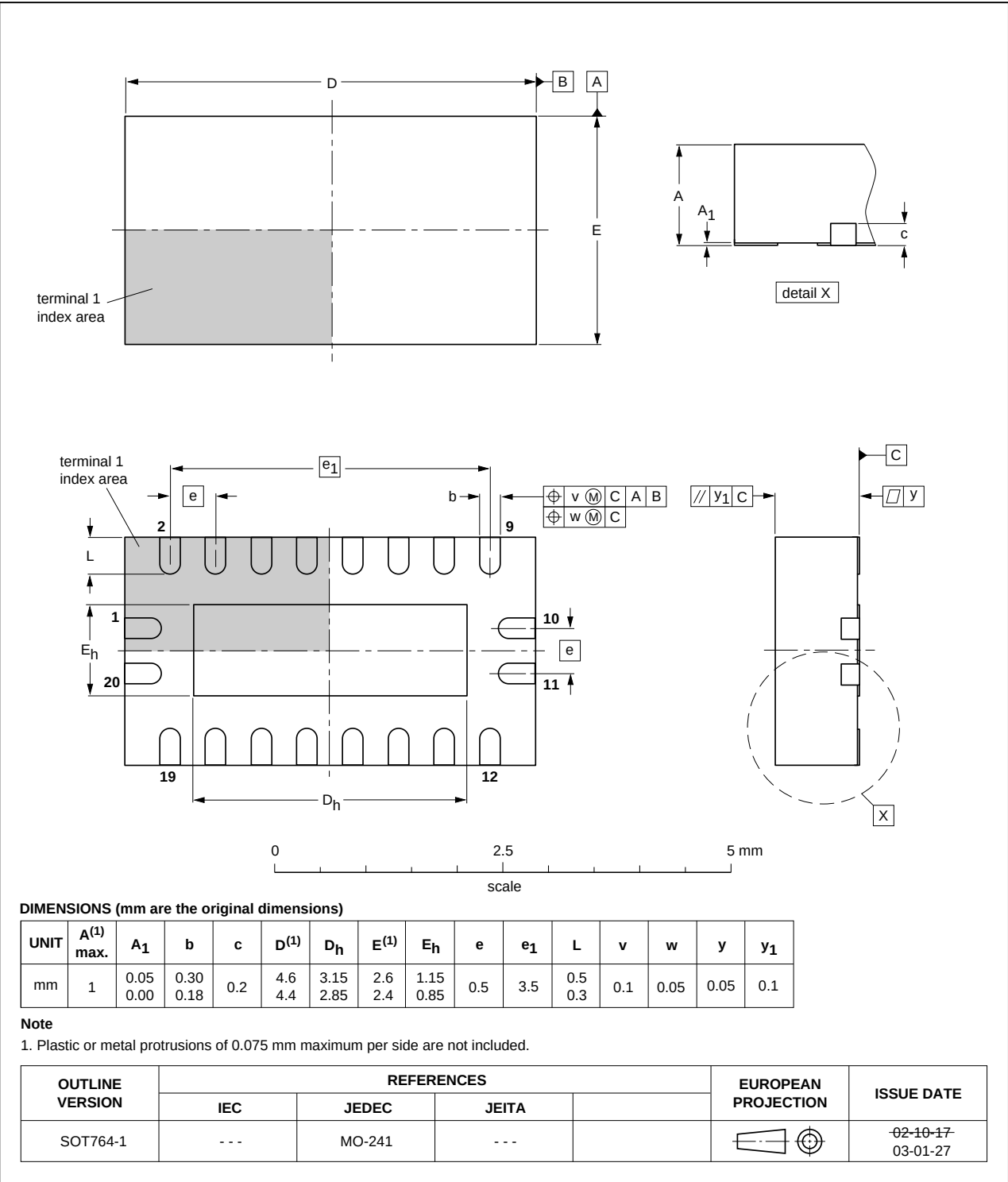


Fig 11. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2245A v.5	20111104	Product data sheet	-	74LVC2245A v.4
Modifications:	- The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7 and Table 8: values added for lower voltage ranges.			
74LVC2245A v.4	20031117	Product specification	-	74LVC2245A v.3
74LVC2245A v.3	20020610	Product specification	-	74LVC2245A v.2
74LVC2245A v.2	19990615	Product specification	-	74LVC2245A v.1
74LVC2245A v.1	19990323	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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