

Vishay Siliconix

Complementary MOSFET (N- and P-Channel)

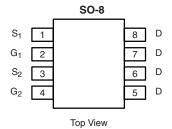
PRODUCT SUMMARY						
	V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)			
N-Channel	30	0.018 at V _{GS} = 10 V	± 9			
	30	$0.027 \text{ at V}_{GS} = 4.5 \text{ V}$	± 7.4			
P-Channel	- 8	0.042 at V _{GS} = - 4.5 V	± 6.2			
		0.060 at V _{GS} = - 2.5 V	± 5.2			

FEATURES

• Compliant to RoHS Directive 2002/95/EC

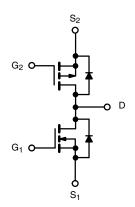






Ordering Information: Si4501DY-T1

Si4501DY-T1-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS	T _A = 25 °C, unl	ess otherwis	e noted			
Parameter		Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage		V _{DS}	30	- 8	V	
Gate-Source Voltage		V_{GS}	± 20	± 8		
Continuous Drain Current (T _J = 150 °C) ^{a, b}	T _A = 25 °C		± 9	± 6.2		
	T _A = 70 °C	ID	± 7.4	± 5.0		
Pulsed Drain Current		I _{DM}	± 30	± 20	A	
Continuous Source Current (Diode Conduction) ^{a, b}		I _S	1.7	- 1.7		
a h	T _A = 25 °C	В	2.5		w	
Maximum Power Dissipation ^{a, b}	T _A = 70 °C	P _D –	1.6			
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150			

THERMAL RESISTANCE RATINGS								
			N-Channel		P-Channel			
Parameter		Symbol	Тур.	Max.	Тур.	Max.	Unit	
Maximum Junction-to-Ambient ^a	t ≤ 10 s	R _{thJA}	38	50	40	50	°C/W	
	Steady State		73	95	73	95		
Maximum Junction-to-Foot	Steady State	R _{thJC}	17	22	20	26		

Notes:

a. Surface Mounted on FR4 board.

b. $t \le 10 \text{ s}$.

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply.

Si4501DY

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Parameter	Symbol	Test Conditions	Conditions		Typ. ^a	Max.	Unit	
Static	•							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	N-Ch	0.8			v	
		$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	P-Ch	- 0.45				
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	N-Ch			± 100	nΛ	
		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$	P-Ch			± 100	nA	
Zon Oak Vallena Buris Oursel		V _{DS} = 24 V, V _{GS} = 0 V	N-Ch			1		
		$V_{DS} = -6.4 \text{ V}, V_{GS} = 0 \text{ V}$ P-Ch $V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$ N-Ch				- 1	μΑ	
Zero Gate Voltage Drain Current	I _{DSS}					5		
		V _{DS} = - 6.4 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			- 5	1	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N-Ch	30			А	
		V _{DS} = - 5 V, V _{GS} = - 4.5 V	P-Ch	- 20				
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 9 A	N-Ch		0.015	0.018		
		V _{GS} = - 4.5 V, I _D = - 6.2 A	P-Ch		0.034	0.042		
		$V_{GS} = 4.5 \text{ V}, I_D = 7.4 \text{ A}$	N-Ch		0.022	0.027	Ω	
		V _{GS} = - 2.5 V, I _D = - 5.2 A	P-Ch		0.048	0.060		
Forward Transconductance ^b	9 _{fs}	V _{DS} = 15 V, I _D = 9 A	N-Ch		20			
		V _{DS} = - 15 V, I _D = - 6.2 A	P-Ch		14		S	
	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	N-Ch		0.71	1.1	.,	
Diode Forward Voltage ^b		I _S = - 1.7 A, V _{GS} = 0 V	P-Ch		- 0.70	- 1.1	V	
Dynamic ^a	•							
Total Gata Chargo	0		N-Ch		14.2	20		
Total Gate Charge	Qg	N-Channel $V_{DS} = 15 \text{ V, } V_{GS} = 5 \text{ V, } I_{D} = 9 \text{ A}$	P-Ch		15	25		
Gate-Source Charge	Q _{gs}	VDS = 10 V, VGS = 0 V, ID = 0 A	N-Ch		3.3		nC	
		P-Channel	P-Ch		3.0		-	
Gate-Drain Charge		$V_{DS} = -4 \text{ V}, V_{GS} = -5 \text{ V}, I_{D} = -6.2 \text{ A}$	N-Ch		6.6			
			P-Ch N-Ch		2.0	20		
Turn-On Delay Time	t _{d(on)}	N-Channel	P-Ch		20	40		
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_L = 15 \Omega$	N-Ch		9	18		
		$I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 6 \Omega$	P-Ch		50	100		
Turn-Off Delay Time	t _{d(off)}	P-Channel	N-Ch		35	50		
		$V_{DD} = -4 \text{ V}, R_L = 4 \Omega$	P-Ch		110	220	ns -	
Fall Time	t _f	$I_D \cong -1 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 6 \Omega$	N-Ch		17	30		
			P-Ch		60	120		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7 A, dI/dt = 100 A/μs	N-Ch		35	70	1	
•			P-Ch		60	100	<u> </u>	

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Guaranteed by design, not subject to production testing.

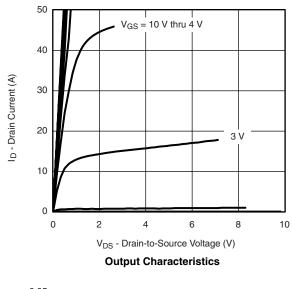
b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.

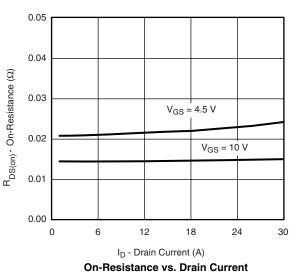


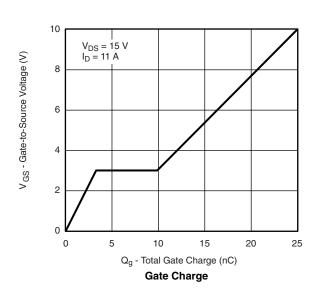


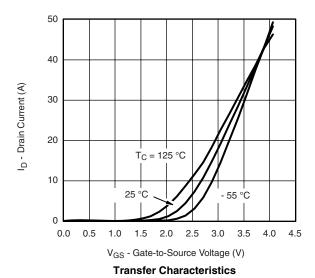


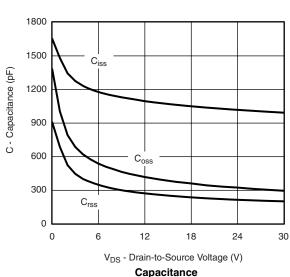
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

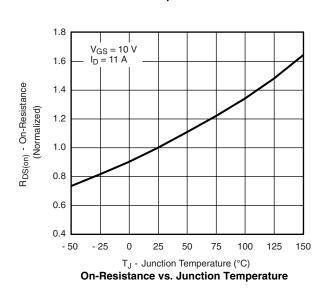








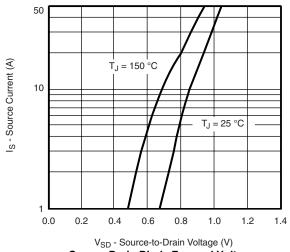




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N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



0.06 UD = 4.5 A

UD = 4.5 A

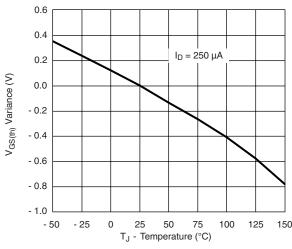
UD = 4.5 A

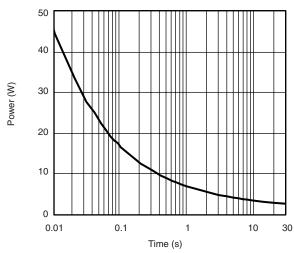
UD = 4.5 A

0.08

Source-Drain Diode Forward Voltage

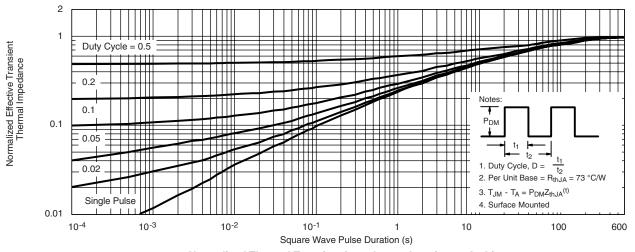






Threshold Voltage

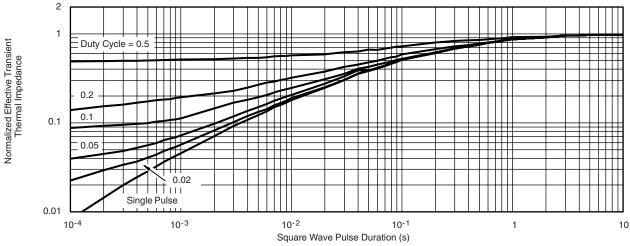
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

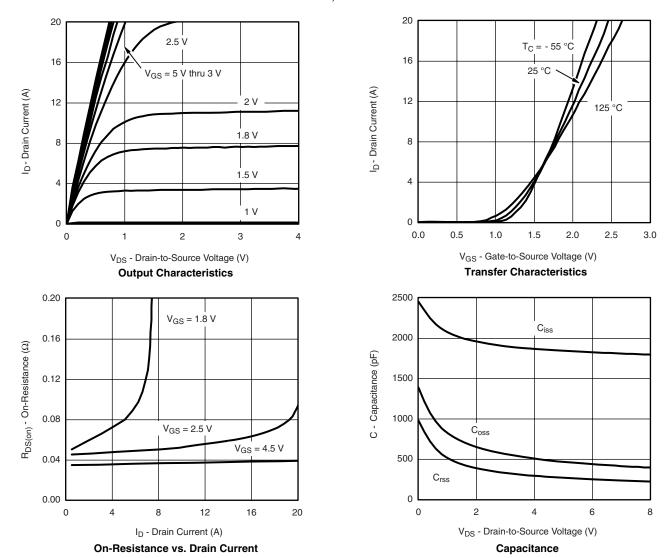


N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

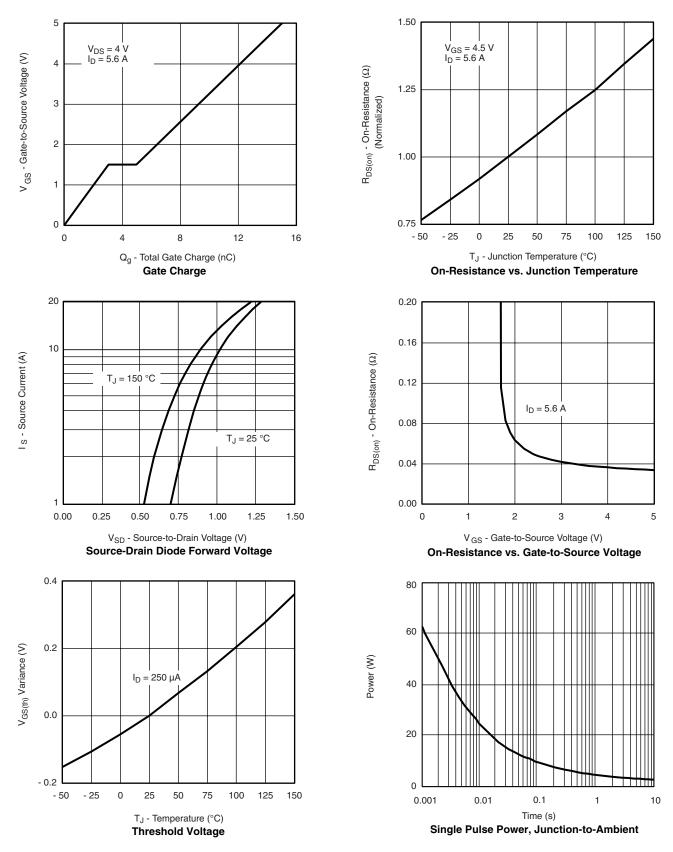
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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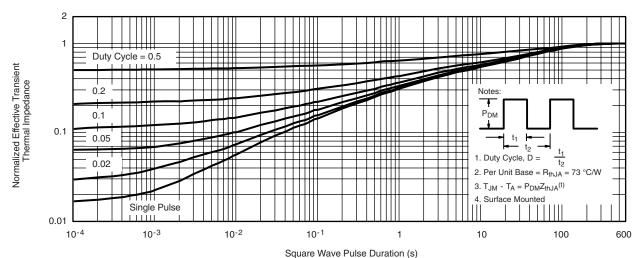
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



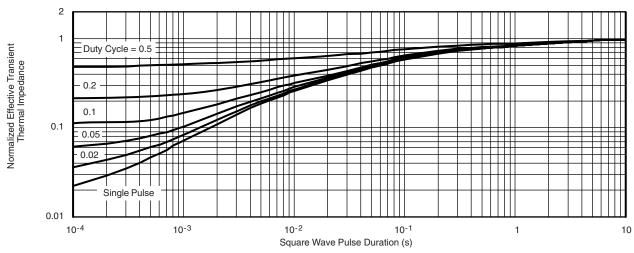




P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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