

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

Bare Die

OptiMOS™3 Power MOS Transistor Chip
IPC302NE7N3

Data Sheet

Rev. 2.5
Final

Industrial & Multimarket

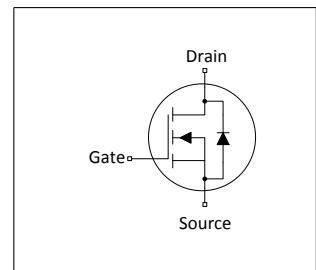
1 Description

- N-channel enhancement mode
- For dynamic characterization refer to the datasheet of IPP023NE7N3 G
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AlCu system
- Passivation: nitride (only on edge structure)
- Package: sawn on foil

Power MOS Transistor Chip


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{(BR)DSS}$	75	V
$R_{DS(on)}$	2.3 ¹⁾	$\text{m}\Omega$
Die size	6.7 x 4.5	mm^2
Thickness	175	μm



Type / Ordering Code	Package	Marking	Related Links
IPC302NE7N3	Chip	not defined	-

2 Electrical Characteristics on Wafer Level

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	75	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(\text{th})}$	2.3	3.1	3.8	V	$V_{DS}=V_{GS}$, $I_D=270\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{GS}=0\text{ V}$, $V_{DS}=75\text{ V}$
Gate-source leakage current	I_{GSS}	-	1	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on- resistance	$R_{DS(\text{on})}$	-	1.2 ²⁾	100 ³⁾	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=2.0\text{ A}$
Reverse diode forward on-voltage	V_{SD}	-	0.9	1.2	V	$V_{GS}=0\text{ V}$, $I_F=1\text{ A}$
Avalanche energy, single pulse	E_{AS}	-	40 ⁴⁾	-	mJ	$I_D=30\text{ A}$, $R_{GS}=25\text{ }\Omega$

¹⁾ packaged in a P-TO220-3 (see ref. product)

²⁾ typical bare die $R_{DS(\text{on})}$; $V_{GS}=10\text{ V}$
³⁾ limited by wafer test-equipment

⁴⁾ Wafer tested. For general avalanche capability refer to the datasheet of IPP023NE7N3 G

3 Package Outlines

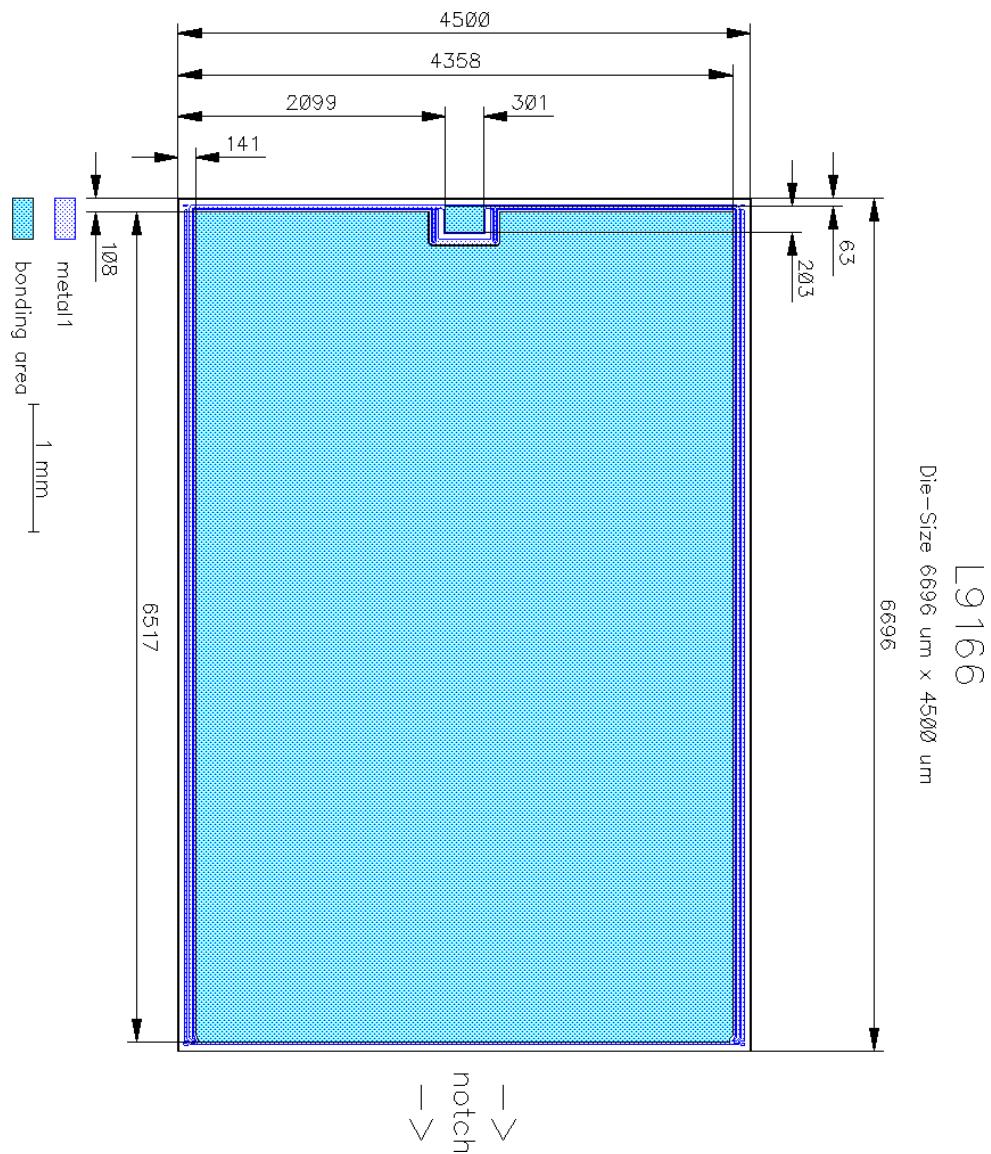


Figure 1 Outline Chip, dimensions in μm

Revision History

IPC302NE7N3

Revision: 2014-07-23, Rev. 2.5

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.5	2014-07-23	Release Final Version

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