19-1995; Rev 0; 4/01

MAXIM

Single LVDS Line Receiver in SC70

General Description

The MAX9115 is a single low-voltage differential signaling (LVDS) line receiver ideal for applications requiring high data rates, low power, and low noise. The device is guaranteed to receive data at speeds up to 200Mbps (100MHz).

The MAX9115 accepts an LVDS differential input and translates it to an LVTTL/LVCMOS output. The fail-safe feature sets the output high when the inputs are undriven and open, terminated, or shorted. The device supports a wide common-mode input range, allowing a ground potential difference and common-mode noise between the driver and the receiver. The MAX9115 conforms to the ANSI TIA/EIA-644 LVDS standard.

The MAX9115 operates from a single +3.3V supply, and is specified for operation from -40°C to +85°C. It is available in a space-saving 5-pin SC70 package. Refer to the MAX9110/MAX9112 data sheet for single/dual LVDS line drivers.

Features

- **Space-Saving SC70 Package (50% Smaller than SOT23)**
- **Guaranteed 200Mbps Data Rate**
- **Low 350ps (max) Pulse Skew**
- **High-Impedance LVDS Inputs When Powered Off Allow Hot Swapping**
- **Conforms to ANSI TIA/EIA-644 LVDS Standard**
- **Single +3.3V Supply**
- **Fail-Safe Circuit Sets Output High for Undriven Inputs (Open, Terminated, or Shorted)**
- **Low 150µA (typ) Supply Current in Fail-Safe Mode**

Applications

Clock Distribution

Cellular Phone Base Stations

Digital Cross-Connects

Network Switches/Routers

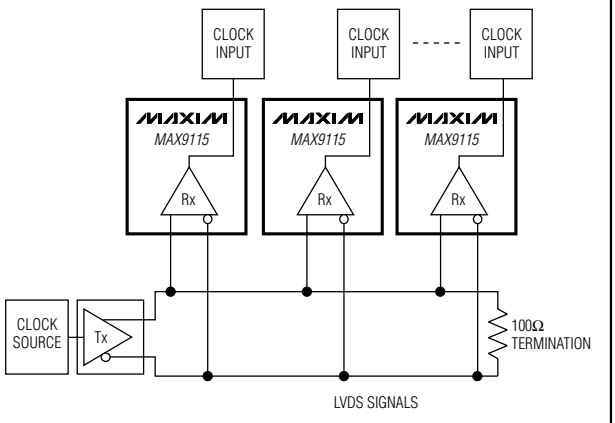
DSLAMs

Laser Printers

Ordering Information

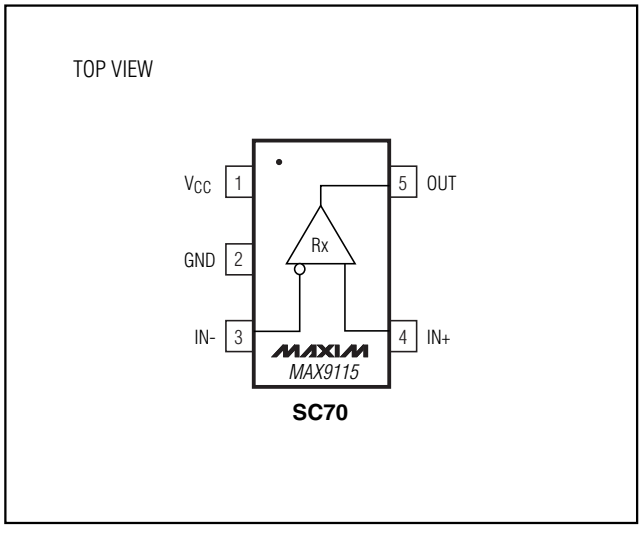
PART	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX9115EXK-T	-40°C to +85°C	5 SC70-5	ACI

Typical Application Circuit



REFERENCE CLOCK DISTRIBUTION
USING MAX9115 IN A MULTIDROP CONFIGURATION

Pin Configuration



Single LVDS Line Receiver in SC70

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.0V
IN+, IN- to GND .....-0.3V to +4.0V
OUT to GND .....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
5-Pin SC70 (derate 3.1mW/°C above +70°C) .....247 mW
Output Short to GND (OUT) (Note 1) 1s
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Lead Temperature (soldering, 10s) .....+300°C
ESD Protection
Human Body Model (IN+, IN-) .....±6kV

Note 1: Package leads soldered to a PC board having copper ground and V_{CC} planes. Do not exceed Maximum Junction Temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.05V to 1.0V, input common voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values at V_{CC} = +3.3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS INPUTS (IN+, IN-)							
Differential Input High Threshold	V_{TH}					50	mV
Differential Input Low Threshold	V_{TL}			-50			mV
Input Current	I_{IN+}, I_{IN-}	0.05V ≤ $\|V_{ID}\|$ ≤ 0.6V		-20		20	µA
		0.6V < $\|V_{ID}\|$ ≤ 1.0V		-25		25	
Power-Off Input Current	I_{INO}	0.05V ≤ $\|V_{ID}\|$ ≤ 0.6V, V_{CC} = 0		-20		20	µA
		0.6V < $\|V_{ID}\|$ ≤ 1.0V, V_{CC} = 0		-25		25	
Input Resistance	R_{IN1}	V_{CC} = +3.6V or 0, Figure 1		35			kΩ
	R_{IN2}	V_{CC} = +3.6V or 0, Figure 1		132			
LVTTL/LVCMOS OUTPUT (OUT)							
Output High Voltage	V_{OH}	I_{OH} = -8.0mA	Inputs open or undriven short or undriven 100Ω termination	V_{CC} - 0.3			V
			V_{ID} = +50mV	V_{CC} - 0.3			
Output Low Voltage	V_{OL}	I_{OL} = +8.0mA, V_{ID} = -50mV				0.25	V
Output Short-Circuit Current	I_{OS}	V_{ID} = +50mV, V_{OUT} = 0				-125	mA
SUPPLY CURRENT							
Supply Current	I_{CC}	No load, inputs undriven (fail-safe)			150	300	µA
		No load, inputs driven				7	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C_L = 15pF, differential input voltage $|V_{ID}|$ = 0.15V to 1.0V, input common voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, input rise and fall time = 1ns (20% to 80%), input frequency = 100MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C.) (Figures 2 and 3) (Notes 4 and 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	t_{PHLD}		1.2	1.9	3	ns
Differential Propagation Delay Low to High	t_{PLHD}		1.2	1.9	3	ns
Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$ (Note 6)	t_{SKD1}				350	ps
Differential Part-to-Part Skew (Note 7)	t_{SKD2}				1.3	ns
Differential Part-to-Part Skew (Note 8)	t_{SKD3}				1.8	ns
Rise-Time	t_{TLH}			0.5	0.8	ns
Fall-Time	t_{THL}			0.5	0.8	ns
Maximum Operating Frequency (Note 9)	f_{MAX}		100			MHz

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

Note 3: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH}, V_{TL}, and V_{ID}.

Note 4: AC parameters are guaranteed by design and characterization.

Note 5: CL includes scope probe and test jig capacitance.

Note 6: t_{SKD1} is the magnitude difference of differential propagation delays. $t_{SKD1} = |t_{PHLD} - t_{PLHD}|$.

Note 7: t_{SKD2} is the magnitude difference of any differential propagation delays between parts operating over rated conditions at the same V_{CC} and within 5°C of each other.

Note 8: t_{SKD3} is the magnitude difference of any differential propagation delays between parts operating over rated conditions.

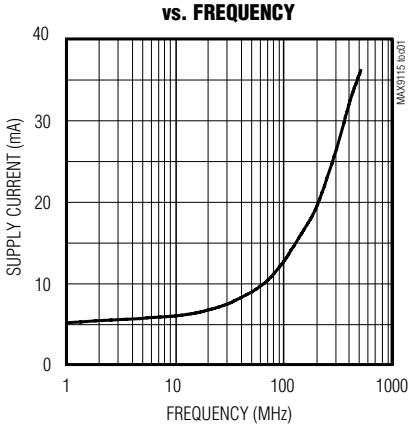
Note 9: f_{MAX} pulse generator output conditions: rise-time = fall-time = 1ns (0% to 100%), 50% duty cycle, V_{OH} = +1.3V, V_{OL} = +1.1V. MAX9115 output criteria: 60% to 40% duty cycle, V_{OL} = 0.25V max, V_{OH} = 2.7V min, load = 15pF.

Single LVDS Line Receiver in SC70

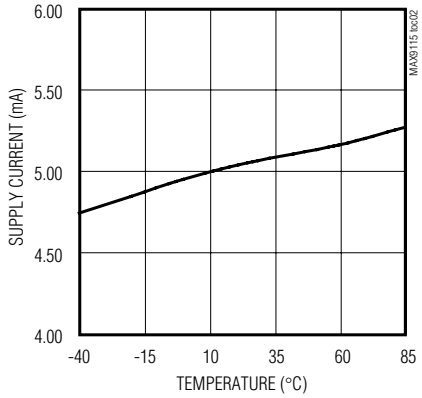
Typical Operating Characteristics

(V_{CC} = +3.3V, C_L = 15pF, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, input rise and fall time = 1ns (20% to 80%), input frequency = 100MHz, 50% duty cycle, T_A = +25°C, unless otherwise noted.)

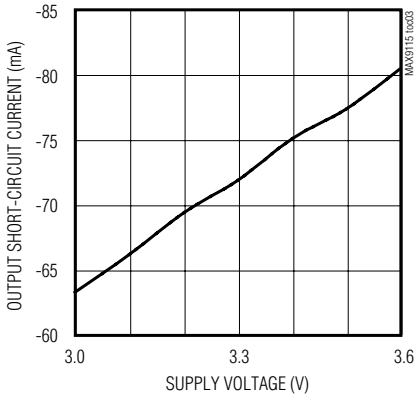
SUPPLY CURRENT vs. FREQUENCY



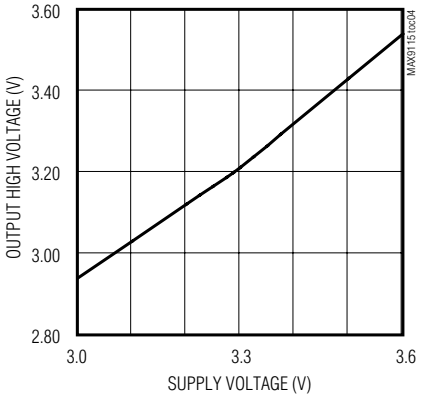
SUPPLY CURRENT vs. TEMPERATURE



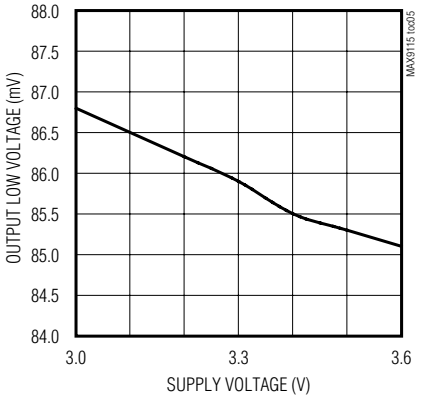
OUTPUT SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAGE



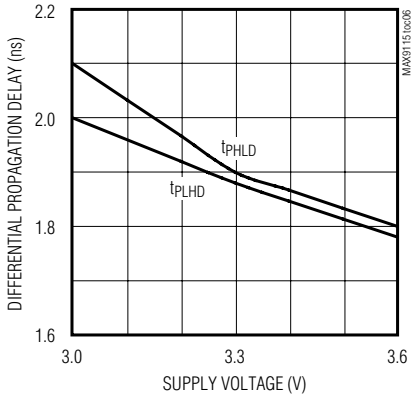
OUTPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



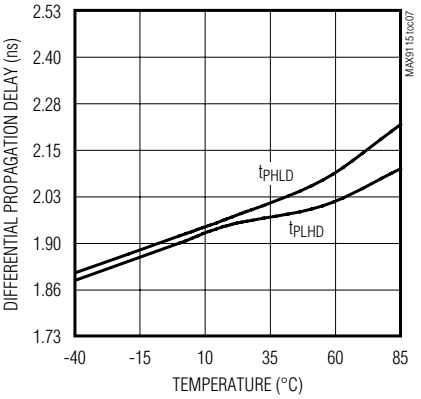
OUTPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



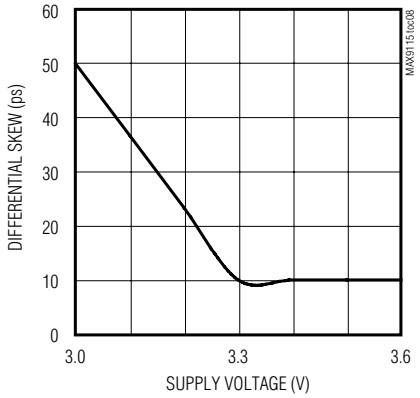
DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



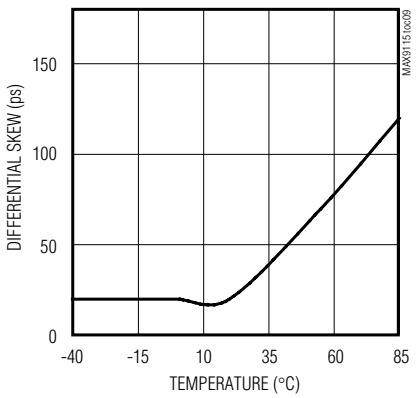
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, C_L = 15pF, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, input rise and fall time = 1ns (20% to 80%), input frequency = 100MHz, 50% duty cycle, T_A = +25°C, unless otherwise noted.)

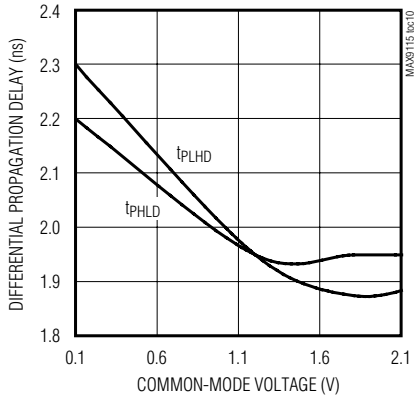
DIFFERENTIAL SKEW vs. SUPPLY VOLTAGE



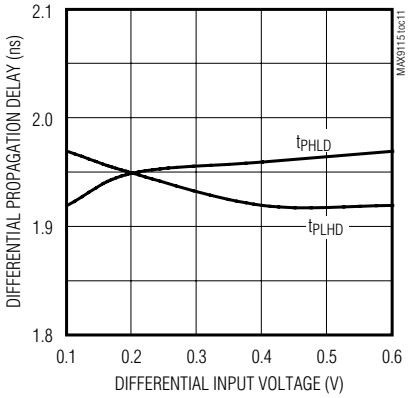
DIFFERENTIAL SKEW vs. TEMPERATURE



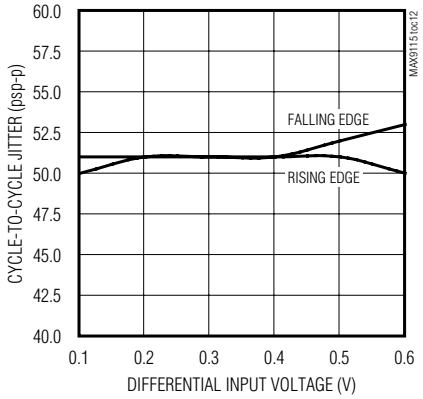
DIFFERENTIAL PROPAGATION DELAY vs. COMMON-MODE VOLTAGE



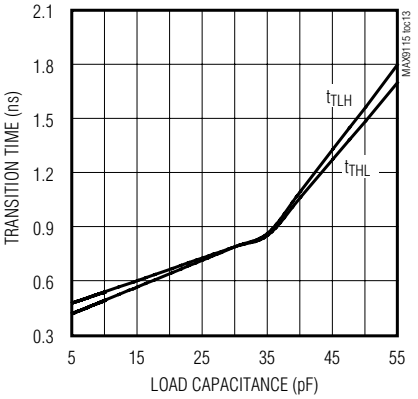
DIFFERENTIAL PROPAGATION DELAY vs. DIFFERENTIAL INPUT VOLTAGE



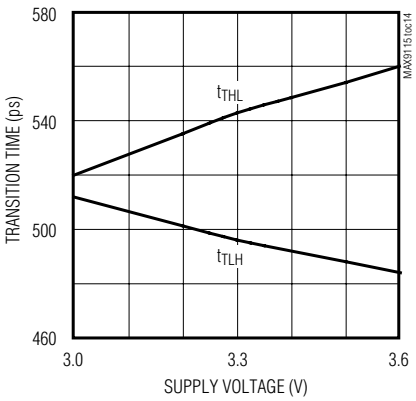
CYCLE-TO-CYCLE JITTER vs. DIFFERENTIAL INPUT VOLTAGE



TRANSITION TIME vs. LOAD CAPACITANCE



TRANSITION TIME vs. SUPPLY VOLTAGE



Single LVDS Line Receiver in SC70

Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 0.01µF ceramic capacitor.
2	GND	Ground
3	IN-	Inverting LVDS Differential Input
4	IN+	Noninverting LVDS Differential Input
5	OUT	LVTTL/LVCMOS Output

Detailed Description

LVDS is intended for point-to-point communication over a controlled-impedance medium as defined by the ANSI TIA/EIA-644 and IEEE 1596.3 standards. LVDS uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The MAX9115 is a single LVDS line receiver ideal for applications requiring high data rates, low power, and low noise. The device accepts an LVDS input and translates it to an LVTTL/LVCMOS output. The receiver detects differential signals as low as 50mV and as high as 1V within an input voltage range of 0 to +2.4V.

The 250mV to 450mV differential output of an LVDS driver is nominally centered around a +1.25V offset. This offset, coupled with the receiver's 0 to +2.4V input voltage range, allows an approximate ±1V shift in the signal (as seen by the receiver). This allows for a difference in ground references of the driver and the receiver, the common-mode effects of coupled noise, or both. The LVDS standards specify an input voltage range of 0 to +2.4V referenced to receiver ground.

Fail-Safe

The fail-safe feature of the MAX9115 sets the output high and reduces supply current when:

- inputs are open
- inputs are undriven and shorted
- inputs are undriven and terminated

A fail-safe circuit is important because under these conditions, noise at the input may switch the receiver and it may appear to the system that data is being received. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when an LVDS driver output is in high impedance. A short condition can occur because of a cable failure.

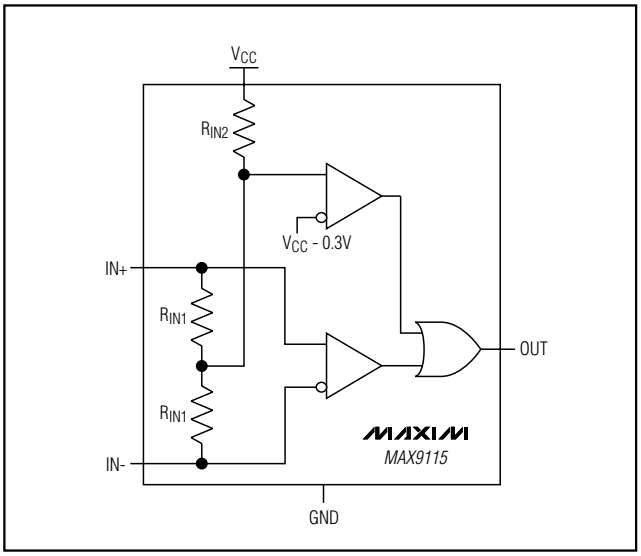


Figure 1. Input Fail-Safe Network

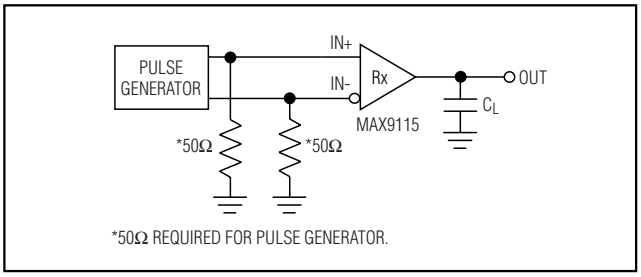


Figure 2. Propagation Delay and Transition Time Test Circuit

The fail-safe input network (Figure 1) samples the input common-mode voltage and compares it to V_{CC} - 0.3V (nominal). When the input is driven to levels specified in the LVDS standards, the input common-mode voltage is less than V_{CC} - 0.3V and the fail-safe circuit is not activated. If the inputs are open or if the inputs are undriven and shorted or undriven and parallel terminated, there is no input current. In this case, a pullup resistor in the fail-safe circuit pulls both inputs above V_{CC} - 0.3V, activating the fail-safe circuit and forcing the output high.

Applications Information

Power-Supply Bypassing

Bypass V_{CC} with a high-frequency surface-mount ceramic 0.01µF capacitor in parallel as close to the device as possible.

Differential Traces

Input trace characteristics affect the performance of the MAX9115. Use controlled-impedance PC board traces, typically 100Ω. Match the termination resistor to this characteristic impedance.

Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Input differential signals should be routed close to each other to cancel their external magnetic field. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Transmission media should typically have a controlled differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

The MAX9115 requires an external termination resistor. The termination resistor should match the differential impedance of the transmission line. Termination resistance is typically 100Ω but may range between 90Ω to 132Ω, depending on the characteristic impedance of the transmission medium.

When using the MAX9115, minimize the distance between the input termination resistor and the MAX9115 receiver inputs. Use 1% surface-mount resistors.

Board Layout

For LVDS applications, a four-layer PC board that provides separate layers, power, ground, and input/output signals is recommended. Keep the LVDS input signals away from the output LVCMOS/LVTTL signal to prevent coupling (Figure 4). To minimize crosstalk, do not run the output in parallel with the inputs. Extend the ground pin trace under the package to the other side between IN+ and OUT to provide isolation between IN+ and OUT.

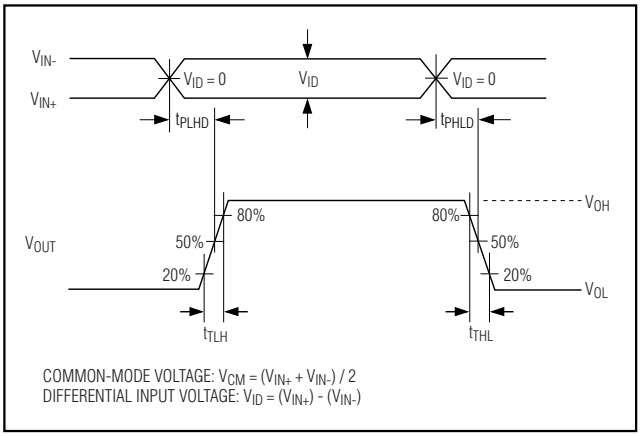


Figure 3. Propagation Delay and Transition-Time Waveforms

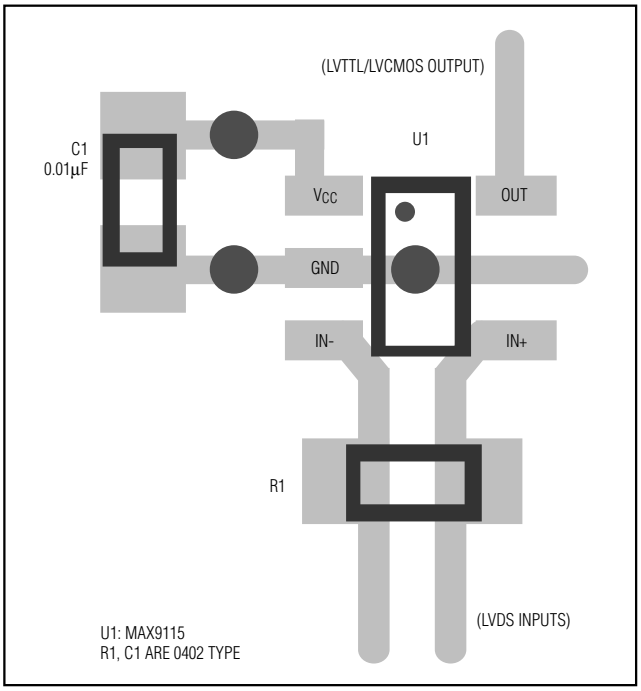


Figure 4. Board Layout

Chip Information

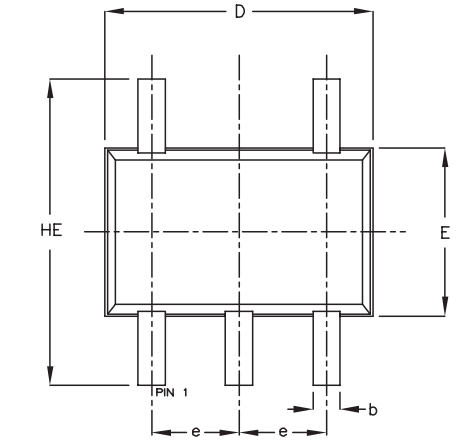
TRANSISTOR COUNT: 201

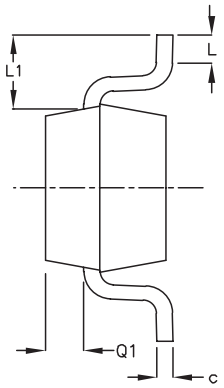
PROCESS: CMOS

Single LVDS Line Receiver in SC70

Package Information

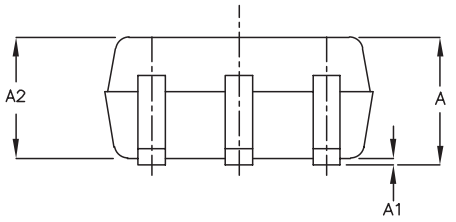
SC70, 5L.EPS





SYMBOL	MIN	MAX
e	0.65 BSC	
D	1.80	2.20
b	0.15	0.30
E	1.15	1.35
HE	1.80	2.40
Q1	0.10	0.40
A2	0.80	1.00
A1	0.00	0.10
A	0.80	1.10
c	0.10	0.18
L	0.10	0.30
L1	0.425 TYP.	

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70
5. COPLANARITY 4 MILS. MAX.



MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, SC70, 5L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0076	B	1/1