TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74LVX573F,TC74LVX573FW,TC74LVX573FT

## Octal D-Type Latch with 3-State Output

The TC74LVX573F/ FW/ FT is a high-speed CMOS octal latch with 3-state output fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low-voltage and battery operated systems.

This 8 bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$). When the $\overline{OE}$ input is high, the eight outputs are in a high-impedance state.

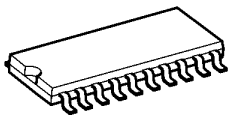
An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

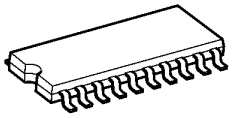
- High speed: $t_{pd}$ = 6.4 ns (typ.) ($V_{CC}$ = 3.3 V)
- Low-power dissipation: $I_{CC}$ = 4 μA (max) (Ta = 25°C)
- Input voltage level: $V_{IL}$ = 0.8 V (max) ($V_{CC}$ = 3 V)
  $V_{IH}$ = 2.0 V (min) ($V_{CC}$ = 3 V)
- Power-down protection provided on all inputs
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Low noise: $V_{OLP}$ = 0.8 V (max)
- Pin and function compatible with 74HC573

Note: xxxFW (JEDEC SOP) is not available in Japan.

TC74LVX573F

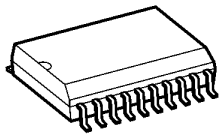


SOP20-P-300-1.27A



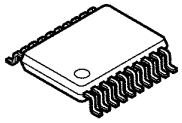
SOP20-P-300-1.27

TC74LVX573FW



SOL20-P-300-1.27

TC74LVX573FT

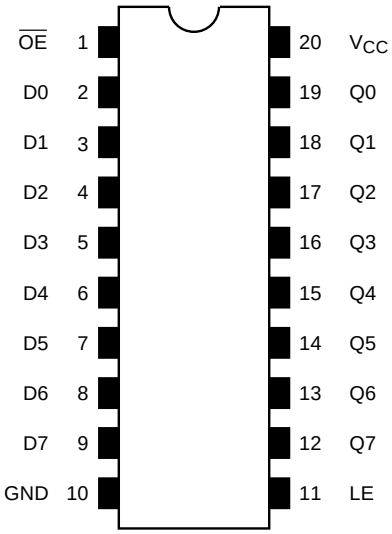


TSSOP20-P-0044-0.65A

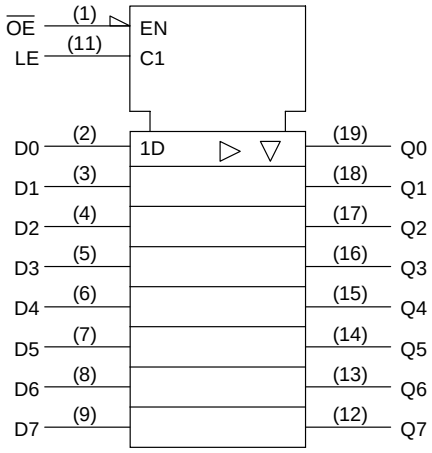
Weight

| | |
|---|---|
| SOP20-P-300-1.27A | : 0.22 g (typ.) |
| SOP20-P-300-1.27 | : 0.22 g (typ.) |
| SOL20-P-300-1.27 | : 0.46 g (typ.) |
| TSSOP20-P-0044-0.65A | : 0.08 g (typ.) |

## Pin Assignment (top view)




## IEC Logic Symbol




## Truth Table

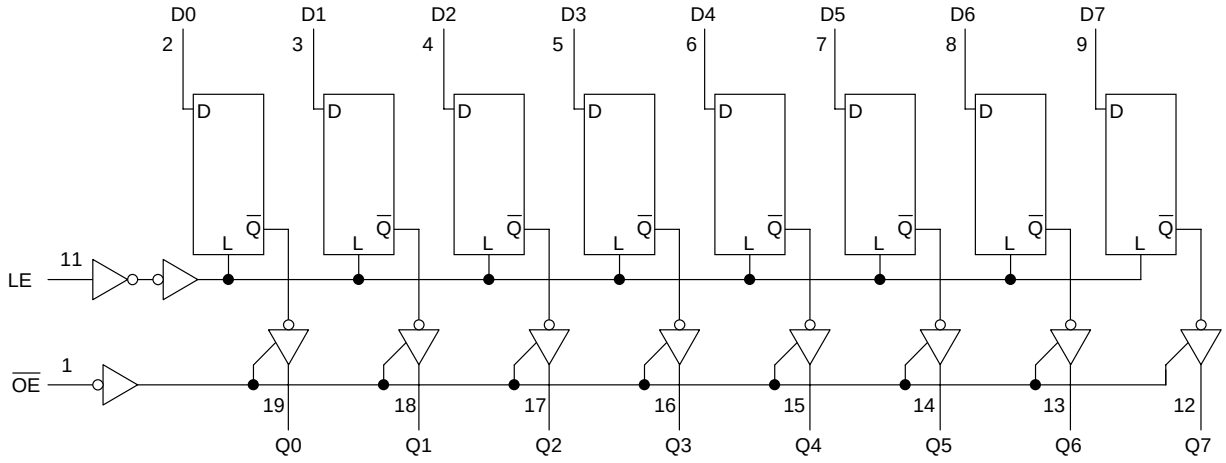
| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE}$ | LE | D | |
| H | X | X | Z |
| L | L | X | Qn |
| L | H | L | L |
| L | H | H | H |

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

## System Diagram



## Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{CC}$ | −0.5 to 7.0 | V |
| DC input voltage | $V_{IN}$ | −0.5 to 7.0 | V |
| DC output voltage | $V_{OUT}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| Input diode current | $I_{IK}$ | −20 | mA |
| Output diode current | $I_{OK}$ | ±20 | mA |
| DC output current | $I_{OUT}$ | ±25 | mA |
| DC $V_{CC}$/ground current | $I_{CC}$ | ±75 | mA |
| Power dissipation | $P_D$ | 180 | mW |
| Storage temperature | $T_{stg}$ | −65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

## Recommended Operating Conditions (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2.0 to 3.6 | V |
| Input voltage | $V_{IN}$ | 0 to 5.5 | V |
| Output voltage | $V_{OUT}$ | 0 to $V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | −40 to 85 | °C |
| Input rise and fall time | dt/dv | 0 to 100 | ns/V |

Note: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

| Characteristics | | Sym-bol | Test Condition | | $V_{CC}$ (V) | Ta = 25°C Min | Typ. | Max | Ta = –40 to 85°C Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Input voltage | H-level | $V_{IH}$ | — | | 2.0 | 1.5 | — | — | 1.5 | — | V |
| | | | | | 3.0 | 2.0 | — | — | 2.0 | — | |
| | | | | | 3.6 | 2.4 | — | — | 2.4 | — | |
| | L-level | $V_{IL}$ | — | | 2.0 | — | — | 0.5 | — | 0.5 | |
| | | | | | 3.0 | — | — | 0.8 | — | 0.8 | |
| | | | | | 3.6 | — | — | 0.8 | — | 0.8 | |
| Output voltage | H-level | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –50 μA | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | $I_{OH}$ = –50 μA | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | | $I_{OH}$ = –4 mA | 3.0 | 2.58 | — | — | 2.48 | — | |
| | L-level | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 2.0 | — | 0 | 0.1 | — | 0.1 | |
| | | | | $I_{OL}$ = 50 μA | 3.0 | — | 0 | 0.1 | — | 0.1 | |
| | | | | $I_{OL}$ = 4 mA | 3.0 | — | — | 0.36 | — | 0.44 | |
| 3-state output Off-state current | | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{OUT}$ = $V_{CC}$ or GND | | 3.6 | — | — | ±0.25 | — | ±2.5 | μA |
| Input leakage current | | $I_{IN}$ | $V_{IN}$ = 5.5 V or GND | | 3.6 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent supply current | | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 3.6 | — | — | 4.0 | — | 40.0 | μA |

### Timing Requirements (input: $t_r = t_f = 3$ ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Ta = 25°C Limit | Ta = –40 to 85°C Limit | Unit |
|---|---|---|---|---|---|---|
| Minimum pulse width (LE) | $t_{W(H)}$ | — | 2.7 | 6.5 | 7.5 | ns |
| | | | 3.3 ± 0.3 | 5.0 | 5.0 | |
| Minimum set-up time | $t_s$ | — | 2.7 | 5.0 | 5.0 | ns |
| | | | 3.3 ± 0.3 | 3.5 | 3.5 | |
| Minimum hold time | $t_h$ | — | 2.7 | 1.5 | 1.5 | ns |
| | | | 3.3 ± 0.3 | 1.5 | 1.5 | |

**AC Characteristics (input: $t_r = t_f = 3$ ns)**

| Characteristics | Symbol | Test Condition | | | Ta = 25°C | | | Ta = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | $C_L$ (pF) | Min | Typ. | Max | Min | Max | |
| Propagation delay time (LE-Q) | $t_{pLH}$ | — | 2.7 | 15 | — | 8.2 | 15.6 | 1.0 | 18.5 | ns |
| | | | | 50 | — | 10.7 | 19.1 | 1.0 | 22.0 | |
| | $t_{pHL}$ | | 3.3 ± 0.3 | 15 | — | 6.4 | 10.1 | 1.0 | 12.0 | |
| | | | | 50 | — | 8.9 | 13.6 | 1.0 | 15.5 | |
| Propagation delay time (D-Q) | $t_{pLH}$ | — | 2.7 | 15 | — | 7.6 | 14.5 | 1.0 | 17.5 | ns |
| | | | | 50 | — | 10.1 | 18.0 | 1.0 | 21.0 | |
| | $t_{pHL}$ | | 3.3 ± 0.3 | 15 | — | 5.9 | 9.3 | 1.0 | 11.0 | |
| | | | | 50 | — | 8.4 | 12.8 | 1.0 | 14.5 | |
| Output enable time | $t_{pZL}$ | $R_L$ = 1 kΩ | 2.7 | 15 | — | 7.8 | 15.0 | 1.0 | 18.5 | ns |
| | | | | 50 | — | 10.3 | 18.5 | 1.0 | 22.0 | |
| | $t_{pZH}$ | | 3.3 ± 0.3 | 15 | — | 6.1 | 9.7 | 1.0 | 12.0 | |
| | | | | 50 | — | 8.6 | 13.2 | 1.0 | 15.5 | |
| Output disable time | $t_{pLZ}$ | $R_L$ = 1 kΩ | 2.7 | 50 | — | 12.1 | 19.1 | 1.0 | 22.0 | ns |
| | $t_{pHZ}$ | | 3.3 ± 0.3 | 50 | — | 10.1 | 13.6 | 1.0 | 15.5 | |
| Output to output skew | $t_{osLH}$ | (Note 1) | 2.7 | 50 | — | — | 1.5 | — | 1.5 | ns |
| | $t_{osHL}$ | | 3.3 ± 0.3 | 50 | — | — | 1.5 | — | 1.5 | |
| Input capacitance | $C_{IN}$ | (Note 2) | | | — | 4 | 10 | — | 10 | pF |
| Output capacitance | $C_{OUT}$ | — | | | — | 6 | — | — | — | pF |
| Power dissipation capacitance | $C_{PD}$ | (Note 3) | | | — | 29 | — | — | — | pF |

Note 1: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

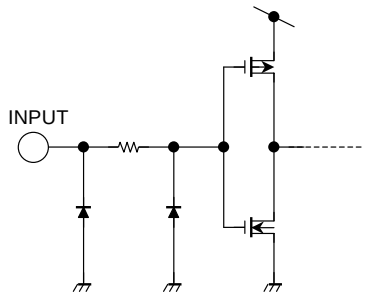
Note 2: Parameter guaranteed by design.

Note 3: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per latch)
And the total $C_{PD}$ when n pcs. of Latch operate can be gained by the following equation:
$C_{PD}$ (total) = 21 + 8·n

**Noise Characteristics (Ta = 25°C, input: $t_r = t_f = 3$ ns, $C_L = 50$ pF)**

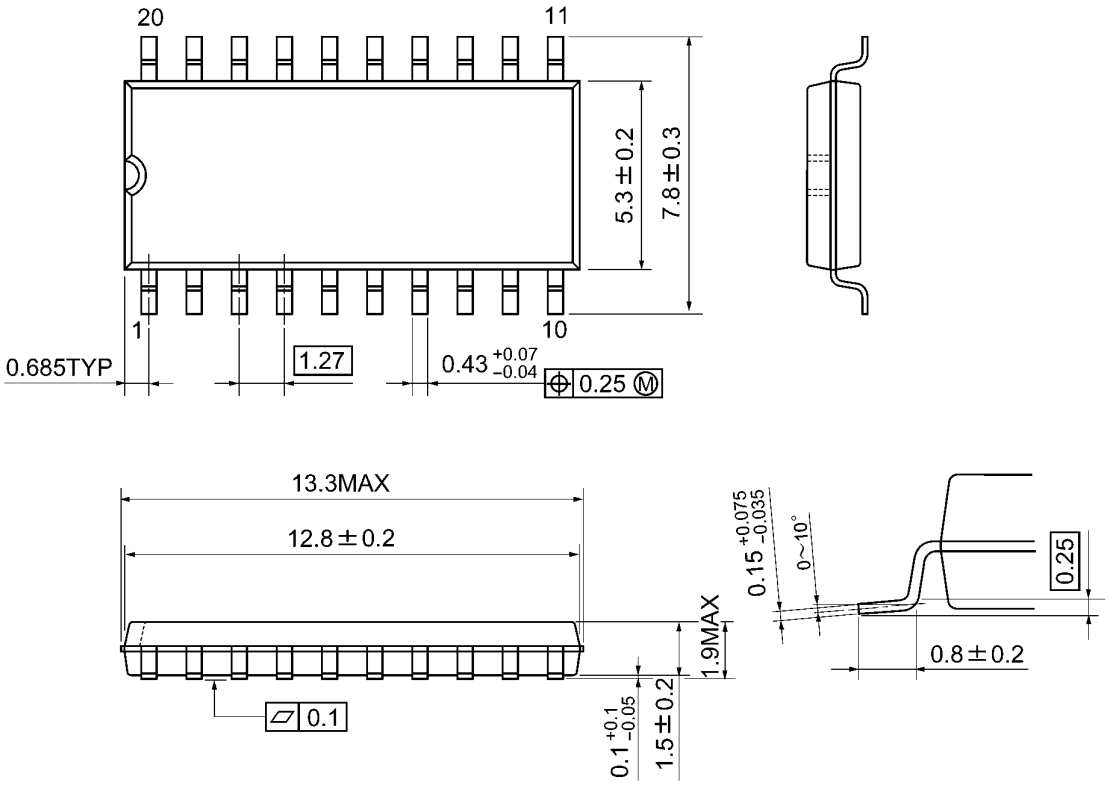
| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Typ. | Limit | Unit |
|---|---|---|---|---|---|---|
| Quiet output maximum dynamic $V_{OL}$ | $V_{OLP}$ | — | 3.3 | 0.5 | 0.8 | V |
| Quiet output minimum dynamic $V_{OL}$ | $V_{OLV}$ | — | 3.3 | –0.5 | –0.8 | V |
| Minimum high level dynamic input voltage $V_{IH}$ | $V_{IHD}$ | — | 3.3 | — | 2.0 | V |
| Maximum low level dynamic input voltage $V_{IL}$ | $V_{ILD}$ | — | 3.3 | — | 0.8 | V |

## Input Equivalent Circuit



## Package Dimensions

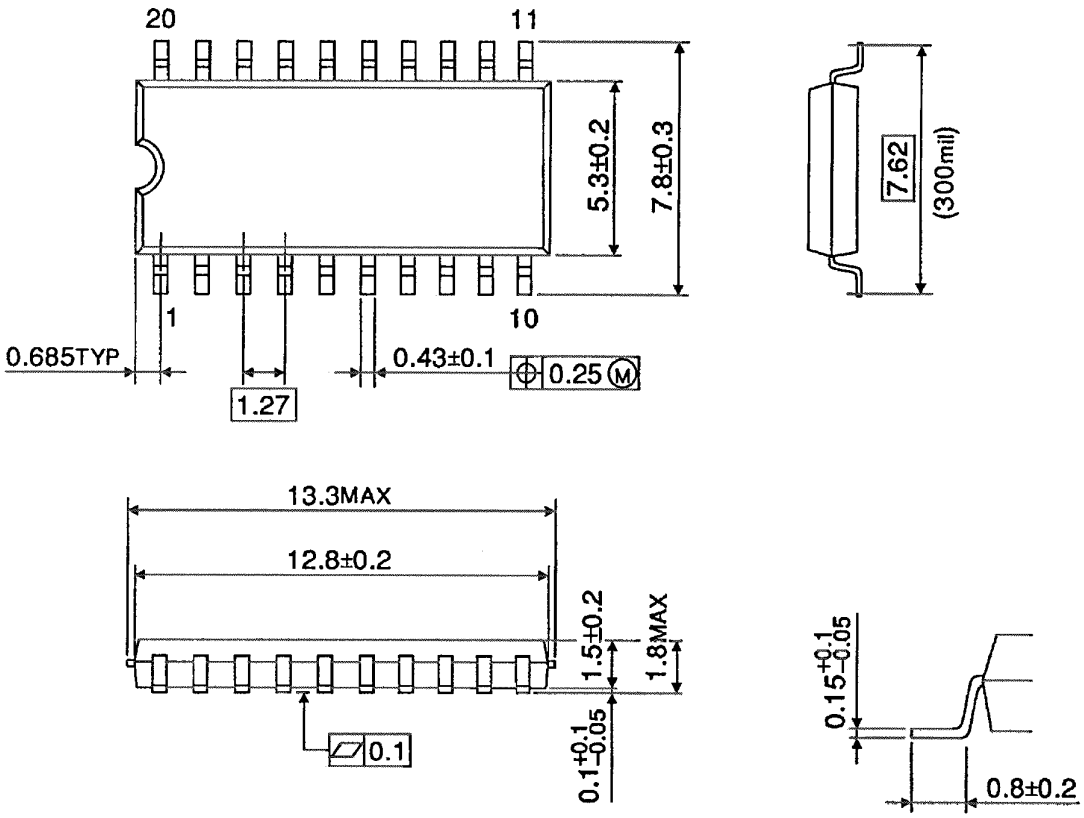
SOP20-P-300-1.27A Unit: mm




Weight: 0.22 g (typ.)

## Package Dimensions

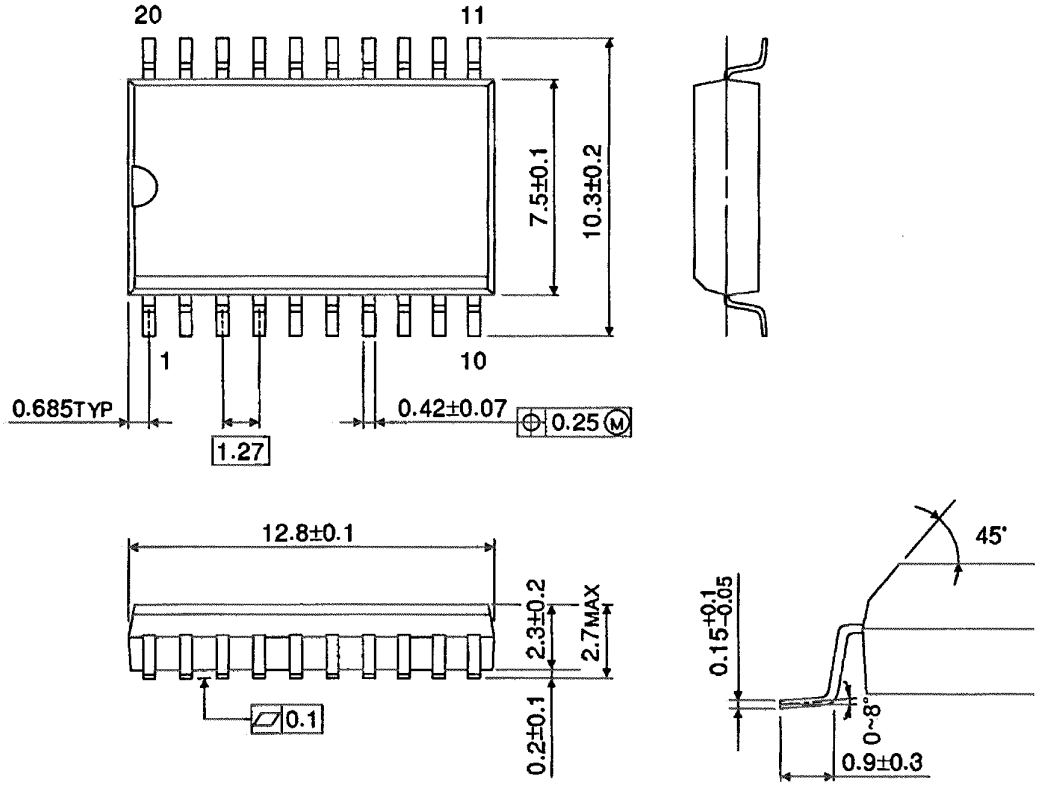
SOP20-P-300-1.27 Unit : mm




Weight: 0.22 g (typ.)

**Package Dimensions (Note)**

SOL20-P-300-1.27 Unit : mm

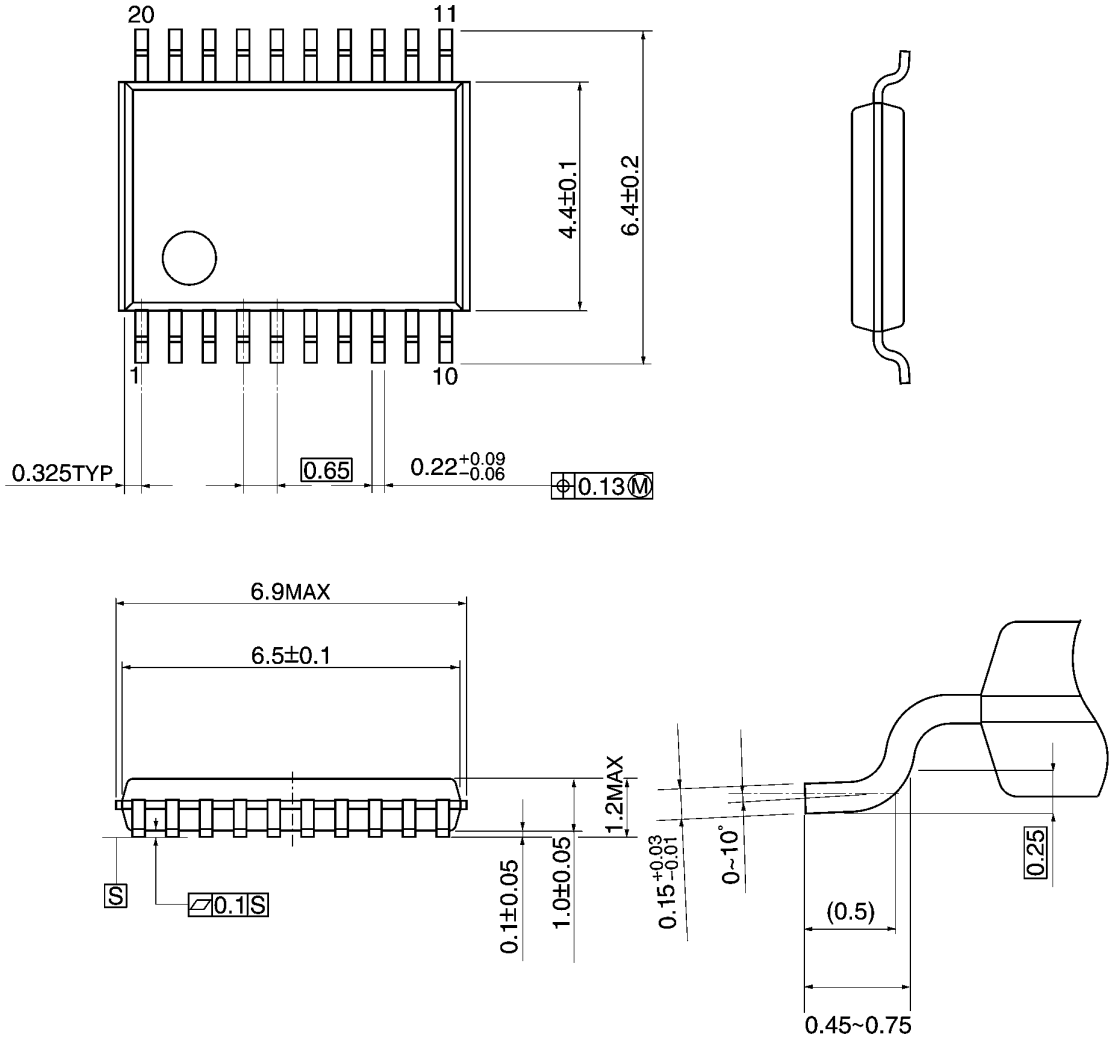



Note: This package is not available in Japan.

Weight: 0.46 g (typ.)

## Package Dimensions

TSSOP20-P-0044-0.65A Unit: mm




Weight: 0.08 g (typ.)

**Note: Lead (Pb)-Free Packages**

**SOP20-P-300-1.27A TSSOP20-P-0044-0.65A**

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