

2M-BIT CMOS STATIC RAM
256K-WORD BY 8-BIT
EXTENDED TEMPERATURE OPERATION**Description**

The μ PD442000L-X is a high speed, low power, 2,097,152 bits (262,144 words by 8 bits) CMOS static RAM.

The μ PD442000L-X has two chip enable pins (/CE1, CE2) to extend the capacity. And battery backup is available.

B, C and D versions are low voltage versions.

- ★ The μ PD442000L-X is packed in 32-pin plastic TSOP (I) (8×13.4 mm) and (8×20 mm).

Features

- 262,144 words by 8 bits organization
- ★ • Fast access time : 70, 85, 100, 120, 150, 180 ns (MAX.)
- Low voltage operation
(B version : $V_{CC} = 2.7$ to 3.6 V, C version : $V_{CC} = 2.2$ to 3.6 V, D version : $V_{CC} = 1.8$ to 3.6 V)
- Low V_{CC} data retention : 1.5 V (MIN.)
- Operating ambient temperature : $T_A = -25$ to $+85$ °C
- Output Enable input for easy application
- Two Chip Enable inputs : /CE1, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby μ A (MAX.)	At data retention μ A (MAX.)
μ PD442000L-BxxX	70 ^{Note} , 85, 100	2.7 to 3.6	-25 to +85	35	2	2
μ PD442000L-CxxX	100, 120, 150	2.2 to 3.6		30		
★ μ PD442000L-DxxX	150, 180	1.8 to 3.6		25		

Note Under development

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

★ Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark	
μ PD442000LGU-B70X-9JH ^{Note}	32-pin Plastic TSOP (I) (8×13.4) (Normal bent)	70	2.7 to 3.6	−25 to +85	B version	
μ PD442000LGU-B85X-9JH		85				
μ PD442000LGU-B10X-9JH		100				
μ PD442000LGU-B70X-9KH ^{Note}	32-pin Plastic TSOP (I) (8×13.4) (Reverse bent)	70				
μ PD442000LGU-B85X-9KH		85				
μ PD442000LGU-B10X-9KH		100				
μ PD442000LGZ-B70X-KJH ^{Note}	32-pin Plastic TSOP (I) (8×20) (Normal bent)	70				
μ PD442000LGZ-B85X-KJH		85				
μ PD442000LGZ-B10X-KJH		100				
μ PD442000LGZ-B70X-KKH ^{Note}	32-pin Plastic TSOP (I) (8×20) (Reverse bent)	70	2.2 to 3.6			C version
μ PD442000LGZ-B85X-KKH		85				
μ PD442000LGZ-B10X-KKH		100				
μ PD442000LGU-C10X-9JH	32-pin Plastic TSOP (I) (8×13.4) (Normal bent)	100				
μ PD442000LGU-C12X-9JH		120				
μ PD442000LGU-C15X-9JH		150				
μ PD442000LGU-C10X-9KH	32-pin Plastic TSOP (I) (8×13.4) (Reverse bent)	100				
μ PD442000LGU-C12X-9KH		120				
μ PD442000LGU-C15X-9KH		150				
μ PD442000LGZ-C10X-KJH	32-pin Plastic TSOP (I) (8×20) (Normal bent)	100				
μ PD442000LGZ-C12X-KJH		120				
μ PD442000LGZ-C15X-KJH		150				
μ PD442000LGZ-C10X-KKH	32-pin Plastic TSOP (I) (8×20) (Reverse bent)	100				
μ PD442000LGZ-C12X-KKH		120				
μ PD442000LGZ-C15X-KKH		150				
μ PD442000LGU-D15X-9JH	32-pin Plastic TSOP (I) (8×13.4) (Normal bent)	150	1.8 to 3.6			D version
μ PD442000LGU-D18X-9JH		180				
μ PD442000LGU-D15X-9KH	32-pin Plastic TSOP (I) (8×13.4) (Reverse bent)	150				
μ PD442000LGU-D18X-9KH		180				
μ PD442000LGZ-D15X-KJH	32-pin Plastic TSOP (I) (8×20) (Normal bent)	150				
μ PD442000LGZ-D18X-KJH		180				
μ PD442000LGZ-D15X-KKH	32-pin Plastic TSOP (I) (8×20) (Reverse bent)	150				
μ PD442000LGZ-D18X-KKH		180				

Note Under development

Pin Configurations (Marking Side)

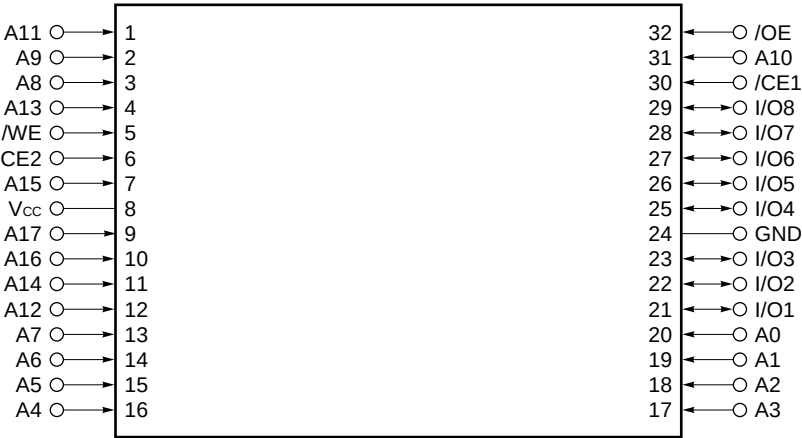
/xxx indicates active low signal.

32-pin Plastic TSOP (I) (8×13.4) (Normal bent)

- [μPD442000LGU-BxxX-9JH]
- [μPD442000LGU-CxxX-9JH]
- [μPD442000LGU-DxxX-9JH]

32-pin Plastic TSOP (I) (8×20) (Normal bent)

- [μPD442000LGZ-BxxX-KJH]
- [μPD442000LGZ-CxxX-KJH]
- [μPD442000LGZ-DxxX-KJH]



- A0 - A17 : Address inputs
- I/O1 - I/O8 : Data inputs / outputs
- /CE1, CE2 : Chip Enable 1, 2
- /WE : Write Enable
- /OE : Output Enable
- Vcc : Power supply
- GND : Ground

Remark Refer to **Package Drawings** for the 1-pin index mark.

32-pin Plastic TSOP (I) (8x13.4) (Reverse bent)

[μPD442000LGU-BxxX-9KH]

[μPD442000LGU-CxxX-9KH]

[μPD442000LGU-DxxX-9KH]

32-pin Plastic TSOP (I) (8x20) (Reverse bent)

[μPD442000LGZ-BxxX-KKH]

[μPD442000LGZ-CxxX-KKH]

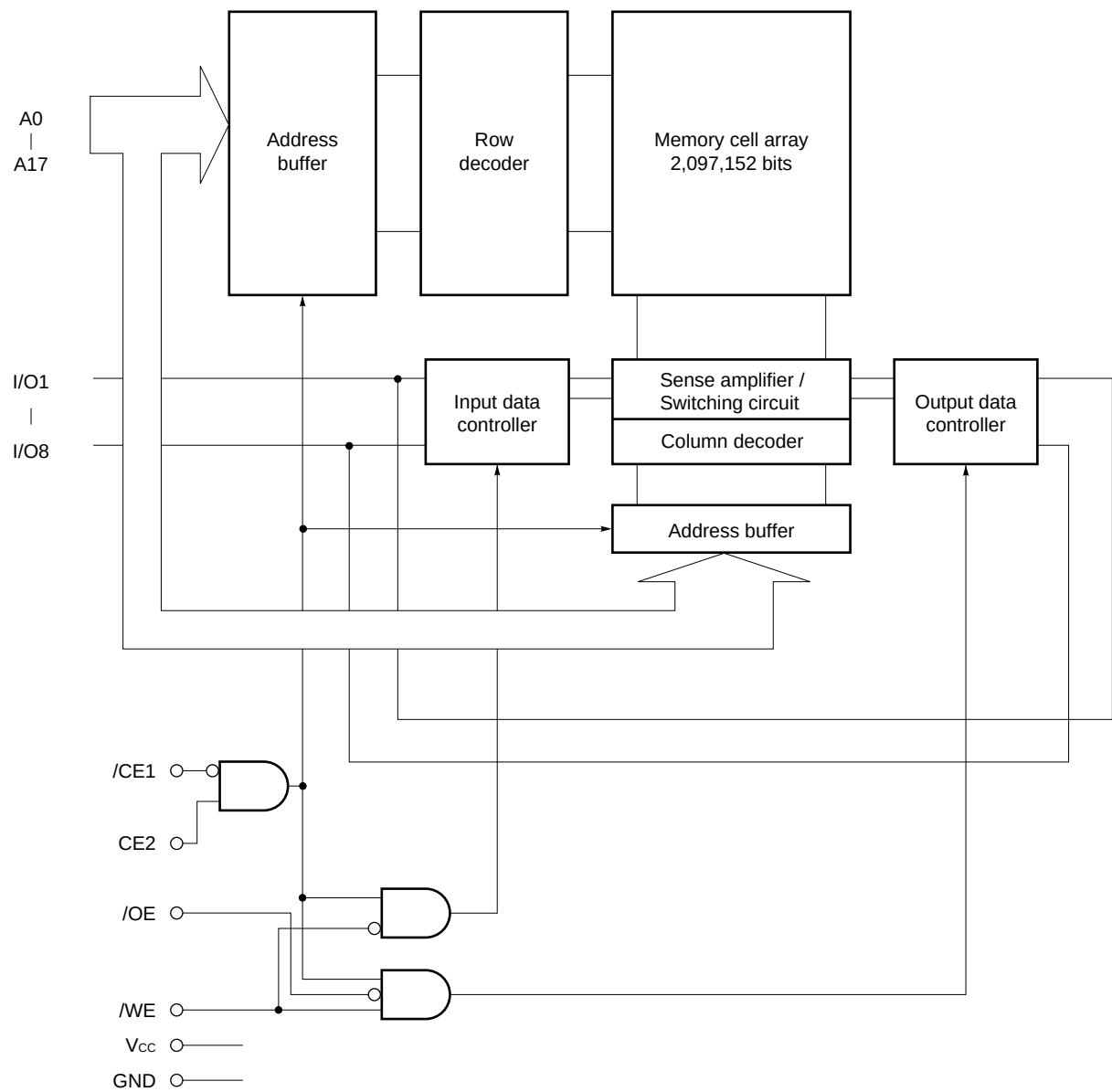
[μPD442000LGZ-DxxX-KKH]



- A0 - A17 : Address inputs
- I/O1 - I/O8 : Data inputs / outputs
- /CE1, CE2 : Chip Enable 1, 2
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Remark Refer to **Package Drawings** for the 1-pin index mark.

Block Diagram



Truth Table

/CE1	CE2	/OE	/WE	Mode	I/O	Supply current
H	x	x	x	Not selected	High impedance	I _{SB}
x	L	x	x	Not selected	High impedance	
L	H	H	H	Output disable	High impedance	I _{CCA}
L	H	L	H	Read	D _{OUT}	
L	H	x	L	Write	D _{IN}	

Remark x : V_{IH} or V_{IL}

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		-0.5 ^{Note} to +4.6	V
Input / Output voltage	V_T		-0.5 ^{Note} to $V_{CC}+0.5$	V
Operating ambient temperature	T_A		-25 to +85	°C
Storage temperature	T_{stg}		-55 to +125	°C

Note -3.0 V (MIN.) (Pulse width : 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD442000L-BxxX		μPD442000L-CxxX		μPD442000L-DxxX		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		2.7	3.6	2.2	3.6	1.8	3.6	V
High level input voltage	V_{IH}	$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	2.4	$V_{CC}+0.5$	2.4	$V_{CC}+0.5$	2.4	$V_{CC}+0.5$	V
		$2.2\text{ V} \leq V_{CC} < 2.7\text{ V}$	—	—	2.0	$V_{CC}+0.5$	2.0	$V_{CC}+0.5$	
		$1.8\text{ V} \leq V_{CC} < 2.2\text{ V}$	—	—	—	—	1.6	$V_{CC}+0.5$	
Low level input voltage	V_{IL}		-0.3 ^{Note}	+0.5	-0.3 ^{Note}	+0.3	-0.3 ^{Note}	+0.2	V
Operating ambient temperature	T_A		-25	+85	-25	+85	-25	+85	°C

Note -1.5 V (MIN.) (Pulse width : 30 ns)

Capacitance ($T_A = 25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0\text{ V}$			8	pF
Input / Output capacitance	C_{IO}	$V_{IO} = 0\text{ V}$			10	pF

Remarks 1. V_{IN} : Input voltage

V_{IO} : Input / Output voltage

2. These parameters are periodically sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition	μPD442000L-BxxX			μPD442000L-CxxX			μPD442000L-DxxX			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}	-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	μA
I/O leakage current	I _{LO}	V _{I/O} = 0 V to V _{CC} , /CE1 = V _{IH} or CE2 = V _{IL} or /WE = V _{IL} or /OE = V _{IH}	-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	μA
Operating supply current	I _{CCA1}	/CE1 = V _{IL} , CE2 = V _{IH} ,		30	35		25	30		20	25	mA
		Minimum cycle time, V _{CC} ≤ 2.7 V		—	—		20	25		15	20	
		I _{I/O} = 0 mA, V _{CC} ≤ 2.2 V		—	—		—	—		10	15	
	I _{CCA2}	/CE1 = V _{IL} , CE2 = V _{IH} ,			10			10			10	
		I _{I/O} = 0 mA, V _{CC} ≤ 2.7 V			—			8			8	
		V _{CC} ≤ 2.2 V			—			—			5	
	I _{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V _{CC} - 0.2 V,			8			8			8	
		Cycle = 1 MHz, I _{I/O} = 0 mA,										
		V _{IL} ≤ 0.2 V, V _{CC} ≤ 2.7 V			—			6			6	
		V _{IH} ≥ V _{CC} - 0.2 V, V _{CC} ≤ 2.2 V			—			—			5	
Standby supply current	I _{SB}	/CE1 = V _{IH} or CE2 = V _{IL}			0.3			0.3			0.3	mA
	I _{SB1}	/CE1 ≥ V _{CC} - 0.2 V,		0.1	2		0.1	2		0.1	2	
		CE2 ≥ V _{CC} - 0.2 V, V _{CC} ≤ 2.7 V		—	—		0.08	2		0.08	2	
		V _{CC} ≤ 2.2 V		—	—		—	—		0.05	1.5	
	I _{SB2}	CE2 ≤ 0.2 V		0.1	2		0.1	2		0.1	2	
		V _{CC} ≤ 2.7 V		—	—		0.08	2		0.08	2	
		V _{CC} ≤ 2.2 V		—	—		—	—		0.05	1.5	
High level output voltage	V _{OH}	I _{OH} = -0.5 mA	2.4			2.4			2.4			V
		V _{CC} ≤ 2.7 V	—			1.8			1.8			
		V _{CC} ≤ 2.2 V	—			—			1.5			
Low level output voltage	V _{OL}	I _{OL} = 1.0 mA			0.4			0.4			0.4	V

Remarks 1. V_{IN} : Input voltage

V_{I/O} : Input / Output voltage

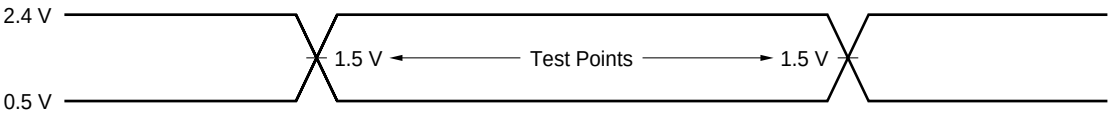
2. These DC characteristics are in common regardless of package types and access time.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

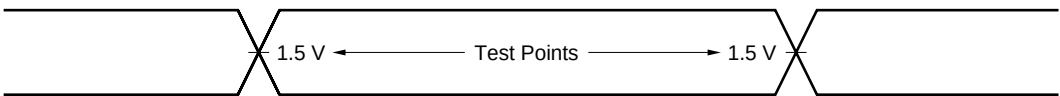
AC Test Conditions

[μPD442000L-B70X, μPD442000L-B85X, μPD442000L-B10X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

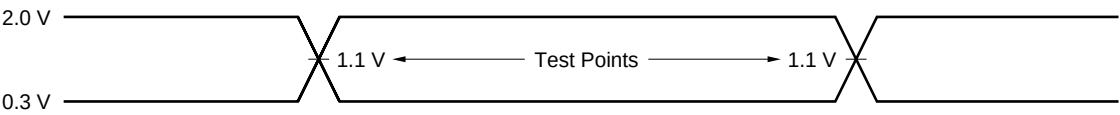


Output Load

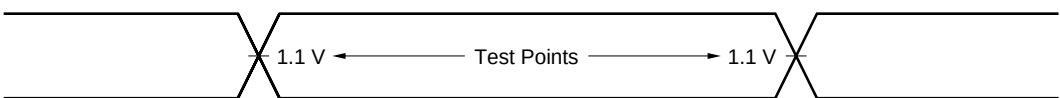
1TTL + 50 pF

[μPD442000L-C10X, μPD442000L-C12X, μPD442000L-C15X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

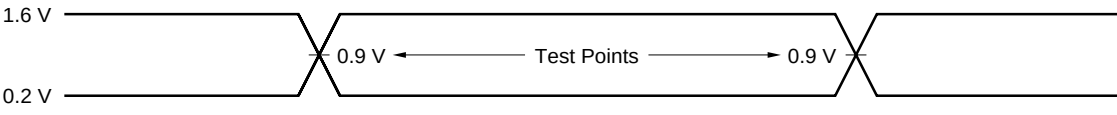


Output Load

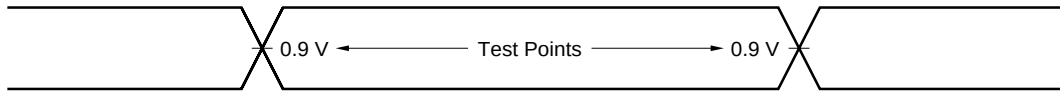
1TTL + 50 pF

★ [μPD442000L-D15X, μPD442000L-D18X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1TTL + 50 pF

Read Cycle (1/3) (B version)

Parameter	Symbol	μPD442000L-B70X		μPD442000L-B85X		μPD442000L-B10X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t _{RC}	70		85		100		ns	
Address access time	t _{AA}		70		85		100	ns	Note 1
/CE1 access time	t _{CO1}		70		85		100	ns	
CE2 access time	t _{CO2}		70		85		100	ns	
/OE to output valid	t _{OE}		35		40		50	ns	
Output hold from address change	t _{OH}	10		10		10		ns	
/CE1 to output in low impedance	t _{LZ1}	10		10		10		ns	Note 2
CE2 to output in low impedance	t _{LZ2}	10		10		10		ns	
/OE to output in low impedance	t _{OLZ}	5		5		5		ns	
/CE1 to output in high impedance	t _{HZ1}		25		30		35	ns	
CE2 to output in high impedance	t _{HZ2}		25		30		35	ns	
/OE to output in high impedance	t _{OHZ}		25		30		35	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle (2/3) (C version)

Parameter	Symbol	μPD442000L-C10X		μPD442000L-C12X		μPD442000L-C15X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t _{RC}	100		120		150		ns	
Address access time	t _{AA}		100		120		150	ns	Note 1
/CE1 access time	t _{CO1}		100		120		150	ns	
CE2 access time	t _{CO2}		100		120		150	ns	
/OE to output valid	t _{OE}		50		60		70	ns	
Output hold from address change	t _{OH}	10		10		10		ns	
/CE1 to output in low impedance	t _{LZ1}	10		10		10		ns	Note 2
CE2 to output in low impedance	t _{LZ2}	10		10		10		ns	
/OE to output in low impedance	t _{OLZ}	5		5		5		ns	
/CE1 to output in high impedance	t _{HZ1}		35		40		45	ns	
CE2 to output in high impedance	t _{HZ2}		35		40		45	ns	
/OE to output in high impedance	t _{OHZ}		35		40		45	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

★ Read Cycle (3/3) (D version)

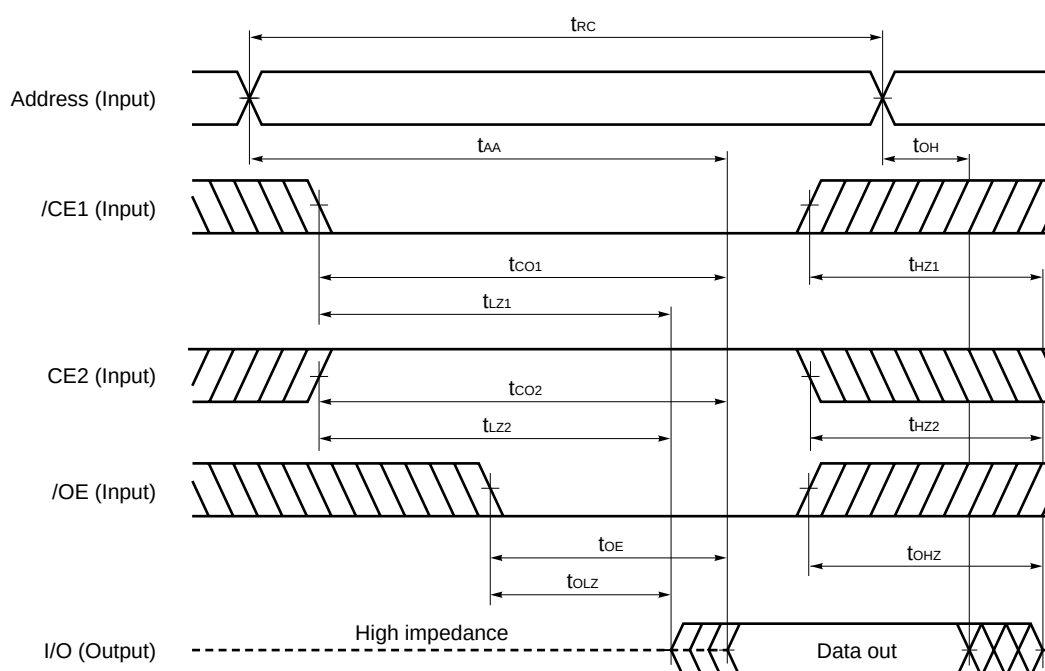
Parameter	Symbol	μPD442000L-D15X		μPD442000L-D18X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	150		180		ns	
Address access time	t_{AA}		150		180	ns	Note 1
/CE1 access time	t_{CO1}		150		180	ns	
CE2 access time	t_{CO2}		150		180	ns	
/OE to output valid	t_{OE}		70		80	ns	
Output hold from address change	t_{OH}	10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		ns	Note 2
CE2 to output in low impedance	t_{LZ2}	10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		ns	
/CE1 to output in high impedance	t_{HZ1}		45		50	ns	
CE2 to output in high impedance	t_{HZ2}		45		50	ns	
/OE to output in high impedance	t_{OHZ}		45		50	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

Write Cycle (1/3) (B version)

Parameter	Symbol	μPD442000L-B70X		μPD442000L-B85X		μPD442000L-B10X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{WC}	70		85		100		ns	
/CE1 to end of write	t _{CW1}	55		70		80		ns	
CE2 to end of write	t _{CW2}	55		70		80		ns	
Address valid to end of write	t _{AW}	55		70		80		ns	
Address setup time	t _{AS}	0		0		0		ns	
Write pulse width	t _{WP}	50		60		60		ns	
Write recovery time	t _{WR}	0		0		0		ns	
Data valid to end of write	t _{DW}	30		35		40		ns	
Data hold time	t _{DH}	0		0		0		ns	
/WE to output in high impedance	t _{WHZ}		25		30		35	ns	Note
Output active from end of write	t _{OW}	5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Write Cycle (2/3) (C version)

Parameter	Symbol	μPD442000L-C10X		μPD442000L-C12X		μPD442000L-C15X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{WC}	100		120		150		ns	
/CE1 to end of write	t _{CW1}	80		100		120		ns	
CE2 to end of write	t _{CW2}	80		100		120		ns	
Address valid to end of write	t _{AW}	80		100		120		ns	
Address setup time	t _{AS}	0		0		0		ns	
Write pulse width	t _{WP}	60		80		100		ns	
Write recovery time	t _{WR}	0		0		0		ns	
Data valid to end of write	t _{DW}	40		50		60		ns	
Data hold time	t _{DH}	0		0		0		ns	
/WE to output in high impedance	t _{WHZ}		35		40		50	ns	Note
Output active from end of write	t _{OW}	5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

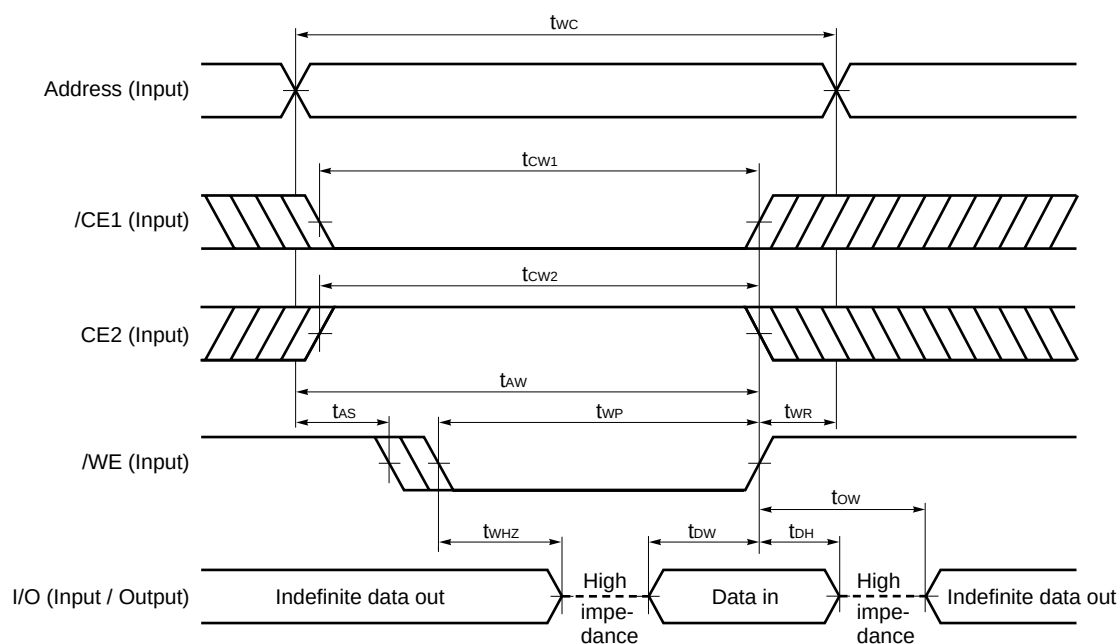
★ Write Cycle (3/3) (D version)

Parameter	Symbol	μPD442000L-D15X		μPD442000L-D18X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{WC}	150		180		ns	
/CE1 to end of write	t _{CW1}	120		150		ns	
CE2 to end of write	t _{CW2}	120		150		ns	
Address valid to end of write	t _{AW}	120		150		ns	
Address setup time	t _{AS}	0		0		ns	
Write pulse width	t _{WP}	100		120		ns	
Write recovery time	t _{WR}	0		0		ns	
Data valid to end of write	t _{DW}	60		75		ns	
Data hold time	t _{DH}	0		0		ns	
/WE to output in high impedance	t _{WHZ}		50		60	ns	Note
Output active from end of write	t _{OW}	5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

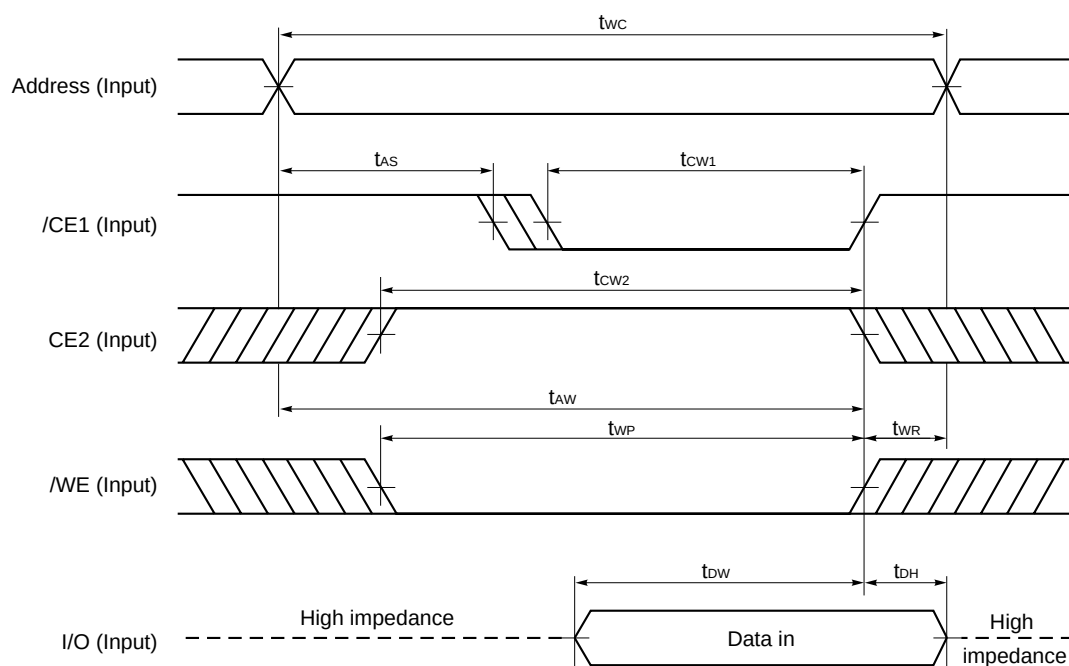
Write Cycle Timing Chart 1 (/WE Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

- Remarks**
1. Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.
 2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.
 3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

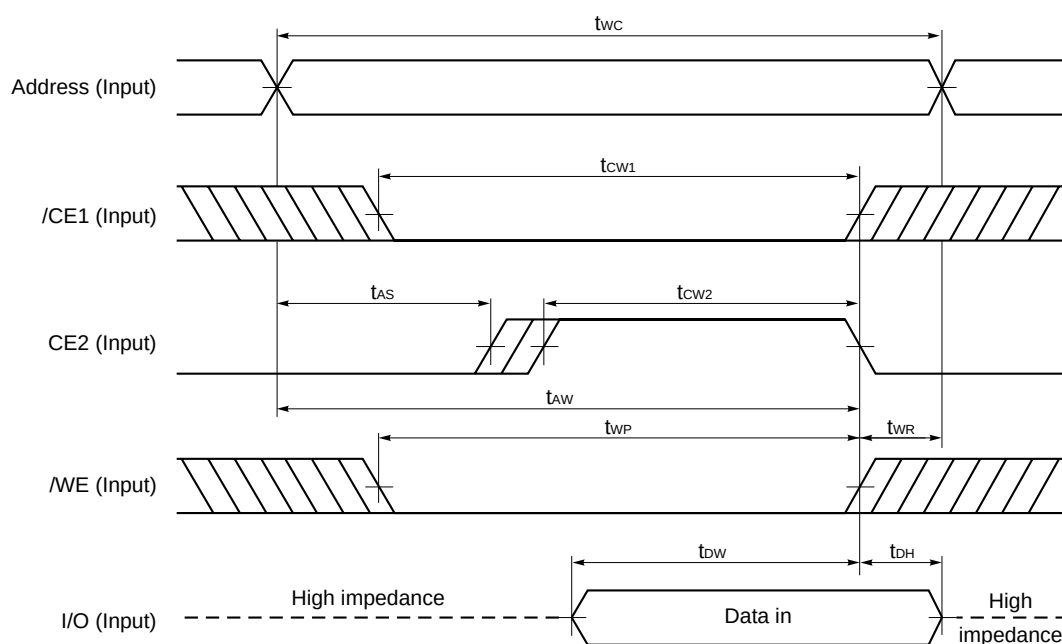
Write Cycle Timing Chart 2 (/CE1 Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, and a high level CE2.

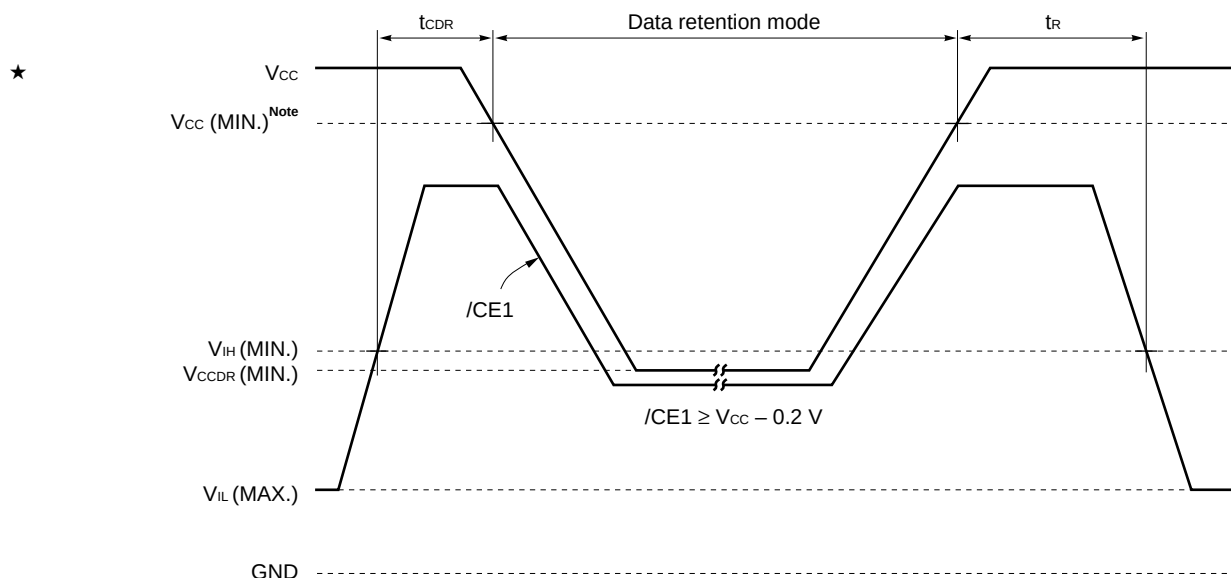
Low V_{CC} Data Retention Characteristics (T_A = -25 to +85 °C)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{CCDR1}	/CE1 ≥ V _{CC} - 0.2 V, CE2 ≥ V _{CC} - 0.2 V	1.5		3.6	V
	V _{CCDR2}	CE2 ≤ 0.2 V	1.5		3.6	
Data retention supply current	I _{CCDR1}	V _{CC} = 3.0 V, /CE1 ≥ V _{CC} - 0.2 V, CE2 ≥ V _{CC} - 0.2 V or CE2 ≤ 0.2 V		0.1	2	μA
	I _{CCDR2}	V _{CC} = 3.0 V, CE2 ≤ 0.2 V		0.1	2	
Chip deselection to data retention mode	t _{CDR}		0			ns
Operation recovery time	t _R		t _{RC} ^{Note}			ns

Note t_{RC} : Read cycle time.

Data Retention Timing Chart

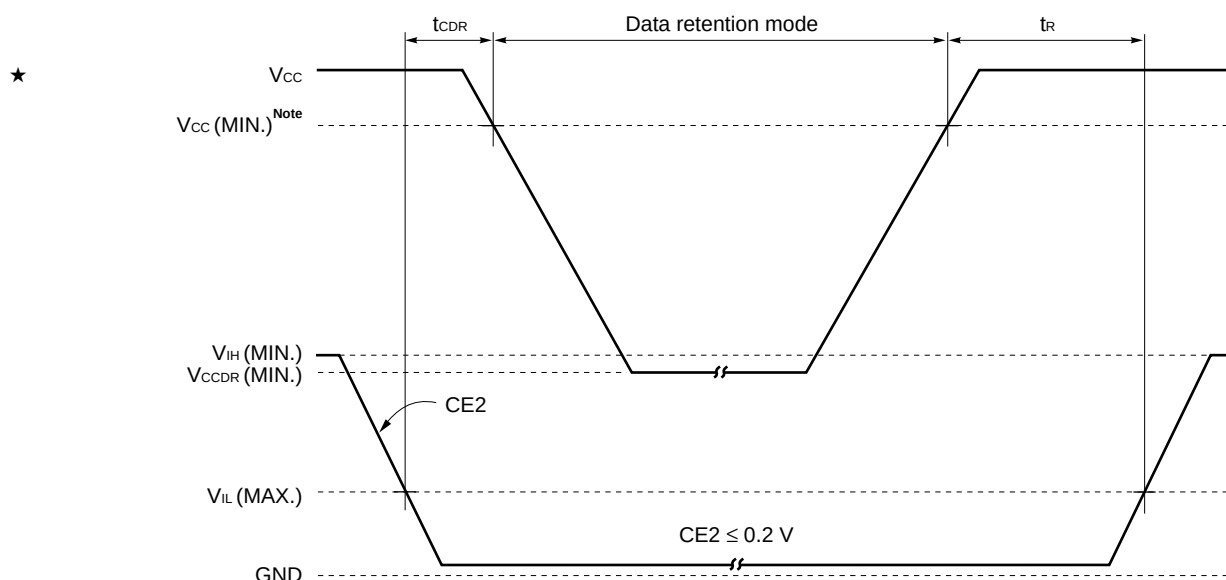
(1) /CE1 Controlled



Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling $\overline{\text{CE1}}$, the input level of CE2 must be $\geq V_{\text{CC}} - 0.2 \text{ V}$ or $\leq 0.2 \text{ V}$.
The other pins (Address, I/O, $\overline{\text{WE}}$, $\overline{\text{OE}}$) can be in high impedance state.

(2) CE2 Controlled

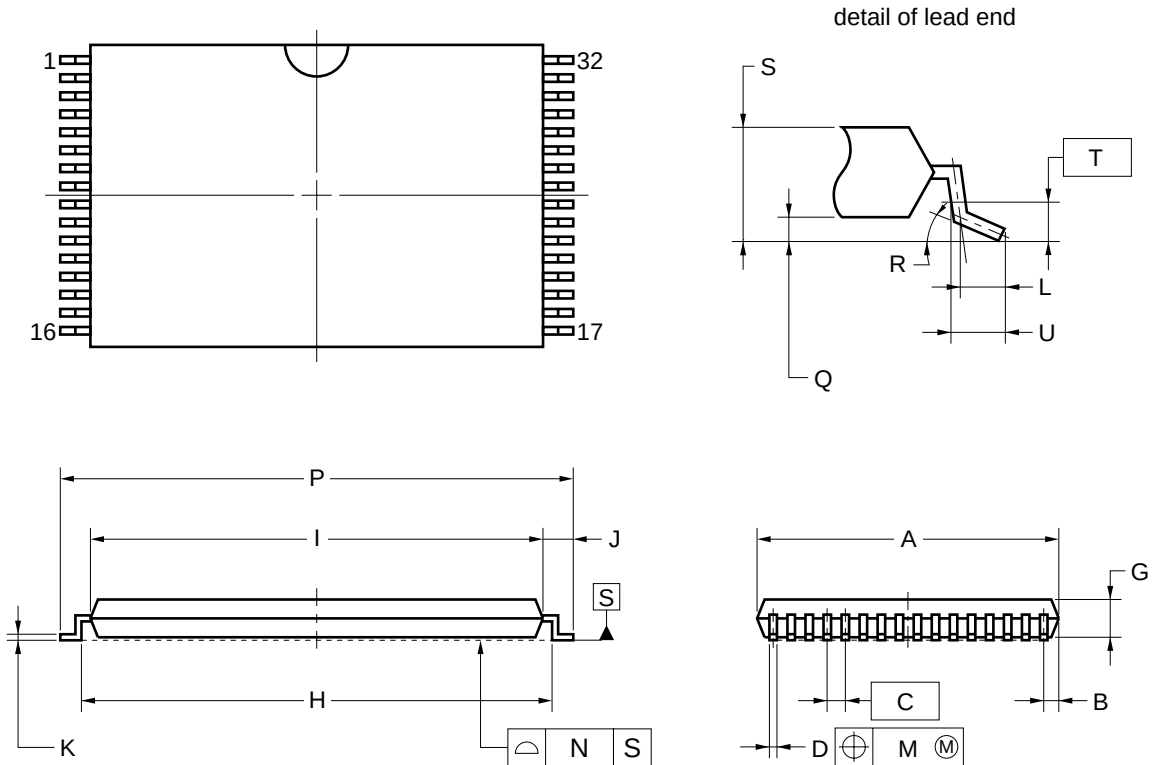


Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling CE2, the other pins ($\overline{\text{CE1}}$, Address, I/O, $\overline{\text{WE}}$, $\overline{\text{OE}}$) can be in high impedance state.

Package Drawings

★ 32-PIN PLASTIC TSOP(I) (8x13.4)



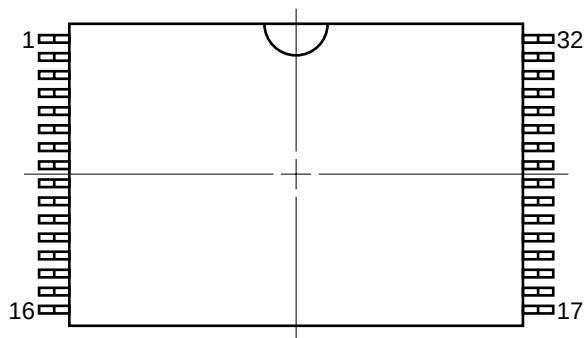
NOTES

1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

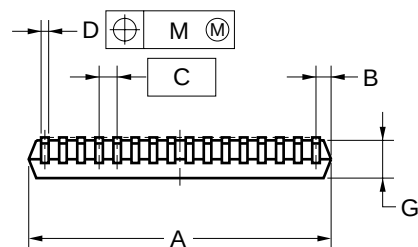
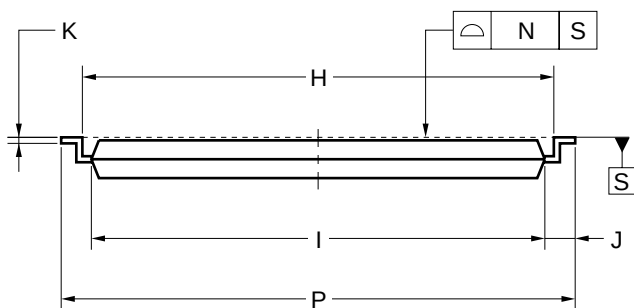
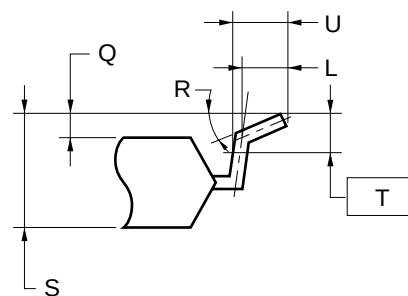
ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
G	1.0±0.05
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	0.145 ^{+0.025} _{-0.015}
L	0.5
M	0.08
N	0.08
P	13.4±0.2
Q	0.1±0.05
R	3° ^{+5°} _{-3°}
S	1.2 MAX.
T	0.25
U	0.6±0.15

P32GU-50-9JH-2

★ 32-PIN PLASTIC TSOP(I) (8x13.4)



detail of lead end



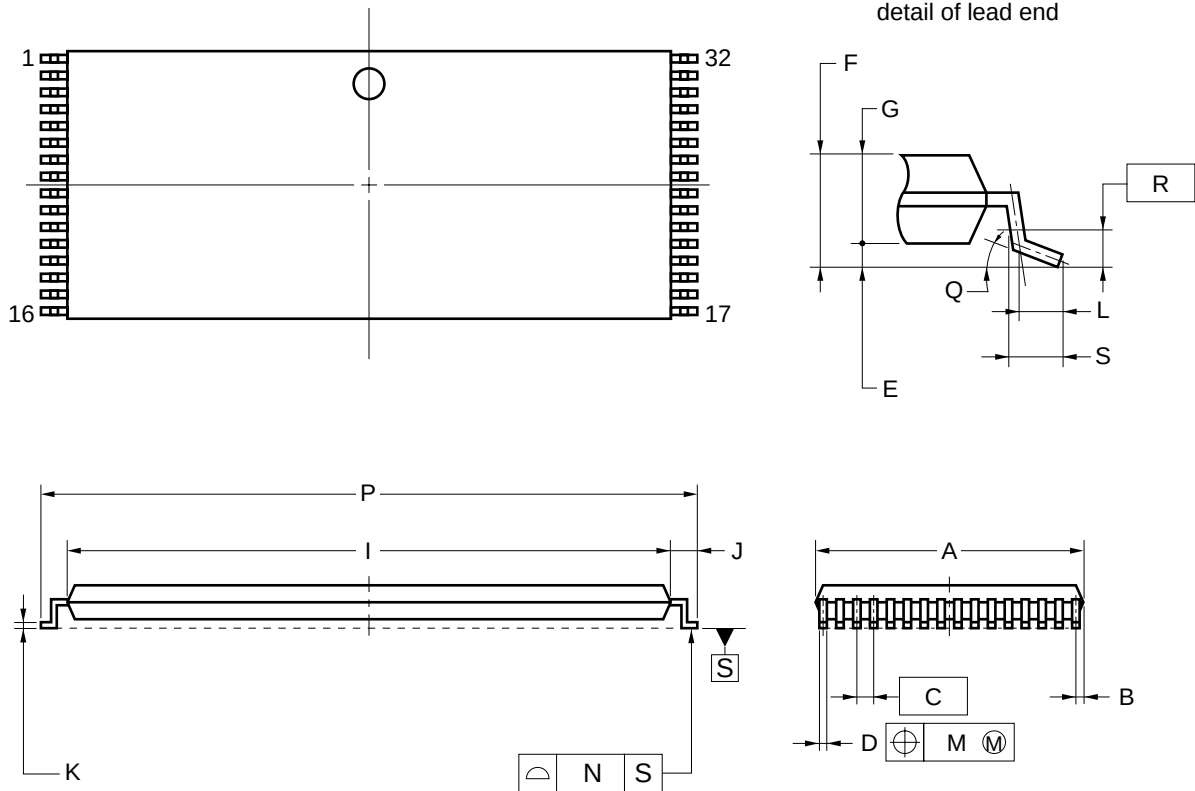
NOTES

1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
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G	1.0±0.05
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	0.145 ^{+0.025} _{-0.015}
L	0.5
M	0.08
N	0.08
P	13.4±0.2
Q	0.1±0.05
R	3° ^{+5°} _{-3°}
S	1.2 MAX.
T	0.25
U	0.6±0.15

P32GU-50-9KH-2

★ 32-PIN PLASTIC TSOP(I) (8x20)



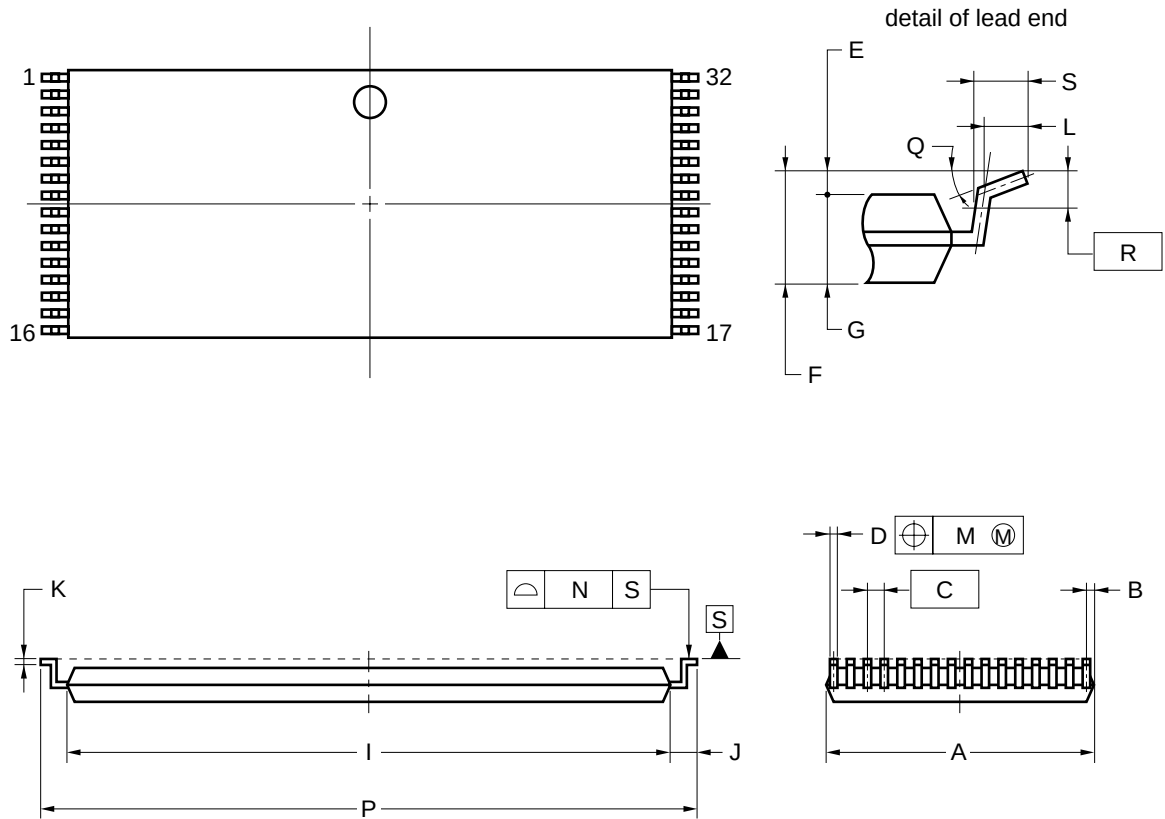
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	0.97±0.08
I	18.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	3° ^{+5°} _{-3°}
R	0.25
S	0.60±0.15

S32GZ-50-KJH1-2

★ 32-PIN PLASTIC TSOP(I) (8x20)



NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	0.97±0.08
I	18.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	3° ^{+5°} _{-3°}
R	0.25
S	0.60±0.15

S32GZ-50-KKH1-2

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD442000L-X.

★ Types of Surface Mount Device

μPD442000LGU-BxxX-9JH	: 32-pin Plastic TSOP (I) (8×13.4) (Normal bent)
μPD442000LGU-CxxX-9JH	: 32-pin Plastic TSOP (I) (8×13.4) (Normal bent)
μPD442000LGU-DxxX-9JH	: 32-pin Plastic TSOP (I) (8×13.4) (Normal bent)
μPD442000LGU-BxxX-9KH	: 32-pin Plastic TSOP (I) (8×13.4) (Reverse bent)
μPD442000LGU-CxxX-9KH	: 32-pin Plastic TSOP (I) (8×13.4) (Reverse bent)
μPD442000LGU-DxxX-9KH	: 32-pin Plastic TSOP (I) (8×13.4) (Reverse bent)
μPD442000LGZ-BxxX-KJH	: 32-pin Plastic TSOP (I) (8×20) (Normal bent)
μPD442000LGZ-CxxX-KJH	: 32-pin Plastic TSOP (I) (8×20) (Normal bent)
μPD442000LGZ-DxxX-KJH	: 32-pin Plastic TSOP (I) (8×20) (Normal bent)
μPD442000LGZ-BxxX-KKH	: 32-pin Plastic TSOP (I) (8×20) (Reverse bent)
μPD442000LGZ-CxxX-KKH	: 32-pin Plastic TSOP (I) (8×20) (Reverse bent)
μPD442000LGZ-DxxX-KKH	: 32-pin Plastic TSOP (I) (8×20) (Reverse bent)

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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