



40V 175°C N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _C = +25°C (Note 9)
40V	$3m\Omega$ @ $V_{GS} = 10V$	100A
	$5m\Omega @ V_{GS} = 4.5V$	100A

Description

This MOSFET is designed to minimize the on-state resistance (RDS(ON)) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Engine Management Systems
- Body Control Electronics
- DC-DC Converters

Features

- Rated to 175° C Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching Ensures More Reliable and Robust End Application
- Low Rdson Minimizes Power Losses
- Low Qg Minimizes Switching Losses
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability
- An Automotive-Compliant Part is Available Under Separate Datasheet (<u>DMTH4004LK3Q</u>)

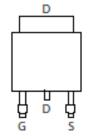
Mechanical Data

- Case: TO252
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Matte Tin annealed over Copper leadframe.
 Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.33 grams (Approximate)

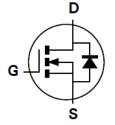


TO252 (DPAK)





Pin Out Top View



Equivalent Circuit

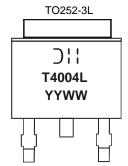
Ordering Information (Notes 4)

Part Number	Case	Packaging
DMTH4004LK3-13	TO252	2,500/Tape & Reel

Notes:

- 1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



Dil =Manufacturer's Marking
T4004L = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year
(ex: 15 = 2015)
WW = Week Code (01 to 53)



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage		V_{DSS}	40	V	
Gate-Source Voltage	V_{GSS}	±20	V		
Continuous Drain Current (Note 6), V _{GS} = 10V	T _C = +25°C (Note 9)	I _D	100	А	
, , , , , ,	$T_{C} = +100^{\circ}C$		100		
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I _{DM}	200	Α		
Maximum Continuous Body Diode Forward Current (Note 6)	I _S	100	Α		
Avalanche Current, L = 0.2mH	I _{AS}	30	A		
Avalanche Energy, L = 0.2mH	E _{AS}	90	mJ		

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)	P_{D}	3.9	W	
Thermal Resistance, Junction to Ambient (Note 5)	$R_{ heta JA}$	38	°C/W	
Total Power Dissipation (Note 6)	P _D	180	W	
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	0.8	°C/W	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +175	°C

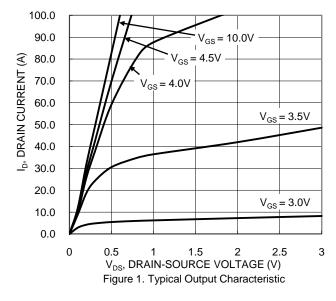
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

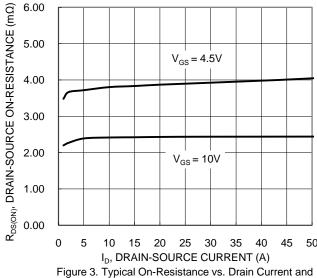
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	40	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current, T _J = +25°C	I _{DSS}	_	_	1	μA	$V_{DS} = 32V, V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V _{GS(TH)}	1	_	3	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	
Static Drain-Source On-Resistance	Proven	_	2.4	3	mΩ	$V_{GS} = 10V, I_D = 50A$	
Static Drain-Source On-Nesistance	R _{DS(ON)}	_	4	5	mΩ	$V_{GS} = 4.5V, I_D = 50A$	
Diode Forward Voltage	V_{SD}	_	0.7	1.2	V	$V_{GS} = 0V, I_{S} = 50A$	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C _{iss}	-	4,450	_	pF	V 05V V 0V	
Output Capacitance	Coss	_	1,407	_	pF	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1MHz	
Reverse Transfer Capacitance	C _{rss}	_	74	_	pF		
Gate Resistance	R_{g}	-	0.7	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	35	_	nC		
Total Gate Charge (V _{GS} = 10V)	Qg	-	83	_	nC	7, , , , , , , , , , , , , , , , , , ,	
Gate-Source Charge	Q_{gs}	1	10	_	nC	$V_{DS} = 20V, I_{D} = 30A$	
Gate-Drain Charge	Q_{gd}	_	11.2	_	nC	7	
Turn-On Delay Time	t _{D(ON)}	_	5.9	_	ns		
Turn-On Rise Time	tr	_	13.2	_	ns	$V_{GS} = 10V, V_{DS} = 20V,$ $R_g = 1.6\Omega, I_D = 30A$	
Turn-Off Delay Time	t _{D(OFF)}	_	25.8	_	ns		
Turn-Off Fall Time	t _F	_	7.9	_	ns		
Body Diode Reverse Recovery Time	t _{RR}	_	48	_	ns	I _F = 50A, di/dt = 100A/μs	
Body Diode Reverse Recovery Charge	Q_{RR}	_	72	_	nC	I _F = 50A, di/dt = 100A/μs	

lotes: 5. Device mounted with exposed drain pad on 25mm by 25mm 2oz copper on a single- sided 1.6mm FR-4 PCB; device is measured under still air conditions whilst operating in a steady state.

- 6. Thermal resistance from junction to solder point (on the exposed drain pin).
- 7. Short duration pulse test used to minimize self-heating effect.
- 8. Guaranteed by design. Not subject to product testing.
- 9. Package Limited.







Gate Voltage

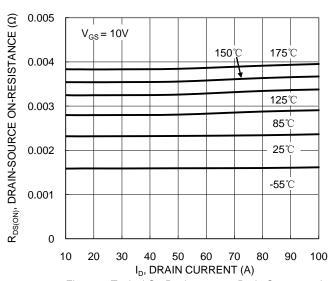
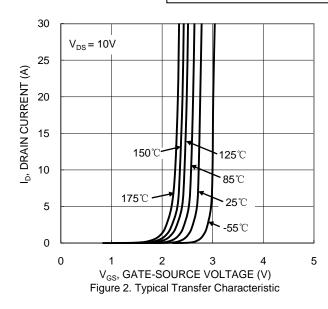
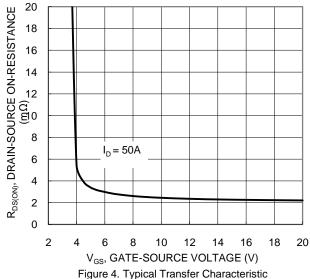


Figure 5. Typical On-Resistance vs. Drain Current and Temperature





2.2 R_{DS(ON)}, DRAIN-SOURCE ON-RESISTANCE 2 1.8 1.6 $V_{GS} = 10V, I_D = 50A$ (NORMALIZED) 1.4 1.2 1 $V_{GS} = 4.5V, I_{D} = 50A$ 8.0 0.6 0.4 25 50 75 100 125 150 175 -50 T_., JUNCTION TEMPERATURE (°C)

Figure 6. On-Resistance Variation with Temperature



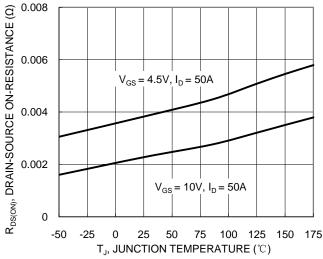


Figure 7. On-Resistance Variation with Temperature

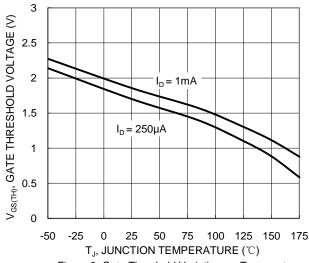
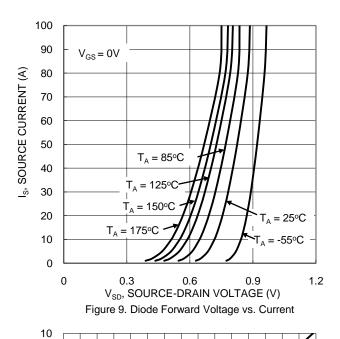


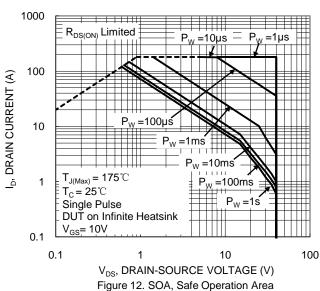
Figure 8. Gate Threshold Variation vs. Temperature



8 V_{DS} = 20V, I_D = 30A V_{DS} = 20V, I_D = 20V, I_D

Figure 11. Gate Charge

10000 f=1MHz C_T, JUNCTION CAPACITANCE (pF) Ciss Cos 1000 Crss 100 10 15 0 10 20 25 30 35 40 V_{DS}, DRAIN-SOURCE VOLTAGE (V) Figure 10. Typical Junction Capacitance





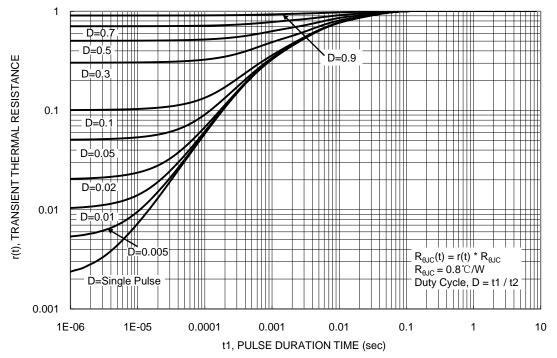


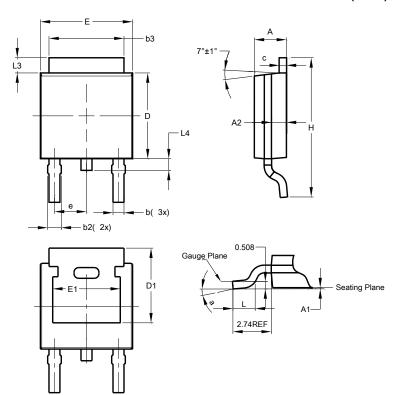
Figure 13. Transient Thermal Resistance



Package Outline

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

TO252 (DPAK)

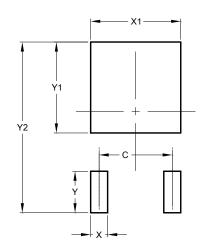


TO252 (DPAK)					
Dim	Min	Max Ty			
Α	2.19	2.39	2.29		
A 1	0.00	0.13	0.08		
A2	0.97	1.17	1.07		
b	0.64	0.88	0.783		
b2	0.76	1.14	0.95		
b3	5.21	5.46	5.33		
С	0.45	0.58	0.531		
D	6.00	6.20	6.10		
D1	5.21	-	-		
е	-	-	2.286		
Е	6.45	6.70	6.58		
E1	4.32	-	-		
Н	9.40	10.41	9.91		
L	1.40	1.78	1.59		
L3	0.88	1.27	1.08		
L4	0.64	1.02	0.83		
а	0°	10°	-		
All Dimensions in mm					

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

TO252 (DPAK)



Dimensions	Value (in mm)			
С	4.572			
Х	1.060			
X1	5.632			
Υ	2.600			
Y1	5.700			
Y2	10 700			



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