

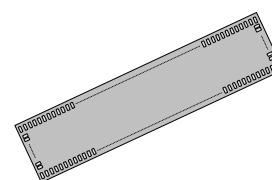
162COMMON x 128RGB LCD DRIVER FOR 4,096-COLOR STN DISPLAY

■ GENERAL DESCRIPTION

The NJU6825 is a 162COMMON x 128RGB LCD driver for 4,096-color STN display. It contains common drivers, RGB drivers, a serial and a parallel MPU interface circuit, an internal LCD power supply, grayscale palettes and 248,832-bit display data RAM. The segment drivers for RGB (Red, Green, Blue) independently produce optimum 16 grayscales from a built-in 32-grayscale palette, and the LSI achieves 4,096 colors (16x16x16).

In addition, the NJU6825 operates with a low voltage of 1.7V and a low operating current, therefore it is ideally suited for battery-powered handheld applications.

■ PACKAGE



BUMP CHIP

■ FEATURES

- 4,096-color STN LCD driver
- Built-in LCD Drivers : 162-common Drivers x 128RGB Drivers (384-segment Drivers in B&W)
- Built-in Display Data RAM (DDRAM) : 248,832 bits for Graphic Display
- Programmable Display Mode
 - Variable 16-grayscale Mode : 4,096 Colors
 - Variable 8-grayscale Mode : 256 Colors
 - Fixed 8-grayscale Mode : 256 Colors
 - B&W Mode : Black & White
- 8-/16-bit Parallel Interface Selectable
- 8-/16-bit Bus Length for Display Data Selectable
- 3-/4-line Serial Interface Selectable
- Programmable Duty Ratio and Bias Ratio
- Programmable Internal Voltage Booster : Maximum 7 times
- Programmable Contrast Control : 128-step Electrical Variable Resistor (EVR)
- Various Useful Instructions
- Low Operating Current : 450uA Typical at $V_{DD}=3V$, 4-time Boost, Checker Flag Display
- Low Logic Voltage : 1.7V to 3.3V
- Wide LCD Voltage Range : 5.0V to 18.0V
- C-MOS Technology
- Slim Chip for COG
- Package : Bump Chip / TCP

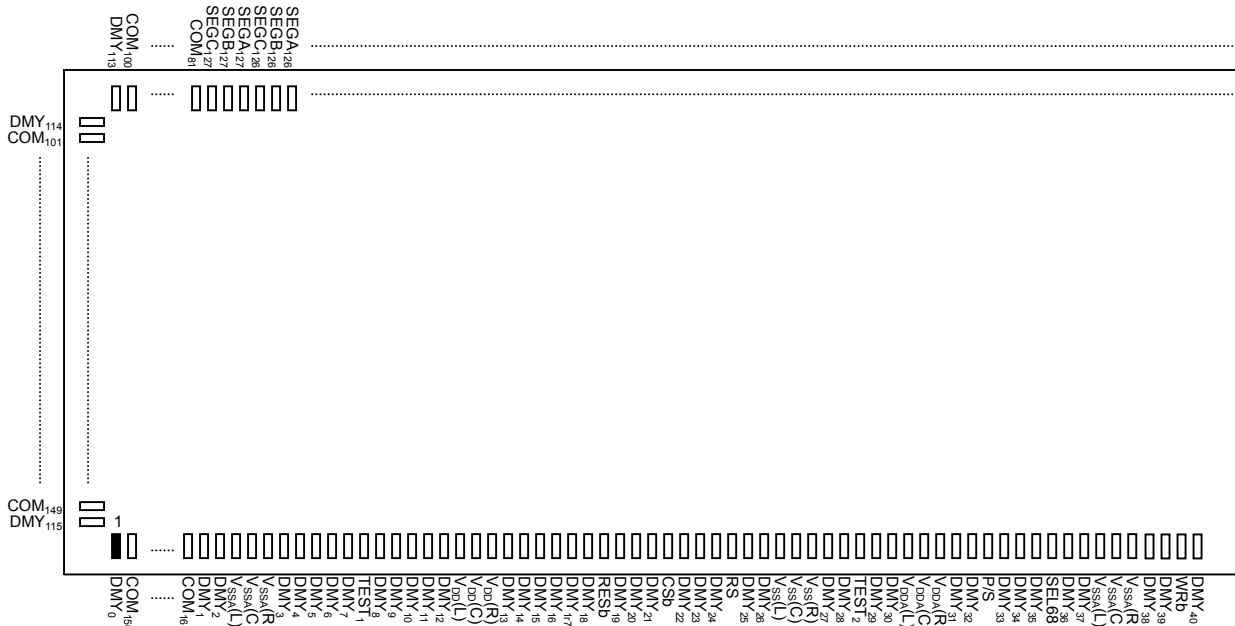
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■ PAD LOCATION



NOTE1) Multiple PADs with successive numbers are internally connected.

NOTE2) Dummy PADs, symbolized with DUMMY, are electrically open.

NOTE3) The purpose of this drawing is to show the order of PADs. Use "PAD CORDINATE TABLE 1 to 6" for design.

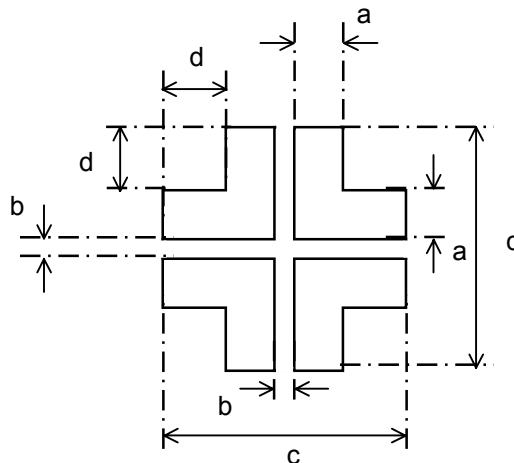
Chip Center :X=0um, Y=0um
 Chip Size :X=20.00mm, Y= 3.13mm
 Chip Thickness :625um $\pm$ 25um
 Bump Pitch :45um(Min)
 Bump Space :15um
 Bump Size :32um x 68um (COM/SEG), 47um x 68um (Interface)
 :68um x 68um (DMY₀, 109, 110, 111, 112, 113, 114, 115)
 Bump Height :17.5um $\pm$ 3.5um
 Bump Material :Au

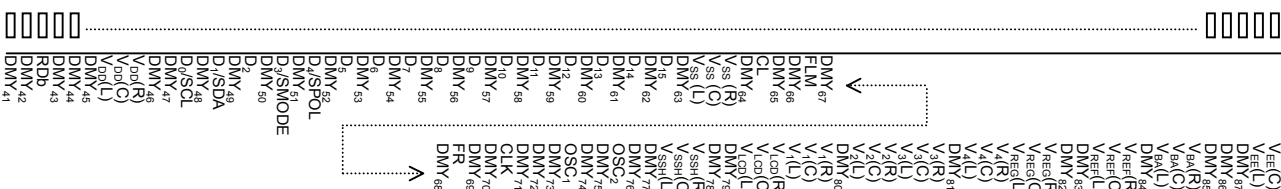
Alignment marks

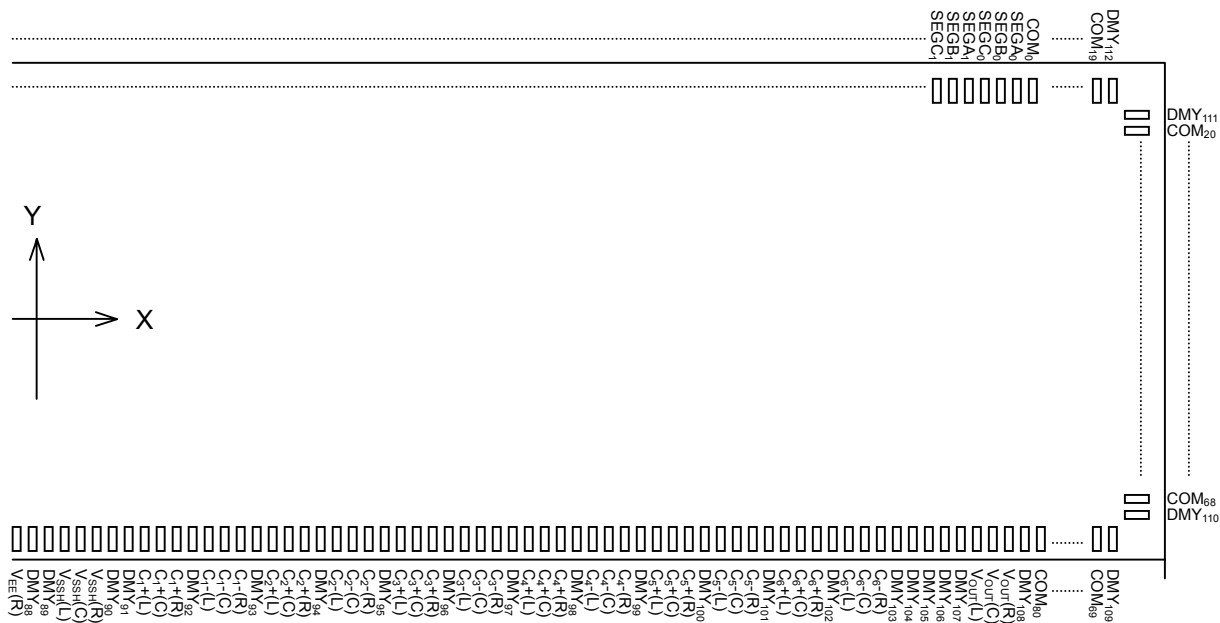
a: 30 μ m
 b: 6 μ m
 c: 120 μ m
 d: 27 μ m

Alignment mark coordinates

X=-9831 μ m, Y=-1396 μ m
 X= 9831 μ m, Y=-1396 μ m







■ PAD COORDINATES 1

Chip Size 20000μm x 3130μm (Chip Center 0μm x 0μm)

No.	PAD NAME	X (μm)	Y (μm)	No.	PAD NAME	X (μm)	Y (μm)	No.	PAD NAME	X (μm)	Y (μm)
1	DMY ₀	-9581	-1396	52	V _{SS} (R)	-6510	-1396	103	DMY ₅₅	-2250	-1396
2	COM ₁₅₀	-9518	-1396	53	DMY ₂₇	-6330	-1396	104	D ₈	-2130	-1396
3	COM ₁₅₁	-9473	-1396	54	DMY ₂₈	-6270	-1396	105	DMY ₅₆	-2010	-1396
4	COM ₁₅₂	-9428	-1396	55	TEST ₂	-6210	-1396	106	D ₉	-1890	-1396
5	COM ₁₅₃	-9383	-1396	56	DMY ₂₉	-6150	-1396	107	DMY ₅₇	-1770	-1396
6	COM ₁₅₄	-9338	-1396	57	DMY ₃₀	-6090	-1396	108	D ₁₀	-1650	-1396
7	COM ₁₅₅	-9293	-1396	58	V _{DDA} (L)	-6030	-1396	109	DMY ₅₈	-1530	-1396
8	COM ₁₅₆	-9248	-1396	59	V _{DDA} (C)	-5970	-1396	110	D ₁₁	-1410	-1396
9	COM ₁₅₇	-9203	-1396	60	V _{DDA} (R)	-5910	-1396	111	DMY ₅₉	-1290	-1396
10	COM ₁₅₈	-9158	-1396	61	DMY ₃₁	-5850	-1396	112	D ₁₂	-1170	-1396
11	COM ₁₅₉	-9113	-1396	62	DMY ₃₂	-5790	-1396	113	DMY ₆₀	-1050	-1396
12	COM ₁₆₀	-9068	-1396	63	P/S	-5730	-1396	114	D ₁₃	-930	-1396
13	COM ₁₆₁	-9023	-1396	64	DMY ₃₃	-5670	-1396	115	DMY ₆₁	-810	-1396
14	DMY ₁	-8910	-1396	65	DMY ₃₄	-5610	-1396	116	D ₁₄	-690	-1396
15	DMY ₂	-8850	-1396	66	DMY ₃₅	-5550	-1396	117	DMY ₆₂	-570	-1396
16	V _{SSA} (L)	-8790	-1396	67	SEL68	-5490	-1396	118	D ₁₅	-450	-1396
17	V _{SSA} (C)	-8730	-1396	68	DMY ₃₆	-5430	-1396	119	DMY ₆₃	-330	-1396
18	V _{SSA} (R)	-8670	-1396	69	DMY ₃₇	-5370	-1396	120	V _{SS} (L)	-270	-1396
19	DMY ₃	-8610	-1396	70	V _{SSA} (L)	-5310	-1396	121	V _{SS} (C)	-210	-1396
20	DMY ₄	-8550	-1396	71	V _{SSA} (C)	-5250	-1396	122	V _{SS} (R)	-150	-1396
21	DMY ₅	-8490	-1396	72	V _{SSA} (R)	-5190	-1396	123	DMY ₆₄	30	-1396
22	DMY ₆	-8430	-1396	73	DMY ₃₈	-5130	-1396	124	CL	150	-1396
23	DMY ₇	-8370	-1396	74	DMY ₃₉	-5070	-1396	125	DMY ₆₅	270	-1396
24	TEST ₁	-8310	-1396	75	WRb	-5010	-1396	126	DMY ₆₆	330	-1396
25	DMY ₈	-8250	-1396	76	DMY ₄₀	-4950	-1396	127	FLM	450	-1396
26	DMY ₉	-8190	-1396	77	DMY ₄₁	-4890	-1396	128	DMY ₆₇	570	-1396
27	DMY ₁₀	-8130	-1396	78	DMY ₄₂	-4830	-1396	129	DMY ₆₈	630	-1396
28	DMY ₁₁	-8070	-1396	79	RDb	-4770	-1396	130	FR	750	-1396
29	DMY ₁₂	-8010	-1396	80	DMY ₄₃	-4710	-1396	131	DMY ₆₉	870	-1396
30	V _{DD} (L)	-7950	-1396	81	DMY ₄₄	-4650	-1396	132	DMY ₇₀	930	-1396
31	V _{DD} (C)	-7890	-1396	82	DMY ₄₅	-4590	-1396	133	CLK	1050	-1396
32	V _{DD} (R)	-7830	-1396	83	V _{DD} (L)	-4530	-1396	134	DMY ₇₁	1170	-1396
33	DMY ₁₃	-7650	-1396	84	V _{DD} (C)	-4470	-1396	135	DMY ₇₂	1230	-1396
34	DMY ₁₄	-7590	-1396	85	V _{DD} (R)	-4410	-1396	136	DMY ₇₃	1290	-1396
35	DMY ₁₅	-7530	-1396	86	DMY ₄₆	-4230	-1396	137	OSC ₁	1350	-1396
36	DMY ₁₆	-7470	-1396	87	DMY ₄₇	-4170	-1396	138	DMY ₇₄	1410	-1396
37	DMY ₁₇	-7410	-1396	88	D ₀	-4050	-1396	139	DMY ₇₅	1470	-1396
38	DMY ₁₈	-7350	-1396	89	DMY ₄₈	-3930	-1396	140	OSC ₂	1650	-1396
39	RESb	-7290	-1396	90	D ₁	-3810	-1396	141	DMY ₇₆	1830	-1396
40	DMY ₁₉	-7230	-1396	91	DMY ₄₉	-3690	-1396	142	DMY ₇₇	1890	-1396
41	DMY ₂₀	-7170	-1396	92	D ₂	-3570	-1396	143	V _{SSH} (L)	1950	-1396
42	DMY ₂₁	-7110	-1396	93	DMY ₅₀	-3450	-1396	144	V _{SSH} (C)	2010	-1396
43	CSb	-7050	-1396	94	D ₃	-3330	-1396	145	V _{SSH} (R)	2070	-1396
44	DMY ₂₂	-6990	-1396	95	DMY ₅₁	-3210	-1396	146	DMY ₇₈	2250	-1396
45	DMY ₂₃	-6930	-1396	96	D ₄	-3090	-1396	147	DMY ₇₉	2310	-1396
46	DMY ₂₄	-6870	-1396	97	DMY ₅₂	-2970	-1396	148	V _{LCD} (L)	2370	-1396
47	RS	-6810	-1396	98	D ₅	-2850	-1396	149	V _{LCD} (C)	2430	-1396
48	DMY ₂₅	-6750	-1396	99	DMY ₅₃	-2730	-1396	150	V _{LCD} (R)	2490	-1396
49	DMY ₂₆	-6690	-1396	100	D ₆	-2610	-1396	151	V ₁ (L)	2670	-1396
50	V _{SS} (L)	-6630	-1396	101	DMY ₅₄	-2490	-1396	152	V ₁ (C)	2730	-1396
51	V _{SS} (C)	-6570	-1396	102	D ₇	-2370	-1396	153	V ₁ (R)	2790	-1396

■ PAD COORDINATES 2

Chip Size 20000μm x 3130μm (Chip Center 0μm x 0μm)

No.	PAD NAME	X (μm)	Y (μm)	No.	PAD NAME	X (μm)	Y (μm)	No.	PAD NAME	X (μm)	Y (μm)
154	DMY ₈₀	2850	-1396	205	DMY ₉₅	6390	-1396	256	COM ₇₀	9473	-1396
155	V ₂ (L)	2910	-1396	206	C ₃₊ (L)	6450	-1396	257	COM ₆₉	9518	-1396
156	V ₂ (C)	2970	-1396	207	C ₃₊ (C)	6510	-1396	258	DMY ₁₀₉	9581	-1396
157	V ₂ (R)	3030	-1396	208	C ₃₊ (R)	6570	-1396	259	DMY ₁₁₀	9831	-1143
158	V ₃ (L)	3210	-1396	209	DMY ₉₆	6630	-1396	260	COM ₆₈	9831	-1080
159	V ₃ (C)	3270	-1396	210	C ₃₋ (L)	6690	-1396	261	COM ₆₇	9831	-1035
160	V ₃ (R)	3330	-1396	211	C ₃₋ (C)	6750	-1396	262	COM ₆₆	9831	-990
161	DMY ₈₁	3390	-1396	212	C ₃₋ (R)	6810	-1396	263	COM ₆₅	9831	-945
162	V ₄ (L)	3450	-1396	213	DMY ₉₇	6870	-1396	264	COM ₆₄	9831	-900
163	V ₄ (C)	3510	-1396	214	C ₄₊ (L)	6930	-1396	265	COM ₆₃	9831	-855
164	V ₄ (R)	3570	-1396	215	C ₄₊ (C)	6990	-1396	266	COM ₆₂	9831	-810
165	V _{REG} (L)	3750	-1396	216	C ₄₊ (R)	7050	-1396	267	COM ₆₁	9831	-765
166	V _{REG} (C)	3810	-1396	217	DMY ₉₈	7110	-1396	268	COM ₆₀	9831	-720
167	V _{REG} (R)	3870	-1396	218	C ₄₋ (L)	7170	-1396	269	COM ₅₉	9831	-675
168	DMY ₈₂	3930	-1396	219	C ₄₋ (C)	7230	-1396	270	COM ₅₈	9831	-630
169	DMY ₈₃	3990	-1396	220	C ₄₋ (R)	7290	-1396	271	COM ₅₇	9831	-585
170	V _{REF} (L)	4050	-1396	221	DMY ₉₉	7350	-1396	272	COM ₅₆	9831	-540
171	V _{REF} (C)	4110	-1396	222	C ₅₊ (L)	7410	-1396	273	COM ₅₅	9831	-495
172	V _{REF} (R)	4170	-1396	223	C ₅₊ (C)	7470	-1396	274	COM ₅₄	9831	-450
173	DMY ₈₄	4230	-1396	224	C ₅₊ (R)	7530	-1396	275	COM ₅₃	9831	-405
174	V _{BA} (L)	4290	-1396	225	DMY ₁₀₀	7590	-1396	276	COM ₅₂	9831	-360
175	V _{BA} (C)	4350	-1396	226	C ₅₋ (L)	7650	-1396	277	COM ₅₁	9831	-315
176	V _{BA} (R)	4410	-1396	227	C ₅₋ (C)	7710	-1396	278	COM ₅₀	9831	-270
177	DMY ₈₅	4470	-1396	228	C ₅₋ (R)	7770	-1396	279	COM ₄₉	9831	-225
178	DMY ₈₆	4530	-1396	229	DMY ₁₀₁	7830	-1396	280	COM ₄₈	9831	-180
179	DMY ₈₇	4590	-1396	230	C ₆₊ (L)	7890	-1396	281	COM ₄₇	9831	-135
180	V _{EE} (L)	4650	-1396	231	C ₆₊ (C)	7950	-1396	282	COM ₄₆	9831	-90
181	V _{EE} (C)	4710	-1396	232	C ₆₊ (R)	8010	-1396	283	COM ₄₅	9831	-45
182	V _{EE} (R)	4770	-1396	233	DMY ₁₀₂	8070	-1396	284	COM ₄₄	9831	0
183	DMY ₈₈	4950	-1396	234	C ₆₋ (L)	8130	-1396	285	COM ₄₃	9831	45
184	DMY ₈₉	5010	-1396	235	C ₆₋ (C)	8190	-1396	286	COM ₄₂	9831	90
185	V _{SSH} (L)	5190	-1396	236	C ₆₋ (R)	8250	-1396	287	COM ₄₁	9831	135
186	V _{SSH} (C)	5250	-1396	237	DMY ₁₀₃	8310	-1396	288	COM ₄₀	9831	180
187	V _{SSH} (R)	5310	-1396	238	DMY ₁₀₄	8370	-1396	289	COM ₃₉	9831	225
188	DMY ₉₀	5370	-1396	239	DMY ₁₀₅	8430	-1396	290	COM ₃₈	9831	270
189	DMY ₉₁	5430	-1396	240	DMY ₁₀₆	8490	-1396	291	COM ₃₇	9831	315
190	C ₁₊ (L)	5490	-1396	241	DMY ₁₀₇	8550	-1396	292	COM ₃₆	9831	360
191	C ₁₊ (C)	5550	-1396	242	V _{OUT} (L)	8610	-1396	293	COM ₃₅	9831	405
192	C ₁₊ (R)	5610	-1396	243	V _{OUT} (C)	8670	-1396	294	COM ₃₄	9831	450
193	DMY ₉₂	5670	-1396	244	V _{OUT} (R)	8730	-1396	295	COM ₃₃	9831	495
194	C ₁₋ (L)	5730	-1396	245	DMY ₁₀₈	8910	-1396	296	COM ₃₂	9831	540
195	C ₁₋ (C)	5790	-1396	246	COM ₈₀	9023	-1396	297	COM ₃₁	9831	585
196	C ₁₋ (R)	5850	-1396	247	COM ₇₉	9068	-1396	298	COM ₃₀	9831	630
197	DMY ₉₃	5910	-1396	248	COM ₇₈	9113	-1396	299	COM ₂₉	9831	675
198	C ₂₊ (L)	5970	-1396	249	COM ₇₇	9158	-1396	300	COM ₂₈	9831	720
199	C ₂₊ (C)	6030	-1396	250	COM ₇₆	9203	-1396	301	COM ₂₇	9831	765
200	C ₂₊ (R)	6090	-1396	251	COM ₇₅	9248	-1396	302	COM ₂₆	9831	810
201	DMY ₉₄	6150	-1396	252	COM ₇₄	9293	-1396	303	COM ₂₅	9831	855
202	C ₂₋ (L)	6210	-1396	253	COM ₇₃	9338	-1396	304	COM ₂₄	9831	900
203	C ₂₋ (C)	6270	-1396	254	COM ₇₂	9383	-1396	305	COM ₂₃	9831	945
204	C ₂₋ (R)	6330	-1396	255	COM ₇₁	9428	-1396	306	COM ₂₂	9831	990

■ PAD COORDINATES 3

Chip Size 20000μm x 3130μm (Chip Center 0μm x 0μm)

No.	PAD NAME	X (μm)	Y (μm)	No.	PAD NAME	X (μm)	Y (μm)	No.	PAD NAME	X (μm)	Y (μm)
307	COM ₂₁	9831	1035	358	SEGA ₉	7403	1396	409	SEGA ₂₆	5108	1396
308	COM ₂₀	9831	1080	359	SEGB ₉	7358	1396	410	SEGB ₂₆	5063	1396
309	DMY ₁₁₁	9831	1144	360	SEGC ₉	7313	1396	411	SEGC ₂₆	5018	1396
310	DMY ₁₁₂	9581	1396	361	SEGA ₁₀	7268	1396	412	SEGA ₂₇	4973	1396
311	COM ₁₉	9518	1396	362	SEGB ₁₀	7223	1396	413	SEGB ₂₇	4928	1396
312	COM ₁₈	9473	1396	363	SEGC ₁₀	7178	1396	414	SEGC ₂₇	4883	1396
313	COM ₁₇	9428	1396	364	SEGA ₁₁	7133	1396	415	SEGA ₂₈	4838	1396
314	COM ₁₆	9383	1396	365	SEGB ₁₁	7088	1396	416	SEGB ₂₈	4793	1396
315	COM ₁₅	9338	1396	366	SEGC ₁₁	7043	1396	417	SEGC ₂₈	4748	1396
316	COM ₁₄	9293	1396	367	SEGA ₁₂	6998	1396	418	SEGA ₂₉	4703	1396
317	COM ₁₃	9248	1396	368	SEGB ₁₂	6953	1396	419	SEGB ₂₉	4658	1396
318	COM ₁₂	9203	1396	369	SEGC ₁₂	6908	1396	420	SEGC ₂₉	4613	1396
319	COM ₁₁	9158	1396	370	SEGA ₁₃	6863	1396	421	SEGA ₃₀	4568	1396
320	COM ₁₀	9113	1396	371	SEGB ₁₃	6818	1396	422	SEGB ₃₀	4523	1396
321	COM ₉	9068	1396	372	SEGC ₁₃	6773	1396	423	SEGC ₃₀	4478	1396
322	COM ₈	9023	1396	373	SEGA ₁₄	6728	1396	424	SEGA ₃₁	4433	1396
323	COM ₇	8978	1396	374	SEGB ₁₄	6683	1396	425	SEGB ₃₁	4388	1396
324	COM ₆	8933	1396	375	SEGC ₁₄	6638	1396	426	SEGC ₃₁	4343	1396
325	COM ₅	8888	1396	376	SEGA ₁₅	6593	1396	427	SEGA ₃₂	4298	1396
326	COM ₄	8843	1396	377	SEGB ₁₅	6548	1396	428	SEGB ₃₂	4253	1396
327	COM ₃	8798	1396	378	SEGC ₁₅	6503	1396	429	SEGC ₃₂	4208	1396
328	COM ₂	8753	1396	379	SEGA ₁₆	6458	1396	430	SEGA ₃₃	4163	1396
329	COM ₁	8708	1396	380	SEGB ₁₆	6413	1396	431	SEGB ₃₃	4118	1396
330	COM ₀	8663	1396	381	SEGC ₁₆	6368	1396	432	SEGC ₃₃	4073	1396
331	SEGA ₀	8618	1396	382	SEGA ₁₇	6323	1396	433	SEGA ₃₄	4028	1396
332	SEGB ₀	8573	1396	383	SEGB ₁₇	6278	1396	434	SEGB ₃₄	3983	1396
333	SEGC ₀	8528	1396	384	SEGC ₁₇	6233	1396	435	SEGC ₃₄	3938	1396
334	SEGA ₁	8483	1396	385	SEGA ₁₈	6188	1396	436	SEGA ₃₅	3893	1396
335	SEGB ₁	8438	1396	386	SEGB ₁₈	6143	1396	437	SEGB ₃₅	3848	1396
336	SEGC ₁	8393	1396	387	SEGC ₁₈	6098	1396	438	SEGC ₃₅	3803	1396
337	SEGA ₂	8348	1396	388	SEGA ₁₉	6053	1396	439	SEGA ₃₆	3758	1396
338	SEGB ₂	8303	1396	389	SEGB ₁₉	6008	1396	440	SEGB ₃₆	3713	1396
339	SEGC ₂	8258	1396	390	SEGC ₁₉	5963	1396	441	SEGC ₃₆	3668	1396
340	SEGA ₂	8213	1396	391	SEGA ₂₀	5918	1396	442	SEGA ₃₇	3623	1396
341	SEGB ₃	8168	1396	392	SEGB ₂₀	5873	1396	443	SEGB ₃₇	3578	1396
342	SEGC ₃	8123	1396	393	SEGC ₂₀	5828	1396	444	SEGC ₃₇	3533	1396
343	SEGA ₄	8078	1396	394	SEGA ₂₁	5783	1396	445	SEGA ₃₈	3488	1396
344	SEGB ₄	8033	1396	395	SEGB ₂₁	5738	1396	446	SEGB ₃₈	3443	1396
345	SEGC ₄	7988	1396	396	SEGC ₂₁	5693	1396	447	SEGC ₃₈	3398	1396
346	SEGA ₅	7943	1396	397	SEGA ₂₂	5648	1396	448	SEGA ₃₉	3353	1396
347	SEGB ₅	7898	1396	398	SEGB ₂₂	5603	1396	449	SEGB ₃₉	3308	1396
348	SEGC ₅	7853	1396	399	SEGC ₂₂	5558	1396	450	SEGC ₃₉	3263	1396
349	SEGA ₆	7808	1396	400	SEGA ₂₃	5513	1396	451	SEGA ₄₀	3218	1396
350	SEGB ₆	7763	1396	401	SEGB ₂₃	5468	1396	452	SEGB ₄₀	3173	1396
351	SEGC ₆	7718	1396	402	SEGC ₂₃	5423	1396	453	SEGC ₄₀	3128	1396
352	SEGA ₇	7673	1396	403	SEGA ₂₄	5378	1396	454	SEGA ₄₁	3083	1396
353	SEGB ₇	7628	1396	404	SEGB ₂₄	5333	1396	455	SEGB ₄₁	3038	1396
354	SEGC ₇	7583	1396	405	SEGC ₂₄	5288	1396	456	SEGC ₄₁	2993	1396
355	SEGA ₈	7538	1396	406	SEGA ₂₅	5243	1396	457	SEGA ₄₂	2948	1396
356	SEGB ₈	7493	1396	407	SEGB ₂₅	5198	1396	458	SEGB ₄₂	2903	1396
357	SEGC ₈	7448	1396	408	SEGC ₂₅	5153	1396	459	SEGC ₄₂	2858	1396

■ PAD COORDINATES 4

Chip Size 20000μm x 3130μm (Chip Center 0μm x 0μm)

No.	PAD NAME	X (μm)	Y (μm)	No.	PAD NAME	X (μm)	Y (μm)	No.	PAD NAME	X (μm)	Y (μm)
460	SEGA ₄₃	2813	1396	511	SEGA ₆₀	518	1396	562	SEGA ₇₇	-1778	1396
461	SEGB ₄₃	2768	1396	512	SEGB ₆₀	473	1396	563	SEGB ₇₇	-1823	1396
462	SEGC ₄₃	2723	1396	513	SEGC ₆₀	428	1396	564	SEGC ₇₇	-1868	1396
463	SEGA ₄₄	2678	1396	514	SEGA ₆₁	383	1396	565	SEGA ₇₈	-1913	1396
464	SEGB ₄₄	2633	1396	515	SEGB ₆₁	338	1396	566	SEGB ₇₈	-1958	1396
465	SEGC ₄₄	2588	1396	516	SEGC ₆₁	293	1396	567	SEGC ₇₈	-2003	1396
466	SEGA ₄₅	2543	1396	517	SEGA ₆₂	248	1396	568	SEGA ₇₉	-2048	1396
467	SEGB ₄₅	2498	1396	518	SEGB ₆₂	203	1396	569	SEGB ₇₉	-2093	1396
468	SEGC ₄₅	2453	1396	519	SEGC ₆₂	158	1396	570	SEGC ₇₉	-2138	1396
469	SEGA ₄₆	2408	1396	520	SEGA ₆₃	113	1396	571	SEGA ₈₀	-2183	1396
470	SEGB ₄₆	2363	1396	521	SEGB ₆₃	68	1396	572	SEGB ₈₀	-2228	1396
471	SEGC ₄₆	2318	1396	522	SEGC ₆₃	23	1396	573	SEGC ₈₀	-2273	1396
472	SEGA ₄₇	2273	1396	523	SEGA ₆₄	-23	1396	574	SEGA ₈₁	-2318	1396
473	SEGB ₄₇	2228	1396	524	SEGB ₆₄	-68	1396	575	SEGB ₈₁	-2363	1396
474	SEGC ₄₇	2183	1396	525	SEGC ₆₄	-113	1396	576	SEGC ₈₁	-2408	1396
475	SEGA ₄₈	2138	1396	526	SEGA ₆₅	-158	1396	577	SEGA ₈₂	-2453	1396
476	SEGB ₄₈	2093	1396	527	SEGB ₆₅	-203	1396	578	SEGB ₈₂	-2498	1396
477	SEGC ₄₈	2048	1396	528	SEGC ₆₅	-248	1396	579	SEGC ₈₂	-2543	1396
478	SEGA ₄₉	2003	1396	529	SEGA ₆₆	-293	1396	580	SEGA ₈₃	-2588	1396
479	SEGB ₄₉	1958	1396	530	SEGB ₆₆	-338	1396	581	SEGB ₈₃	-2633	1396
480	SEGC ₄₉	1913	1396	531	SEGC ₆₆	-383	1396	582	SEGC ₈₃	-2678	1396
481	SEGA ₅₀	1868	1396	532	SEGA ₆₇	-428	1396	583	SEGA ₈₄	-2723	1396
482	SEGB ₅₀	1823	1396	533	SEGB ₆₇	-473	1396	584	SEGB ₈₄	-2768	1396
483	SEGC ₅₀	1778	1396	534	SEGC ₆₇	-518	1396	585	SEGC ₈₄	-2813	1396
484	SEGA ₅₁	1733	1396	535	SEGA ₆₈	-563	1396	586	SEGA ₈₅	-2858	1396
485	SEGB ₅₁	1688	1396	536	SEGB ₆₈	-608	1396	587	SEGB ₈₅	-2903	1396
486	SEGC ₅₁	1643	1396	537	SEGC ₆₈	-653	1396	588	SEGC ₈₅	-2948	1396
487	SEGA ₅₂	1598	1396	538	SEGA ₆₉	-698	1396	589	SEGA ₈₆	-2993	1396
488	SEGB ₅₂	1553	1396	539	SEGB ₆₉	-743	1396	590	SEGB ₈₆	-3038	1396
489	SEGC ₅₂	1508	1396	540	SEGC ₆₉	-788	1396	591	SEGC ₈₆	-3083	1396
490	SEGA ₅₃	1463	1396	541	SEGA ₇₀	-833	1396	592	SEGA ₈₇	-3128	1396
491	SEGB ₅₃	1418	1396	542	SEGB ₇₀	-878	1396	593	SEGB ₈₇	-3173	1396
492	SEGC ₅₃	1373	1396	543	SEGC ₇₀	-923	1396	594	SEGC ₈₇	-3218	1396
493	SEGA ₅₄	1328	1396	544	SEGA ₇₁	-968	1396	595	SEGA ₈₈	-3263	1396
494	SEGB ₅₄	1283	1396	545	SEGB ₇₁	-1013	1396	596	SEGB ₈₈	-3308	1396
495	SEGC ₅₄	1238	1396	546	SEGC ₇₁	-1058	1396	597	SEGC ₈₈	-3353	1396
496	SEGA ₅₅	1193	1396	547	SEGA ₇₂	-1103	1396	598	SEGA ₈₉	-3398	1396
497	SEGB ₅₅	1148	1396	548	SEGB ₇₂	-1148	1396	599	SEGB ₈₉	-3443	1396
498	SEGC ₅₅	1103	1396	549	SEGC ₇₂	-1193	1396	600	SEGC ₈₉	-3488	1396
499	SEGA ₅₆	1058	1396	550	SEGA ₇₃	-1238	1396	601	SEGA ₉₀	-3533	1396
500	SEGB ₅₆	1013	1396	551	SEGB ₇₃	-1283	1396	602	SEGB ₉₀	-3578	1396
501	SEGC ₅₆	968	1396	552	SEGC ₇₃	-1328	1396	603	SEGC ₉₀	-3623	1396
502	SEGA ₅₇	923	1396	553	SEGA ₇₄	-1373	1396	604	SEGA ₉₁	-3668	1396
503	SEGB ₅₇	878	1396	554	SEGB ₇₄	-1418	1396	605	SEGB ₉₁	-3713	1396
504	SEGC ₅₇	833	1396	555	SEGC ₇₄	-1463	1396	606	SEGC ₉₁	-3758	1396
505	SEGA ₅₈	788	1396	556	SEGA ₇₅	-1508	1396	607	SEGA ₉₂	-3803	1396
506	SEGB ₅₈	743	1396	557	SEGB ₇₅	-1553	1396	608	SEGB ₉₂	-3848	1396
507	SEGC ₅₈	698	1396	558	SEGC ₇₅	-1598	1396	609	SEGC ₉₂	-3893	1396
508	SEGA ₅₉	653	1396	559	SEGA ₇₆	-1643	1396	610	SEGA ₉₃	-3938	1396
509	SEGB ₅₉	608	1396	560	SEGB ₇₆	-1688	1396	611	SEGB ₉₃	-3983	1396
510	SEGC ₅₉	563	1396	561	SEGC ₇₆	-1733	1396	612	SEGC ₉₃	-4028	1396

■ PAD COORDINATES 5

Chip Size 20000μm x 3130μm (Chip Center 0μm x 0μm)

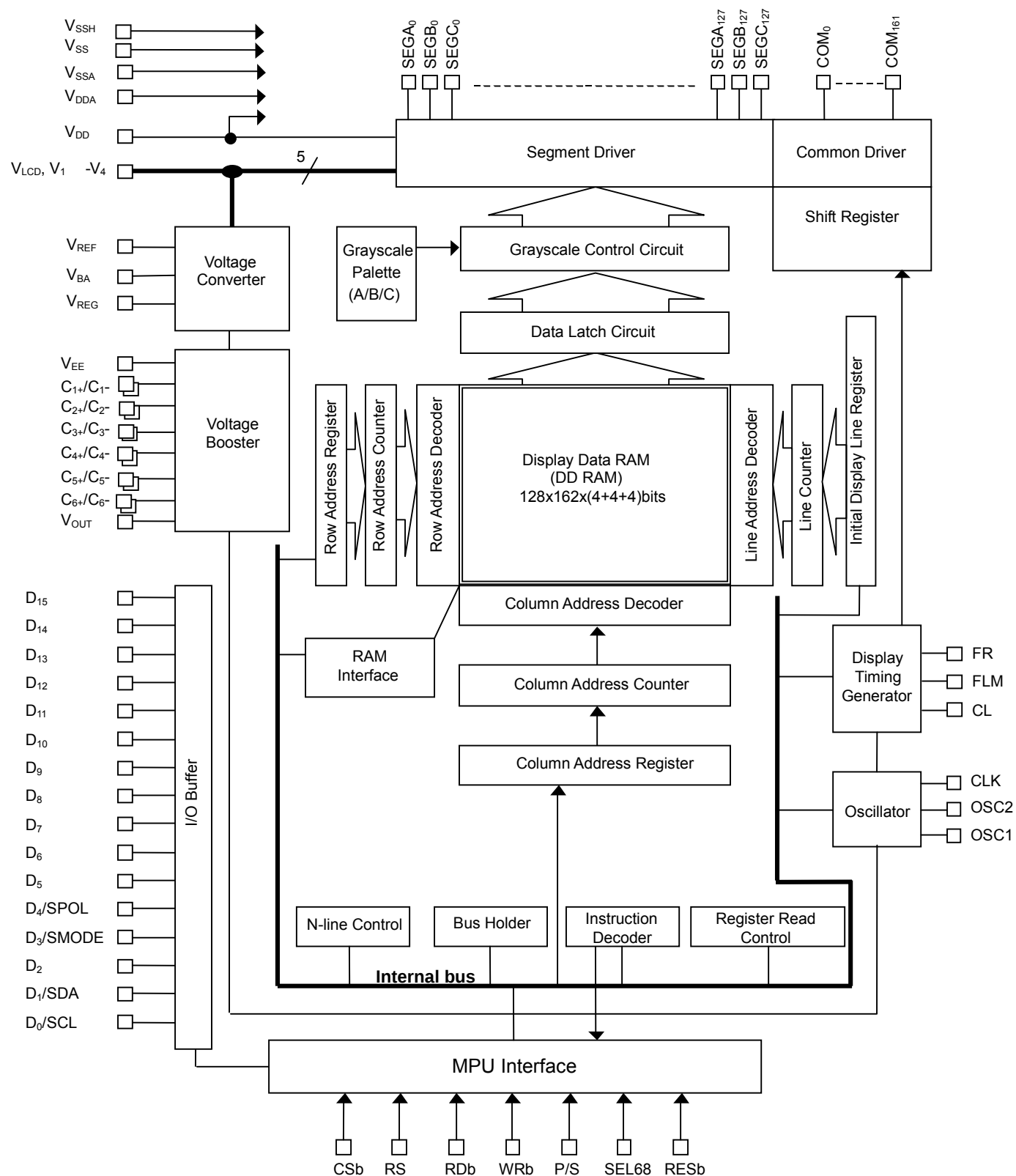
No.	PAD NAME	X (μm)	Y (μm)	No.	PAD NAME	X (μm)	Y (μm)	No.	PAD NAME	X (μm)	Y (μm)
613	SEGA ₉₄	-4073	1396	664	SEGA ₁₁₁	-6368	1396	715	COM ₈₁	-8663	1396
614	SEGB ₉₄	-4118	1396	665	SEGB ₁₁₁	-6413	1396	716	COM ₈₂	-8708	1396
615	SEGC ₉₄	-4163	1396	666	SEGC ₁₁₁	-6458	1396	717	COM ₈₃	-8753	1396
616	SEGA ₉₅	-4208	1396	667	SEGA ₁₁₂	-6503	1396	718	COM ₈₄	-8798	1396
617	SEGB ₉₅	-4253	1396	668	SEGB ₁₁₂	-6548	1396	719	COM ₈₅	-8843	1396
618	SEGC ₉₅	-4298	1396	669	SEGC ₁₁₂	-6593	1396	720	COM ₈₆	-8888	1396
619	SEGA ₉₆	-4343	1396	670	SEGA ₁₁₃	-6638	1396	721	COM ₈₇	-8933	1396
620	SEGB ₉₆	-4388	1396	671	SEGB ₁₁₃	-6683	1396	722	COM ₈₈	-8978	1396
621	SEGC ₉₆	-4433	1396	672	SEGC ₁₁₃	-6728	1396	723	COM ₈₉	-9023	1396
622	SEGA ₉₇	-4478	1396	673	SEGA ₁₁₄	-6773	1396	724	COM ₉₀	-9068	1396
623	SEGB ₉₇	-4523	1396	674	SEGB ₁₁₄	-6818	1396	725	COM ₉₁	-9113	1396
624	SEGC ₉₇	-4568	1396	675	SEGC ₁₁₄	-6863	1396	726	COM ₉₂	-9158	1396
625	SEGA ₉₈	-4613	1396	676	SEGA ₁₁₅	-6908	1396	727	COM ₉₃	-9203	1396
626	SEGB ₉₈	-4658	1396	677	SEGB ₁₁₅	-6953	1396	728	COM ₉₄	-9248	1396
627	SEGC ₉₈	-4703	1396	678	SEGC ₁₁₅	-6998	1396	729	COM ₉₅	-9293	1396
628	SEGA ₉₉	-4748	1396	679	SEGA ₁₁₆	-7043	1396	730	COM ₉₆	-9338	1396
629	SEGB ₉₉	-4793	1396	680	SEGB ₁₁₆	-7088	1396	731	COM ₉₇	-9383	1396
630	SEGC ₉₉	-4838	1396	681	SEGC ₁₁₆	-7133	1396	732	COM ₉₈	-9428	1396
631	SEGA ₁₀₀	-4883	1396	682	SEGA ₁₁₇	-7178	1396	733	COM ₉₉	-9473	1396
632	SEGB ₁₀₀	-4928	1396	683	SEGB ₁₁₇	-7223	1396	734	COM ₁₀₀	-9518	1396
633	SEGC ₁₀₀	-4973	1396	684	SEGC ₁₁₇	-7268	1396	735	DMY ₁₁₃	-9581	1396
634	SEGA ₁₀₁	-5018	1396	685	SEGA ₁₁₈	-7313	1396	736	DMY ₁₁₄	-9831	1143
635	SEGB ₁₀₁	-5063	1396	686	SEGB ₁₁₈	-7358	1396	737	COM ₁₀₁	-9831	1080
636	SEGC ₁₀₁	-5108	1396	687	SEGC ₁₁₈	-7403	1396	738	COM ₁₀₂	-9831	1035
637	SEGA ₁₀₂	-5153	1396	688	SEGA ₁₁₉	-7448	1396	739	COM ₁₀₃	-9831	990
638	SEGB ₁₀₂	-5198	1396	689	SEGB ₁₁₉	-7493	1396	740	COM ₁₀₄	-9831	945
639	SEGC ₁₀₂	-5243	1396	690	SEGC ₁₁₉	-7538	1396	741	COM ₁₀₅	-9831	900
640	SEGA ₁₀₃	-5288	1396	691	SEGA ₁₂₀	-7583	1396	742	COM ₁₀₆	-9831	855
641	SEGB ₁₀₃	-5333	1396	692	SEGB ₁₂₀	-7628	1396	743	COM ₁₀₇	-9831	810
642	SEGC ₁₀₃	-5378	1396	693	SEGC ₁₂₀	-7673	1396	744	COM ₁₀₈	-9831	765
643	SEGA ₁₀₄	-5423	1396	694	SEGA ₁₂₁	-7718	1396	745	COM ₁₀₉	-9831	720
644	SEGB ₁₀₄	-5468	1396	695	SEGB ₁₂₁	-7763	1396	746	COM ₁₁₀	-9831	675
645	SEGC ₁₀₄	-5513	1396	696	SEGC ₁₂₁	-7808	1396	747	COM ₁₁₁	-9831	630
646	SEGA ₁₀₅	-5558	1396	697	SEGA ₁₂₂	-7853	1396	748	COM ₁₁₂	-9831	585
647	SEGB ₁₀₅	-5603	1396	698	SEGB ₁₂₂	-7898	1396	749	COM ₁₁₃	-9831	540
648	SEGC ₁₀₅	-5648	1396	699	SEGC ₁₂₂	-7943	1396	750	COM ₁₁₄	-9831	495
649	SEGA ₁₀₆	-5693	1396	700	SEGA ₁₂₃	-7988	1396	751	COM ₁₁₅	-9831	450
650	SEGB ₁₀₆	-5738	1396	701	SEGB ₁₂₃	-8033	1396	752	COM ₁₁₆	-9831	405
651	SEGC ₁₀₆	-5783	1396	702	SEGC ₁₂₃	-8078	1396	753	COM ₁₁₇	-9831	360
652	SEGA ₁₀₇	-5828	1396	703	SEGA ₁₂₄	-8123	1396	754	COM ₁₁₈	-9831	315
653	SEGB ₁₀₇	-5873	1396	704	SEGB ₁₂₄	-8168	1396	755	COM ₁₁₉	-9831	270
654	SEGC ₁₀₇	-5918	1396	705	SEGC ₁₂₄	-8213	1396	756	COM ₁₂₀	-9831	225
655	SEGA ₁₀₈	-5963	1396	706	SEGA ₁₂₅	-8258	1396	757	COM ₁₂₁	-9831	180
656	SEGB ₁₀₈	-6008	1396	707	SEGB ₁₂₅	-8303	1396	758	COM ₁₂₂	-9831	135
657	SEGC ₁₀₈	-6053	1396	708	SEGC ₁₂₅	-8348	1396	759	COM ₁₂₃	-9831	90
658	SEGA ₁₀₉	-6098	1396	709	SEGA ₁₂₆	-8393	1396	760	COM ₁₂₄	-9831	45
659	SEGB ₁₀₉	-6143	1396	710	SEGB ₁₂₆	-8438	1396	761	COM ₁₂₅	-9831	0
660	SEGC ₁₀₉	-6188	1396	711	SEGC ₁₂₆	-8483	1396	762	COM ₁₂₆	-9831	-45
661	SEGA ₁₁₀	-6233	1396	712	SEGA ₁₂₇	-8528	1396	763	COM ₁₂₇	-9831	-90
662	SEGB ₁₁₀	-6278	1396	713	SEGB ₁₂₇	-8573	1396	764	COM ₁₂₈	-9831	-135
663	SEGC ₁₁₀	-6323	1396	714	SEGC ₁₂₇	-8618	1396	765	COM ₁₂₉	-9831	-180

■ PAD COORDINATES 6

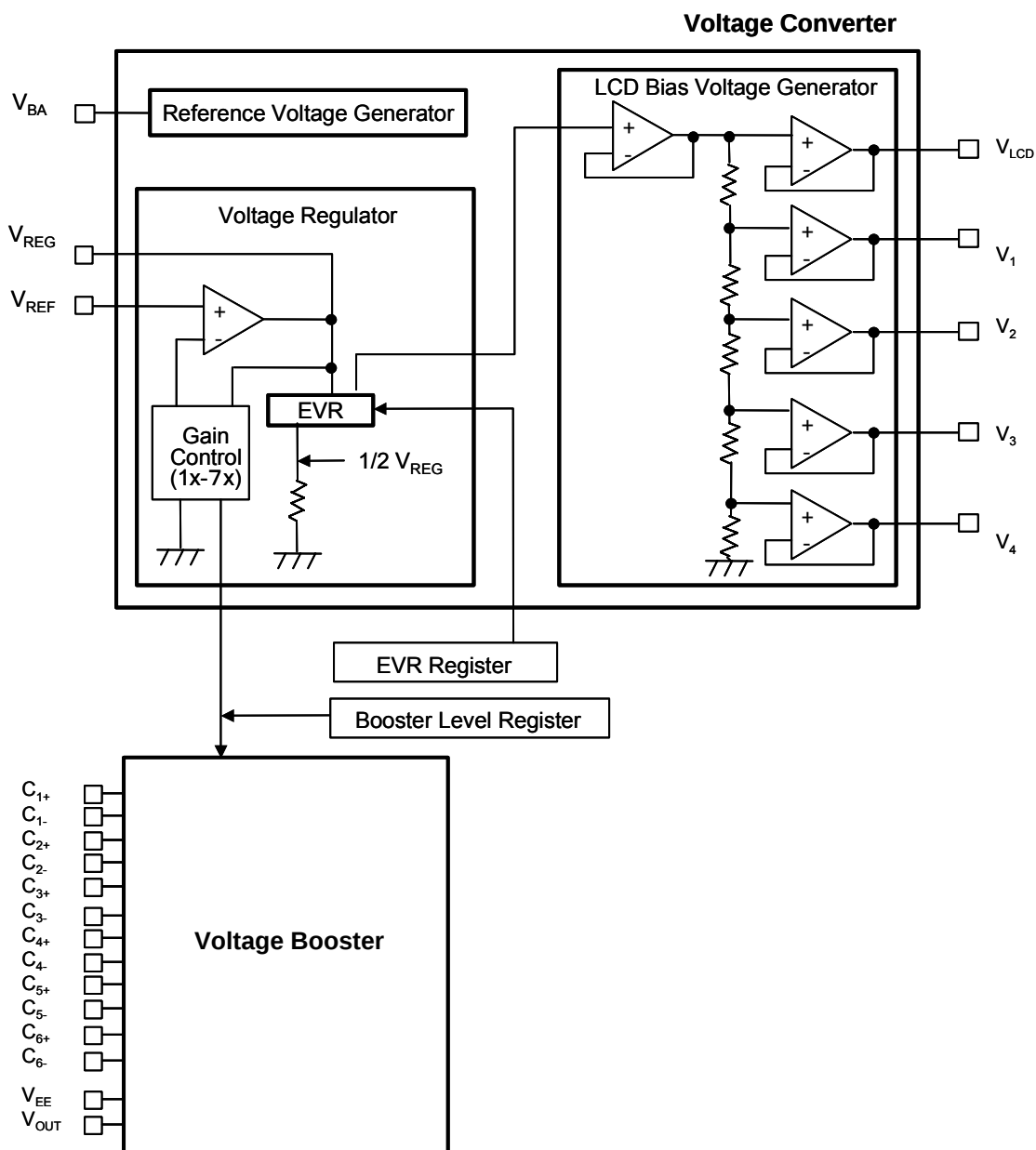
Chip Size 20000μm x 3130μm (Chip Center 0μm x 0μm)

No.	PAD NAME	X (um)	Y (um)
766	COM ₁₃₀	-9831	-225
767	COM ₁₃₁	-9831	-270
768	COM ₁₃₂	-9831	-315
769	COM ₁₃₃	-9831	-360
770	COM ₁₃₄	-9831	-405
771	COM ₁₃₅	-9831	-450
772	COM ₁₃₆	-9831	-495
773	COM ₁₃₇	-9831	-540
774	COM ₁₃₈	-9831	-585
775	COM ₁₃₉	-9831	-630
776	COM ₁₄₀	-9831	-675
777	COM ₁₄₁	-9831	-720
778	COM ₁₄₂	-9831	-765
779	COM ₁₄₃	-9831	-810
780	COM ₁₄₄	-9831	-855
781	COM ₁₄₅	-9831	-900
782	COM ₁₄₆	-9831	-945
783	COM ₁₄₇	-9831	-990
784	COM ₁₄₈	-9831	-1035
785	COM ₁₄₉	-9831	-1080
786	DMY ₁₁₅	-9831	-1144

■ BLOCK DIAGRAM



■ LCD POWER SUPPLY BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	Terminal	I/O	Function
30~32, 83-85	V _{DD}	Power	Power Supply for Logic Circuits
50-52, 120-122	V _{SS}	Power	GND for Logic Circuits
143~145 185~187	V _{SSH}	Power	GND for High Voltage Circuits
58~60	V _{DDA}	Power	V _{DDA} is internally connected to V _{DD} to fix SEL68 or P/S to "H" if necessary, and cannot be used as main power supply. • V _{DDA} should be open if not used.
16~18, 70~72	V _{SSA}	Power	V _{SSA} is internally connected to V _{SS} to fix SEL68 or P/S to "L" if necessary, and cannot be used as main GND. • V _{SSA} should be open if not used.
148-150, 151-153, 155-157, 158-160, 162-164	V _{LCD} V ₁ V ₂ V ₃ V ₄	Power	LCD Bias Voltages • When the internal LCD power supply is used, internal LCD bias voltages (V _{LCD} and V ₁ -V ₄) are activated by the "Power Control" instruction. Stabilizing capacitors are required between each bias voltage and V _{SS} . • When the external LCD power supply is used, LCD bias voltages are externally supplied on V _{LCD} , V ₁ , V ₂ , V ₃ and V ₄ individually, with the following relation maintained: V _{SSH} <V ₄ <V ₃ <V ₂ <V ₁ <V _{LCD}
190-192, 194-196	C ₁₊ C ₁₋	Power	Capacitor Connection for Voltage Booster
198-200, 202-204	C ₂₊ C ₂₋	Power	Capacitor Connection for Voltage Booster
206-208, 210-212	C ₃₊ C ₃₋	Power	Capacitor Connection for Voltage Booster
214-216, 218-220	C ₄₊ C ₄₋	Power	Capacitor Connection for Voltage Booster
222-224, 226-228	C ₅₊ C ₅₋	Power	Capacitor Connection for Voltage Booster
230-232, 234-236	C ₆₊ C ₆₋	Power	Capacitor Connection for Voltage Booster
174-176	V _{BA}	Power	Reference-Voltage Generator Output
170-172	V _{REF}	Power	Voltage Regulator Input
180-182	V _{EE}	Power	Voltage Booster Input • V _{EE} is normally connected to V _{DD} .
242-244	V _{OUT}	Power	Voltage Booster Output • Input if an external LCD power supply is used.
165-167	V _{REG}	Power	Voltage Regulator Output
39	RESb	I	Reset • Active "L"

■ TERMINAL DESCRIPTION 2

No.	Terminal	I/O	Function						
88	D ₀ /SCL	I/O	1. <u>Parallel Interface</u> D₇ to D₀ : 8-bit Bi-directional Bus - In the parallel interface mode (P/S="H"), D₇-D₀ are connected to 8-bit bi-directional MPU bus. <u>Serial Interface</u> SDA : Serial Data SCL : Serial Clock SMODE : 3-/4-line Serial Mode Select SPOL : RS Polarity Select (3-line Serial Interface Mode) - In the 3 or 4-line serial interface mode (P/S="L"), D₀ is assigned to SCL, and D₁ to SDA. - In the 3-line serial interface mode, D₄ is assigned to SPOL. - Serial data on SDA is latched at the rising edge of SCL signal in order of D₇, D₆,... and D₀, and then converted into 8-bit parallel data at the timing of the internal signal produced from the 8th SCL. - SCL should be set to "L" right after data transmission or during non-access.						
90	D ₁ /SDA	I/O							
94	D ₃ /SMODE	I/O							
96	D ₄ /SPOL	I/O							
92, 98, 100,102	D ₂ D ₅ D ₆ D ₇	I/O							
104,106,108, 110,112,114, 116,118	D ₈ D ₉ D ₁₀ D ₁₁ D ₁₂ D ₁₃ D ₁₄ D ₁₅	I/O	8-bit Bi-directional Bus - In the 16-bit bus length mode, D₁₅-D₈ are assigned to upper 8-bit data bus. - In the serial interface mode or the 8-bit parallel interface mode, D₁₅-D₈ should be fixed to "H" or "L".						
43	CSb	I	Chip Select Active "L"						
47	RS	I	Register Select This signal interprets transferred data as display data or instruction. <table border="1"> <thead> <tr> <th>RS</th><th>H</th><th>L</th></tr> </thead> <tbody> <tr> <td>Data</td><td>Instruction</td><td>Display Data</td></tr> </tbody> </table>	RS	H	L	Data	Instruction	Display Data
RS	H	L							
Data	Instruction	Display Data							
79	RD _b (E)	I	80-series MPU Interface (P/S="H", SEL68="L") Data Read (RD_b) Signal - Active "L" 68-series MPU Interface (P/S="H", SEL68="H") Enable Signal - Active "H"						
75	WR _b (R/W)	I	80-series MPU Interface (P/S="H", SEL68="L") Data Write (WR_b) Signal Active "L" 68-series MPU Interface (P/S="H", SEL68="H") Data Read or Write (R/W) Signal <table border="1"> <thead> <tr> <th>R/W</th><th>H</th><th>L</th></tr> </thead> <tbody> <tr> <td>Status</td><td>Read</td><td>Write</td></tr> </tbody> </table>	R/W	H	L	Status	Read	Write
R/W	H	L							
Status	Read	Write							
24	TEST ₁	I	Maker test terminal This terminal must be fixed to "L" in the user's application.						
55	TEST ₂	I	Maker test terminal This terminal must be fixed to "H" in the user's application.						

■ TERMINAL DESCRIPTION 3

No.	Terminal	I/O	Function																		
67	SEL68	I	MPU Mode Select <table border="1"> <tr> <td>SEL86</td><td>H</td><td>L</td></tr> <tr> <td>MPU</td><td>68-series</td><td>80-series</td></tr> </table>	SEL86	H	L	MPU	68-series	80-series												
SEL86	H	L																			
MPU	68-series	80-series																			
63	P/S	I	Parallel/Serial Interface Mode Select <table border="1"> <tr> <th>P/S</th><th>Chip Select</th><th>Display / Instruction</th><th>Data</th><th>Read /Write</th><th>Serial Clock</th></tr> <tr> <td>H</td><td>CSb</td><td>RS</td><td>D₀ ~ D₇</td><td>RDb, WRb</td><td>-</td></tr> <tr> <td>L</td><td>CSb</td><td>RS</td><td>SDA (D₁)</td><td>Write Only</td><td>SCL (D₀)</td></tr> </table> In the serial interface mode (P/S="L"), RDb, WRb, D₂ and D₅-D₁₅ should be fixed to "H" or "L",.	P/S	Chip Select	Display / Instruction	Data	Read /Write	Serial Clock	H	CSb	RS	D ₀ ~ D ₇	RDb, WRb	-	L	CSb	RS	SDA (D ₁)	Write Only	SCL (D ₀)
P/S	Chip Select	Display / Instruction	Data	Read /Write	Serial Clock																
H	CSb	RS	D ₀ ~ D ₇	RDb, WRb	-																
L	CSb	RS	SDA (D ₁)	Write Only	SCL (D ₀)																
124	CL	O	Line Clock CL is normally open.																		
127	FLM	O	First Line Maker FLM is normally open.																		
130	FR	O	Frame Rate FR is normally open.																		
133	CLK	O	Clock Output CLK is normally open.																		
137, 140	OSC1 OSC2	I O	OSC - When the internal oscillator is used, fix OSC1 to "H" or "L" and leave OSC2 open. To attain more accurate frequency, connect OSC1 and OSC2 with an external resistor. - When the internal oscillator is not used, input external clock to OSC1 and leave OSC2 open.																		
331-714	SEG A ₀ ~ SEG A ₁₂₇ SEG B ₀ ~ SEG B ₁₂₇ SEG C ₀ ~ SEG C ₁₂₇	O	Segment Drivers <table border="1"> <tr> <th>REV Register</th><th>OFF</th><th>ON</th></tr> <tr> <td>Normal</td><td>0</td><td>1</td></tr> <tr> <td>Reverse</td><td>1</td><td>0</td></tr> </table> Segment drivers output the following voltage levels. <u>B/W Mode (Example)</u> FR Signal Display Data Reverse Display OFF (Normal) Reverse Display ON V₂, V_{LCD}, V₃, V_{SSH}	REV Register	OFF	ON	Normal	0	1	Reverse	1	0									
REV Register	OFF	ON																			
Normal	0	1																			
Reverse	1	0																			
311-330, 260-308, 246-257, 715-734, 737-785, 2-13	COM ₀ ~ COM ₁₆₁	O	Common Drivers Common drivers output the following voltage levels. <table border="1"> <tr> <th>Data</th><th>FR</th><th>Output Levels</th></tr> <tr> <td>H</td><td>H</td><td>V_{SSH}</td></tr> <tr> <td>L</td><td>H</td><td>V₁</td></tr> <tr> <td>H</td><td>L</td><td>V_{LCD}</td></tr> <tr> <td>L</td><td>L</td><td>V₄</td></tr> </table>	Data	FR	Output Levels	H	H	V _{SSH}	L	H	V ₁	H	L	V _{LCD}	L	L	V ₄			
Data	FR	Output Levels																			
H	H	V _{SSH}																			
L	H	V ₁																			
H	L	V _{LCD}																			
L	L	V ₄																			

NOTE) DUMMY PADs: No. 14, 15, 20-23, 25-29, 33-38, 40-42, 44-46, 48, 49, 53, 54, 56, 57, 61, 62, 64-66, 68, 69, 73, 74, 76-78, 80-82, 86, 87, 89, 91, 93, 95, 97, 99, 101, 103, 105, 107, 109, 111, 113, 115, 117, 119, 123, 125, 126, 128, 129, 131, 132, 134-136, 138, 139, 141, 142, 146, 147, 154, 161, 168, 169, 173, 177-179, 183, 184, 188, 189, 193, 197, 201, 205, 209, 213, 217, 221, 225, 229, 233, 237-241, 245, 258, 259, 309, 310, 735, 736, and 786.

■ FUNCTIONAL DESCRIPTION

(1) MPU INTERFACE

(1-1) Selection of Parallel/Serial Interface Mode

The P/S selects a parallel or a serial interface mode, as shown in Table 1. In the serial interface mode, neither display data in the DDRAM nor instruction data in the registers can be read out.

Table 1 Selection of Parallel/Serial Interface Mode

P/S	I/F Mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D ₇ -D ₀ (D ₁₅ -D ₀)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

NOTE) “-” : Fix to “H” or “L”.

(1-2) Selection of MPU Mode

In the parallel interface mode, the SEL68 selects 68 or 80-series MPU mode, as shown in Table 2.

Table 2 Selection of MPU Mode

SEL68	MPU Mode	CSb	RS	RDb	WRb	Data
H	68-series MPU	CSb	RS	E	R/W	D ₇ -D ₀ (D ₁₅ -D ₀)
L	80-series MPU	CSb	RS	RDb	WRb	D ₇ -D ₀ (D ₁₅ -D ₀)

(1-3) Data Recognition

In the parallel interface mode, the data from MPU is interpreted as display data or instruction according to the combination of the RS, RDb and WRb (R/W) signals, as shown in Table 3.

Table 3 Data Recognition (Parallel Interface Mode)

RS	68-series	80-series		Function
	R/W	RDb	WRb	
H	H	L	H	Read Instruction
H	L	H	L	Write Instruction
L	H	L	H	Read Display Data
L	L	H	L	Write Display Data

(1-4) Selection of 3-/4-line Serial Interface Mode

In the serial interface mode, the SMODE selects 3- or 4-line serial interface mode, as shown in Table 4.

Table 4 Selection of 3-/4-line Serial Interface Mode

SMODE	Serial Interface Mode
H	3-line
L	4-line

(1-5) 4-line Serial Interface Mode

While the chip select is active (CSb=“L”), the SDA and SCL are enabled. While the chip select is inactive (CSb=“H”), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 8-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of D₇, D₆,..., and D₀, and converted into 8-bit parallel data at the timing of the internal signal produced from the 8th SCL signal. The data on the SDA is interpreted as display data or instruction according to the RS.

Table 5 Data Recognition (4-line Serial Interface)

RS	Data Recognition
H	Instruction
L	Display Data

Note that the SCL should be set to “L” right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb=“H”) temporary whenever 8-bit data transmission is completed. Fig 1 illustrates the interface timing of the 4-line serial interface mode.

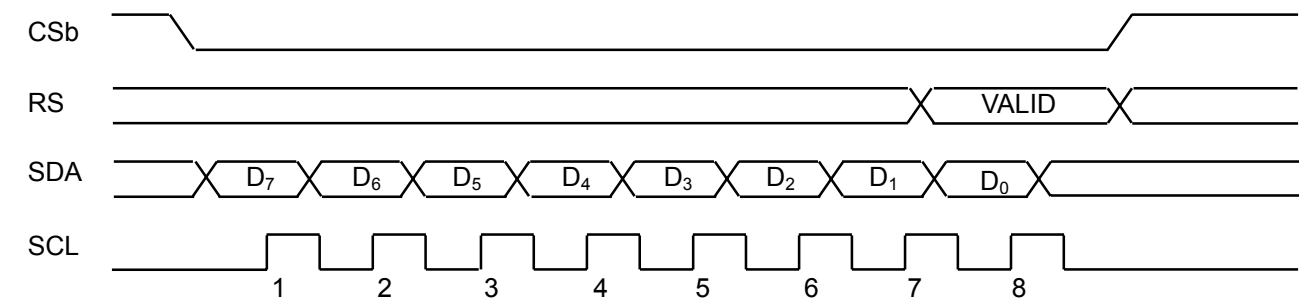


Fig 1 4-line Serial Interface Timing

(1-6) 3-line Serial Interface Mode

While the chip select is active (CSb=“L”), the SDA and SCL are enabled. While the chip select is not active (CSb=“H”), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 9-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of RS, D7, D6,..., and D0, and then converted into 9-bit parallel data at the timing of the internal signal produced from the 9th SCL signal. The data on the SDA is interpreted as display data or instruction according to the combination of the RS bit and the SPOL status, as follows.

Table 6 Data Recognition (3-line Serial Interface)

SPOL=L		SPOL=H	
RS	Data Recognition	RS	Data Recognition
0	Display Data	0	Instruction
1	Instruction	1	Display Data

Note that the SCL should be set to “L” right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb=“H”) temporary whenever 9-bit data transmission is completed. Fig 2 illustrates the interface timing of the 3-line serial interface mode.

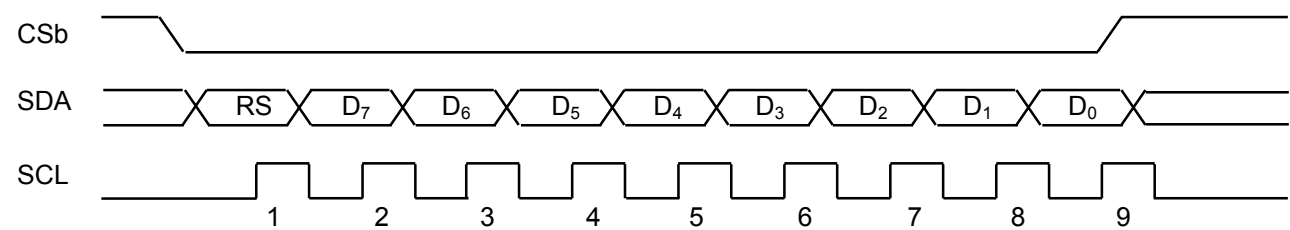


Fig 2 3-line Serial Interface Timing

(1-7) Accessing DDRAM

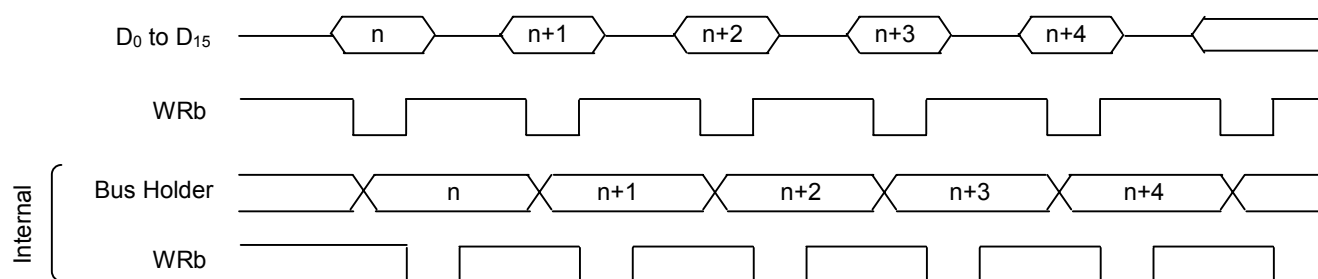
While the chip select is active (CSb="L"), the data from MPU can be written into the DDRAM or the instruction register. When the RS is "L", the data is interpreted as display data which is stored in the DDRAM. The display data is latched at the rising edge of the WRb signal in the 80-series MPU mode, or at the falling edge of the E signal in the 68-series MPU mode.

Table 7 Data Recognition

RS	Data Recognition
L	Display Data
H	Instruction

In the DDRAM read sequence, be sure to execute a dummy read right after setting an address or right after writing display data or instruction. The data from MPU is temporarily held in the internal bus-holder, then released on the internal data-bus, therefore a dummy data is read out by the 1st "Display Data Read" instruction. After that, the display data is read out from a specified address by the 2nd instruction. Note that the "Display Data Read" instruction cannot be used in the serial interface mode.

Display Data Write Operation



Display Data Read Operation

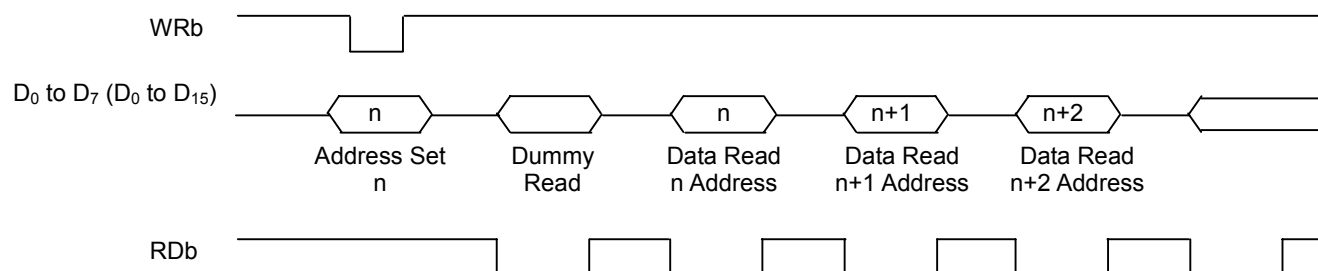


Fig 3 Internal-signal Timing of Display Data Read/Write Operations

NOTE) In 16-bit bus length mode, instruction is transmitted to/from instruction register in 16 bits, as well as display data.

(1-8) Accessing Instruction Register

Each instruction register has a specific address in between (0H) and (FH), and instruction data is read out from the register by the “Register Address” and “Register Read” instructions. For more information, refer to “(14-23) Register Address” and “(14-24) Register Read”.

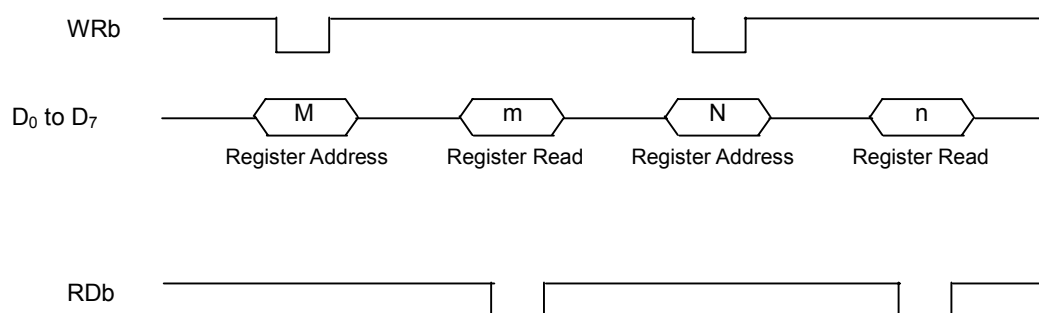


Fig 4 Access Timing of Instruction Register

(1-9) Selection of 8-/16-bit Bus Length (Parallel Interface Mode)

Either 8- or 16-bit bus length is selected by the D₀ (WLS) bit of the “Bus Length” instruction. In the 16-bit bus length mode, instruction as well as display data is transmitted to/from the instruction registers in 16 bits (D₁₅ to D₀). However, only lower 8 bits (D₇ to D₀) are valid for instruction register access. And only 12 bits are actually stored in the DDRAM, even though entire 16 bits (D₁₅ to D₀) are transmitted for DDRAM access. For more information, refer to “(4-4) Bit Assignment of Display Data”.

Table 8 Selection of 8-/16-bit Bus Length Mode

WLS	Bus Length Mode
L	8-bit Bus Length
H	16-bit Bus Length

(2) INITIAL DISPLAY LINE REGISTER

The address data in the initial display line register specifies the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. The initial COM is the start position of common scanning, which is specified by the “Initial COM” instruction.

The row address, which is established in the initial display line register, is preset into the line counter whenever the FLM becomes “H”. At the rising edge of the CL signal, the line counter is counted-up, then 384-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit to decide a grayscale level, then the segment drivers A_i, B_i and C_i (i=0 to 127) generate LCD waveforms.

(3) COLUMN AND ROW ADDRESS COUNTERS

The column and row address counters designate a column address and a row address respectively for DDRAM access, but they are completely independent from the line counter. The line counter provides a line address which is synchronized with display control timings such as the FLM and the CL.

(4) DDRAM

(4-1) DDRAM Address Range

The DDRAM is capable of 162 bits for row address and 1,536 bits (12-bit x 128-segment) for column address. The range of the column address is varied depending on the settings as follows, and the row address is from (00H) to (A1H). Setting outside these ranges is not allowed, otherwise it may cause malfunctions. For DDRAM access, two data transmissions are needed for 1 RGB-pixel in the 8-bit bus length mode, and one transmission in the 16-bit bus length mode.

8-bit Bus Length

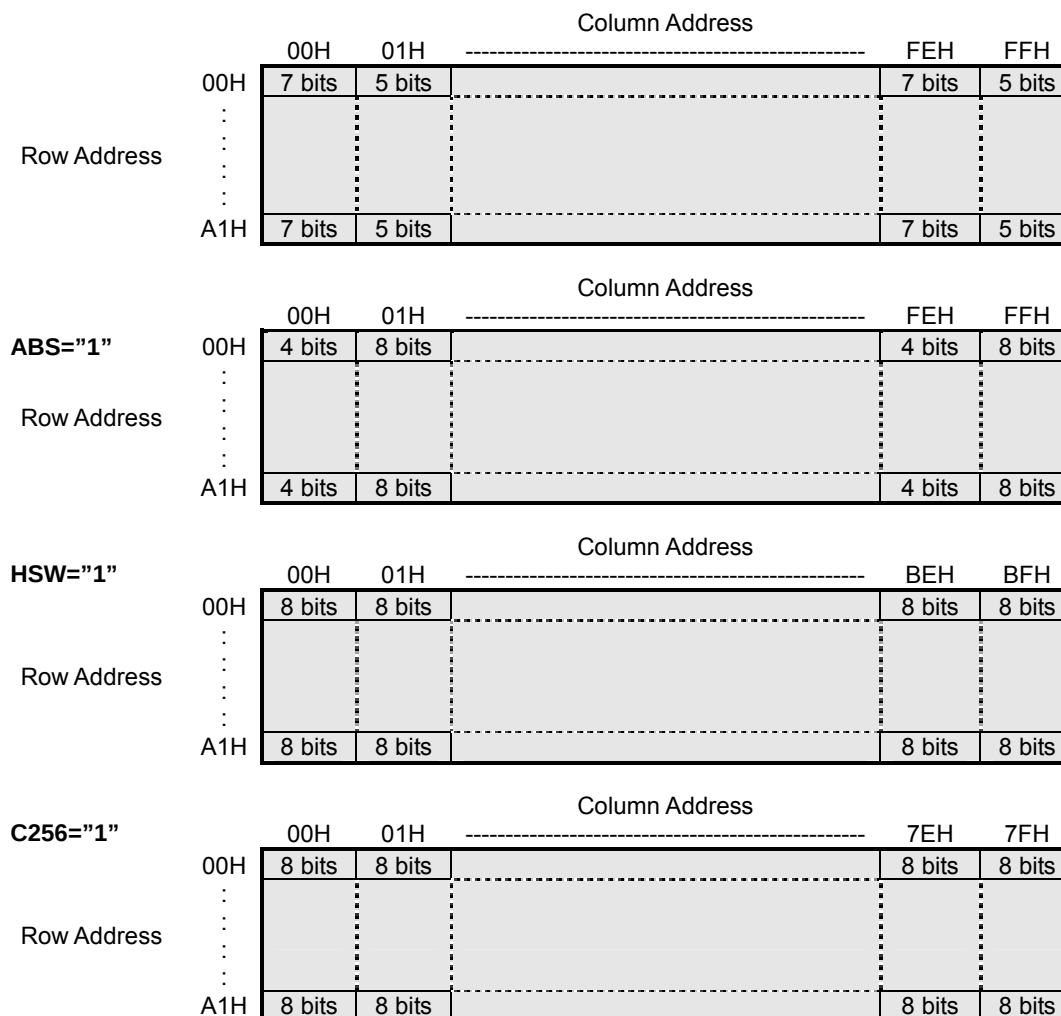


Fig 5 Range of Column Address in 8-bit Bus Length

16-bit Bus Length

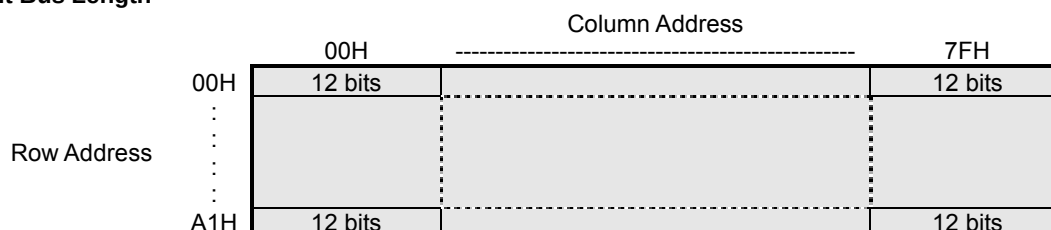


Fig 6 Range of Column Address in 16-bit Bus Length

(4-2) Window Area for DDRAM Access

In addition to the normal DDRAM access discussed previously, the window area access can be used. This area is set by the “Increment Control” instruction and the designation of the start point and the end point.

By the “Increment Control”, auto-increment is set for column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up, whenever the DDRAM is accessed. And, the start point is specified by the “Column Address” and “Row Address” instructions, and the end point by the “Window End Column Address” and “Window End Row Address” instructions. For more information, refer to “(14-9) Increment Control”, “(14-25) Window End Column Address” and “(14-26) Window End Row Address”. The typical sequence of the window area setting is listed below.

1. Set “1” at D₃ (WIN), D₁ (AYI) and D₀ (AXI) of “Increment Control” instruction.
2. Set start point by “Column Address” and “Row Address” instructions.
3. Set end point by “Window End Column Address” and “Window End Row Address” instructions.
4. Window area is set up, and DDRAM can be accessed.

NOTE) The order of address setting is column address first, then row address.

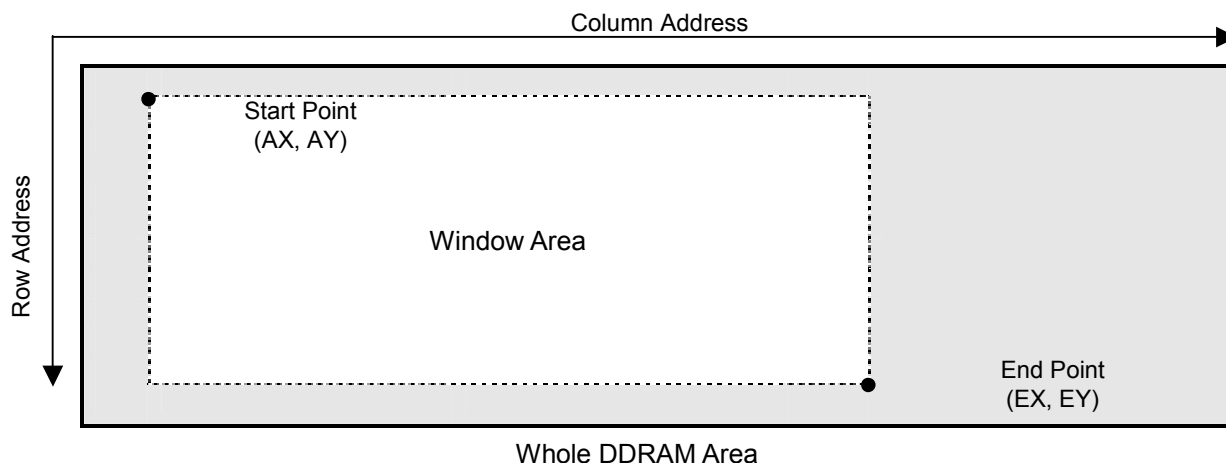
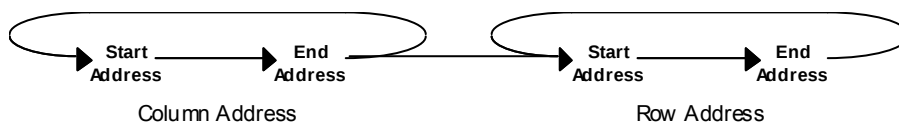


Fig 7 Window Area

NOTE1) The following relation should be maintained to avoid malfunctions.

- AX (Window Start Column Address) < EX (Window End Column Address) < Maximum Column Address
- AY (Window Start Row Address) < EY (Window End Row Address) < Maximum Row Address

NOTE3) Auto-increment in the window area



NOTE2) A read-modify-write operation is enabled by setting “1” at the D₂ (AIM) of the “Increment Control” instruction. Refer to the description about “AIM” bit in “(14-9) Increment Control”.

(4-3) Segment Direction

The DDRAM access direction is controlled by the D₀ (REF) bit of the “Display Control (2)” instruction. This function is used to reverse the segment direction for reducing the restrictions on the IC position of an LCD module.

(4-4) Bit Assignment of Display Data

(4-4-1) Bit Assignment Overview

These maps is used for grasping general outlines of the variations in the bit assignment of display data.

Table 9-1 RAM MAP 1 (Variable 16-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

Mode	WLS	ABS	HSW	REF	C256	SEG ₀						SEG ₁						SEG ₁₂₆						SEG ₁₂₇																													
						Palette A		Palette B		Palette C		Palette A		Palette B		Palette C		Palette A		Palette B		Palette C		Palette A		Palette B		Palette C		Palette A		Palette B		Palette C																			
						A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀												
	1	0	x	0	0	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₈	D ₇	D ₆	D ₄	D ₃	D ₂	D ₁	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₈	D ₇	D ₆	D ₄	D ₃	D ₂	D ₁	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₈	D ₇	D ₆	D ₄	D ₃	D ₂	D ₁	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₈	D ₇	D ₆	D ₄	D ₃	D ₂	D ₁
	1	0	x	1	0	X=7FH						X=7EH						X=01H						X=00H																													
						D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₈	D ₇	D ₆	D ₄	D ₃	D ₂	D ₁	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₈	D ₇	D ₆	D ₄	D ₃	D ₂	D ₁	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₈	D ₇	D ₆	D ₄	D ₃	D ₂	D ₁	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₈	D ₇	D ₆	D ₄	D ₃	D ₂	D ₁
	1	1	x	0	0	D ₁₁	D ₁₀	D ₉	D ₈	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₁	D ₁₀	D ₉	D ₈	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₁	D ₁₀	D ₉	D ₈	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₁	D ₁₀	D ₉	D ₈	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
	1	1	x	1	0	D ₁₁	D ₁₀	D ₉	D ₈	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₁	D ₁₀	D ₉	D ₈	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₁	D ₁₀	D ₉	D ₈	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₁	D ₁₀	D ₉	D ₈	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
	0	0	0	0	0	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
	0	0	0	1	0	X=FEH						X=FFH						X=02H						X=03H						X=FDH						X=00H						X=01H											
	0	0	0	0	0	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
	0	1	0	0	0	X=00H						X=01H						X=02H						X=03H						X=FDH						X=FEH						X=FFH											
	0	1	0	0	0	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
	0	1	0	1	0	X=FEH						X=FFH						X=02H						X=03H						X=FDH						X=FEH						X=01H											
	0	1	0	1	0	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
	0	x	1	0	0	X=00H						X=01H						X=BDH						X=BEH						X=BFH						X=00H						X=01H											
	0	x	1	1	0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
	0	x	1	1	0	X=BEH(L)						X=BFH						X=BDH						X=BEH(H)						X=00H						X=01H(H)																	
	0	x	1	1	0	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

Table 9-2 RAM MAP 2 (Variable 8-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

[illegible]

Table 10 SWAP

		Palette A				Palette B				Palette C			
SWAP		A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀
0	0	SEGAx				SEGBx				SEGCx			
1	1	SEGAx				SEGBx				SEGCx			
0	1	SEGCx				SEGBx				SEGAx			
1	0	SEGCx				SEGBx				SEGAx			

NOTE1) On the RAM MAP 2, A₀, B₀, C₁ and C₀ bits are fixed to "1".

NOTE2) The functions of the variable 8-grayscale mode are different from those of the fixed 8-grayscale mode.

NOTE3) The contents of the DDRAM at "C256=0" are not compatible with the contents at "C256=1".

NOTE4) "C256=1" can be used in the 8-bit bus length mode, but not in the 16-bit bus length mode.

(4-4-2) Bit Assignment in Variable 16-grayscale Mode

16-bit Bus Length (MON=0, PWM=0, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																									
*	0	0	0	X=00H												↔		X=7FH											
*	0	1	1	X=7FH												↔		X=00H											
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↔		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
Grayscale Palette				Palette A				Palette B				Palette C				↔		Palette A				Palette B				Palette C			
Segment Driver				SEGA ₀				SEGB ₀				SEGC ₀				↔		SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																									
*	0	0	1	X=00H												↔		X=7FH											
*	0	1	0	X=7FH												↔		X=00H											
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↔		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
Grayscale Palette				Palette A				Palette B				Palette C				↔		Palette A				Palette B				Palette C			
Segment Driver				SEGC ₀				SEGB ₀				SEGA ₀				↔		SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																									
*	1	0	0	X=00H												↔		X=7FH											
*	1	1	1	X=7FH												↔		X=00H											
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette				Palette A				Palette B				Palette C				↔		Palette A				Palette B				Palette C			
Segment Driver				SEGA ₀				SEGB ₀				SEGC ₀				↔		SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																									
*	1	0	1	X=00H												↔		X=7FH											
*	1	1	0	X=7FH												↔		X=00H											
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette				Palette A				Palette B				Palette C				↔		Palette A				Palette B				Palette C			
Segment Driver				SEGC ₀				SEGB ₀				SEGA ₀				↔		SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

8-bit Bus Length (MON=0, PWM=0, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
0	0	0	0	X=00H				X=01H				←→				X=FEH			
0	0	1	1	X=FEH				X=FFH				←→				X=00H			
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				←→				←→				←→				←→			
				←→				←→				←→				←→			
Grayscale Palette				Palette A				Palette B				Palette C				←→			
Segment Driver				SEGA ₀				SEGB ₀				SEGC ₀				←→			
																SEGA ₁₂₇			
																SEGB ₁₂₇			
																SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
0	0	0	1	X=00H				X=01H				←→				X=FEH			
0	0	1	0	X=FEH				X=FFH				←→				X=00H			
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				←→				←→				←→				←→			
				←→				←→				←→				←→			
Grayscale Palette				Palette A				Palette B				Palette C				←→			
Segment Driver				SEGC ₀				SEGB ₀				SEGA ₀				←→			
																SEGC ₁₂₇			
																SEGB ₁₂₇			
																SEGA ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
0	1	0	0	X=00H				X=01H				←→				X=FEH			
0	1	1	1	X=FEH				X=FFH				←→				X=00H			
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄
				←→				←→				←→				←→			
				←→				←→				←→				←→			
Grayscale Palette				Palette A				Palette B				Palette C				←→			
Segment Driver				SEGA ₀				SEGB ₀				SEGC ₀				←→			
																SEGA ₁₂₇			
																SEGB ₁₂₇			
																SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
0	1	0	1	X=00H				X=01H				←→				X=FEH			
0	1	1	0	X=FEH				X=FFH				←→				X=00H			
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄
				←→				←→				←→				←→			
				←→				←→				←→				←→			
Grayscale Palette				Palette A				Palette B				Palette C				←→			
Segment Driver				SEGC ₀				SEGB ₀				SEGA ₀				←→			
																SEGC ₁₂₇			
																SEGB ₁₂₇			
																SEGA ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	0	0	X=00H								X=01H								X=02H								..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	..			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				...			

Column Address / Display Data / Segment Driver																												
...	X=BDH								X=BEH								X=BFH											
..	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C							
...	SEGA ₁₂₆				SEGB ₁₂₆				SEGC ₁₂₆				SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	0	1	X=00H								X=01H								X=02H								..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	..			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGC ₀				SEGB ₀				SEGA ₀				SEGC ₁				SEGB ₁				SEGA ₁				...			

Column Address / Display Data / Segment Driver																												
...	X=BDH								X=BEH								X=BFH											
..	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C							
...	SEGC ₁₂₆				SEGB ₁₂₆				SEGA ₁₂₆				SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
1	*	1	0	X=BEH				X=BFH								X=BDH								X=BEH				..
Display Data in DDRAM Grayscale Palette Segment Driver				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	..
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...
				SEGC ₀				SEGB ₀				SEGA ₀				SEGC ₁				SEGB ₁				SEGA ₁				...

Column Address / Display Data / Segment Driver																												
...	X=01H				X=02H								X=00H								X=01H							
..	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄				
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C							
...	SEGC ₁₂₆				SEGB ₁₂₆				SEGA ₁₂₆				SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	1	1	X=BEH				X=BFH								X=BDH								X=BEH				..			
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	...			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				...			

Column Address / Display Data / Segment Driver																												
...	X=01H				X=02H								X=00H								X=01H							
..	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄				
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C							
...	SEGA ₁₂₆				SEGB ₁₂₆				SEGC ₁₂₆				SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇							

(4-4-3) Bit Assignment in Variable 8-level Gradation Mode

8-bit Bus Length (MON=0, PWM=0, C256=1, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																
*	*	0	0	X=00H								↔	X=7FH							
*	*	1	1	X=7FH								↔	X=00H							
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
				SEGA ₀			SEGB ₀			SEGC ₀		↔	SEGA ₁₂₇			SEGB ₁₂₇			SEGC ₁₂₇	

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	1	X=00H								↔	X=7FH								
*	*	1	0	X=7FH								↔	X=00H								
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C		
				SEGC ₀			SEGB ₀			SEGA ₀		↔	SEGC ₁₂₇			SEGB ₁₂₇			SEGA ₁₂₇		

(4-4-4) Bit Assignment in Fixed 8-level Gradation Mode

16-bit Bus Length (MON=0, PWM=1, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
*	0	0	0	X=00H														↔		X=7FH											
*	0	1	1	X=7FH														↔		X=00H											
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁		
				Palette A				Palette B				Palette C				↔		Palette A				Palette B				Palette C					
				SEGA ₀				SEGB ₀				SEGC ₀				↔		SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇					

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	0	0	1	X=00H												↔	X=7FH											
*	0	1	0	X=7FH												↔	X=00H											
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	1	0	0	X=00H												↔	X=7FH											
*	1	1	1	X=7FH												↔	X=00H											
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																												
*	1	0	1	X=00H														↔	X=7FH													
*	1	1	0	X=7FH														↔	X=00H													
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C							
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇							

NOTE) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length (MON=0, PWM=1, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver							
0	0	0	0	X=00H		X=01H		↔	X=FEH		X=FFH
0	0	1	1	X=FEH		X=FFH		↔	X=00H		X=01H
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette				Palette A		Palette B		↔	Palette A		Palette B
Segment Driver				SEGA ₀		SEGB ₀		↔	SEGA ₁₂₇		SEGB ₁₂₇

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver							
0	0	0	1	X=00H		X=01H		↔	X=FEH		X=FFH
0	0	1	0	X=FEH		X=FFH		↔	X=00H		X=01H
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette				Palette A		Palette B		↔	Palette A		Palette B
Segment Driver				SEGC ₀		SEGB ₀		↔	SEGC ₁₂₇		SEGB ₁₂₇

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver							
0	1	0	0	X=00H		X=01H		↔	X=FEH		X=FFH
0	1	1	1	X=FEH		X=FFH		↔	X=00H		X=01H
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄
Grayscale Palette				Palette A		Palette B		↔	Palette A		Palette B
Segment Driver				SEGA ₀		SEGB ₀		↔	SEGA ₁₂₇		SEGB ₁₂₇

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver							
0	1	0	1	X=00H		X=01H		↔	X=FEH		X=FFH
0	1	1	0	X=FEH		X=FFH		↔	X=00H		X=01H
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄
Grayscale Palette				Palette A		Palette B		↔	Palette A		Palette B
Segment Driver				SEGC ₀		SEGB ₀		↔	SEGC ₁₂₇		SEGB ₁₂₇

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	0	0	X=00H								X=01H								X=02H								..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	..			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				...			

Column Address / Display Data / Segment Driver																											
...	X=BDH								X=BEH								X=BFH										
...	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀			
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C						
...	SEGA ₁₂₆				SEGB ₁₂₆				SEGC ₁₂₆				SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇						

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	0	1	X=00H								X=01H								X=02H								..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	..			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGC ₀				SEGB ₀				SEGA ₀				SEGC ₁				SEGB ₁				SEGA ₁				...			

Column Address / Display Data / Segment Driver																											
...	X=BDH								X=BEH								X=BFH										
...	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀			
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C						
...	SEGC ₁₂₆				SEGB ₁₂₆				SEGA ₁₂₆				SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇						

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																												
1	*	1	0	X=BEH				X=BFH								X=BDH								X=BEH				..				
Display Data in DDRAM Grayscale Palette Segment Driver				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄	..
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...				
				SEGC ₀				SEGB ₀				SEGA ₀				SEGC ₁				SEGB ₁				SEGA ₁				...				

Column Address / Display Data / Segment Driver																									
...	X=01H				X=02H								X=00H								X=01H				
...	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
...	SEGC ₁₂₆				SEGB ₁₂₆				SEGA ₁₂₆				SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇				

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	1	1	X=BEH				X=BFH								X=BDH								X=BEH				..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	...			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				...			

Column Address / Display Data / Segment Driver																									
...	X=01H				X=02H								X=00H								X=01H				
...	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
...	SEGA ₁₂₆				SEGB ₁₂₆				SEGC ₁₂₆				SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇				

8-bit Bus Length (MON=0, PWM=1, C256=1, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																
*	*	0	0	X=00H								↔	X=7FH							
*	*	1	1	X=7FH								↔	X=00H							
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
				SEGA ₀			SEGB ₀			SEGC ₀		↔	SEGA ₁₂₇			SEGB ₁₂₇			SEGC ₁₂₇	

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																
*	*	0	1	X=00H								↔	X=7FH							
*	*	1	0	X=7FH								↔	X=00H							
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
				SEGC ₀			SEGB ₀			SEGA ₀		↔	SEGC ₁₂₇			SEGB ₁₂₇			SEGA ₁₂₇	

(4-4-5) Bit Assignment in B&W Mode

16-bit Bus Length (MON=1, PWM=*, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
*	0	0	0	X=00H						X=7FH					
*	0	1	1	X=7FH						X=00H					
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
Grayscale Palette				Palette A			Palette B			Palette C			Palette A		
Segment Driver				SEGA ₀			SEGB ₀			SEGC ₀			SEGA ₁₂₇		

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
*	0	0	1	X=00H						X=7FH					
*	0	1	0	X=7FH						X=00H					
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
Grayscale Palette				Palette A			Palette B			Palette C			Palette A		
Segment Driver				SEGC ₀			SEGB ₀			SEGA ₀			SEGC ₁₂₇		

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
*	1	0	0	X=00H						X=7FH					
*	1	1	1	X=7FH						X=00H					
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette				Palette A			Palette B			Palette C			Palette A		
Segment Driver				SEGA ₀			SEGB ₀			SEGC ₀			SEGA ₁₂₇		

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
*	1	0	1	X=00H						X=7FH					
*	1	1	0	X=7FH						X=00H					
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette				Palette A			Palette B			Palette C			Palette A		
Segment Driver				SEGC ₀			SEGB ₀			SEGA ₀			SEGC ₁₂₇		

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
0	0	0	0	X=00H				X=01H		↔	X=FEH				X=FFH													
0	0	1	1	X=FEH				X=FFH		↔	X=00H				X=01H													
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																					
0	0	0	1	X=00H				X=01H		↔	X=FEH				X=FFH										
0	0	1	0	X=FEH				X=FFH		↔	X=00H				X=01H										
Display Data in DDRAM				D ₇		D ₆		D ₅		D ₄		↔		D ₇		D ₆		D ₅		D ₄					
				D ₂		D ₁		D ₀		D ₇		D ₄		D ₃		D ₂		D ₁		D ₀					
				D ₇		D ₆		D ₅		D ₄		D ₂		D ₁		D ₀		D ₇		D ₄					
Grayscale Palette				Palette A				Palette B				↔		Palette A				Palette B				Palette C			
Segment Driver				SEGC ₀				SEGB ₀				↔		SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																
0	1	0	0	X=00H	X=01H			↔	X=FEH	X=FFH										
0	1	1	1	X=FEH	X=FFH			↔	X=00H	X=01H										
Display Data in DDRAM				D ³	D ²	D ¹	D ⁰	↔	D ³	D ²	D ¹	D ⁰	D ⁷	D ⁶	D ⁵	D ⁴	D ³	D ²	D ¹	D ⁰
				Palette A		Palette B			↔	Palette A		Palette B		Palette C						
				SEGA ₀		SEGB ₀			↔	SEGA ₁₂₇		SEGB ₁₂₇		SEGC ₁₂₇						

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
0	1	0	1	X=00H		X=01H		↔	X=FEH		X=FFH										
0	1	1	0	X=FEH		X=FFH		↔	X=00H		X=01H										
Display Data in DDRAM												↔									
				Palette A		Palette B		Palette C		↔		Palette A		Palette B		Palette C					
				SEGC ₀		SEGB ₀		SEGA ₀		↔		SEGC ₁₂₇		SEGB ₁₂₇		SEGA ₁₂₇					

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
1	*	0	0	X=00H				X=01H				X=02H			
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄
Grayscale Palette Segment Driver				Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
				SEGA ₀	SEGB ₀	SEGC ₀	SEGA ₁	SEGB ₁	SEGC ₁	SEGA ₂	SEGB ₂	SEGC ₂	SEGA ₃	SEGB ₃	SEGC ₃

Column Address / Display Data / Segment Driver											
X=BDH				X=BEH				X=BFH			
D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄
Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
SEGA ₁₂₆	SEGB ₁₂₆	SEGC ₁₂₆	SEGA ₁₂₇	SEGB ₁₂₇	SEGC ₁₂₇	SEGA ₁₂₈	SEGB ₁₂₈	SEGC ₁₂₈	SEGA ₁₂₉	SEGB ₁₂₉	SEGC ₁₂₉

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
1	*	0	1	X=00H				X=01H				X=02H			
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄
Grayscale Palette Segment Driver				Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
				SEGC ₀	SEGB ₀	SEGA ₀	SEGC ₁	SEGB ₁	SEGA ₁	SEGC ₂	SEGB ₂	SEGA ₂	SEGC ₃	SEGB ₃	SEGA ₃

Column Address / Display Data / Segment Driver											
X=BDH				X=BEH				X=BFH			
D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄
Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
SEGC ₁₂₆	SEGB ₁₂₆	SEGA ₁₂₆	SEGC ₁₂₇	SEGB ₁₂₇	SEGA ₁₂₇	SEGC ₁₂₈	SEGB ₁₂₈	SEGA ₁₂₈	SEGC ₁₂₉	SEGB ₁₂₉	SEGA ₁₂₉

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
1	*	1	0	X=BEH			X=BFH			X=BDH			X=BEH		
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁
Grayscale Palette Segment Driver				Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
				SEGC ₀	SEGB ₀	SEGA ₀	SEGC ₁	SEGB ₁	SEGA ₁	SEGC ₂	SEGB ₂	SEGA ₂	SEGC ₃	SEGB ₃	SEGA ₃

Column Address / Display Data / Segment Driver											
X=01H			X=02H			X=00H			X=01H		
D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁
Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
SEGC ₁₂₆	SEGB ₁₂₆	SEGA ₁₂₆	SEGC ₁₂₇	SEGB ₁₂₇	SEGA ₁₂₇	SEGC ₁₂₈	SEGB ₁₂₈	SEGA ₁₂₈	SEGC ₁₂₉	SEGB ₁₂₉	SEGA ₁₂₉

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
1	*	1	1	X=BEH			X=BFH			X=BDH			X=BEH		
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁
Grayscale Palette Segment Driver				Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
				SEGA ₀	SEGB ₀	SEGC ₀	SEGA ₁	SEGB ₁	SEGC ₁	SEGA ₂	SEGB ₂	SEGC ₂	SEGA ₃	SEGB ₃	SEGC ₃

Column Address / Display Data / Segment Driver											
X=01H			X=02H			X=00H			X=01H		
D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁
Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
SEGA ₁₂₆	SEGB ₁₂₆	SEGC ₁₂₆	SEGA ₁₂₇	SEGB ₁₂₇	SEGC ₁₂₇	SEGA ₁₂₈	SEGB ₁₂₈	SEGC ₁₂₈	SEGA ₁₂₉	SEGB ₁₂₉	SEGC ₁₂₉

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=1, WLS=0)

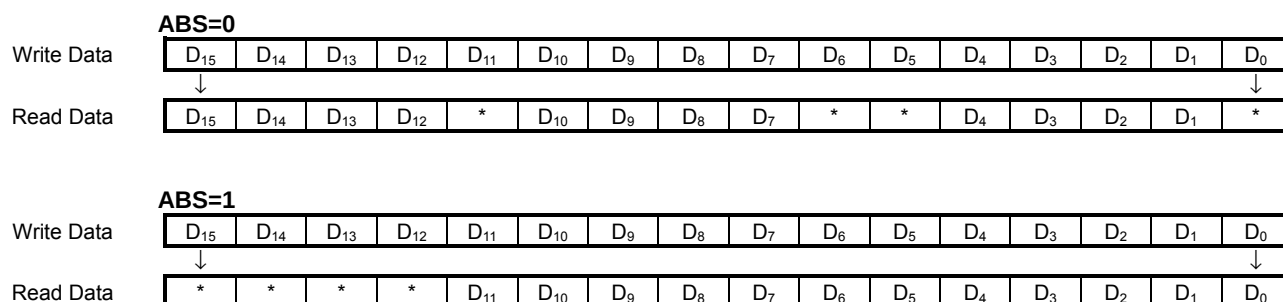
HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																
*	*	0	0	X=00H						↔	X=7FH									
*	*	1	1	X=7FH						↔	X=00H									
Display Data in DDRAM				D₇			D₄			D₁		↔	D₇			D₄			D₁	
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
				SEGA ₀			SEGB ₀			SEGC ₀		↔	SEGA ₁₂₇			SEGB ₁₂₇			SEGC ₁₂₇	

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	1	X=00H						↔	X=7FH										
*	*	1	0	X=7FH						↔	X=00H										
Display Data in DDRAM				D₇			D₄			D₁		↔	D₇			D₄			D₁		D ₀
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C		
				SEGC ₀			SEGB ₀			SEGA ₀		↔	SEGC ₁₂₇			SEGB ₁₂₇			SEGA ₁₂₇		

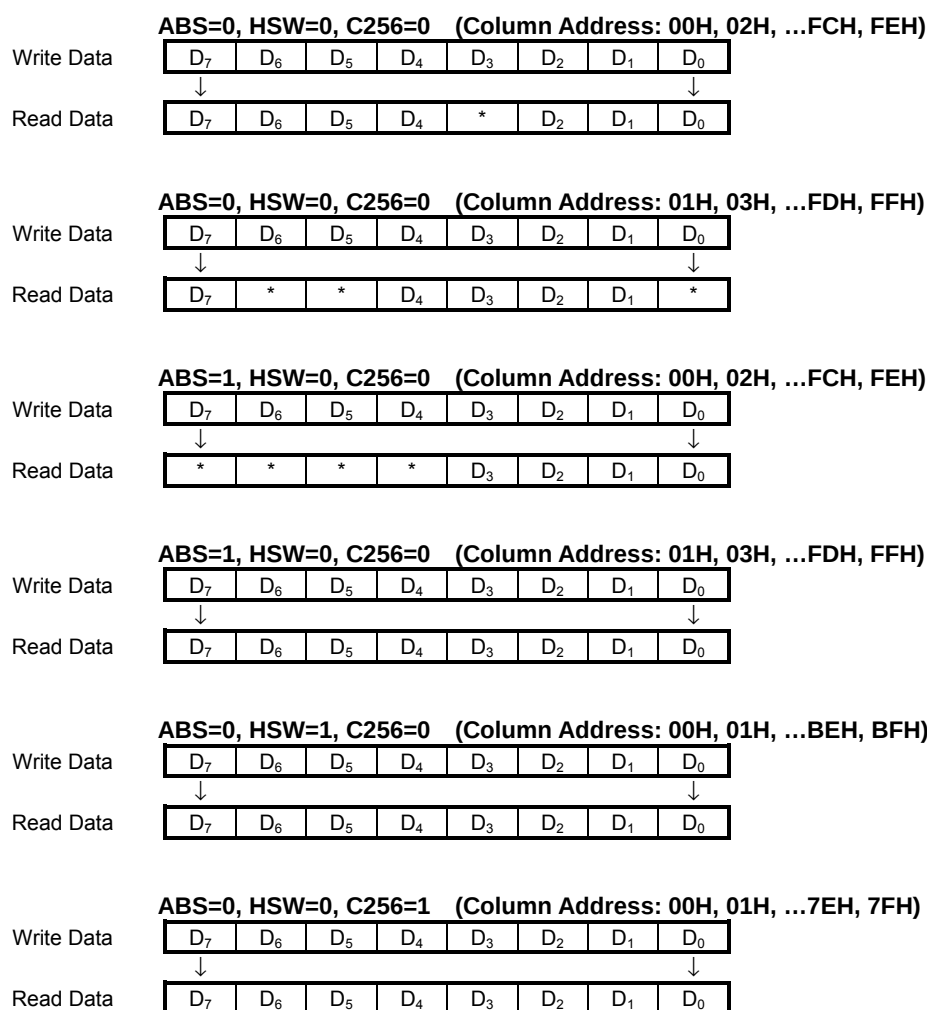
NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

(4-5) Write Data and Read Data

16-bit Bus Length



8-bit Bus Length



NOTE) * : Invalid Data

(5) GRAYSCALE CONTROL CIRCUIT

(5-1) Display Mode Selection

A display mode is selected by the combination of the D₂ (MON) bit of the “Display Control (1)” instruction and the D₃ (PWM) and D₂ (C256) bits of the “Display Mode Control” instruction, as shown below.

Table 11 Display Mode Selection

MON	PWM	C256 (NOTE1)	Display Mode		Bus Length		Oscillation (NOTE2)
0	0	0	Variable 16-grayscale Mode	4096 Colors	8-/16-bit	(WLS=0/1)	f _{osc1}
		1	Variable 8-grayscale Mode	256 Colors	8-bit	(WLS=0)	
	1	0	Fixed 8-grayscale Mode	256 Colors	8-/16-bit	(WLS=0/1)	f _{osc2}
		1			8-bit	(WLS=0)	
1	*	0	B&W Mode	Black & White	8-/16-bit	(WLS=0/1)	f _{osc3}
		1			8-bit	(WLS=0)	

NOTE1) In the variable grayscale mode, “C256” bit selects either 16-grayscale (4K colors) or 8-grayscale (256 colors). When C256=“0” (16-grayscale), all 12 bits are assigned to 1 RGB-pixel. When C256=“1” (8-grayscale), only 8 bits are assigned and the 8-bit bus length should be used. In the fixed 8-grayscale mode or the B&W mode, the “C256” bit is usually “1”. For more information how the display data is assigned, refer to “(4-4) Bit Assignment of Display Data”.

NOTE2) Oscillation frequency is decided according to the display mode, and is fine-tuned by the “Frequency Control” Instruction. Refer to “(10) OSCILLATOR” and “OSCILLATION FREQUENCY AND FRAME FREQUENCY”.

(5-1-1) Variable 16-grayscale Mode

In this mode, each of the palettes A_j, B_j and C_j (j=0-15) is capable of selecting 16 from 32 grayscales (0/31-31/31) by setting palette data in the grayscale palette. Then, each of the segment drivers SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0 to 127) generates 16 grayscales to achieve 4,096 colors. Refer to Table 12-1 and Table 12-2.

(5-1-2) Variable 8-grayscale Mode

Each of the palettes A_j, B_j and C_j (j=0-15) is capable of selecting 8 from 32 grayscales (0/31-31/31). 2 segment drivers of 1 RGB-group (SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0 to 127)) generate 8 grayscales, and the other driver does 4 grayscales to achieve 256 colors. Refer to Table 13-1 through Table 13-4. The 8-bit bus length is usually used in this mode.

(5-1-3) Fixed 8-grayscale Mode

The palette setting is not necessary, because the palettes A_j, B_j and C_j (j=0-15) are always fixed at 4 or 8 grayscales between 0/7 and 7/7. 2 segment drivers of 1 RGB-group (SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0 to 127)) are fixed at 8 grayscales, and the other driver is 4 grayscales, then results in 256 colors. Refer to Table 14-1 and Table 14-2.

(5-1-4) B&W Mode

The palette setting is not necessary, where the only MSB bits of display data are valid. Refer to Table 15.

(6) GRAYSCALE PALETTE

(6-1) Grayscale Selection in Variable 16-grayscale Mode

Table 12-1 Grayscale selection

(Palette Aj, Bj, and Cj)

Display Data MSB----LSB	Palette Name
0 0 0 0	Palette A0/B0/C0
0 0 0 1	Palette A1/B1/C1
0 0 1 0	Palette A2/B2/C2
0 0 1 1	Palette A3/B3/C3
0 1 0 0	Palette A4/B4/C4
0 1 0 1	Palette A5/B5/C5
0 1 1 0	Palette A6/B6/C6
0 1 1 1	Palette A7/B7/C7
1 0 0 0	Palette A8/B8/C8
1 0 0 1	Palette A9/B9/C9
1 0 1 0	Palette A10/B10/C10
1 0 1 1	Palette A11/B11/C11
1 1 0 0	Palette A12/B12/C12
1 1 0 1	Palette A13/B13/C13
1 1 1 0	Palette A14/B14/C14
1 1 1 1	Palette A15/B15/C15

Table 12-2 Grayscale Palette

(Palette Aj, Bj, and Cj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0	Palette A0/B0/C0	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette A8/B8/C8
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette A2/B2/C2	1 0 1 0 1	21/31	Palette A10/B10/C10
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette A4/B4/C4	1 1 0 0 1	25/31	Palette A12/B12/C12
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette A6/B6/C6	1 1 1 0 1	29/31	Palette A14/B14/C14
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=0"

NOTE2) Applied to palette Aj, Bj and Cj (j=0 to 15)

(6-2) Grayscale Selection in Variable 8-grayscale Mode

Table 13-1 Grayscale selection

(Palette Aj and Bj)

Display Data MSB---LSB	Palette Name
0 0 0 *	Palette A1/B1/C1
0 0 1 *	Palette A3/B3/C3
0 1 0 *	Palette A5/B5/C5
0 1 1 *	Palette A7/B7/C7
1 0 0 *	Palette A9/B9/C9
1 0 1 *	Palette A11/B11/C11
1 1 0 *	Palette A13/B13/C13
1 1 1 *	Palette A15/B15/C15

Table 13-2 Grayscale Palette

(Palette Aj and Bj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0		1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=1".

NOTE2) Applied to palette Aj and Bj (j=0 to 15)

NOTE3) Palette 0, 2, 4, 6, 8, 10, 12 and 14 are disabled.

Table 13-3 Grayscale selection

(Palette Cj)

Display Data MSB---LSB	Palette Name
0 0 **	Palette A3/B3/C3
0 1 **	Palette A7/B7/C7
1 0 **	Palette A11/B11/C11
1 1 **	Palette A15/B15/C15

Table 13-4 Grayscale Palette

(Palette Cj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0		1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=1"

NOTE2) Applied to palette Cj (j=0 to 15)

NOTE3) Palette 0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13 and 14 are disabled.

(6-3) Grayscale Selection in Fixed 8-grayscale Mode

Table 14-1 Grayscale Selection

(Palette Aj and Bj)

Display Data MSB- - - -LSB	Grayscale
0 0 0 *	0/7
0 0 1 *	1/7
0 1 0 *	2/7
0 1 1 *	3/7
1 0 0 *	4/7
1 0 1 *	5/7
1 1 0 *	6/7
1 1 1 *	7/7

Table 14-2 Grayscale Palette

(Palette Cj)

Display Data MSB- - - -LSB	Grayscale
0 0 **	0/7
0 1 **	3/7
1 0 **	5/7
1 1 **	7/7

NOTE1) "MON=0", "PWM=1", "C256=0 or 1"

(6-4) Grayscale Selection in B&W Mode

Table 15 Grayscale Selection

Display Data MSB- - - -LSB	Grayscale
0 ***	0
1 ***	1

NOTE1) "MON=1", "PWM=0 or 1" and "C256=0 or 1"

(7) DISPLAY TIMING GENERATOR

The display timing generator generates timing clocks such as the CL (Line Clock), FR (Frame Rate) and FLM (First Line Maker) by dividing an oscillation frequency. These clocks are used inside the LSI, and are activated by setting “1” at the D₀ (SON) bit of the “Duty-1 /Display Clock ON/OFF” instruction.

The CL is used for the line counter and the data latch circuit. At the rising edge of the CL signal, the line counter is counted up, then 384-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit, then segment drivers A_i, B_i and C_i (i=0 to 127) produce LCD driving waveforms. The internal data-transmission timing between the DDRAM and segment drivers is completely independent of external data-transmission timing, so that MPU makes access to the LSI without concern for the LSI's internal operation.

The FR and FLM are generated by the CL. The FR toggles once every frame in the default status, and is programmed to toggle once every N lines. And the FLM is used to specify an initial display line, which is preset whenever the FLM becomes “H”.

(8) DATA LATCH CIRCUIT

The data latch circuit is used to temporarily store display data which is released to the grayscale control circuit. The display data in this circuit is updated in synchronization with the CL. The “All Pixels ON/OFF”, “Display ON/OFF” and “Reverse Display ON/OFF” instructions control the data in this circuit, but does not change the data in the DDRAM.

(9) COMMON DRIVERS AND SEGMENT DRIVERS

The LSI includes 162-common drivers and 384-segment drivers. The common drivers generate LCD driving waveforms formed on the V_{LCD}, V₁, V₄ and V_{SSH} levels. The segment drivers generate waveforms formed on the V_{LCD}, V₂, V₃ and V_{SSH} levels.

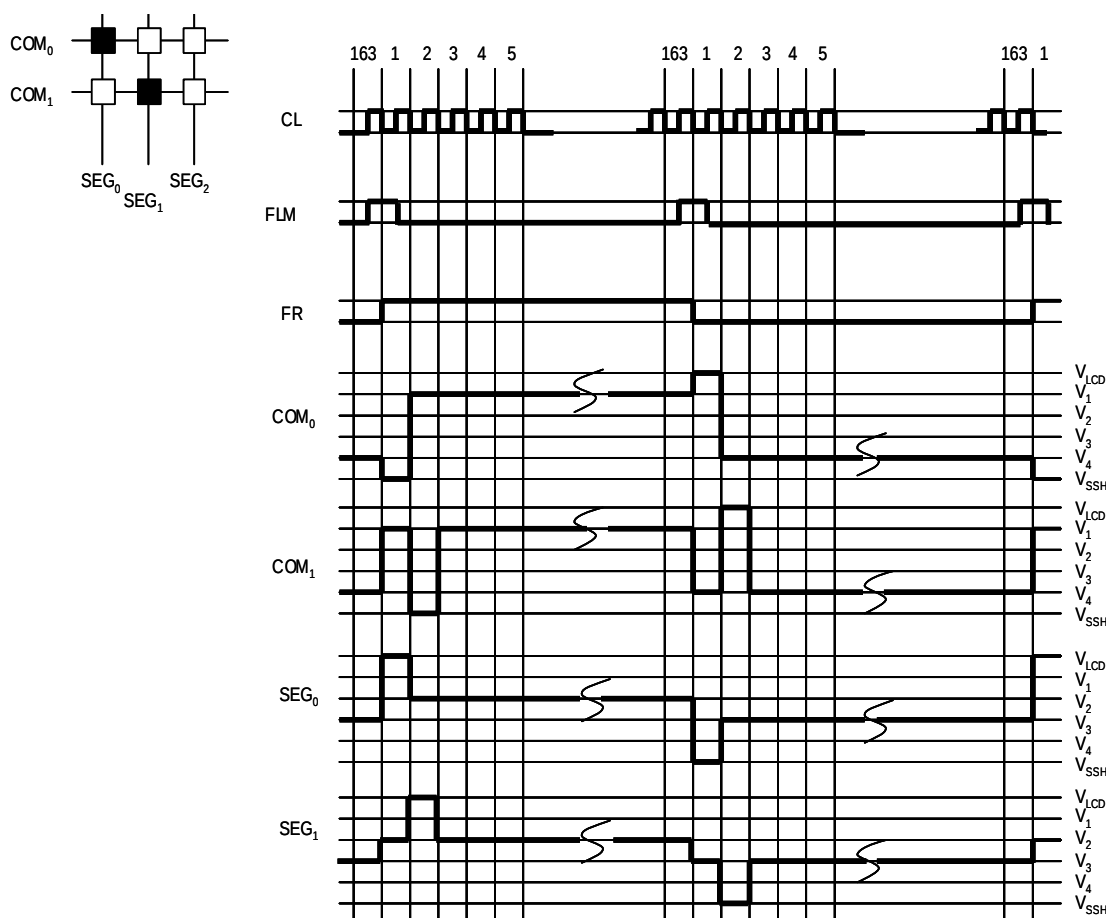


Fig 8 LCD Driving Waveforms (B&W Mode, Color Reverse OFF, 1/163 Duty)

(10) OSCILLATOR

The oscillator is equipped with a resistor and a capacitor, and generates internal clocks used for the display timing generator and the voltage booster. The internal resistor is enabled by setting “0” at the D₁ (CKS) bit of the “Bus Length” instruction. For more accurate frequency, using an external resistor or external clock is recommended.

When using the internal resistor, the resistance is controlled to optimize frame frequency for different LCD panels, by setting the D₂-D₀ (RF2-RF0) bits of the “Frequency Control” instruction. For more safety, make sure what is the best frequency in the particular application.

(10-1) Using Internal Resistor (CKS=0)

In this case, the OSC1 should be fixed at “H” or “L” and the OSC2 is open. The oscillation frequency is varied according to the display mode, as follows.

Table 16 Oscillation Frequency vs. Display Mode

Symbol	MON	PWM	Display Mode
f _{OSC1}	0	0	Variable 8-/16-grayscale Mode
f _{OSC2}	0	1	Fixed 8-grayscale Mode
f _{OSC3}	1	*	B&W Mode

*: Don't care

(10-2) Using External Resistor (CKS=1)

Be sure to connect the OSC1 and OSC2 with an external resistor. The frequency of the oscillator should be adjusted to the same value generated by the internal resistor.

(10-3) Using External Clock (CKS=1)

Input external clock to the OSC1 and leave the OSC2 open. The external clock with 50% duty is recommended. The frequency of the external clock should be the same value generated by the internal resistor.

(11) LCD POWER SUPPLY

The internal LCD power supply is organized into the voltage converter and the voltage booster. The voltage converter consists of the reference voltage generator, the voltage regulator with EVR and the LCD bias voltage generator. The configuration of the LCD power supply is arranged by setting the D₃ (AMPON) and D₁ (DCON) bits of the “Power Control” instruction. For this configuration, the internal LCD power supply can be partially used in combination with an external supply voltage, as shown in Table 17.

Table 17 Configuration of LCD Power Supply

DCON	AMPON	Voltage Booster	Voltage Converter	External Supply Voltage	NOTE
0	0	Inactive	Inactive	V _{OUT} , V _{LCD} , V ₁ , V ₂ , V ₃ , V ₄	1, 3, 4
0	1	Inactive	Active	V _{OUT}	2, 3, 4
1	1	Active	Active	—	-

NOTE1) No internal LCD power supply is used. The LCD bias voltages are externally supplied, and the C₁₊, C₁₋, C₂₊, C₂₋, C₃₊, C₃₋, C₄₊, C₄₋, C₅₊, C₅₋, C₆₊, C₆₋, V_{REF}, V_{REG} and V_{EE} are open.

NOTE2) Only the voltage converter is used. The V_{OUT} is externally supplied, and the C₁₊, C₁₋, C₂₊, C₂₋, C₃₊, C₃₋, C₄₊, C₄₋, C₅₊, C₅₋, C₆₊, C₆₋, and V_{EE} are open. The reference voltage is supplied on the V_{REF}.

NOTE3) The following relation among each LCD bias voltages must be maintained.

$$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SSH}$$

NOTE4) If the internal LCD power supply doesn't have enough capability to drive the particular LCD panel, use the external LCD power supply. Otherwise, it may affect display quality.

(11-1) Voltage Booster

The internal voltage booster generates up to $7 \times V_{EE}$ voltage. The boost level is selected from 2x, 3x, 4x, 5x, 6x or 7x by setting the D_2 - D_0 ($VU2$ - $VU0$) bits of the “Boost Level” instruction. The boost voltage V_{OUT} must not exceed 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

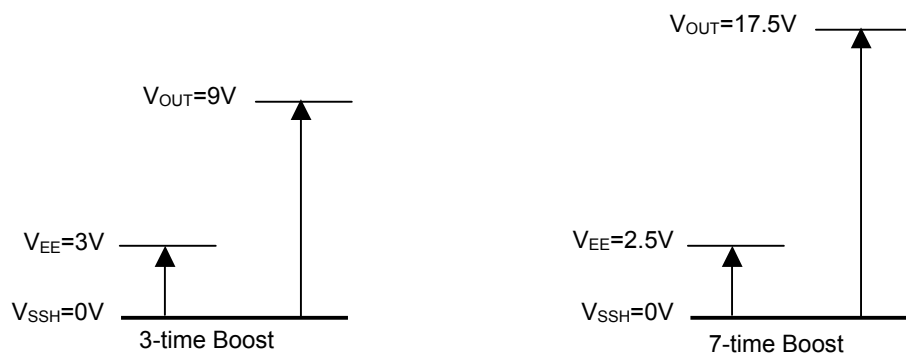


Fig 9 Boost Voltage

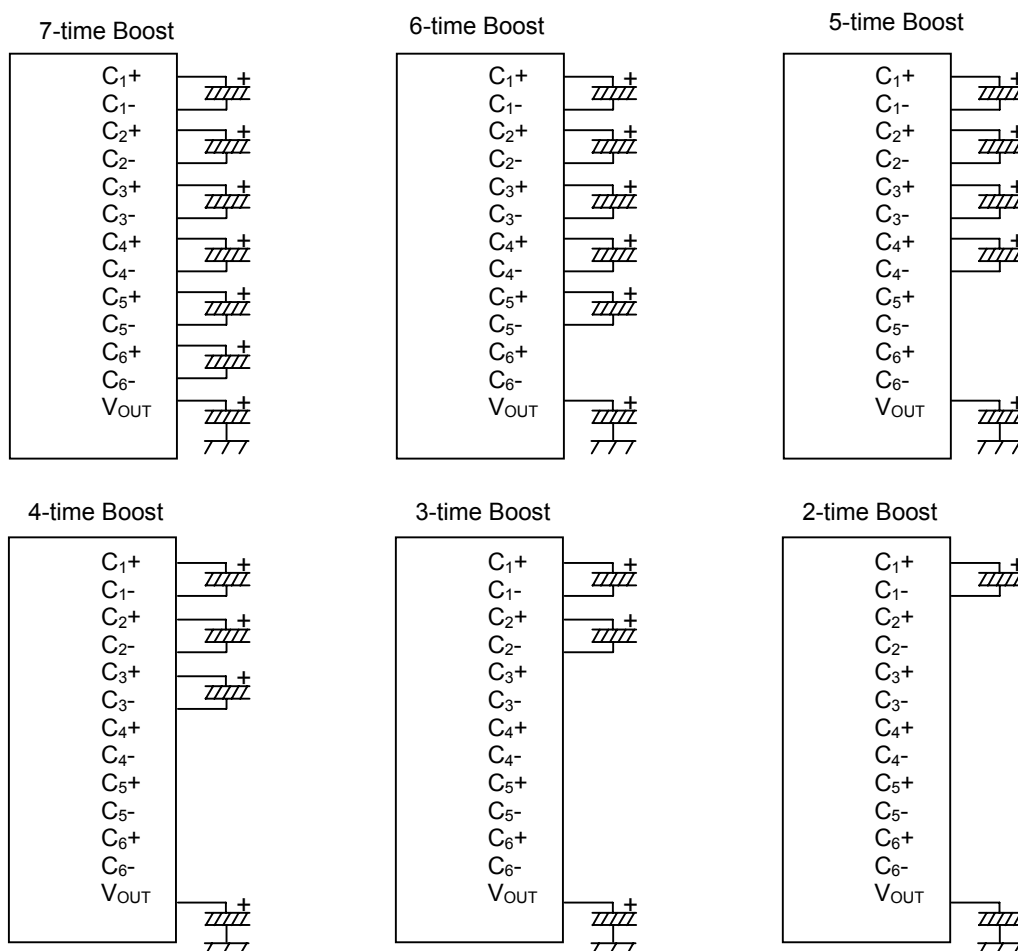


Fig 10 External Capacitor Connection of Voltage Booster

(11-2) Voltage Converter

(11-2-1) Reference Voltage Generator

The reference voltage generator produces the reference voltage ($V_{BA}=0.9 \times V_{EE}$). When using the internal LCD power supply, connect the V_{BA} and the V_{REF} , or supply $0.9 \times V_{EE}$ or lower voltage on the V_{REF} . When using an external LCD power supply, the V_{BA} should be open.

(11-2-2) Voltage Regulator

The voltage regulator consists of an operational amplifier with gain control and EVR. The V_{REF} voltage is multiplied to obtain the V_{REG} voltage, and its multiple (boost level) is set by the D_2 - D_0 ($VU2$ - $VU0$) bits of the “Boost Level” instruction. The formula is shown below.

$$V_{REG} = V_{REF} \times N \quad (N: \text{Boost Level})$$

(11-2-3) Electrical Variable Resistor (EVR)

The EVR is used to fine-tune the V_{LCD} voltage to optimize display contrast. The EVR value is controlled in 128 steps by setting the D_2 - D_0 (DV_2 - DV_0) bits of the “EVR Control” instruction. The formula is shown below.

$$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127 \quad (M: \text{EVR Value})$$

(11-2-4) LCD Bias Voltage Generator

The LCD bias voltage generator consists of buffer amplifiers and bleeder resistors to generate the LCD bias voltages such as the V_{LCD} , V_1 , V_2 , V_3 and V_4 , and its bias ratio is selected from 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11 or 1/12.

As shown in Fig 11, when using only the internal LCD power supply, the capacitors CA2 are connected to the V_{LCD} , V_1 , V_2 , V_3 and V_4 respectively.

As shown in Fig 12, when using no internal LCD power supply, the LCD bias voltages are externally supplied on the V_{LCD} , V_1 , V_2 , V_3 and V_4 , and the internal LCD power supply should be turned off by setting “0” at the “DCON” and “AMPON” bits. And the C_{1+} , C_{1-} , C_{2+} , C_{2-} , C_{3+} , C_{3-} , C_{4+} , C_{4-} , C_{5+} , C_{5-} , C_{6+} , C_{6-} , V_{EE} , V_{REF} and V_{REG} are open.

Fig 13 and 14 show typical peripheral circuits when partially using the LCD power supply without the reference voltage generator.

Fig 15 shows the circuit when partially using the LCD power supply without the voltage booster.

(11-3) External Components for LCD Power Supply

Using Only Internal LCD Power Supply (7x boost)

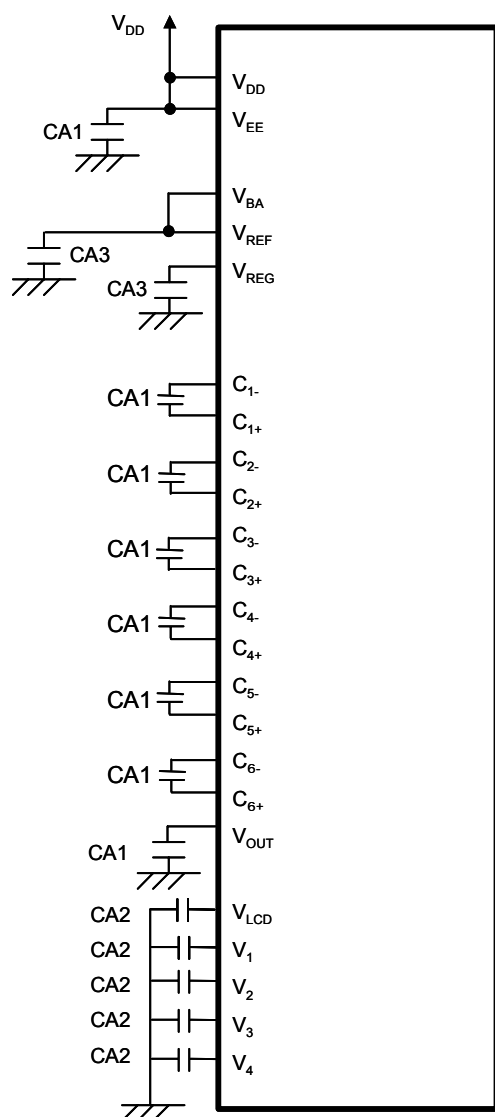


Fig 11

Using Only External LCD Power Supply

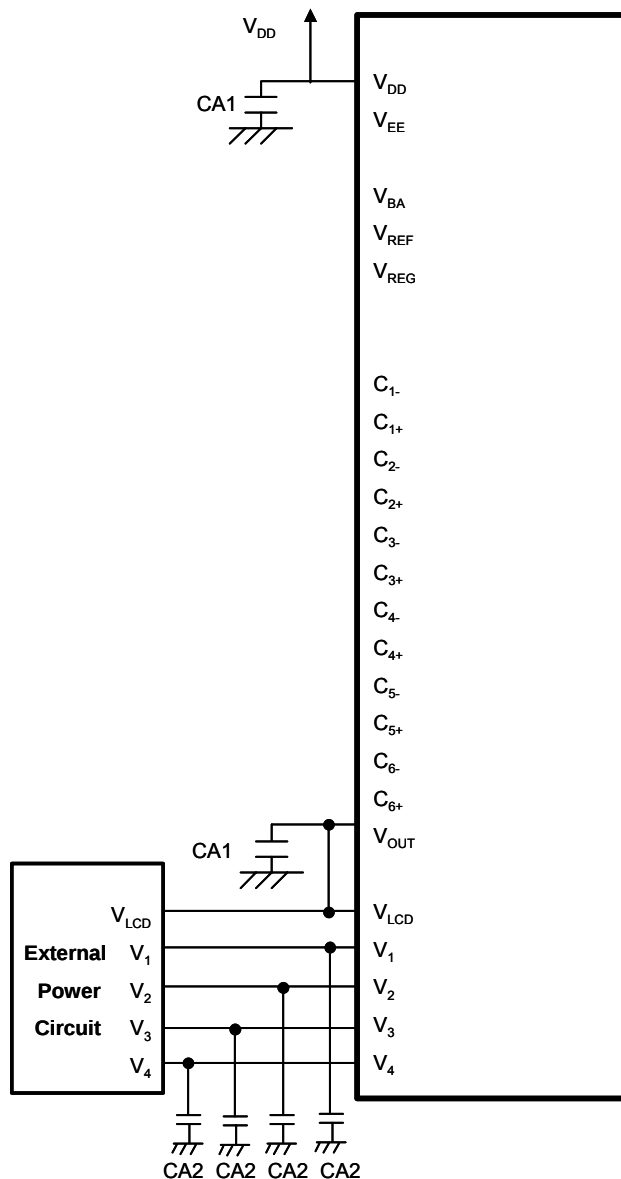


Fig 12

Reference Values

CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD} , V_{SS} , V_{EE} , V_{SSH} , V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal LCD Power Supply Without Reference Voltage generator (1) (7x boost)

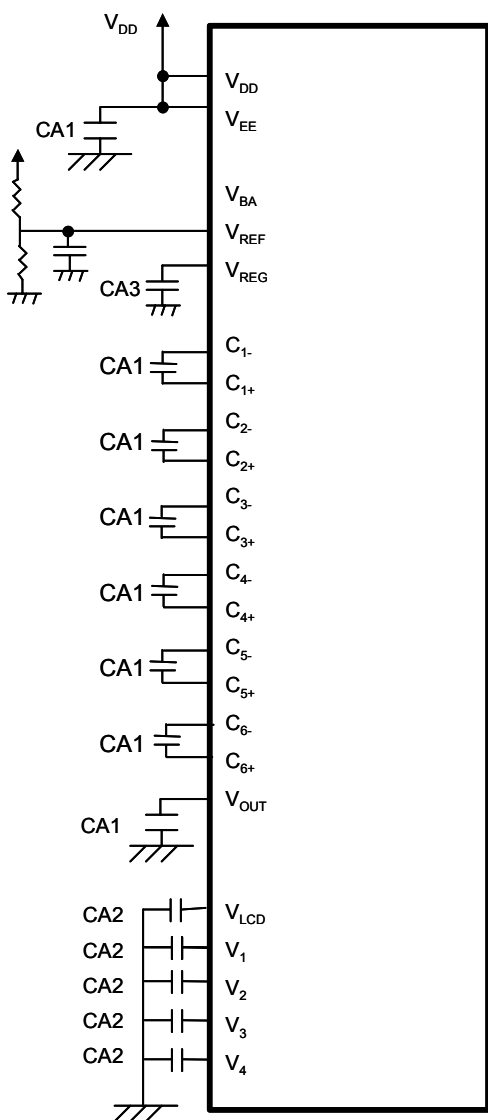


Fig 13

Using Internal LCD Power Supply Without Reference Voltage generator (2) (7x boost)

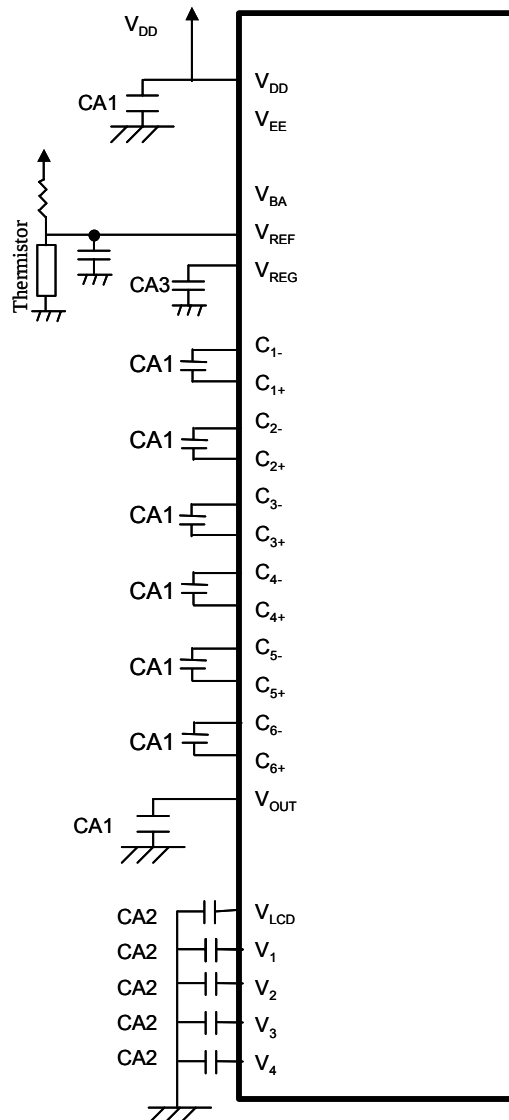


Fig 14

Reference Values

CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD} , V_{SS} , V_{EE} , V_{SSH} , V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal LCD Power Supply Without Voltage Booster

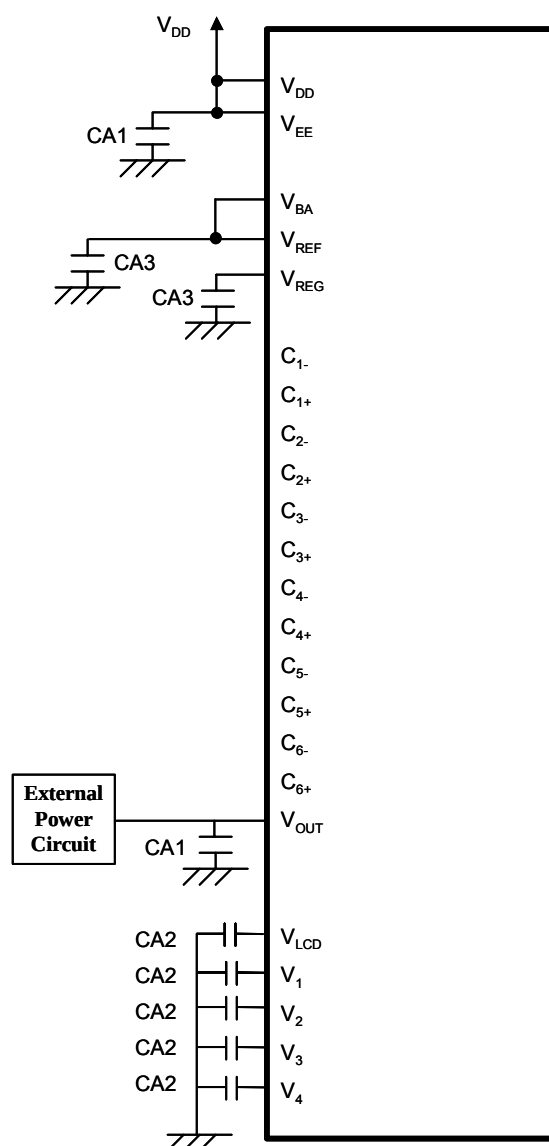


Fig 15

Reference Values

CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD} , V_{SS} , V_{EE} , V_{SSH} , V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

(11-4) Discharge Circuit

The LSI incorporates two discharge circuits which are independently controlled for the V_{LCD} and V_1 - V_4 and for the V_{OUT} . The V_{LCD} and V_1 - V_4 are discharged by setting "1" at the D_0 (DIS) bit of the "Discharge ON/OFF" instruction or the reset by the RESb. Be sure to turn off the internal or external LCD power supply when this instruction is executed, otherwise it may function as a current load and affect an operating current. Refer to "(14-22) Discharge ON/OFF".

(11-5) Power ON/OFF

To protect the LSI from overcurrent, the following sequences must be maintained to turn on and off the power supply. In addition to the following discussions, refer to "(18) TYPICAL INSTRUCTION SEQUENCES".

(11-5-1) Power ON/OFF in Using Internal LCD Power Supply

Power ON

First " V_{DD} and V_{EE} ON", next "Reset by RESb", then "Internal LCD power supply ON". Be sure to execute the "Display ON" instruction later than the completion of this power ON sequence. Otherwise, unexpected pixels may be turned on instantly.

Power OFF

First "Reset by RESb or "HALT" instruction", next " V_{DD} and V_{EE} OFF". If using different power sources for the V_{DD} and the V_{EE} individually, the V_{EE} must be turned off after the reset or the "HALT". After that, the V_{DD} can be turned off, waiting until the LCD bias voltages (V_{LCD} , V_1 , V_2 , V_3 and V_4) drop below the threshold level of LCD pixels.

(11-5-2) Power ON/OFF in Using External LCD Power Supply

Power ON

First " V_{DD} and V_{EE} ON", next "Reset by RESb", then "External LCD power supply ON". When using only external V_{OUT} , first " V_{DD} ON", next "Reset by RESb", then "External V_{OUT} ON", as well.

Power OFF

First "Reset by RESb or "HALT" instruction" to isolate external LCD bias voltages, next " V_{DD} OFF". For more safety, placing a resistor in series on the V_{LCD} line (or the V_{OUT} line in using only the external V_{OUT}) is recommended. That resistance is usually between 50 Ω and 100 Ω .

(12) RESET FUNCTION

The reset function initializes the LSI to the following default status by setting the RESb to “L”. Connecting the RESb with MPU’s reset is recommended so that the LSI and MPU is initialized at a time.

Default Status

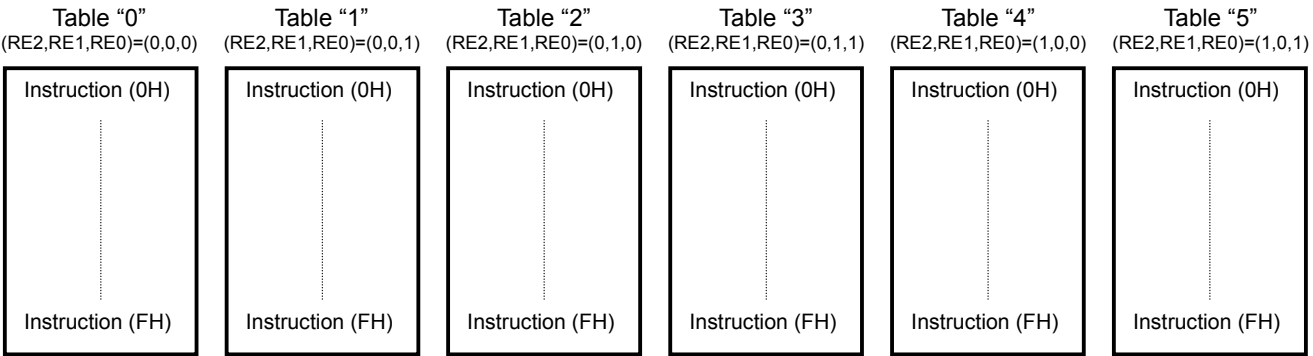
1. Display Data in DDRAM	:Undefined
2. Column Address	:(00)H
3. Row Address	:(00)H
4. Initial Display Line	:(0)H (1st line)
5. Display ON/OFF	:OFF
6. Reverse Display ON/OFF	:OFF (Normal)
7. Duty Cycle Ratio	:1/163 Duty (DSE=0)
8. N-line Inversion ON/OFF	:OFF
9. COM Scan Direction	:COM ₀ → COM ₁₆₁
10. Increment Control	:Auto-increment OFF (AIM, AXI, AYI)=(0, 0, 0)
11. REF	:REF=0 (Normal)
12. Swap	:OFF (Normal)
13. EVR Value	:(0, 0, 0, 0, 0, 0, 0)
14. Internal LCD Power Supply	:OFF
15. Display Mode	:Grayscale Mode
16. LCD Bias Ratio	:1/9 Bias
17. Palette 0	:(0, 0, 0, 0, 0)
18. Palette 1	:(0, 0, 0, 1, 1)
19. Palette 2	:(0, 0, 1, 0, 1)
20. Palette 3	:(0, 0, 1, 1, 1)
21. Palette 4	:(0, 1, 0, 0, 1)
22. Palette 5	:(0, 1, 0, 1, 1)
23. Palette 6	:(0, 1, 1, 0, 1)
24. Palette 7	:(0, 1, 1, 1, 1)
25. Palette 8	:(1, 0, 0, 0, 1)
26. Palette 9	:(1, 0, 0, 1, 1)
27. Palette 10	:(1, 0, 1, 0, 1)
28. Palette 11	:(1, 0, 1, 1, 1)
29. Palette 12	:(1, 1, 0, 0, 1)
30. Palette 13	:(1, 1, 0, 1, 1)
31. Palette 14	:(1, 1, 1, 0, 1)
32. Palette 15	:(1, 1, 1, 1, 1)
33. Display Mode Control	:Variable 16-grayscale Mode (4,096 Colors)
34. Bus Length	:8-bit Bus Length
35. Discharge ON/OFF	:OFF (DIS)=(0)

(13) INSTRUCTION TABLES

(13-1) Instruction Table and Register Address

The LSI incorporates 6 instruction tables as shown in Fig 16, and each instruction table has a specific address in between “0” and “5”. And each instruction register has a specific address in between (0H) and (FH), and instruction is read out from the register by the “Register Address” and “Register Read” instructions.

Fig 17 shows part of the instruction sequence, where the instruction table should be specified prior to other instructions. However, when some instructions of the same table are sequentially executed, the table selection may be omitted. In addition, the “Display Data Write”, “Display Data Read” and “Register Read” instructions can be performed in any table.



NOTE) Address (FH) is assigned to “Instruction Table Select” in any table.

Fig 16 Instruction Table Overview

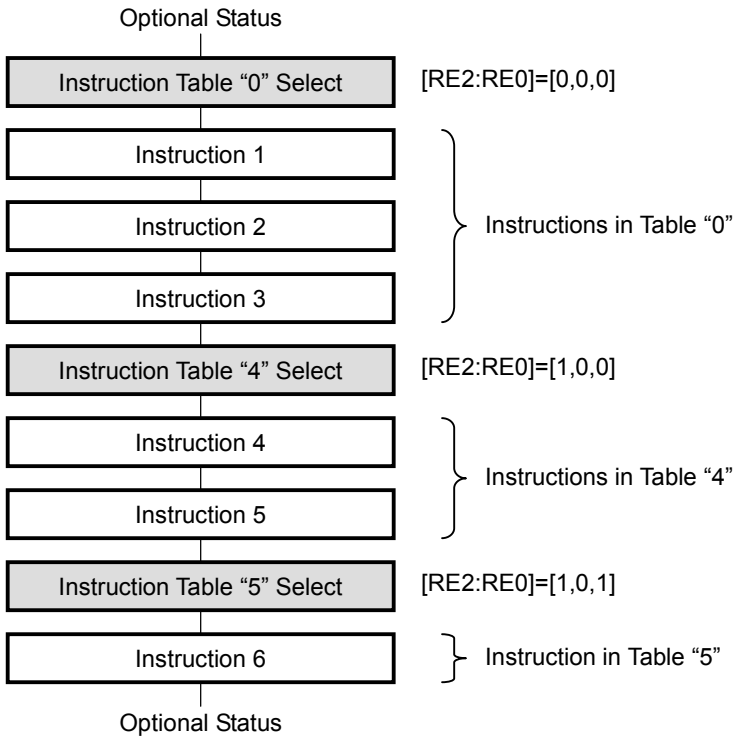


Fig 17 Outline of Instruction Sequence

(13-2) Instruction Table 0 (RE2, RE1, RE0)=(0, 0, 0)

Instructions/ Register Address [NH]		Code (80 Series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
1	Display Data Write	0	0	1	0	0/1	0/1	0/1	Write Data								Writing Display Data
2	Display Data Read	0	0	0	1	0/1	0/1	0/1	Read Data								Reading Display Data
3	Column Address (Lower) [0H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Setting Column Address for start point
	Column Address (Upper) [1H]	0	1	1	0	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	Setting Column Address for start point
4	Row Address (Lower) [2H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Setting Row Address for start point
	Row Address (Upper) [3H]	0	1	1	0	0	0	0	0	0	1	1	AY7	AY6	AY5	AY4	Setting Row Address for start point
5	Initial Display Line (Lower) [4H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Setting Row Address for Initial COM
	Initial Display Line (Upper) [5H]	0	1	1	0	0	0	0	0	1	0	1	LA7	LA6	LA5	LA4	Setting Row Address for Initial COM
6	N-line Inversion (Lower) [6H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	Setting the Number of N-line Inversion
	N-line Inversion (Upper) [7H]	0	1	1	0	0	0	0	0	1	1	1	N7	N6	N5	N4	Setting the Number of N-line Inversion
7	Display Control (1) [8H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/ OFF	SHIFT : Common Scan Direction MON : Grayscale/B/W Mode ALLON : All Pixels ON/OFF ON/OFF : Display ON/OFF
8	Display Control (2) [9H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV : Reverse Display ON/OFF NLIN : N-line Inversion ON/OFF SWAP : SWAP ON/OFF REF : Segment Direction
9	Increment Control [AH]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN : Window Area ON/OFF AIM : Read-Modify-Write ON/OFF AYI : Row Increment AXI : Column Increment
10	Power Control [BH]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON : Voltage Converter ON/OFF HALT : Power Save ON/OFF DCON : Voltage Booster ON/OFF ACL : Reset
11	Duty Cycle Ratio [CH]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Setting LCD Duty Cycle Ratio
12	Boost Level [DH]	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	VU2-0 : Setting Boost Level
13	LCD Bias Ratio [EH]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Setting LCD Bias Ratio
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-3) Instruction Table 1 (RE2, RE1, RE0)=(0, 0, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
15	Palette A0/A8 (Lower) [0H]	0	1	1	0	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Setting Palette Data : A0(PS=0) /A8(PS=1)
	Palette A0/A8 (Upper) [1H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/ PA84	Setting Palette Data : A0(PS=0) /A8(PS=1)
	Palette A1/A9 (Lower) [2H]	0	1	1	0	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Setting Palette Data : A1(PS=0) /A9(PS=1)
	Palette A1/A9 (Upper) [3H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/ PA94	Setting Palette Data : A1(PS=0) /A9(PS=1)
	Palette A2/A10 (Lower) [4H]	0	1	1	0	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Setting Palette Data : A2(PS=0) /A10(PS=1)
	Palette A2/A10 (Upper) [5H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/ PA104	Setting Palette Data : A2(PS=0) /A10(PS=1)
	Palette A3/A11 (Lower) [6H]	0	1	1	0	0	0	1	0	1	1	0	PA33/ PA113	PA32/P A112	PA31/ PA111	PA30/ PA110	Setting Palette Data : A3(PS=0) /A11(PS=1)
	Palette A3/A11 (Upper) [7H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/ PA114	Setting Palette Data : A3(PS=0) /A11(PS=1)
	Palette A4/A12 (Lower) [8H]	0	1	1	0	0	0	1	1	0	0	0	PA43/ PA123	PA42/P A122	PA41/ PA121	PA40/ PA120	Setting Palette Data : A4(PS=0) /A12(PS=1)
	Palette A4/A12 (Upper) [9H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/ PA124	Setting Palette Data : A4(PS=0) /A12(PS=1)
	Palette A5/A13 (Lower) [AH]	0	1	1	0	0	0	1	1	0	1	0	PA53/ PA133	PA52/P A132	PA51/ PA131	PA50/ PA130	Setting Palette Data : A5(PS=0) /A13(PS=1)
	Palette A5/A13 (Upper) [BH]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/ PA134	Setting Palette Data : A5(PS=0) /A13(PS=1)
	Palette A6/A14 (Lower) [CH]	0	1	1	0	0	0	1	1	1	0	0	PA63/ PA143	PA62/P A142	PA61/ PA141	PA60/ PA140	Setting Palette Data : A6(PS=0) /A14(PS=1)
	Palette A6/A14 (Upper) [DH]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/ PA144	Setting Palette Data : A6(PS=0) /A14(PS=1)
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-4) Instruction Table 2 (RE2, RE1, RE0)=(0, 1, 0)

Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code								Functions	
	CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
15	Palette A7/A15 (Lower) [0H]	0	1	1	0	0	1	0	0	0	0	PA73/ PA153	PA72/P A152	PA71/ PA151	PA70/ PA150	Setting Palette Data : A7(PS=0) /A15(PS=1)	
	Palette A7/A15 (Upper) [1H]	0	1	1	0	0	1	0	0	0	1	*	*	*	PA74/ PA154	Setting Palette Data : A7(PS=0) /A15(PS=1)	
	Palette B0/B8 (Lower) [2H]	0	1	1	0	0	1	0	0	0	1	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Setting Palette Data : B0(PS=0) /B8(PS=1)	
	Palette B0/B8 (Upper) [3H]	0	1	1	0	0	1	0	0	0	1	*	*	*	PB04/ PB84	Setting Palette Data : B0(PS=0) /B8(PS=1)	
	Palette B1/B9 (Lower) [4H]	0	1	1	0	0	1	0	0	1	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Setting Palette Data : B1(PS=0) /B9(PS=1)	
	Palette B1/B9 (Upper) [5H]	0	1	1	0	0	1	0	0	1	0	*	*	*	PB14/ PB94	Setting Palette Data : B1(PS=0) /B9(PS=1)	
	Palette B2/B10 (Lower) [6H]	0	1	1	0	0	1	0	0	1	1	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Setting Palette Data : B2(PS=0) /B10(PS=1)	
	Palette B2/B10 (Upper) [7H]	0	1	1	0	0	1	0	0	1	1	*	*	*	PB24/ PB104	Setting Palette Data : B2(PS=0) /B10(PS=1)	
	Palette B3/B11 (Lower) [8H]	0	1	1	0	0	1	0	1	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Setting Palette Data : B3(PS=0) /B11(PS=1)	
	Palette B3/B11 (Upper) [9H]	0	1	1	0	0	1	0	1	0	1	*	*	*	PB34/ PB114	Setting Palette Data : B3(PS=0) /B11(PS=1)	
	Palette B4/B12 (Lower) [AH]	0	1	1	0	0	1	0	1	0	1	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Setting Palette Data : B4(PS=0) /B12(PS=1)	
	Palette B4/B12 (Upper) [BH]	0	1	1	0	0	1	0	1	0	1	*	*	*	PB44/ PB124	Setting Palette Data : B4(PS=0) /B12(PS=1)	
	Palette B5/B13 (Lower) [CH]	0	1	1	0	0	1	0	1	1	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Setting Palette Data : B5(PS=0) /B13(PS=1)	
	Palette B5/B13 (Upper) [DH]	0	1	1	0	0	1	0	1	1	0	*	*	*	PB54/ PB134	Setting Palette Data : B5(PS=0) /B13(PS=1)	
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Tablet

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-5) Instruction Table 3 (RE2, RE1, RE0)=(0, 1, 1)

Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code								Functions	
	CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0		
15	Palette B6/B14 (Lower) [0H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Setting Palette Data : B6(PS=0) /B14(PS=1)
	Palette B6/B14 (Upper) [1H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Setting Palette Data : B6(PS=0) /B14(PS=1)
	Palette B7/B15 (Lower) [2H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Setting Palette Data : B7(PS=0) /B15(PS=1)
	Palette B7/B15 (Upper) [3H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Setting Palette Data : B7(PS=0) /B15(PS=1)
	Palette C0/C8 (Lower) [4H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Setting Palette Data : C0(PS=0) /C8(PS=1)
	Palette C0/C8 (Upper) [5H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Setting Palette Data : C0(PS=0) /C8(PS=1)
	Palette C1/C9 (Lower) [6H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Setting Palette Data : C1(PS=0) /C9(PS=1)
	Palette C1/C9 (Upper) [7H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Setting Palette Data : C1(PS=0) /C9(PS=1)
	Palette C2/C10 (Lower) [8H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Setting Palette Data : C2(PS=0) /C10(PS=1)
	Palette C2/C10 (Upper) [9H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Setting Palette Data : C2(PS=0) /C10(PS=1)
	Palette C3/C11 (Lower) [AH]	0	1	1	0	0	1	1	1	0	1	0	PC33P C113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Setting Palette Data : C3(PS=0) /C11(PS=1)
	Palette C3/C11 (Upper) [BH]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Setting Palette Data : C3(PS=0) /C11(PS=1)
	Palette C4/C12 (Lower) [CH]	0	1	1	0	0	1	1	1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Setting Palette Data : C4(PS=0) /C12(PS=1)
	Palette C4/C12 (Upper) [DH]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC44/ PC124	Setting Palette Data : C4(PS=0) /C12(PS=1)
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-6) Instruction Table 4 (RE2, RE1, RE0)=(1, 0, 0)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
15	Palette C5/C13 (Lower) [0H]	0	1	1	0	1	0	0	0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130	Setting Palette Data : C5(PS=0) /C13(PS=1)
	Palette C5/C13 (Upper) [1H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/ PC134	Setting Palette Data : C5(PS=0) /C13(PS=1)
	Palette C6/C14 (Lower) [2H]	0	1	1	0	1	0	0	0	0	1	0	PC63/P C143	PC62/ PC142	PC61/ PC141	PC60/ PC140	Setting Palette Data : C6(PS=0) /C14(PS=1)
	Palette C6/C14 (Upper) [3H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/ PC144	Setting Palette Data : C6(PS=0) /C14(PS=1)
	Palette C7/C15 (Lower) [4H]	0	1	1	0	1	0	0	0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150	Setting Palette Data : C7(PS=0) /C15(PS=1)
	Palette C7/C15 (Upper) [5H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/ PC154	Setting Palette Data : C7(PS=0) /C15(PS=1)
16	Initial COM [6H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Setting start COM for scanning
17	Duty-1 /Display Clock ON/OFF [7H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : Display Clock ON/OFF DSE : Duty-1 ON/OFF
18	Display Mode Control [8H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	FDC1	FDC2	PWM : Variable/Fixed Grayscale Mode C256 : 256-color Mode ON/OFF. FDC : Boost clock
19	Bus Length [9H]	0	1	1	0	1	0	0	1	0	0	1	HSW	ABS	CKS	WLS	HSW : High Speed Writing ABS : Bit Assignment CKS : Oscillator Set WLS : 8-/16-bit Bus Length
20	EVR Control (Lower) [AH]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Setting EVR Value (Lower Bit)
	EVR Control (Upper) [BH]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Setting EVR Value (Upper Bit)
21	Frequency Control [DH]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Adjusting Oscillation Frequency
22	Discharge ON/OFF [EH]	0	1	1	0	1	0	0	1	1	1	0	*	*	*	DIS	Discharge ON/OFF
23	Register Address [CH]	0	1	1	0	1	0	0	1	1	0	0	Register Address				Setting Register Address
24	Register Read	0	1	0	1	0/1	0/1	0/1					Read Data				Reading Instruction
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table Select

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-7) Instruction Table 5 (RE2, RE1, RE0)=(1, 0, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
25	Window End Column Address (Lower) [0H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Setting Column Address for end point
	Window End Column Address (Upper) [1H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Setting Column Address for end point
26	Window End Row Address (Lower) [2H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Setting Row Address for end point
	Window End Row Address (Upper) [3H]	0	1	1	0	1	0	1	0	0	1	1	EY7	EY6	EY5	EY4	Setting Row Address for end point
27	Initial Line-reverse Address (Lower) [4H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Setting Start Line for Line-reverse Display
	Initial Line-reverse Address (Upper) [5H]	0	1	1	0	1	0	1	0	1	0	1	LS7	LS6	LS5	LS4	Setting Start Line for Line-reverse Display
28	Last Line-reverse Address (Lower) [6H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Setting End Line for Line-reverse Display
	Last Line-reverse Address (Upper) [7H]	0	1	1	0	1	0	1	0	1	1	1	LE7	LE6	LE5	LE4	Setting End Line for Line-reverse Display
29	Line Reverse ON/OFF [8H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink Set LREV : Line-reverse ON/OFF
30	Upper/Lower Palette Select [9H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	PS	PS : Upper/Lower Palette Register
31	PWM Control [AH]	0	1	1	0	1	0	1	1	0	1	0	PWM S	PWM A	PWM B	PWM C	Setting PWM Mode
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(14) INSTRUCTION DESCRIPTIONS

This chapter provides detailed descriptions about each instruction. These descriptions are written with the assumption that 80-series MPU is used. When using 68-series MPU, the polarities of the E and R/W signals differ from those of the RDb and WRb signals.

(14-1) Display Data Write

The “Display Data Write” instruction writes display data on a specified DDRAM address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display Data							

(14-2) Display Data Read

The “Display Data Read” instruction reads out display data from a specified DDRAM address. One dummy read is necessary right after DDRAM address setting.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display Data							

(14-3) Column Address

The “Column Address” instruction specifies the column address of the start point. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	AX3	AX2	AX1	AX0

(Default: AX3-AX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	AX7	AX6	AX5	AX4

(Default: AX7-AX4=0H / Register Address: 1H)

(14-4) Row Address

The “Row Address” instruction specifies the row address of the start point. Available setting range is from (00H) to (A1H), and outside this range is not allowed. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	AY3	AY2	AY1	AY0

(Default: AY3-AY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	AY7	AY6	AY5	AY4

(Default: AY7-AY4=0H / Register Address: 3H)

(14-5) Initial Display Line

This instruction sets the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. For more information, refer to “(14-16) Initial COM”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LA3	LA2	LA1	LA0

(Default: LA3-LA0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	LA7	LA6	LA5	LA4

(Default: LA7-LA4=0H / Register Address: 5H)

Table 18 Initial Display Line Address

LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	Row Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:								:
1	0	1	0	0	0	0	1	161

(14-6) N-line Inversion

The number of N line is selected in between “2” and “162”. When the N-line inversion is enabled by setting “1” at the D₂ (NLIN) bit of the “Display Control (2)” instruction, the FR toggles once every N lines. When the N-line inversion is disabled by setting “0” at this bit, the FR toggles by the frame.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	N3	N2	N1	N0

(Default: N3-N0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	N7	N6	N5	N4

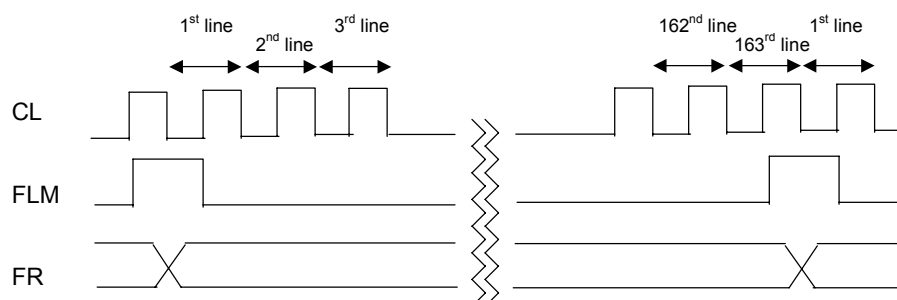
(Default: N7-N4=0H / Register Address: 7H)

Table 19 N-line Inversion

N7	N6	N5	N4	N3	N2	N1	N0	N Line
0	0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	0	1	2
:								:
1	0	1	0	0	0	0	1	162

NOTE1) N Line=(N Value)+1

N-line inversion OFF



N-line inversion ON

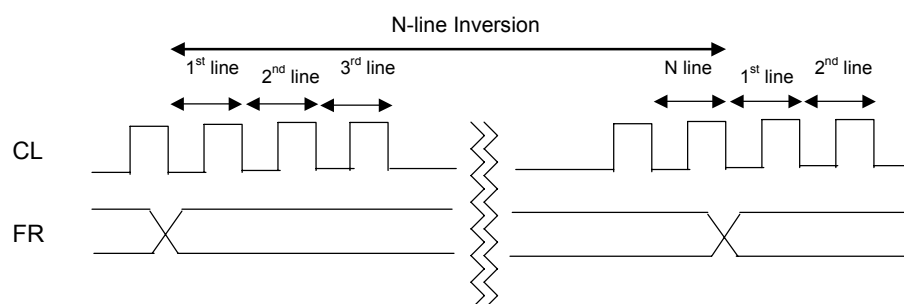


Fig 18 N-line Inversion Timing (1/163 Duty)

(14-7) Display Control (1)

The “Display Control (1)” instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON /OFF

(Default: [SHIFT,MON,ALLON,ON/OFF]=0H / Register Address: 8H)

D₀ (ON/OFF)

ON/OFF=0 : Display OFF (All COM/SEG fixed at V_{SSH} level)

ON/OFF=1 : Display ON

D₁ (ALLON)

This bit forcibly turns on all pixels regardless of display data. This bit has a priority over the “REV” bit of the “Display Control (2)” instruction.

ALLON=0 : Normal

ALLON=1 : All pixels ON

D₂ (MON)

MON=0 : Grayscale Mode (Variable 16-grayscale, Variable 8-grayscale or Fixed 8-grayscale Mode)

MON=1 : B&W Mode

D₃ (SHIFT)

SHIFT=0 : COM₀ → COM₁₆₁

SHIFT=1 : COM₀ ← COM₁₆₁

(14-8) Display Control (2)

The “Display Control (2)” instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	REV	NLIN	SWAP	REF

(Default: [REV,NLIN,SWAP,REF]=0H / Register Address: 9H)

D₀ (REF)

This bit controls the DDRAM access direction which reverses the segment direction for reducing the restrictions on the IC position of an LCD module. For more information, refer to “(17) SWAP FUNCTION”.

D₁ (SWAP)

This bit swaps palettes A_j and palettes C_j (j=0-15). This function reduces the restrictions on the IC position of an LCD module. Refer to “(16) SWAP FUNCTION”.

SWAP=0 : SWAP OFF
SWAP=1 : SWAP ON

D₂ (NLIN)

This bit enables the N-line inversion.

NLIN=0 : N-line Inversion OFF (FR toggles by the frame.)
NLIN=1 : N-line Inversion ON (FR toggles once every N lines.)

D₃ (REV)

This bit enables the reverse display function that reverses the polarities of all display data without changing the DDRAM.

REV=0 : Reverse Display OFF (Normal)
REV=1 : Reverse Display ON

Table 20 Reverse Display ON/OFF

REV	Display	DDRAM Data → Display Data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(14-9) Increment Control

The “AIM”, “AYI” and “AXI” bits set an auto-increment operation to the column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up, whenever the DDRAM is accessed. The “WIN” bits enables/disables the window area access.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	WIN	AIM	AYI	AXI

(Default: [WIN,AIM,AYI,AXI]=0H / Register Address: AH)

D₂ (AIM)

Table 21 Read-modify-write ON/OFF

AIM	Increment Mode	NOTE
0	Read-modify-write OFF	1
1	Read-modify-write ON	2

NOTE1) Increment in writing and reading display data

NOTE2) Increment in writing display data only

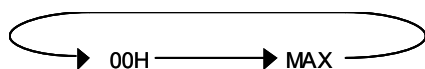
D₁, D₀ (AYI, AXI)

Table 22 Column/Row Increment

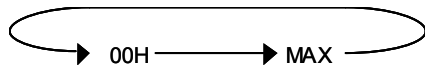
AYI	AXI	Column/Row Increment	NOTE
0	0	Non Increment	1
0	1	Column Address Increment	2
1	0	Row Address Increment	3
1	1	Column & Row Addresses Increment	4

NOTE1) Non increment. The “AIM” bit is disabled.

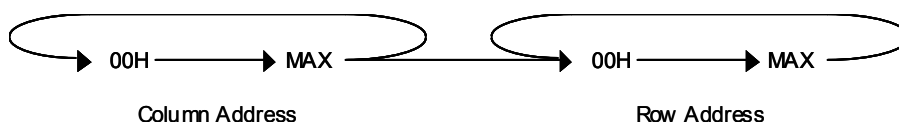
NOTE2) Increment operation of column address. The “AIM” bit is enabled.



NOTE3) Row address increment. The “AIM” bit is enabled.



NOTE4) Column & row addresses increment. The “AIM” bit is enabled.

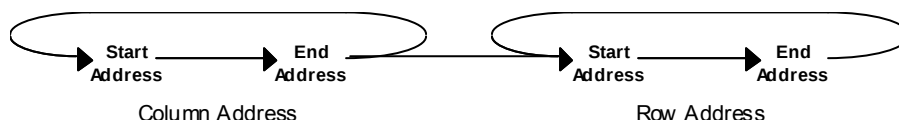


D₃ (WIN)

The window access should be enabled (WIN=1) in combination with the auto-increment operation (AXI=1, AYI=1). The typical sequence of the window area setting is discussed in “(4-2) Window Area for DDRAM Access”.

WIN=0 : Window Area Access OFF (Normal DDRAM Access)

WIN=1 : Window Area Access ON



(14-10) Power Control

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	AMPON	HALT	DCON	ACL

(Default: [AMPON,HALT,DCON,ACL]=0H / Register Address: BH)

D₀ (ACL)

This bit initializes the internal LCD power supply.

ACL=0 : Initialization OFF (Normal)
 ACL=1 : Initialization ON

NOTE) During the initialization, "1" is read out as the status of the "ACL" bit by the "Register Read" instruction. After the initialization, it is "0". As the CLK triggers the initialization, the "wait time" at least equivalent to 2 cycles of the CLK is required for the next instruction.

D₁ (DCON)

The "DCON" bit activates the voltage booster.

DCON=0 : Voltage Booster OFF
 DCON=1 : Voltage Booster ON

D₂ (HALT)

The "HALT" bit enables the power save mode. During the power save, operating current is down to the stand-by level. The internal state of the LSI in the power save mode is listed below.

HALT=0 : Power Save OFF (Normal)
 HALT=1 : Power Save ON

Internal State in Power Save Mode (HALT="1")

- Internal oscillator and internal LCD power supply are halted.
- All segment and common drivers are fixed at V_{SSH} level.
- External clock to the OSC1 cannot be accepted.
- Display data in the DDRAM is being maintained.
- Data in the instruction registers are being maintained.
- V_{LCD}, V₁, V₂, V₃ and V₄ are in high impedance.

NOTE) In the power save ON sequence, execute the "Display OFF" prior to the "Power Save ON". In the power save OFF sequence, execute the "Power save OFF" prior to the "Display ON". If the "Power Save ON/OFF" instruction is executed during the "Display ON", unexpected pixels may be turned on instantly.

D₃ (AMPON)

The "AMPON" bit activates the voltage converter which includes the reference voltage generator, the voltage regulator and the LCD bias generator.

AMPON=0 : Voltage Converter OFF
 AMPON=1 : Voltage Converter ON

(14-11) Duty Cycle Ratio

The “Duty Cycle Ratio” instruction selects LCD duty cycle ratio, and is used to carry out the partial display in combination with other instructions such as the “Boost Level”, the “LCD Bias Ratio” and the “EVR Control”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	DS3	DS2	DS1	DS0

(Default: DS3-DS0=0H / Register Address: CH)

Table 23 Duty Cycle Ratio

DS3	DS2	DS1	DS0	Duty Cycle Ratio		# of Commons
				DSE=0	DES=1	
0	0	0	0	1/163	1/162	162 commons
0	0	0	1	1/161	1/160	160 commons
0	0	1	0	1/145	1/144	144 commons
0	0	1	1	1/133	1/132	132 commons
0	1	0	0	1/129	1/128	128 commons
0	1	0	1	1/113	1/112	112 commons
0	1	1	0	1/97	1/96	96 commons
0	1	1	1	1/81	1/80	80 commons
1	0	0	0	1/73	1/72	72 commons
1	0	0	1	1/65	1/64	64 commons
1	0	1	0	1/57	1/56	56 commons
1	0	1	1	1/49	1/48	48 commons
1	1	0	0	1/41	1/40	40 commons
1	1	0	1	1/33	1/32	32 commons
1	1	1	0	1/25	1/24	24 commons
1	1	1	1	1/17	1/16	16 commons

NOTE) Duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting “1” at the D₁ (DSE) bit of the “Duty-1 ON/OFF” instruction. Refer to “(14-17) Duty-1 /Display Clock ON/OFF”.

(14-12) Boost Level

The “Boost Level” selects the multiple of the voltage booster.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	VU2	VU1	VU0

(Default: VU2-VU0=0H / Register Address: DH)

D₂, D₁, D₀ (VU2, VU1, VU0)

Table 24 Boost Level

VU2	VU1	VU0	Boost Level
0	0	0	1 time (No boost)
0	0	1	2 times
0	1	0	3 times
0	1	1	4 times
1	0	0	5 times
1	0	1	6 times
1	1	0	7 times
1	1	1	Inhibited

(14-13) LCD Bias Ratio

The “LCD bias ratio” selects LCD bias ratio.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	0	*	B2	B1	B0

(Default: B2-B0=0H / Register Address: EH)

Table 25 LCD Bias Ratio

B2	B1	B0	LCD Bias Ratio
0	0	0	1/9
0	0	1	1/8
0	1	0	1/7
0	1	1	1/6
1	0	0	1/5
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

(14-14) Instruction Table Select

This instruction specifies an instruction table, and should be executed prior to other instructions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	1	TST0	RE2	RE1	RE0

(Default: TST0, RE2-RE0=0H / Register Address: FH)

Table 26 Instruction Table Select

RE2	RE1	RE0	Instructions
0	0	0	Instruction Table (0)
0	0	1	Instruction Table (1)
0	1	0	Instruction Table (2)
0	1	1	Instruction Table (3)
1	0	0	Instruction Table (4)
1	0	1	Instruction Table (5)

NOTE) “TST0” bit must be “0”. This is used for maker tests only.

(14-15) Palette A / B / C

Palette A0 (PS=0) / Palette A8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

(Register Address: 0H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA04/ PA84

(Register Address: 1H)

Palette A1 (PS=0) / Palette A9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PA14/ PA94

(Register Address: 3H)

Palette A2 (PS=0) / Palette A10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PA24/ PA104

(Register Address: 5H)

Palette A3 (PS=0) / Palette A11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PA34/ PA114

(Register Address: 7H)

Palette A4 (PS=0) / Palette A12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PA44/ PA124

(Register Address: 9H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette A5 (PS=0) / Palette A13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PA54/ PA134

(Register Address: BH)

Palette A6 (PS=0) / Palette A14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PA64/ PA144

(Register Address: DH)

Palette A7 (PS=0) / Palette A15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA74/ PA154

(Register Address: 1H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette B0 (PS=0) / Palette B8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB04/ PB84

(Register Address: 3H)

Palette B1 (PS=0) / Palette B9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PB14/ PB94

(Register Address: 5H)

Palette B2 (PS=0) / Palette B10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PB24/ PB104

(Register Address: 7H)

Palette B3 (PS=0) / Palette B11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PB34/ PB114

(Register Address: 9H)

Palette B4 (PS=0) / Palette B12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PB44/ PB124

(Register Address: BH)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette B5 (PS=0) / Palette B13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PB54/ PB134

(Register Address: DH)

Palette B6 (PS=0) / Palette B14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PB64/ PB144

(Register Address: 1H)

Palette B7 (PS=0) / Palette B15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB74/ PB154

(Register Address: 3H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette C0 (PS=0) / Palette C8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC04/ PC84

(Register Address: 5H)

Palette C1 (PS=0) / Palette C9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PC14/ PC94

(Register Address: 7H)

Palette C2 (PS=0) / Palette C10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PC24/ PC104

(Register Address: 9H)

Palette C3 (PS=0) / Palette C11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PC34/ PC114

(Register Address: BH)

Palette C4 (PS=0) / Palette C12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PC44/ PC124

(Register Address: DH)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette C5 (PS=0) / Palette C13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PC54/ PC134

(Register Address: 1H)

Palette C6 (PS=0) / Palette C14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PC63/ PC143	PC62/ PC142	PC61/ PB141	PC60/ PB140

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PC64/ PC144

(Register Address: 3H)

Palette C7 (PS=0) / Palette C15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC74/ PC154

(Register Address: 5H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

(14-16) Initial COM

The “Initial COM” instruction specifies the common driver for a scan start common.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	SC3	SC2	SC1	SC0

(Default: SC3-SC0=0H / Register Address: 6H)

Table 27 Initial COM

SC3	SC2	SC1	SC0	Initial COM (SHIFT=0)	Initial COM (SHIFT=1)
0	0	0	0	COM ₀	COM ₁₆₁
0	0	0	1	COM ₁	COM ₁₆₀
0	0	1	0	COM ₉	COM ₁₅₂
0	0	1	1	COM ₁₄	COM ₁₄₆
0	1	0	0	COM ₁₇	COM ₁₄₄
0	1	0	1	COM ₂₅	COM ₁₃₆
0	1	1	0	COM ₃₃	COM ₁₂₈
0	1	1	1	COM ₄₁	COM ₁₂₀
1	0	0	0	COM ₄₉	COM ₁₁₂
1	0	0	1	COM ₅₇	COM ₁₀₄
1	0	1	0	COM ₆₅	COM ₉₆
1	0	1	1	COM ₇₃	COM ₈₈
1	1	0	0	COM ₁₂₂	COM ₃₉
1	1	0	1	COM ₁₃₀	COM ₃₁
1	1	1	0	COM ₁₃₈	COM ₂₃
1	1	1	1	COM ₁₄₆	COM ₁₅

(14-17) Duty-1 /Display Clock ON/OFF

This instruction controls ON (Duty-1) /OFF (Duty-0) and Display Clock ON/OFF.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	DSE	SON

(Default: SON,DSE=0H / Register Address: 7H)

D₀ (SON)

SON=0 : CL, FLM, FR, and CLK are fixed at “L” level.

SON=1 : CL, FLM, FR, and CLK are enabled.

D₁ (DSE)

The duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting “1” at the “DSE” bit.

DSE=0 : OFF (Duty-0)

DSE=1 : ON (Duty-1)

NOTE) For the last common timing at “DSE=0”, all common drivers generate non-selective waveforms, and segment drivers generate the same waveforms as for the previous common timing. For instance, in 1/163 duty cycle, the segment waveforms for 163rd common timing are the same as for 162nd common timing (last line).

(14-18) Display Mode Control

The “Display Mode Control” instruction sets up display modes such as the variable or fixed grayscale mode and the variable 8- or 16-grayscale mode. The D₂ (MON) bit of the “Display Control (1)” is used in combination. Refer to “(5) GRAY SCALE CONTROL CIRCUIT” and “(14-7) Display Control (1).”

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PWM	C256	FDC1	FDC2

(Default: PWM,C256=0H / Register Address: 8H)

D₃ (PWM)

PWM=0 : Variable grayscale Mode (Variable 8-/16-grayscale Mode)

PWM=1 : Fixed 8-grayscale Mode

D₂ (C256)

C256=0 : Variable 16-grayscale Mode at “PWM=0” (4096 colors)
 C256=1 : Variable 8-grayscale Mode at “PWM=0” (256 colors)

D₁(FDC1), D₀(FDC2)

These bits are used to select clock multiply for voltage booster.

FDC1	FDC2	Boost Clock
0	0	×1
0	1	×2
1	0	×4
1	1	×1/2

(14-19) Bus Length

This instruction selects 8- or 16-bit bus length, and sets oscillator configuration, ABS mode ON/OFF and high speed writing ON/OFF as well.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	HSW	ABS	CKS	WLS

(Default: HSW,ABS,CKS,WLS=0H / Register Address: 9H)

D₀ (WLS)

WLS=0: 8-bit Bus Length
 WLS=1: 16-bit Bus Length

D₁ (CKS)

CKS =0: Internal Oscillator using an internal resistor
 CKS =1: External Clock, or Internal Oscillator using an external resistor

NOTE) Refer to “(10) OSCILLATOR”.

D₂ (ABS)

ABS=0: ABS Mode OFF (Normal)
 ABS=1: ABS Mode ON

D₃ (HSW)

HSW=0: High Speed Writing OFF (Normal)
 HSW=1: High Speed Writing ON

(14-20) EVR Control

The “EVR Control” instruction adjusts V_{LCD} to optimize display contrast. This instruction is finally effective when both upper and lower bytes are transmitted in order to prevent high V_{LCD} . The setting order is upper byte first, then lower byte. Refer to “(11-2-3) Electrical Variable Resistor (EVR)”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	DV ₃	DV ₂	DV ₁	DV ₀

(Default: DV₃-DV₀=0H / Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	DV ₆	DV ₅	DV ₄

(Default: DV₆-DV₄=0H / Register Address: BH)

Table 28 EVR Control

DV ₆	DV ₅	DV ₄	DV ₃	DV ₂	DV ₁	DV ₀	V_{LCD}
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	1	High

Formula of VLCD

$$VLCD [V] = 0.5 \times VREG + M (VREG - 0.5 \times VREG) / 127$$

$$VBA = VEE \times 0.9$$

$$VREG = VREF \times N$$

VBA : Output of the reference voltage generator

VREF : Input of the voltage regulator

VREG : Output of the voltage regulator

N : Boost level

M : EVR Value

(14-21) Frequency Control

The “Frequency Control” instruction adjusts the frame frequency.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	Rf2	Rf1	Rf0

(Default: DV₃-DV₀=0H / Register Address: DH)

Table 29 Frequency Control

Rf 2	Rf 1	Rf 0	Feedback Resistor Value
0	0	0	Reference Value
0	0	1	0.8 x Reference Value
0	1	0	0.9 x Reference Value
0	1	1	1.1 x Reference Value
1	0	0	1.2 x Reference Value
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

(14-22) Discharge ON/OFF

Discharge circuit is used to discharge out of the stabilizing capacitors placed on the V_{LCD}, V₁, V₂, V₃, V₄ and V_{OUT}. Refer to “(11-4) Discharge Circuit”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	0	*	*	*	DIS

(Default: DIS₂, DIS₁=0H / Register Address: EH)

D₀ (DIS)

DIS=0 : Discharge OFF

DIS=1 : Discharge ON (Discharge from V_{LCD}, V₁, V₂, V₃ and V₄)

NOTE) Resistance is 100KΩ typical.

(14-23) Register Address

The “Register Address” instruction specifies a register address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	RA3	RA2	RA1	RA0

(Default: RA3-RA0=BH / Register Address: CH)

(14-24) Register Read

The “Register Read” instruction reads out instruction data from the register which address is specified by the “Register Address” instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
*	*	*	*	Internal register data			

(14-25) Window End Column Address

The “Window End Column Address” instruction specifies the column address of the end point. Refer to “(4-2) Window Area for DDRAM Access”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	EX3	EX2	EX1	EX0

(Default: EX3-EX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	EX7	EX6	EX5	EX4

(Default: EX7-EX4=0H / Register Address: 1H)

(14-26) Window End Row Address

The “Window End Row Address” instruction specifies the row address of the end point. Refer to “(4-2) Window Area for DDRAM Access”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	EY3	EY2	EY1	EY0

(Default: EY3-EY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	EY7	EY6	EY5	EY4

(Default: EY7-EY4=0H / Register Address: 3H)

(14-27) Initial Line-reverse Address

The “Initial Line-reverse Address” instruction specifies the start line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LS3	LS2	LS1	LS0

(Default: LS3-LS0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	LS7	LS6	LS5	LS4

(Default: LS7-LS4=0H / Register Address: 5H)

(14-28) Last Line-reverse Address

The “Last Line-reverse Address” instruction specifies the end line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	LE3	LE2	LE1	LE0

(Default: LE3-LE0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	LE7	LE6	LE5	LE4

(Default: LE7-LE4=0H / Register Address: 7H)

(14-29) Line Reverse ON/OFF

The “Line Reverse ON/OFF” instruction enables the line-reverse display, and blink function as well. Note that the line reverse display cannot be used for entire display area. In this case, use the reverse display function by the D₃ (REV) bit of the “Display Control (2)” instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	*	*	BT	LREV

(Default: BT,LREV=0H / Register Address: 8H)

D₀ (LREV)

LREV =0 : Line Reverse OFF (Normal)
LREV =1 : Line Reverse ON

D₁ (BT)

BT =0 : No Blink
BT =1 : Blink once every 32 frames

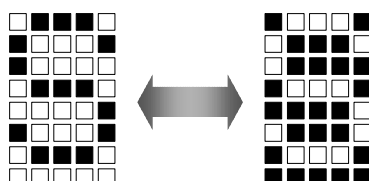


Fig 19 On-screen Image in Using Line-reverse Display and Blink Function

(14-30) Upper/Lower Palette Select

The “Upper/Lower Palette Select” instruction selects either upper or lower palette register.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PS

(Default: PS=0 / Register Address: 9H)

D₀ (PS)

PS=0 : Lower Palettes (PA00, PA01, PA02, PA03, ..., PC74)
 PS=1 : Upper Palettes (PA80, PA81, PA82, PA83, ..., PC154)

(14-31) PWM Control

The “PWM control” instruction selects PWM type, as shown in Fig 20.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PWMS	PWMA	PWMB	PWMC

(Default: PWMS,PWMA,PWMB,PWMC=0H / Register Address: AH)

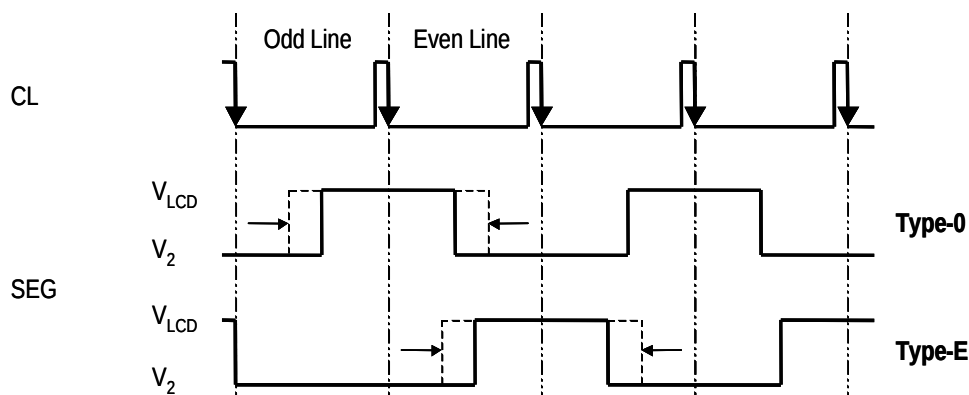
D₃ (PWMS)

PWMS=0 : Type 1
 PWMS=1 : Type 2

D₂ (PWMA), D₁ (PWMB), D₀ (PWMC)

PWMZ=0 (Z=A, B and C): Type 1-O
 PWMZ=1 (Z=A, B and C): Type 1-E

PWM Type 1 (PWMS=0)



PWM Type 2 (PWMS=1)

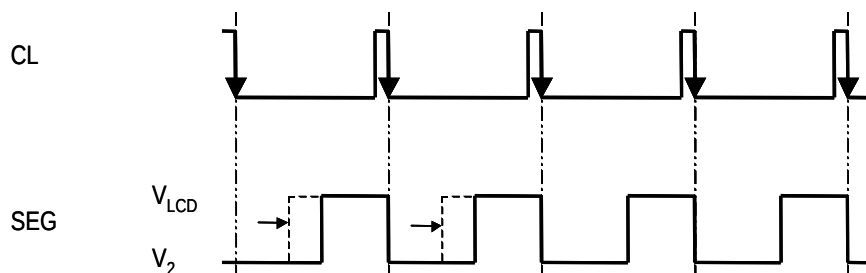


Fig 20 PWM Control

(15) PARTIAL DISPLAY FUNCTION

The partial display function activates specified area on an LCD screen, or equivalently, common drivers are simply scanning this specified area. This function allows LCD modules to work in a minimum duty cycle ratio to minimize power consumption. The partial display function is carried out by the combination of the “Duty Cycle Ratio”, “LCD Bias Ratio”, “Boost Level” and “EVR Control” instructions. For more information, refer to “(14-11) Duty Cycle Ratio”, “(14-12) Boost Level”, “(14-13) LCD Bias Ratio” and “(14-20) EVR Control”. Typical setting sequence is shown in “(18-4) Partial Display Sequence”.

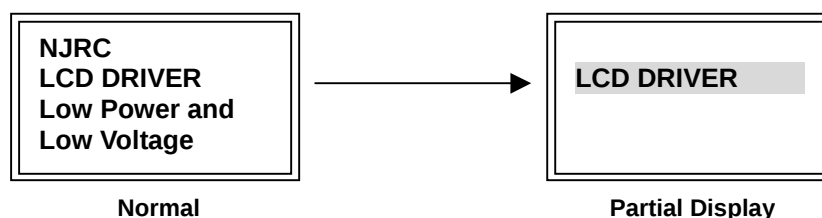
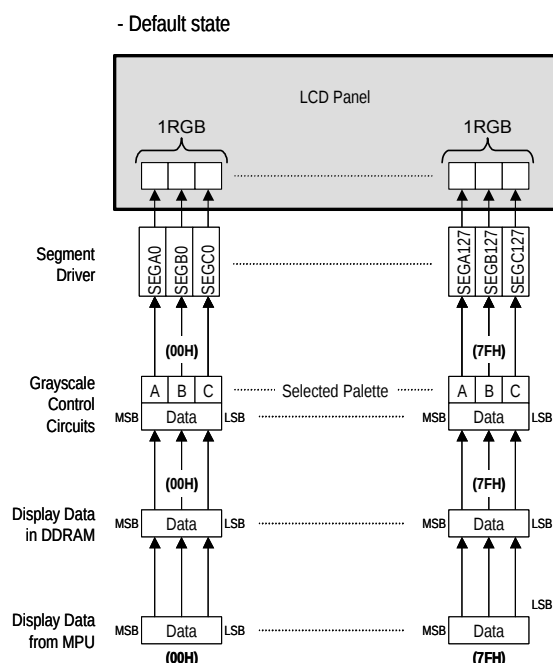


Fig 21 On-screen Image in Using Partial Display Function

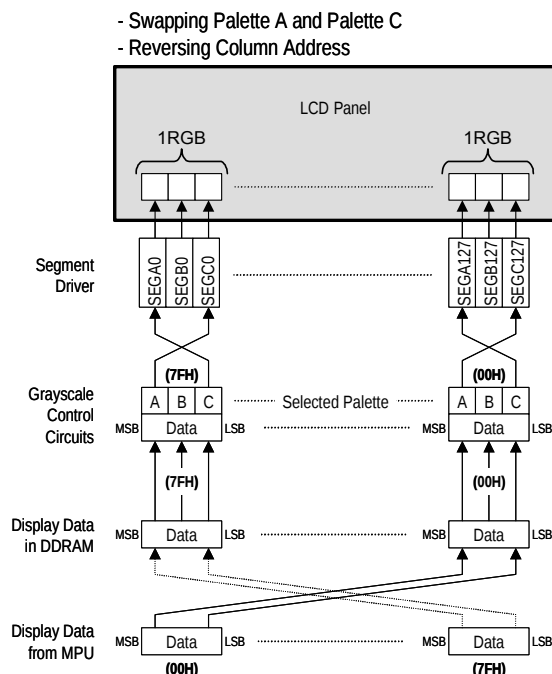
(16) SWAP FUNCTION

The swap function switches the palettes A_j and the palettes C_j ($j=0-15$), and is controlled by the D_1 (SWAP) bit of the “Display Control (2)” instruction. This function reduces the restrictions on the IC position of an LCD module. Fig 22 “Overview of Swap Function” illustrates general outlines of internal operations, and (16-1-1) through (16-1-4) show each configuration on a mode-by-mode basis.

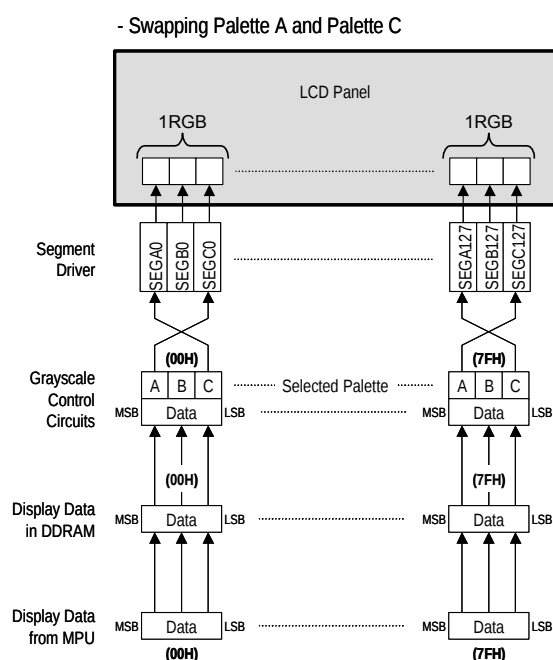
(SWAP, REF)=(0,0)



(SWAP, REF)=(0,1)



(SWAP, REF)=(1,0)



(SWAP, REF)=(1,1)

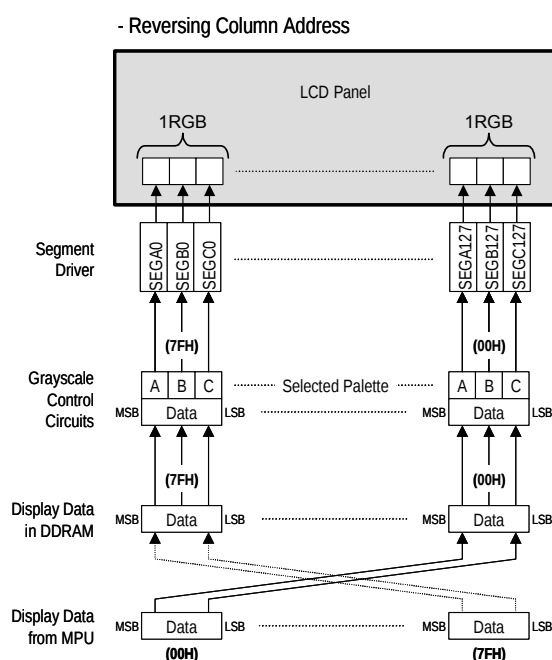
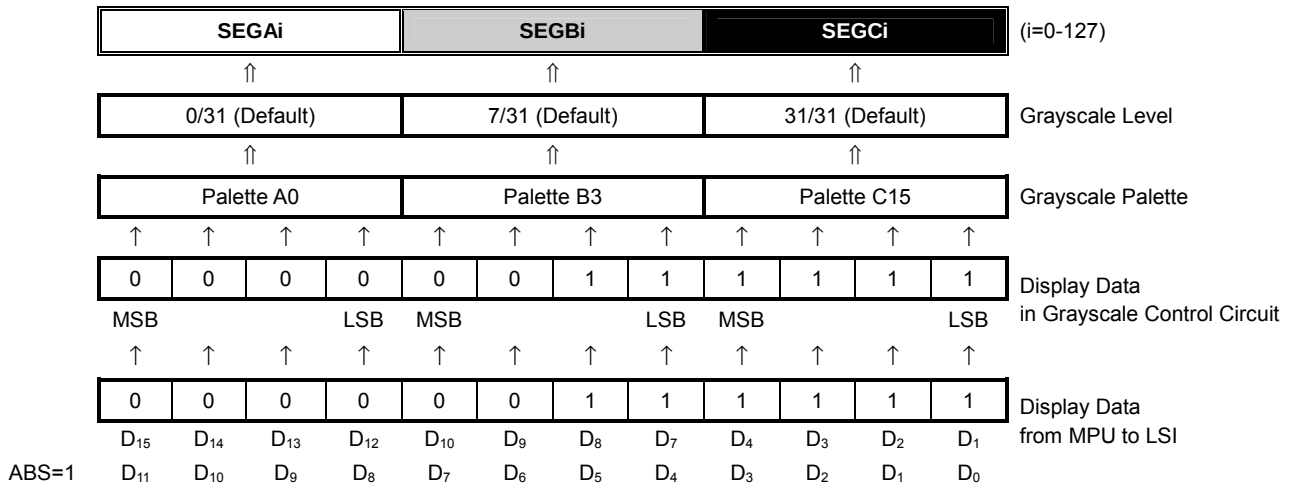


Fig 22 Overview of SWAP Function

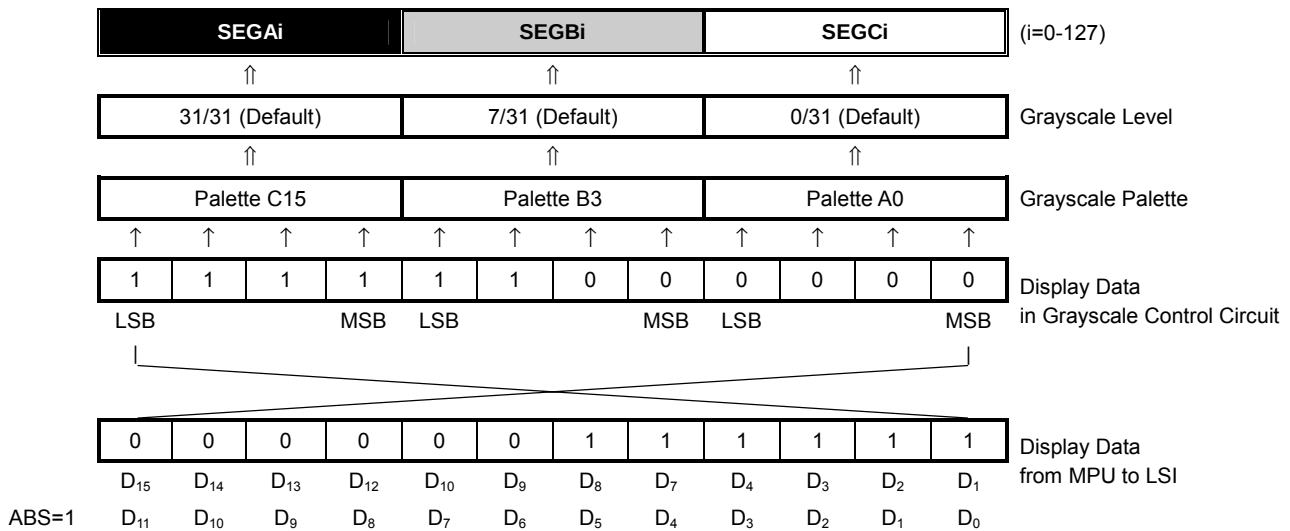
(16-1) Swap Function in Variable 16-grayscale Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



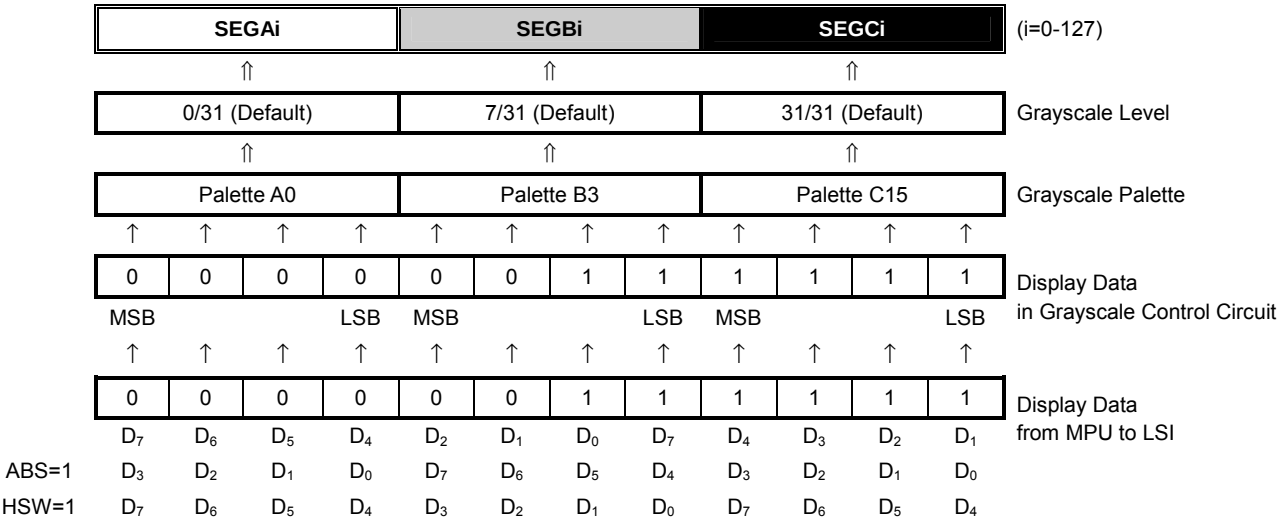
(REF, SWAP)=(0,1) or (1,0)



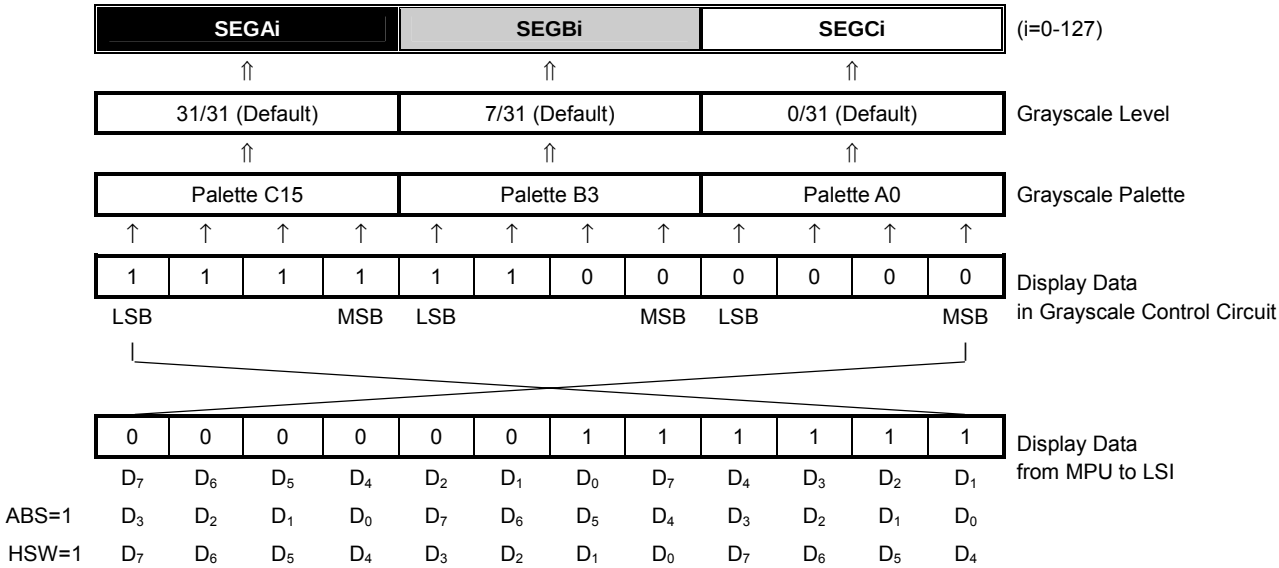
NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

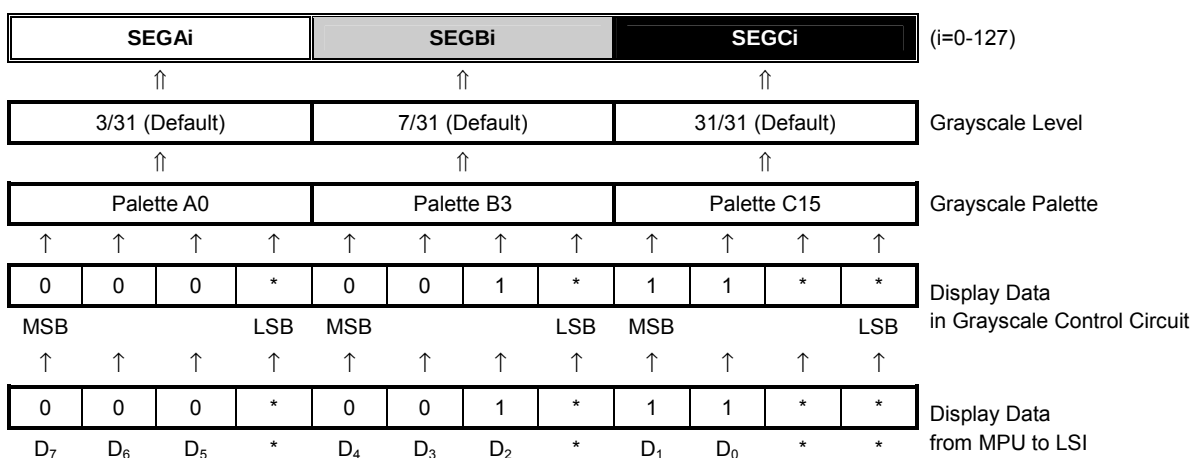


NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.

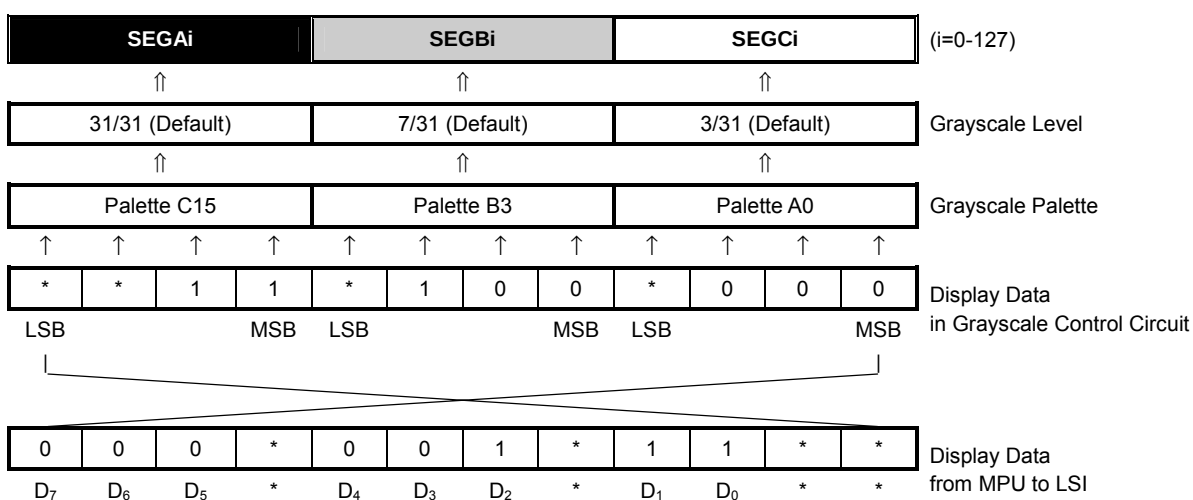
(16-2) Swap Function in Variable 8-grayscale Mode

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

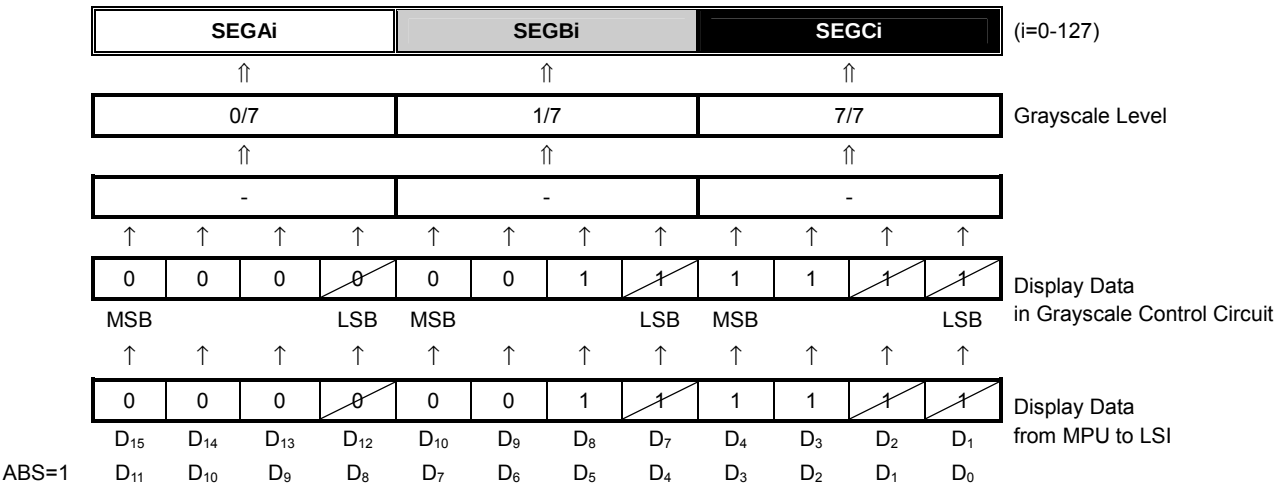


NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".

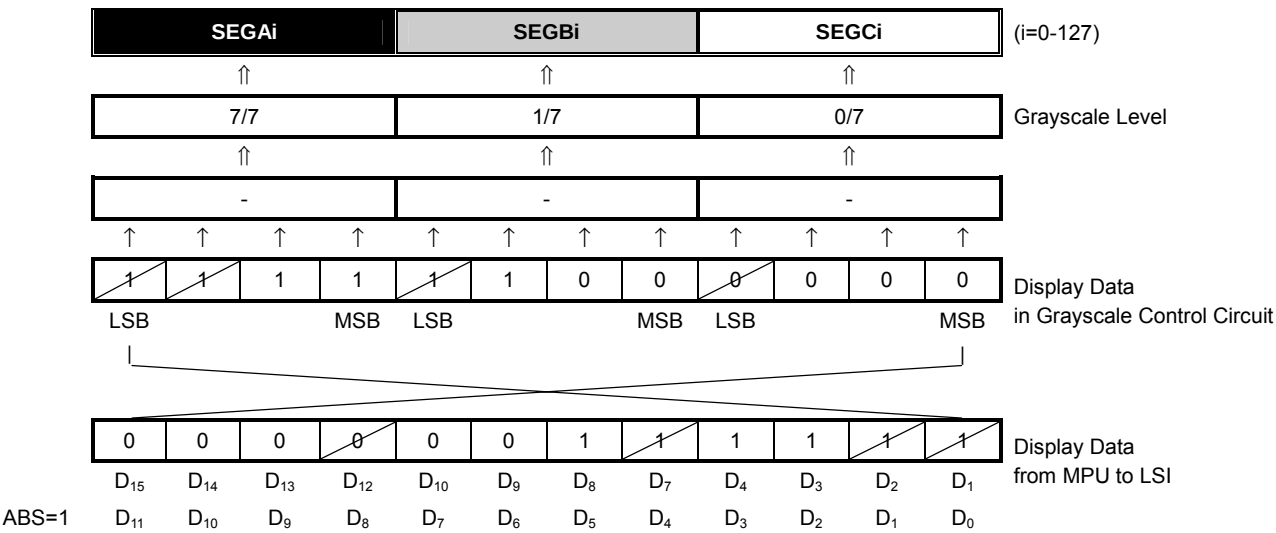
(16-3) Swap Function in Fixed 8-grayscale Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



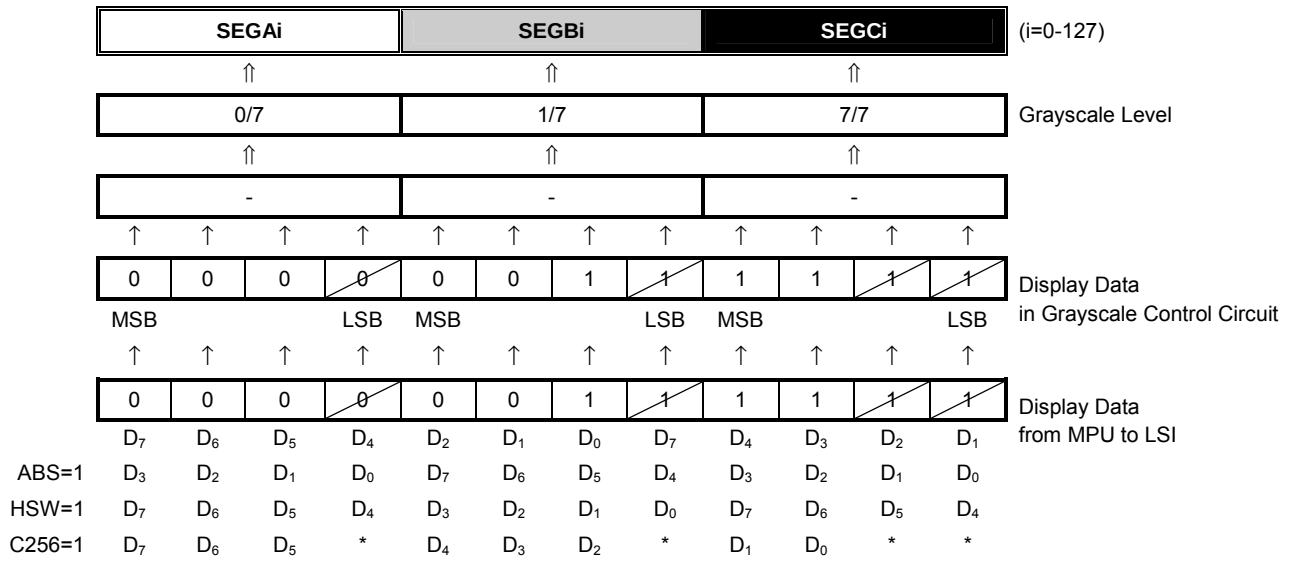
(REF, SWAP)=(0,1) or (1,0)



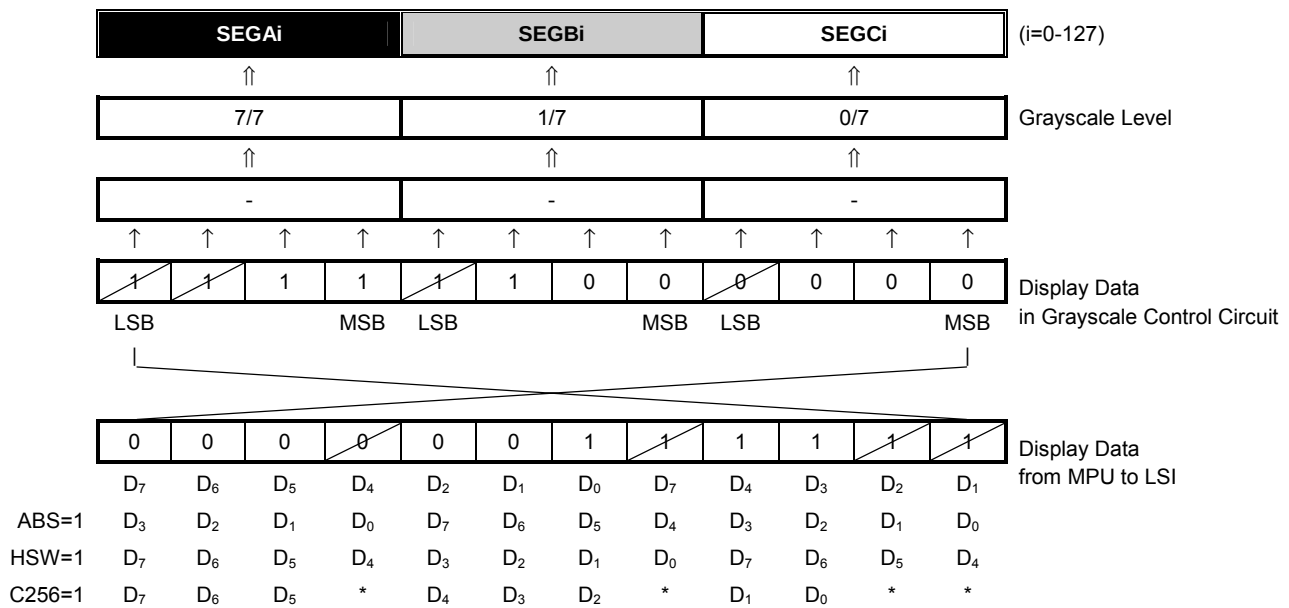
NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)



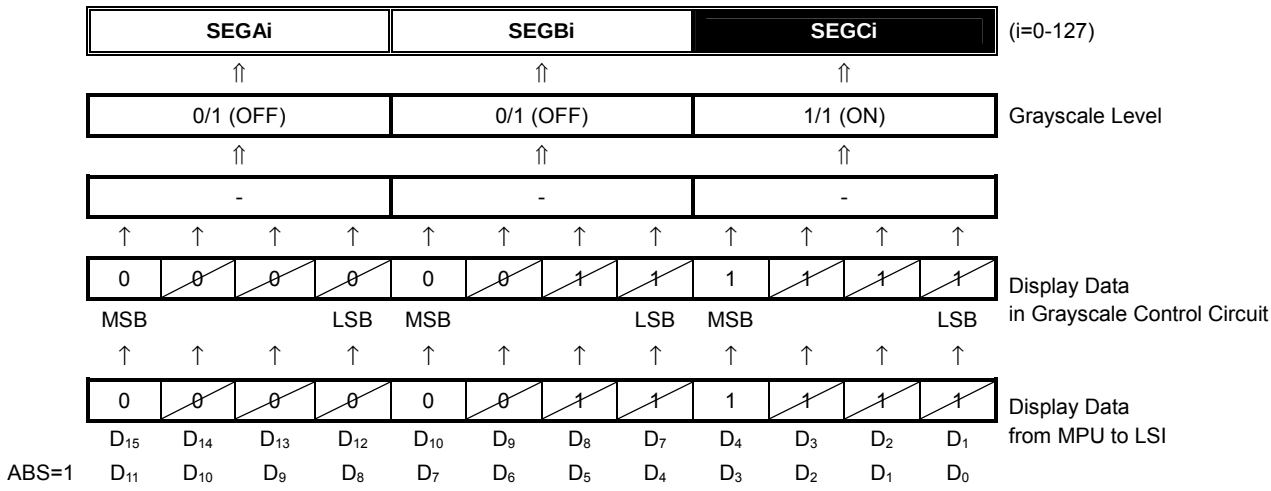
NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".

NOTE2) The data indicated with a slash mark (/) is invalid.

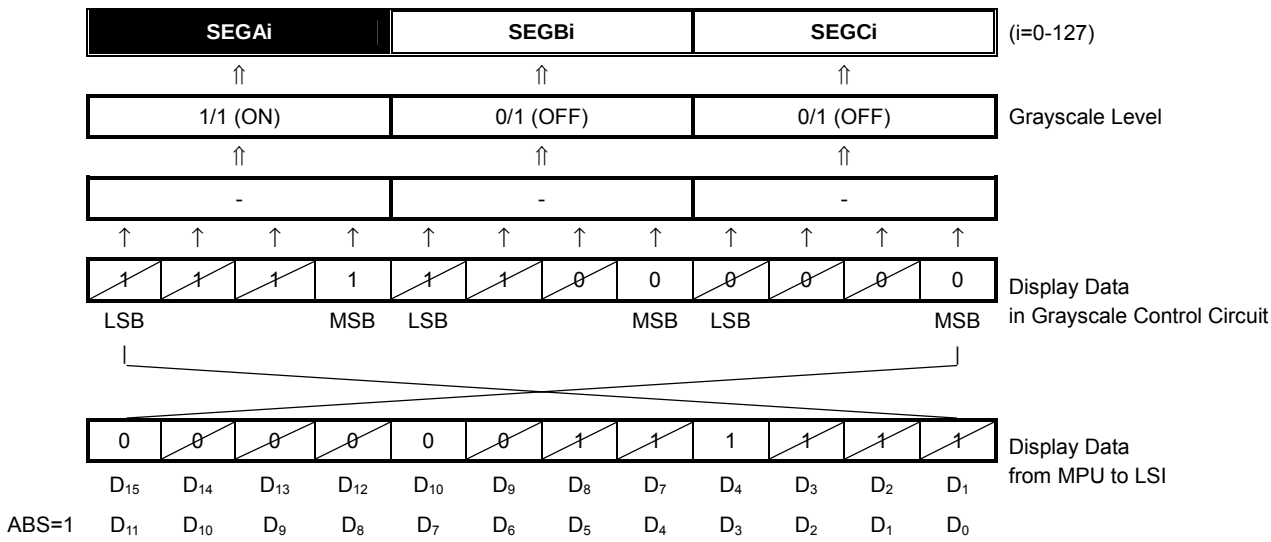
(16-4) Swap Function in B&W Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



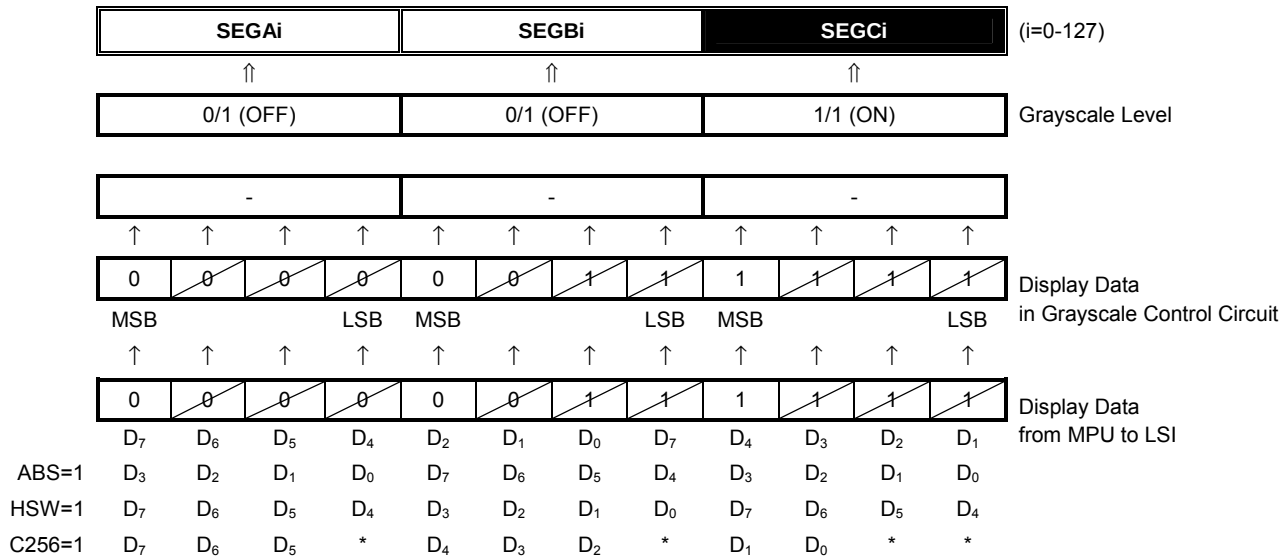
(REF, SWAP)=(0,1) or (1,0)



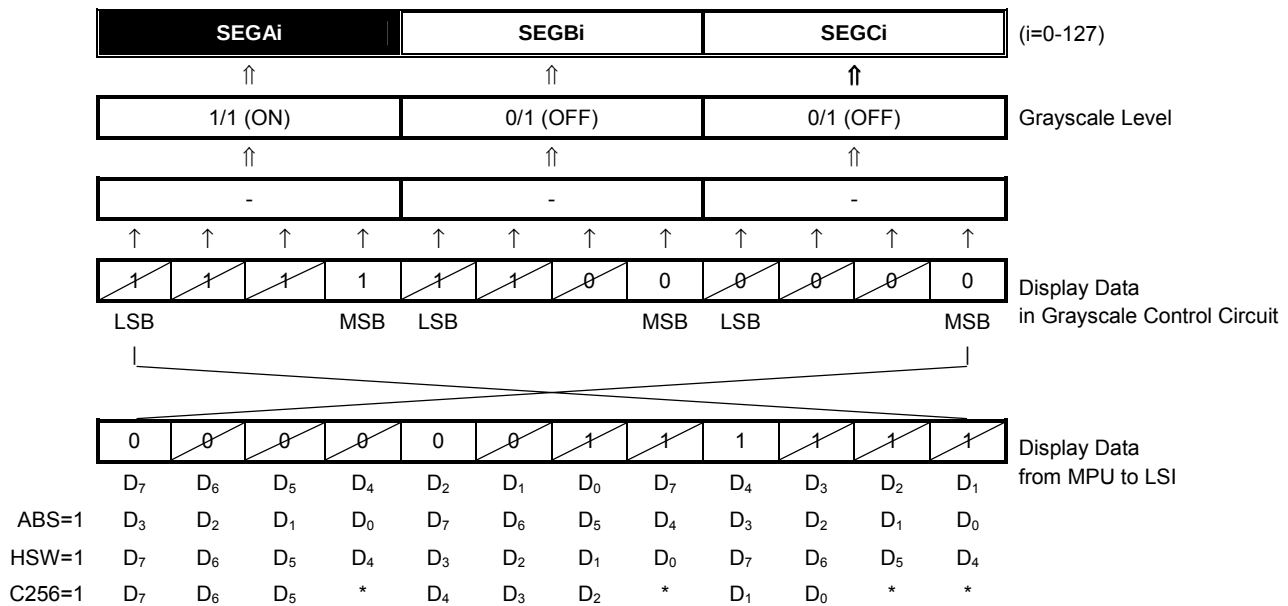
NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

SWAP=0



SWAP=1



NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".

NOTE2) The data indicated with a slash mark (/) is invalid.

(17) RELATION BETWEEN ROW ADDRESS AND COMMON DRIVER

The relation between row address and common driver is changed by the D₃ (SHIFT) bit of the "Display Control (1)" and the "Duty Cycle Ratio", "Initial Display Line" and "Initial COM" instructions.

When the "Initial Display Line" is set to (LA7:LA0=00H: Address "0"), the row address corresponding to an initial COM is "0". However, if the "Initial Display Line" is other than "0", the row address is shifted from "0" by just that address. For instance, when the initial display line address is (LA7:LA0=05H: Address "5") and the initial COM is (SC3:SC0=1H), the row address on the initial COM is "5" and the initial COM is "COM₁".

(17-1) through (17-5) illustrate the examples of the relation between row address and common driver.

SHIFT="0"(Common forward scan), DS_{3, 2, 1, 0}="0000", LA₇....LA₀="00000000"(Initial display line 0) DSE="0"

NOTE2) Segment waveforms for 163rd COM timing are the same as for 162nd COM timing (Row address "A1H").

	SHIFT="0"(Common forward scan), DS _{3,2,1,0} ="1111", LA ₇ ...LA ₀ ="00000000"(Initial display line 0) DSE="1"
--	---

SHIFT="0"(Common forward scan), DS _{3,2,1} , o="1111", LA ₇ ...LA ₀ ="00000000"(Initial display line 0) DSE="1"																			
SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
COM ₁				0															
COM ₁					0														
COM ₂																			
COM ₃																			
COM ₄						0													
COM ₅																			
COM ₆																			
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Fig 25 Relation between Row address and Common Driver (3)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

SHIFT="0"(Common forward scan), DS_{3, 2, 1, 0}="0000", LA₇...LA₀="00000101"(Initial display line 5) DSE="0"

“

```

PROT=1, _DOT=dot, _OFS=OFS, _INITIAL=INITIAL, _END=END, _DISP=DISP, _INFO=INFO

```

(17-5) SHIFT=0, Initial Display Line "0", Duty Cycle Ratio "1/162"

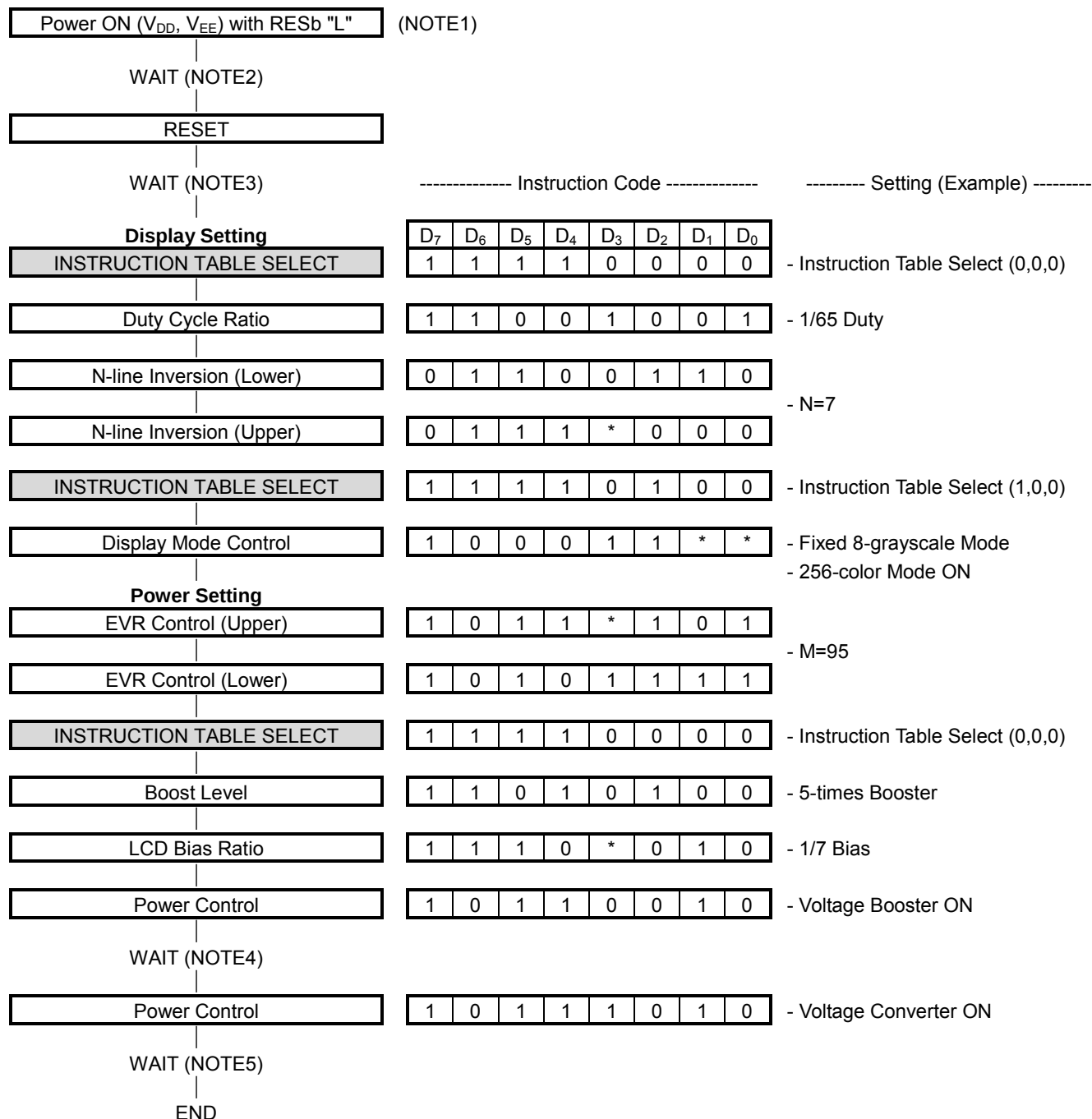
SHIFT="0" (Common forward scan), DS3, 2, 1, o="0000", LA7.....LA0="00000000"(initial display line 0) DSE="1"																			
SC3	SC2	SC1	SC0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
COM0				0	161														
COM1					0														
COM2																			
COM3																			
COM4																			
COM5																			
COM6																			
COM7																			
COM8																			
COM9																			
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COM135																			
COM136																			
COM137																			

Fig 27 Relation between Row address and Common Driver (5)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

(18) TYPICAL INSTRUCTION SEQUENCES

(18-1) Initialization Sequence in Using Internal LCD Power Supply



NOTE1) If different power sources are applied to the V_{DD} and the V_{EE} , turn on the V_{DD} first.

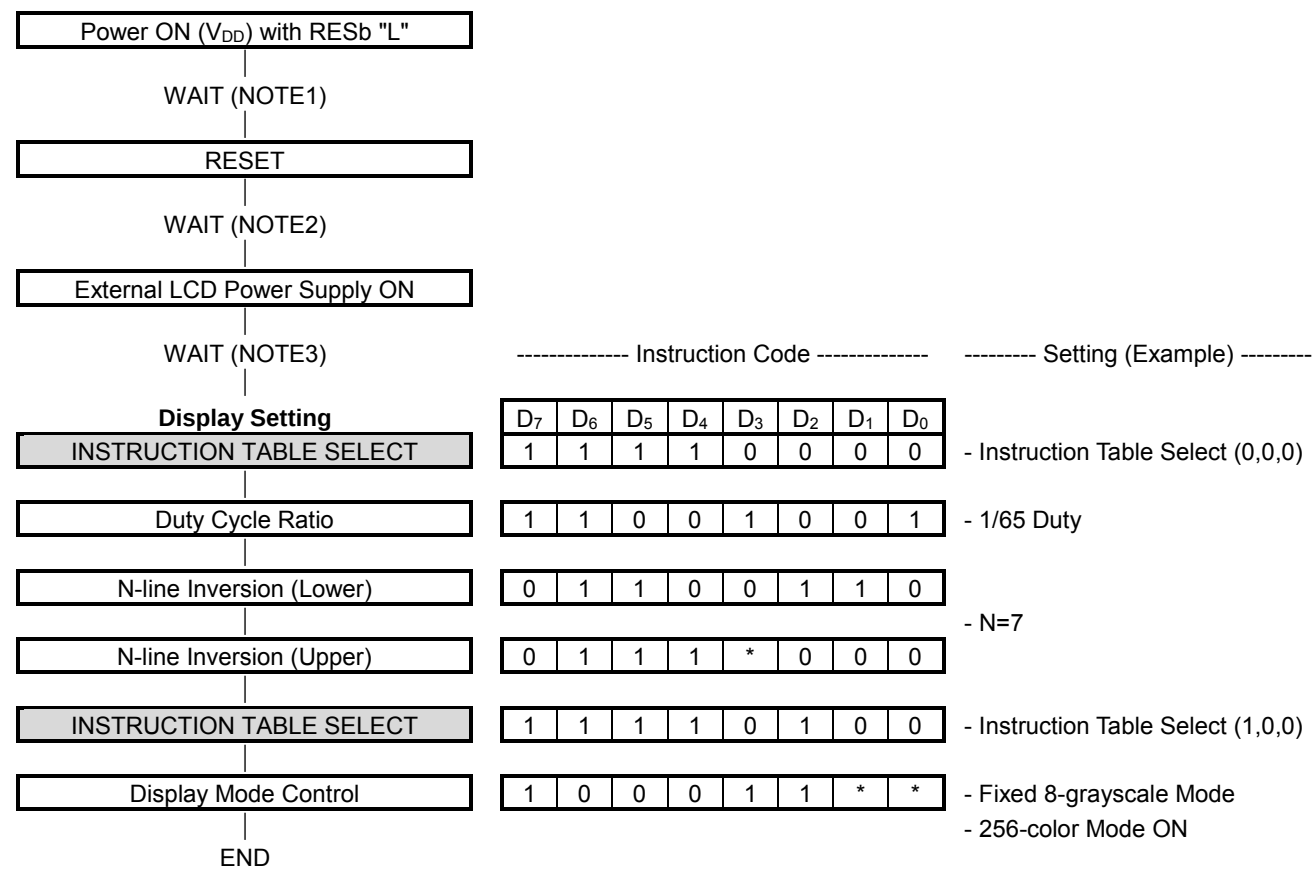
NOTE2) Wait until the V_{DD} and V_{EE} are stabilized.

NOTE3) Wait 10 [μ s] or more.

NOTE4) Wait until the V_{OUT} is stabilized.

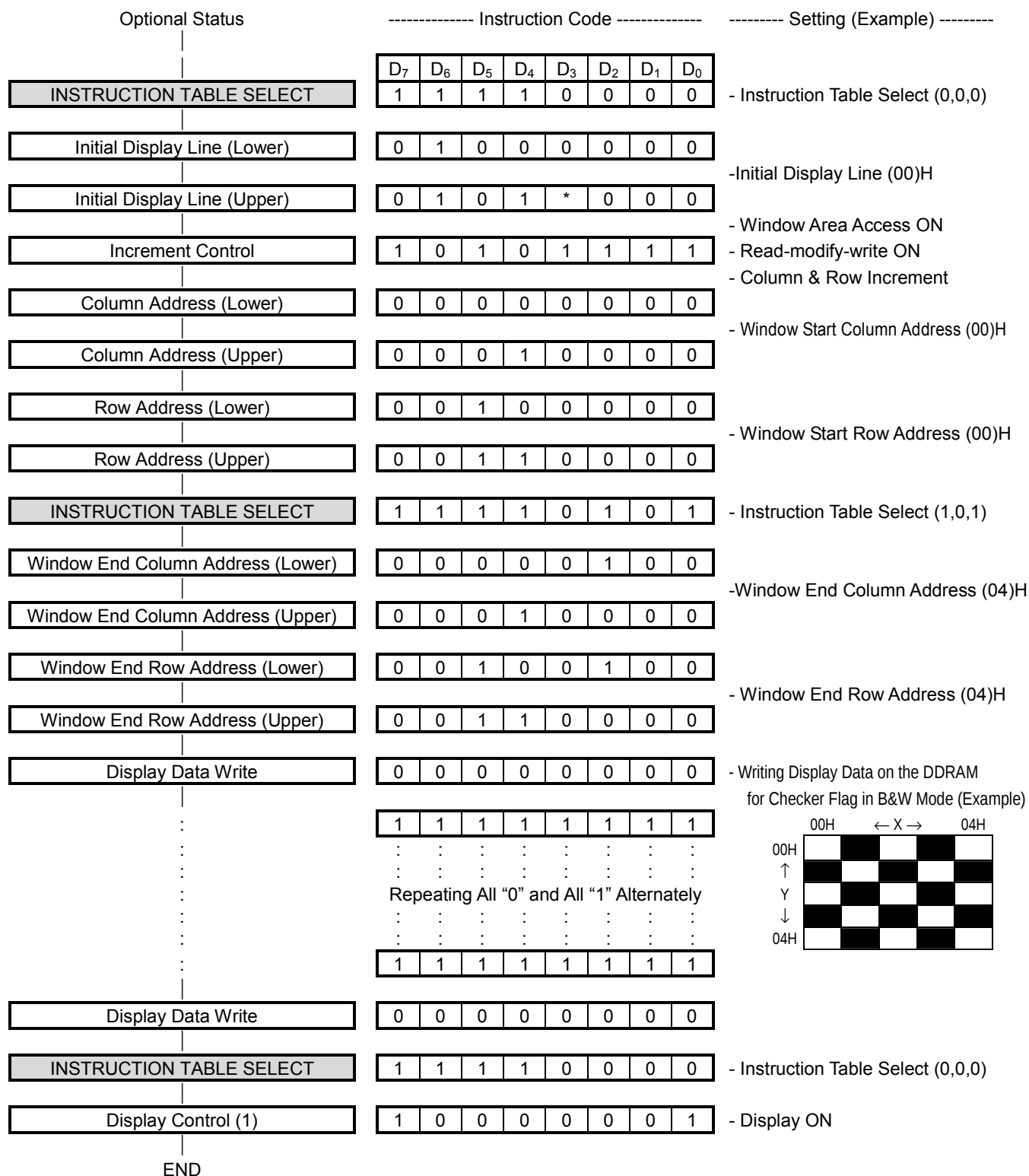
NOTE5) Wait until the V_{LCD} and V_1 - V_4 are stabilized.

(18-2) Initialization Sequence in Using External LCD Power Supply

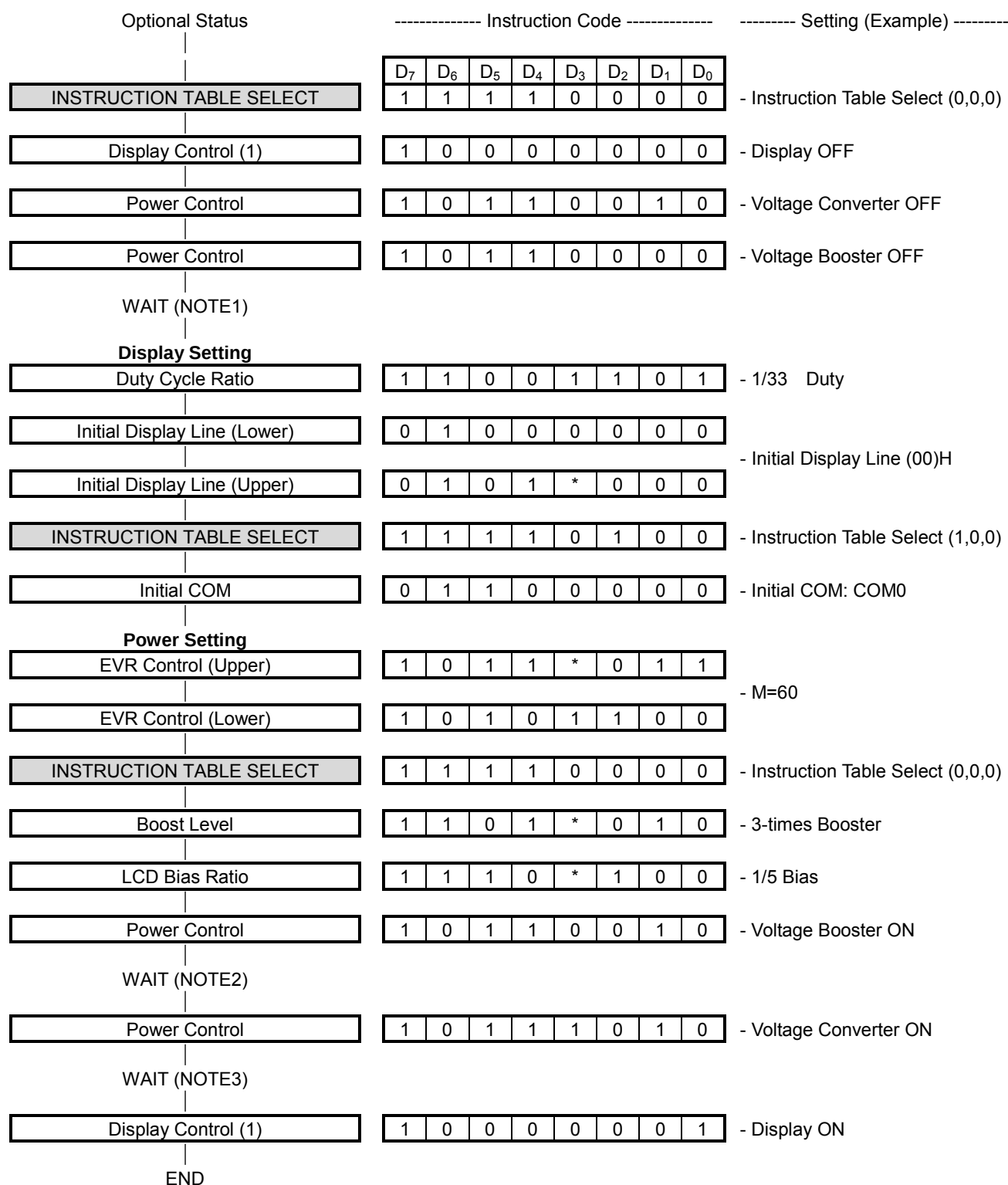


NOTE1) Wait until the V_{DD} is stabilized.
NOTE2) Wait 10 [us] or more.
NOTE3) Wait until the external LCD power supply (V_{OUT}, V_{LCD}, V₁-V₄) are stabilized.

(18-3) Display Data Write Sequence



(18-4) Partial Display Sequence

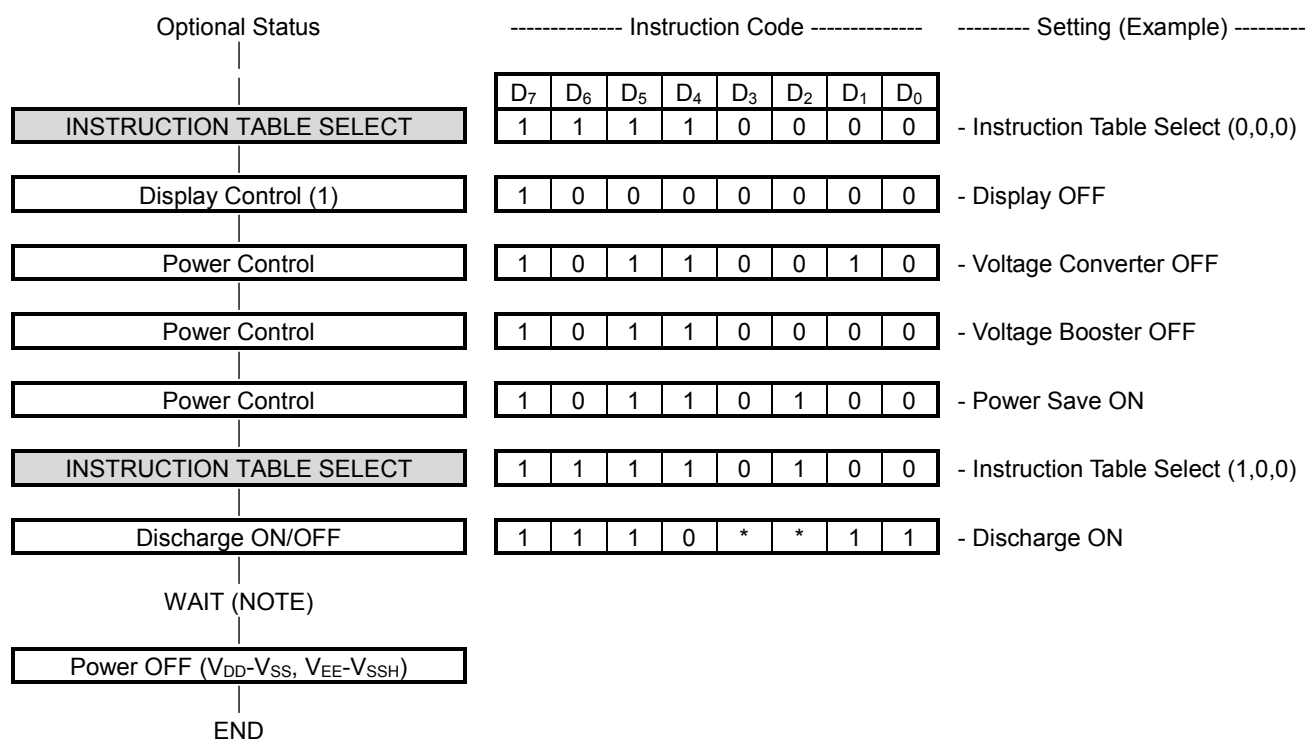


NOTE1) Wait until the voltage booster is completely turned off. Make sure what is the wait time in the particular application.

NOTE2) Wait until the V_{OUT} is stabilized.

NOTE3) Wait until the V_{LCD} and V_1 - V_4 are stabilized.

(18-5) Power OFF Sequence



NOTE) Wait until the Discharge is completed.

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	$V_{SS}=0V$ $T_a = +25^{\circ}C$	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +19.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +19.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +19.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to $V_{LCD} + 0.3$	V
Input Voltage	V_I		*1	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	T_{stg}			-45 to +125	$^{\circ}C$

NOTE1) D_0 to D_{15} , CSb, RS, RDb, WRb, OSC1, RESb, TEST1, and TEST2

NOTE2) To stabilize the LSI operation, place decoupling capacitors between V_{DD} and V_{SS} and between V_{EE} and V_{SSH} .

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	1
	V_{DD2}		2.4		3.3	V	2
	V_{EE}	V_{EE}	2.4		3.3	V	3
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	5
Operating Temperature	$Topr$		-30		85	$^{\circ}C$	

NOTE1) Applied to the condition when the reference voltage generator is not used.

NOTE2) Applied to the condition when the reference voltage generator is used.

NOTE3) Applied to the condition when the voltage booster is used.

NOTE4) The following relation among the LCD bias voltages must be maintained.

$$V_{SSH} < V_4 < V_3 < V_2 < V_1 < V_{LCD} < V_{OUT}$$

NOTE5) Relation: $V_{REF} < V_{EE}$ must be maintained.

■ DC CHARACTERISTICS

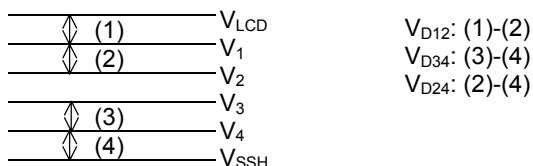
$V_{SS} = 0V$, $V_{DD} = +1.7$ to $+3.3V$, $T_a = -30$ to $+85^{\circ}C$

PARAMETER	SYM BOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}		$0.8 V_{DD}$		V_{DD}	V	*1
Low level input voltage	V_{IL}		0		$0.2V_{DD}$	V	*1
High level output voltage	V_{OH1}	$I_{OH} = -0.4mA$	$V_{DD} - 0.4$			V	*2
Low level output voltage	V_{OL1}	$I_{OL} = 0.4mA$			0.4	V	*2
High level output voltage	V_{OH2}	$I_{OH} = -0.1mA$	$V_{DD} - 0.4$			V	*3
Low level output voltage	V_{OL2}	$I_{OL} = 0.1mA$			0.4	V	*3
Input leakage current	I_{LI}	$V_I = V_{SS}$ or V_{DD}	-10		10	μA	*4
Output leakage current	I_{LO}	$V_I = V_{SS}$ or V_{DD}	-10		10	μA	*5
Driver ON-resistance	R_{ON1}	$ \Delta V_{ON} = 0.5V$					
		$V_{LCD} = 10V$		1	2	$k\Omega$	*6
		$V_{LCD} = 6V$		2	4		
Stand-by current	I_{STB}	$CSb = V_{DD}$, $T_a = 25^{\circ}C$			15	μA	*7
Internal oscillation Frequency	f_{OSC1}	$V_{DD} = 3V$ $T_a = 25^{\circ}C$	625	763	900	kHz	*8
	f_{OSC2}		141	172	203		*9
	f_{OSC3}		20.5	25	29.5		*10
External oscillation Frequency	f_{f1}	$Rf = 10k\Omega$		750		kHz	*11
	f_{f2}	$Rf = 51k\Omega$		185			
	f_{f3}	$Rf = 390k\Omega$		27.2			
Voltage converter output voltage	V_{OUT}	N-time booster ($N=2$ to 7) $RL = 500k\Omega$ ($V_{OUT} - V_{SS}$)	$(N \times V_{EE})$ $\times 0.95$			V	*12
Supply current (1)	I_{DD1}	$V_{DD} = 2.5V$, 7-time booster Whole ON pattern		870	1300	μA	*13
Supply current (2)	I_{DD2}	$V_{DD} = 2.5V$, 7-time booster Checker pattern		1060	1590		
Supply current (3)	I_{DD3}	$V_{DD} = 3V$, 6-time booster Whole ON pattern		760	1140		
Supply current (4)	I_{DD4}	$V_{DD} = 3V$, 6-time booster Checker pattern		930	1400		
Supply current (5)	I_{DD5}	$V_{DD} = 3V$, 5-time booster Whole ON pattern		520	780		
Supply current (6)	I_{DD6}	$V_{DD} = 3V$, 5-time booster Checker pattern		650	980		
Supply current (7)	I_{DD7}	$V_{DD} = 3V$, 4-time booster Whole ON pattern		360	540		
Supply current (8)	I_{DD8}	$V_{DD} = 3V$, 4-time booster Checker pattern		450	680		
V_{BA} Operating voltage	V_{BA}	$V_{EE} = 2.4$ to $3.3V$	$(0.9 V_{EE})$ $\times 0.98$	$0.9 V_{EE}$	$(0.9 V_{EE})$ $\times 1.02$	V	*14
V_{REG} Operating voltage	V_{REG}	$V_{EE} = 2.4$ to $3.3V$ $V_{REF} = 0.9 \times V_{EE}$ N-time booster ($N=2$ to 7)	$(V_{REF} \times N)$ $\times 0.97$	$(V_{REF} \times N)$	$(V_{REF} \times N)$ $\times 1.03$	V	*15
Output Voltage	V_2		-100	0	+100	mV	*16
	V_3		-100	0	+100		
	V_{D12}		-30	0	+30		
	V_{D34}		-30	0	+30		
	V_{D24}		-30	0	+30		

■ OSCILLATION FREQUENCY AND FRAME FREQUENCY

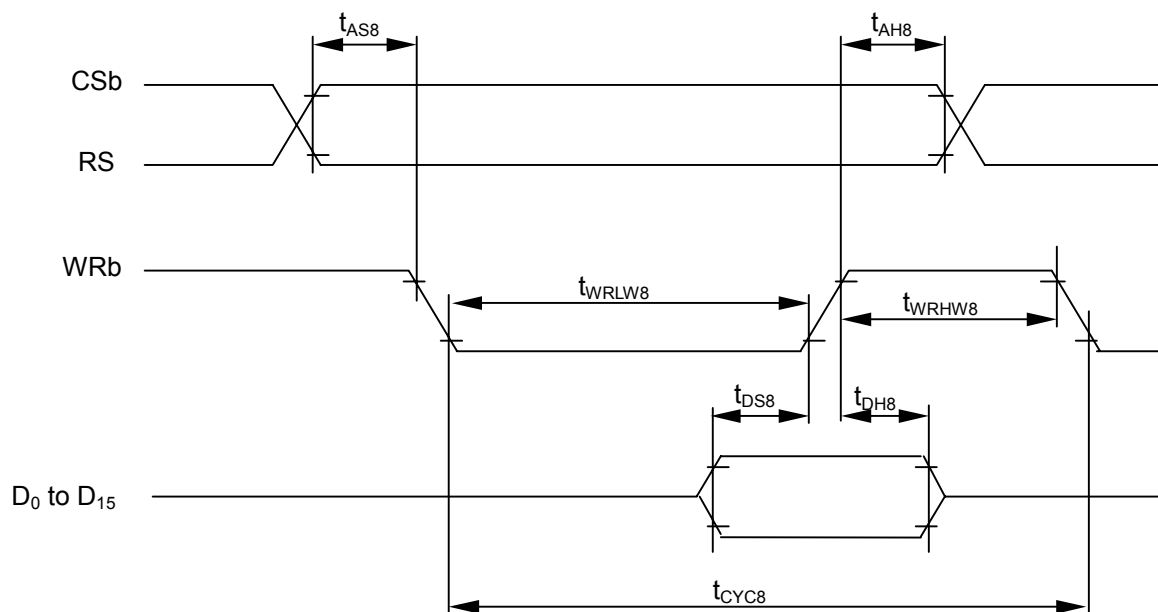
PARAMETER	SYMBOL	Display mode	Display duty cycle ratio (1/D) <DSE=0>				NOTE
			1/163 to 1/97	1/81 to 1/57	1/49 to 1/33	1/25 to 1/17	
Internal clock	f_{osc}	Variable 8-/16-level Grayscale Mode	$f_{osc} / (62xD)$	$f_{osc} / (62xDx2)$	$f_{osc} / (62xDx4)$	$f_{osc} / (62xDx8)$	FLM
		Fixed 8-level Grayscale Mode	$f_{osc} / (14xD)$	$f_{osc} / (14xDx2)$	$f_{osc} / (14xDx4)$	$f_{osc} / (14xDx8)$	
		B&W Mode	$f_{osc} / (2xD)$	$f_{osc} / (2xDx2)$	$f_{osc} / (2xDx4)$	$f_{osc} / (2xDx8)$	
External clock	f_{ck}	Variable 8-/16-level Grayscale Mode	$f_{ck} / (62xD)$	$f_{ck} / (62xDx2)$	$f_{ck} / (62xDx4)$	$f_{ck} / (62xDx8)$	
		Fixed 8-level Grayscale Mode	$f_{ck} / (14xD)$	$f_{ck} / (14xDx2)$	$f_{ck} / (14xDx4)$	$f_{ck} / (14xDx8)$	
		B&W Mode	$f_{ck} / (2xD)$	$f_{ck} / (2xDx2)$	$f_{ck} / (2xDx4)$	$f_{ck} / (2xDx8)$	

- NOTE1) D_0 - D_{15} , CSb, RS, RDb, WRb, P/S, SEL68 and RESb
- NOTE2) D_0 - D_{15}
- NOTE3) CL, FLM, FR and CLK
- NOTE4) CSb, RS, SEL68, RDb, WRb, P/S, RESb and OSC1
- NOTE5) D_0 - D_{15} in high impedance
- NOTE6) SEGA₀-SEGA₁₂₇, SEGB₀-SEGB₁₂₇, SEGC₀-SEGC₁₂₇ and COM₀-COM₁₆₁
This parameter defines the resistance between each COM/SEG and each LCD bias (V_{LCD} , V_1 , V_2 , V_3 and V_4).
- 0.5V Difference / 1/9 LCD Bias
- NOTE7) V_{DD}
Oscillator is halted.
- CSb=1 (Disabled) / No-load on COM/SEG
- NOTE8) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the Variable grayscale mode.
- (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE9) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the 8-level fixed grayscale mode.
- (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE10) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the B&W mode.
- (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE11) OSC2
- $V_{DD}=3V$ / $T_a=25^\circ C$
- NOTE12) V_{OUT}
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.
- $V_{EE}=2.4V$ to $3.3V$ / EVR= (1,1,1,1,1,1,1) / 1/5 to 1/12 LCD Bias / 1/163 Duty Cycle / No-load on COM/SEG / $RL=500k\Omega$ between V_{OUT} and V_{SSH} / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1"
- NOTE13) V_{SS}
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.
- EVR= (1,1,1,1,1,1,1) / All Pixels ON or Checker Flag Display / No-load on COM/SEG / No-access from MPU / $V_{DD}=V_{EE}$ / $V_{REF}=0.9V_{EE}$ / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1" / NLIN="0" / 1/163 Duty cycle / $T_a=25^\circ C$
- NOTE14) V_{BA}
- $V_{BA}=V_{REF}$ / Boost Level (N)="1", / DCON="0" / $V_{OUT}=13.5V$
- NOTE15) V_{REG}
- $V_{EE}=2.4V$ to $3.3V$ / $V_{REF}=0.9V_{EE}$ / $V_{OUT}=18V$ / 1/5 to 1/12 LCD bias ratio / 1/163 duty cycle / EVR=(1,1,1,1,1,1,1) / Checker flag display / No-load on COM/SEG / Boost Level (N)="2" to "7" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1" / NLIN="0"
- NOTE16) V_{LCD} , V_1 , V_2 , V_3 and V_4
- $V_{EE}=3.0V$ / $V_{REF}=0.9V_{EE}$ / $V_{OUT}=15V$ / 1/5 to 1/12 LCD Bias / EVR= (1,1,1,1,1,1,1) / Display OFF / No-load on COM/SEG / Boost Level (N)="5" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1"



■ AC CHARACTERISTICS

(1) Write Operation (Parallel Interface / 80-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		90		ns	
Enable "L" level pulse width	t_{WRLW8}		35		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		35		ns	
Data setup time	t_{DS8}		30		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

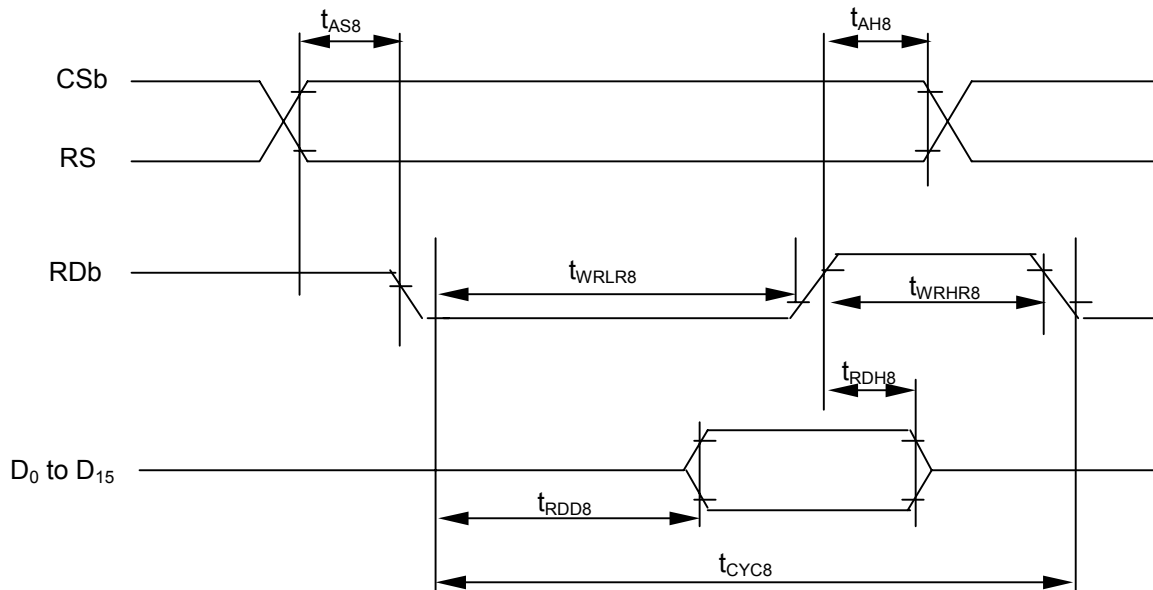
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		160		ns	
Enable "L" level pulse width	t_{WRLW8}		70		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		70		ns	
Data setup time	t_{DS8}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	
Enable "L" level pulse width	t_{WRLW8}		80		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		80		ns	
Data setup time	t_{DS8}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		10		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(2) Read Operation (Parallel Interface / 80-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	RDb
Enable "L" level pulse width	t_{WRLR8}		80		ns	
Enable "H" level pulse width	t_{WRHR8}		80		ns	
Read Data delay time	t_{RDD8}	CL=15pF	0	60	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}				ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

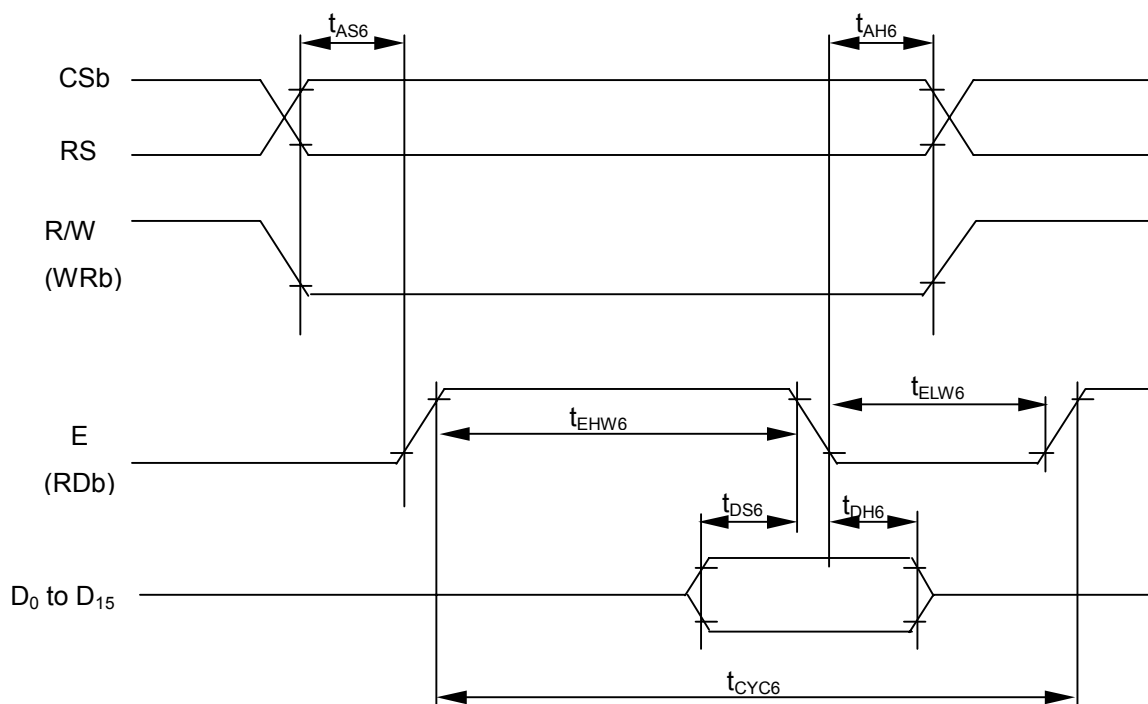
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	RDb
Enable "L" level pulse width	t_{WRLR8}		80		ns	
Enable "H" level pulse width	t_{WRHR8}		80		ns	
Read Data delay time	t_{RDD8}	CL=15pF	0	60	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}				ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		250		ns	RDb
Enable "L" level pulse width	t_{WRLR8}		120		ns	
Enable "H" level pulse width	t_{WRHR8}		120		ns	
Read Data delay time	t_{RDD8}	CL=15pF	0	110	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}				ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(3) Write Operation (Parallel Interface / 68-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		90		ns	E
Enable "L" level pulse width	t_{ELW6}		35		ns	
Enable "H" level pulse width	t_{EHW6}		35		ns	
Data setup time	t_{DS6}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

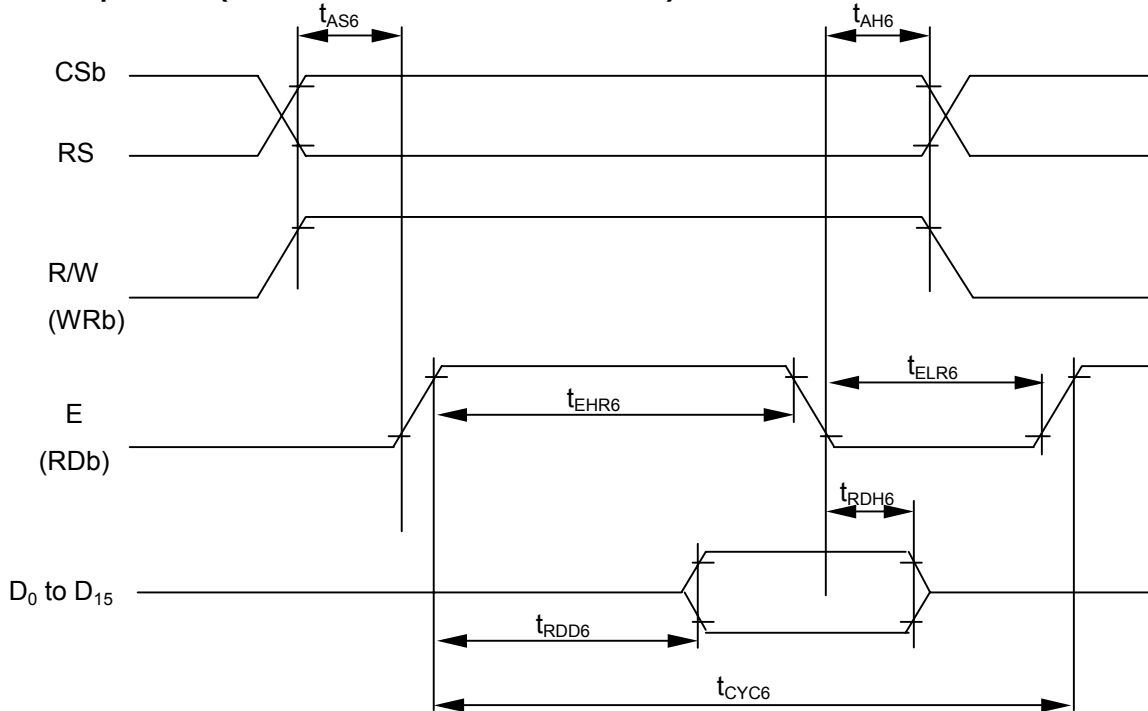
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		160		ns	E
Enable "L" level pulse width	t_{ELW6}		70		ns	
Enable "H" level pulse width	t_{EHW6}		70		ns	
Data setup time	t_{DS6}		50		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELW6}		80		ns	
Enable "H" level pulse width	t_{EHW6}		80		ns	
Data setup time	t_{DS6}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		10		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(4) Read Operation (Parallel Interface / 68-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELR6}		80		ns	
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}		0		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

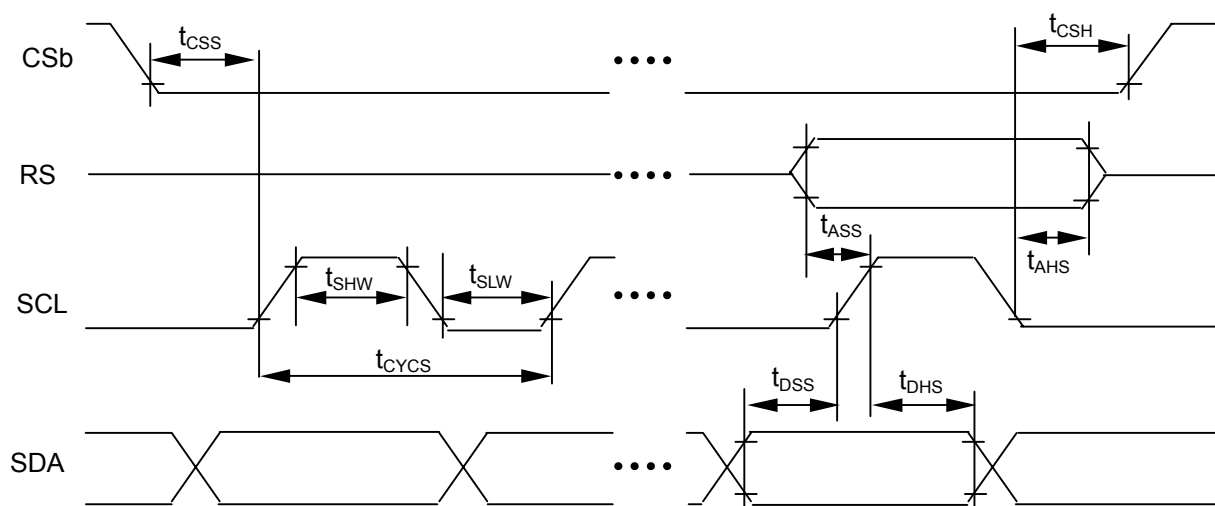
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELR6}		80		ns	
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}		0		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		250		ns	E
Enable "L" level pulse width	t_{ELR6}		120		ns	
Enable "H" level pulse width	t_{EHR6}		120		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	110	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}		0		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(5) Write Operation (Serial Interface)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

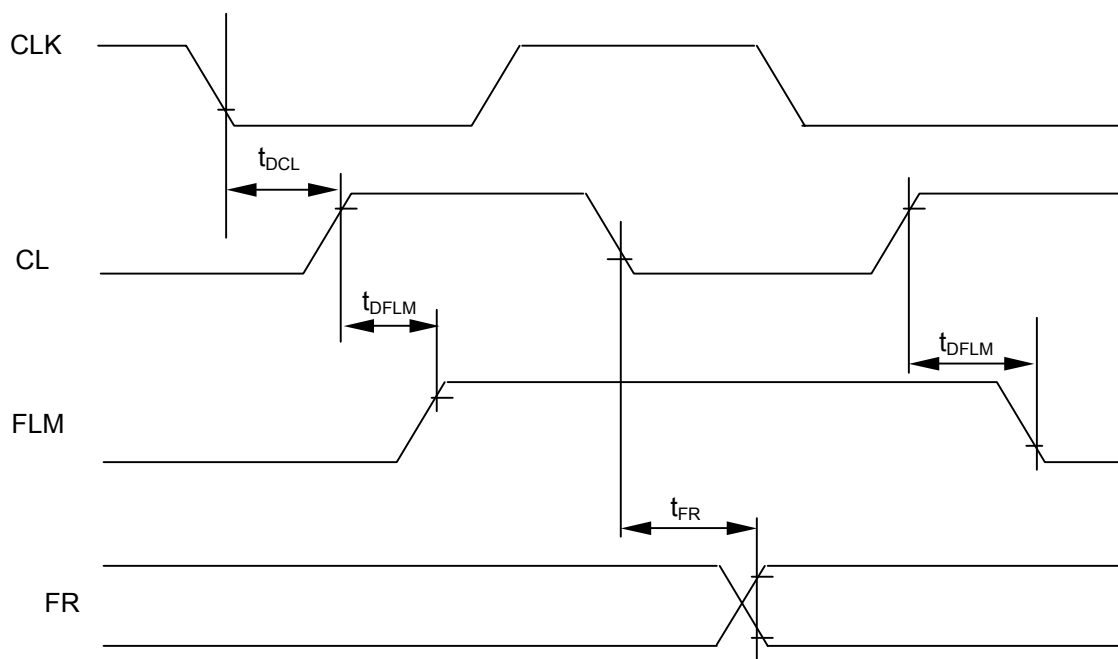
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		80		ns	SCL
SCL "H" level pulse width	t_{SHW}		35		ns	
SCL "L" level pulse width	t_{SLW}		35		ns	
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	
CSb – SCL time	t_{CSS}		35		ns	CSb
CSb hold time	t_{CSH}		35		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(6) Display Control Timing



Output timing

($V_{DD}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DCLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

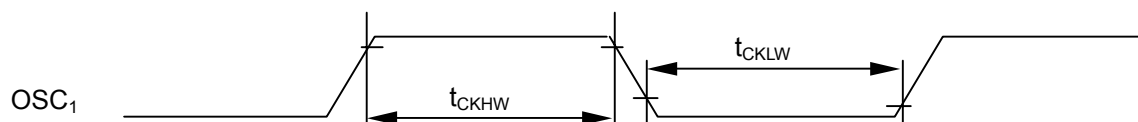
Output timing

($V_{DD}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DCLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(7) Input Clock Timing



($V_{DD}=1.7$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC1 "H" level pulse width (1)	t_{CKHW1}		0.555	0.800	μs	OSC1 (NOTE2)
OSC1 "L" level pulse width (1)	t_{CKLW1}		0.555	0.800	μs	
OSC1 "H" level pulse width (2)	t_{CKHW2}		2.46	3.54	μs	OSC1 (NOTE3)
OSC1 "L" level pulse width (2)	t_{CKLW2}		2.46	3.54	μs	
OSC1 "H" level pulse width (3)	t_{CKHW3}		16.9	24.4	μs	OSC1 (NOTE4)
OSC1 "L" level pulse width (3)	t_{CKLW3}		16.9	24.4	μs	

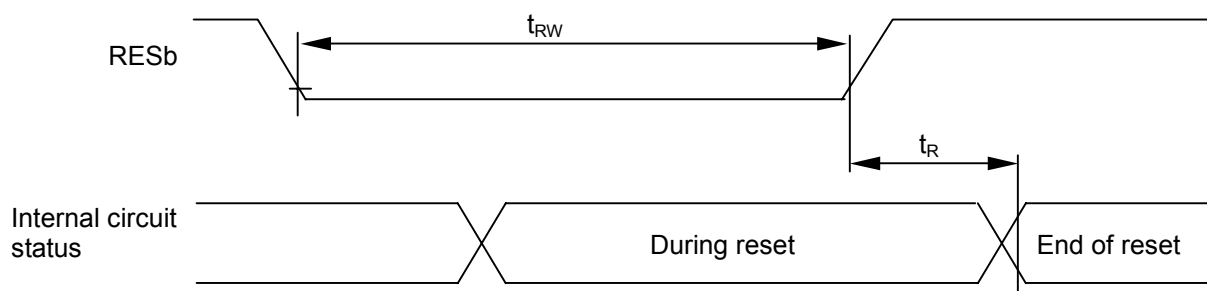
NOTE1) Each timing is specified based on 20% and 80% of V_{DD} .

NOTE2) Applied to Variable 8-/16-level grayscale mode (MON="0", PWM="0")

NOTE3) Applied to fixed 8-level grayscale mode (MON="0", PWM="1")

NOTE4) Applied to B&W mode (MON="1")

(8) Reset Input Timing



($V_{DD}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	μs	
RESb "L" level pulse width	t_{RW}		10.0		μs	RESb

($V_{DD}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	μs	
RESb "L" level pulse width	t_{RW}		10.0		μs	RESb

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

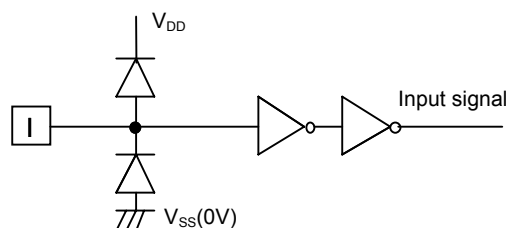
(9) Delay Time of Gate

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Delay time of gate	$T_a=+25^{\circ}C$, $V_{SS}=0V$, $V_{DD}=3.0V$		10		ns

INPUT/OUTPUT BLOCK DIAGRAMS

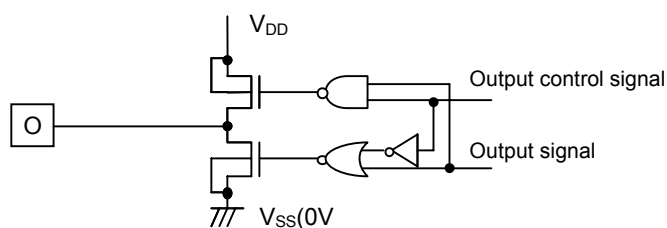
Input Block Diagram

Terminals CSb, RS, RDb, WRb, SEL68, P/S, RESb



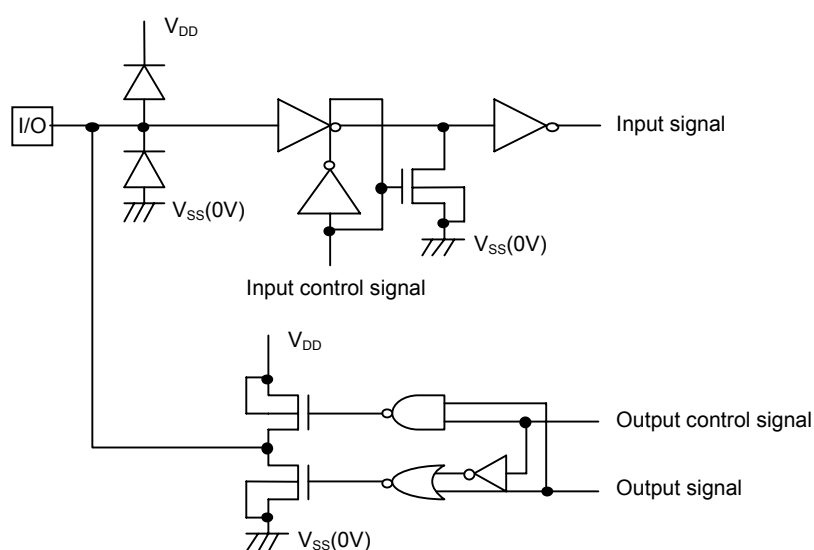
Output Block Diagram

Terminals : FLM, CL, FR, CLK



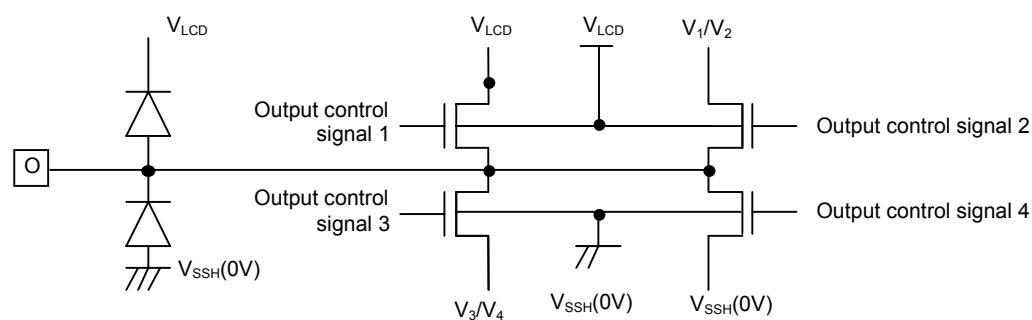
Input/Output Block Diagram

Terminals : D₀ - D₁₅



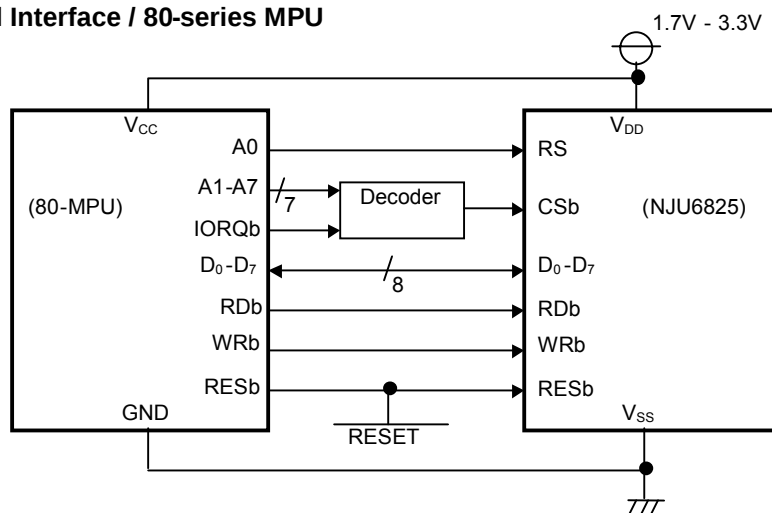
COM/SEG Driver Block Diagram

Terminals : SEGA₀/B₀/C₀ - SEGA₁₂₇/B₁₂₇/C₁₂₇, COM₀ - COM₁₆₁

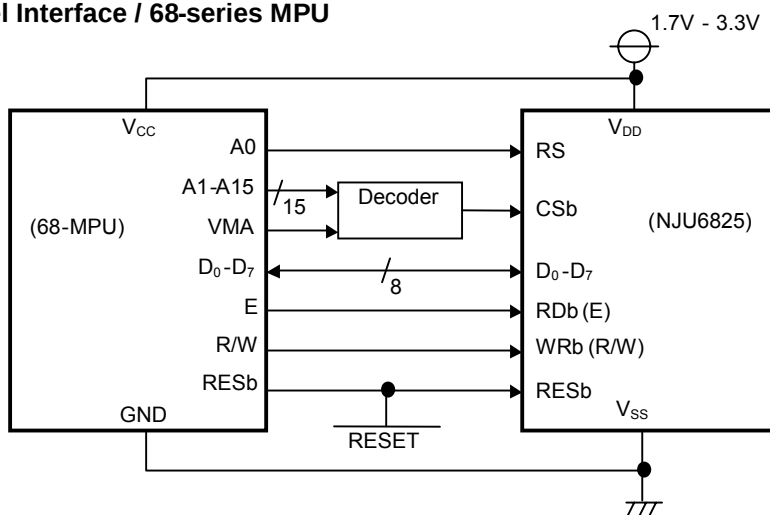


■ MPU CONNECTIONS

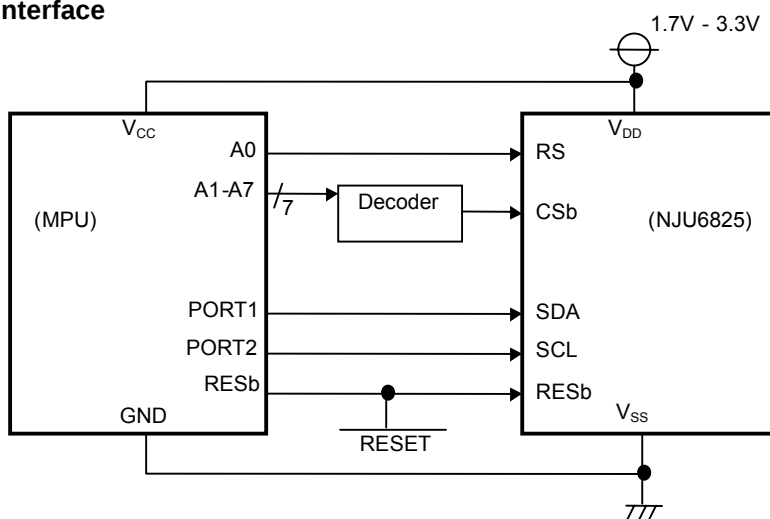
Parallel Interface / 80-series MPU



Parallel Interface / 68-series MPU



Serial Interface



[CAUTION]

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