TPS6126x, Low-Input Voltage, Boost Converter Evaluation Module

This user's guide describes the TPS6126x evaluation module (EVM) and how to perform a stand-alone evaluation to allow the EVM to interface with the system and host. The TPS61260EVM-673 converter is programmed from the factory to deliver a 3.3-Vdc output voltage for a continuous load of up to 100 mA. The boost converter can be enabled or disabled with the JP1 shunt jumper. Other options with a fixed output voltage are available.

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1 Introduction

The TPS6126x devices provide a power supply solution for products powered by either single- or dual-cell alkaline, NiCd, or NiMH batteries. It also is suitable for products powered by high-output impedance battery types, like coin cells. Output currents can go as high as 100 mA while using a single-cell alkaline battery and discharge it down to 1 V or lower. The boost converter is based on a quasi-fixed-frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low-load currents, the converter enters Power Save mode to ensure high efficiency over a wide-load current range. The maximum average current in the switches is limited to a typical value of 300 mA. The output voltage is programmable using an external resistor divider or is fixed internally on the chip. Additionally, the average output current can be programmed. The converter then regulates the programmed output voltage or the programmed output current, whichever demands lower output power. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery. The device is packaged in a 6-pin, SON PowerPAD™ package measuring 2 × 2 mm (DRV).

2 Considerations When Evaluating the TPS6126x

The TPS6126x has a voltage loop, current loop, PFM loop, and burst mode. Operations at these transitions are seamless, but one can see the waveforms adjust between modes, and they may appear erratic. If the input voltage rises up close to the output voltage, the duty cycle decreases until the minimum on-time is reached, and then the switching frequency decreases. Further increase in input voltage starts to push the output voltage higher above regulation, and the part goes into burst mode. For low-input voltage, the duty cycle increases and transitions into burst mode. This increases the ripple voltage. Increasing the load can put the IC in average current mode. This typically means dropping out of voltage regulation and going into current mode, which changes the duty cycle and frequency.

At lower input voltage, < 1 V, the maximum delivered output current is less than 100 mA; see the plot in the TPS61260/1 data sheet (SLVSA99).

Consider the impedance of the source; for higher impedances and larger loads, consider putting more input capacitance. The waveforms can look different depending on whether the load is resistive or a constant-current load.

3 Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	UNIT
Input dc voltage, DC	Recommended Vin range	0.8		4	V
Output load current, DC	Maximum load current			50	mA

4 Test Summary

The TPS61260EVM-673 board requires an adjustable laboratory power supply set between 0.8 Vdc and 4 Vdc with an input current limit set to ~450 mA and a load of 100 mA or less (>33 Ω). The test setup connections and jumper-setting selections are configured for a stand-alone evaluation, but can be changed to interface with external hardware such as a system load and microcontroller. As the input voltage drops below 1 V, the 100-mA maximum output current may roll off due to power limitations.

4.1 Equipment

- Adjustable dc power supply between 0.8 V and 4 V with adjustable current limit set to ~450 mA
- Load: system load or resistive load ≥ 33 Ω
- Three Fluke 75 digital multimeters (DMM) (equivalent or better)
- Oscilloscope, model TDS222 (equivalent or better)

4.2 Equipment and EVM Setup

Table 1. Setup I/O Connections and Configuration for Evaluation of TPS61260EVM

Jack/Component (Silk Screen)	Connect or Adjust to:
J1-1/2 (Vin)	Power supply positive lead, preset to 1.5-Vdc, 350-mA current limit
J3-1/2 (GND)	Power supply negative lead (1.5-Vdc supply)
J2-1 (+ SNS); input	Positive lead of DMM #1
J2-2 (– SNS); input	Negative lead of DMM #1
J4-1/2 (Vout)	Positive lead to system load or load resistance
J6-1/2 (GND)	Negative lead to system load or load resistance
J5-1 (+ SNS); output	Positive lead of DMM #2
J5-2 (– SNS); output	Negative lead of DMM #2
JP1-1/2 Vin/EN (On)	Apply shunt to ON for converter operation
JP1-2/3 EN/GND (Off)	See procedure

Connect the meters, scope probes, output load, shunt, and input power supply as listed in Table 1 or shown in Figure 1. Set scope to 200 ns/div, positive trigger, dc-coupled on CH1, 1 V/div; CH2: ac-coupled and 10 mV/div. Additional channels can be added or probes can be moved to view Vin and Ven. The resistive load can be replaced with a system load or decade load box to vary the load between 1 kΩ and 33 Ω.

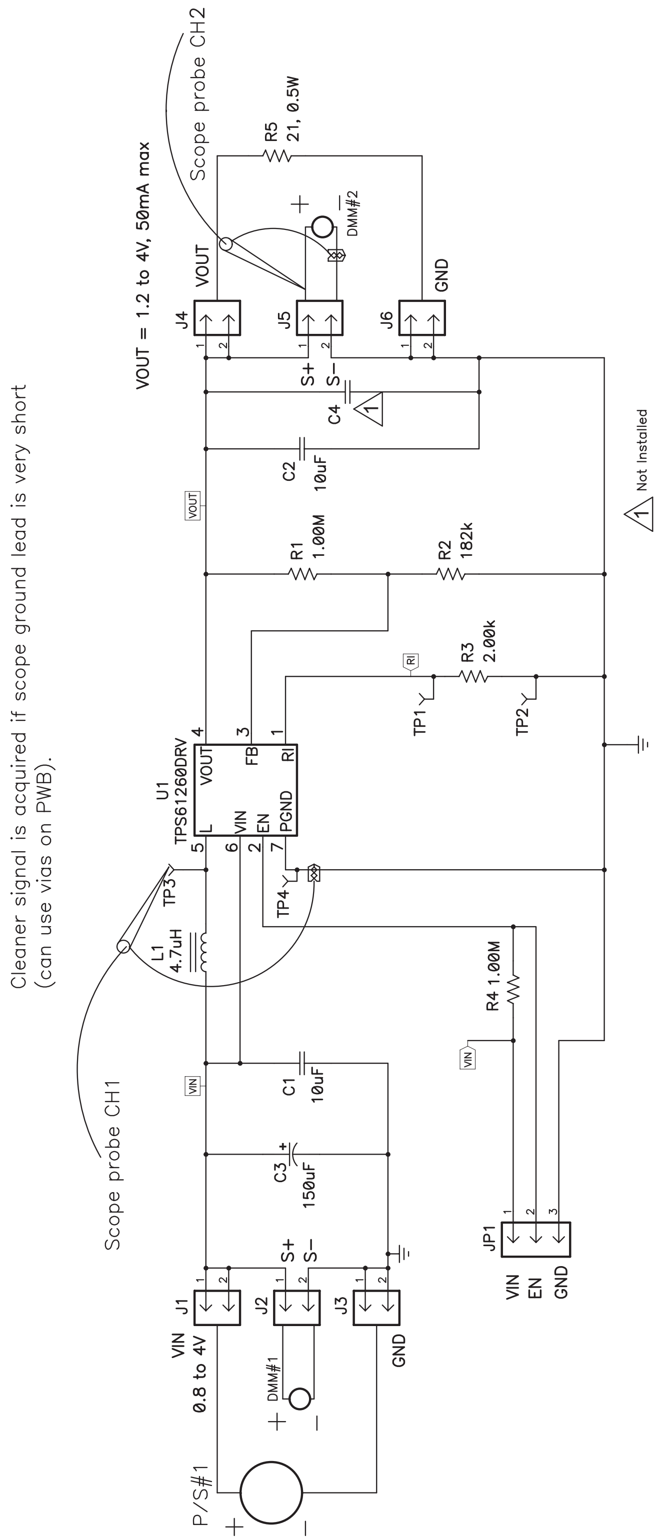

Figure 1. EVM Schematic and Evaluation Setup

4.3 Test Procedure – Input: One Alkaline Battery Cell (1.5 V) or Equivalent Power Source

1. Make sure that the EVM is set up according to Table 1 and Figure 1, and that the power supply is preset to 1.5 Vdc at ~350 mA current limit.
2. Turn on the input supply, and verify the input voltage is ~1.5 Vdc (DMM#1), and the output voltage is between 3.15 Vdc and 3.4 Vdc (DMM#2).
3. Look at CH1 and CH2, and verify that the duty cycle is between 54% and 60%, and the ripple is less than 10 mV. Note that the duty cycle is the on-time (low) divided by the period (Figure 2).
4. Move shunt on JP1-ON to JP1-OFF, and verify that the boost converter is disabled (see Figure 3).
5. Remove the shunt on JP1-OFF and place on JP1-ON. Verify that the converter starts back up (see Figure 4).
6. Vary input voltage and load to understand performance of EVM. The EVM's output cuts off when the input drops to ~0.8 V, and the circuit goes into a PFM mode when the input approaches 3.3 V.

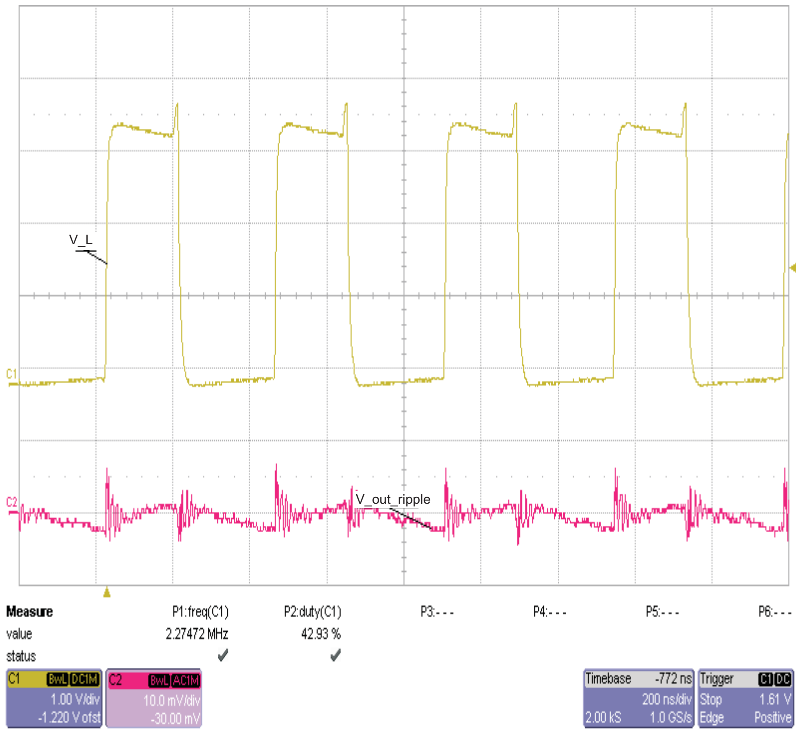

Figure 2. Boost Switch Node, V_L and Output Ripple; Vin = 1.5 V, Vout = 3.3 Vdc With 49.9-Ω Load

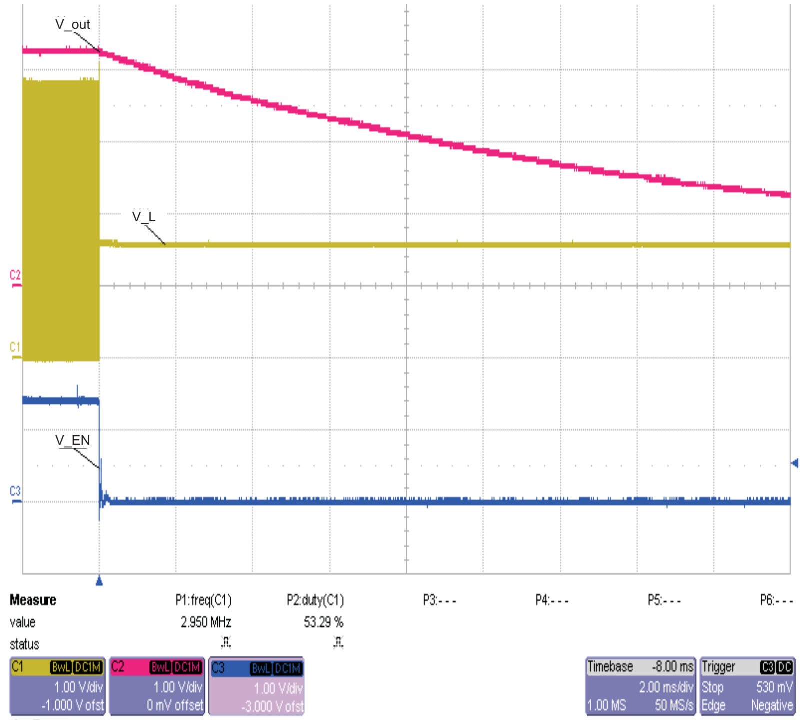

Figure 3. Power Down With Enable: Boost Switch Node, V_L, Output, Enable; Vin = 1.5 V, Vout = 3.3 Vdc With 49.9-Ω Load

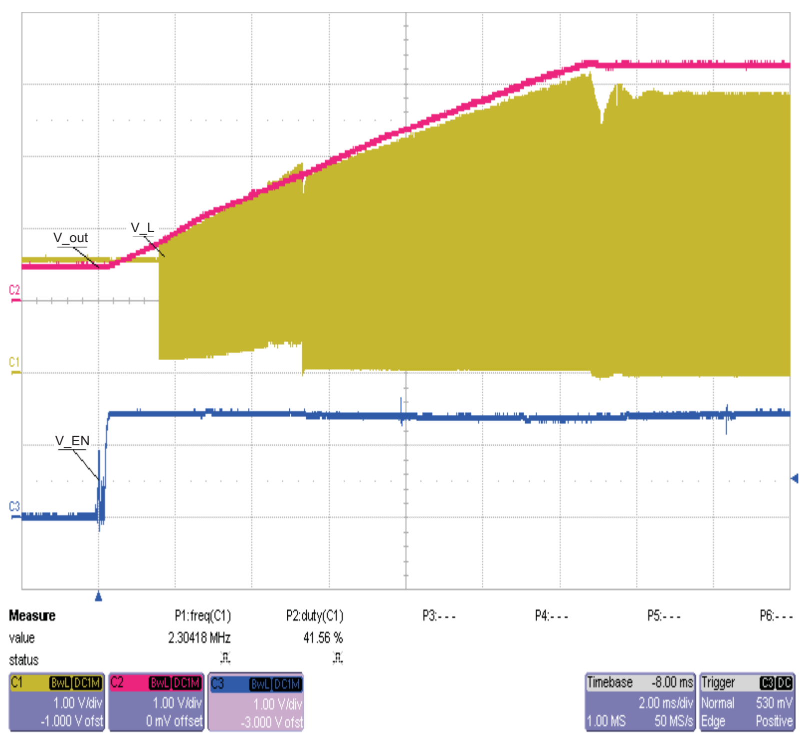

Figure 4. Power-Up With Enable: Boost Switch Node, V_L, Output, Enable; Vin = 1.5 V, Vout = 3.3 Vdc With 49.9-Ω Load

5 Schematic, Physical Layouts, and Bill of Materials

5.1 Schematic

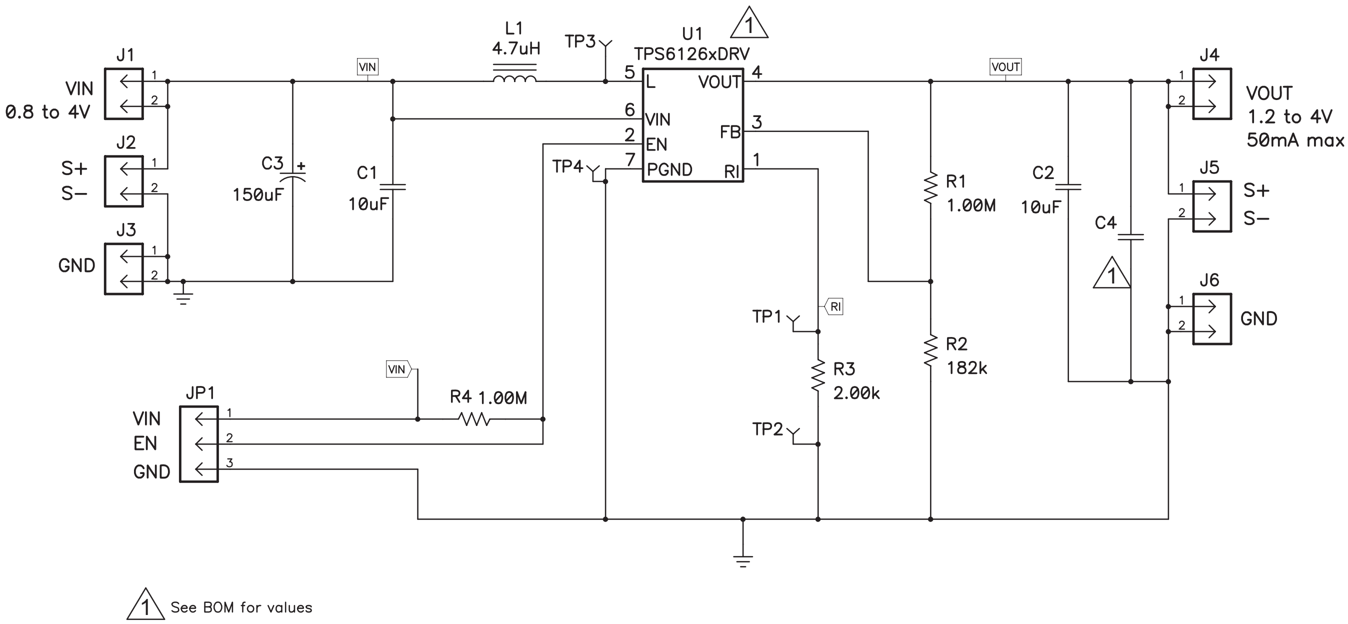

Figure 5. Schematic

5.2 Physical Layouts

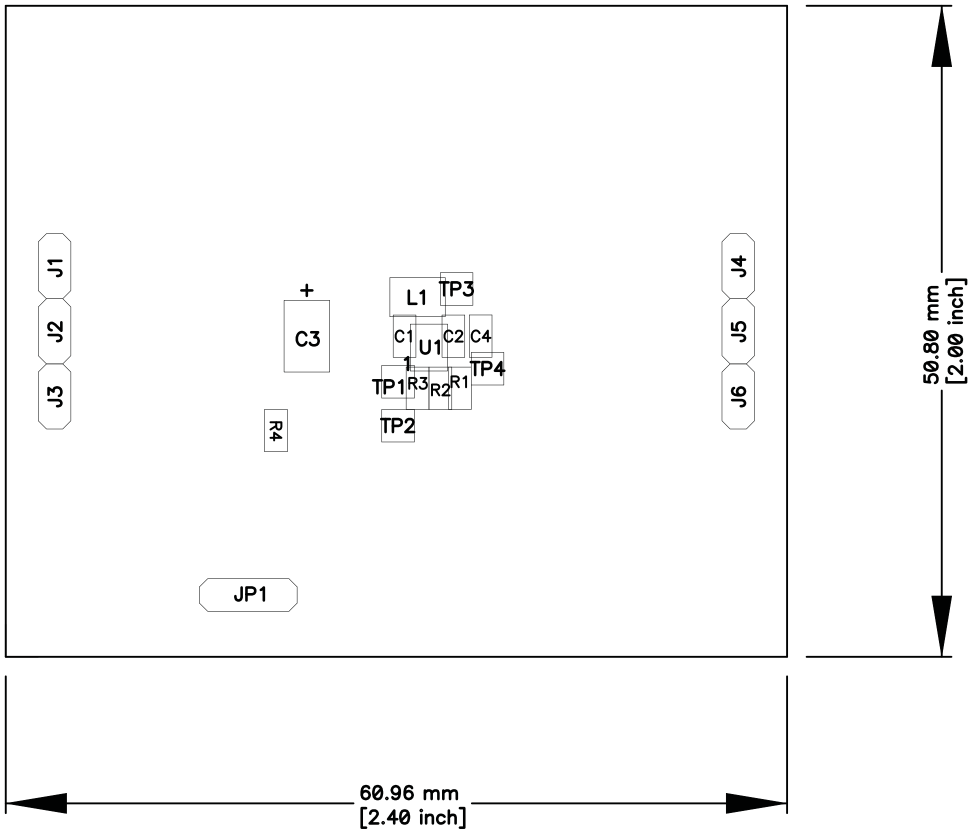

Figure 6. Assembly Layer

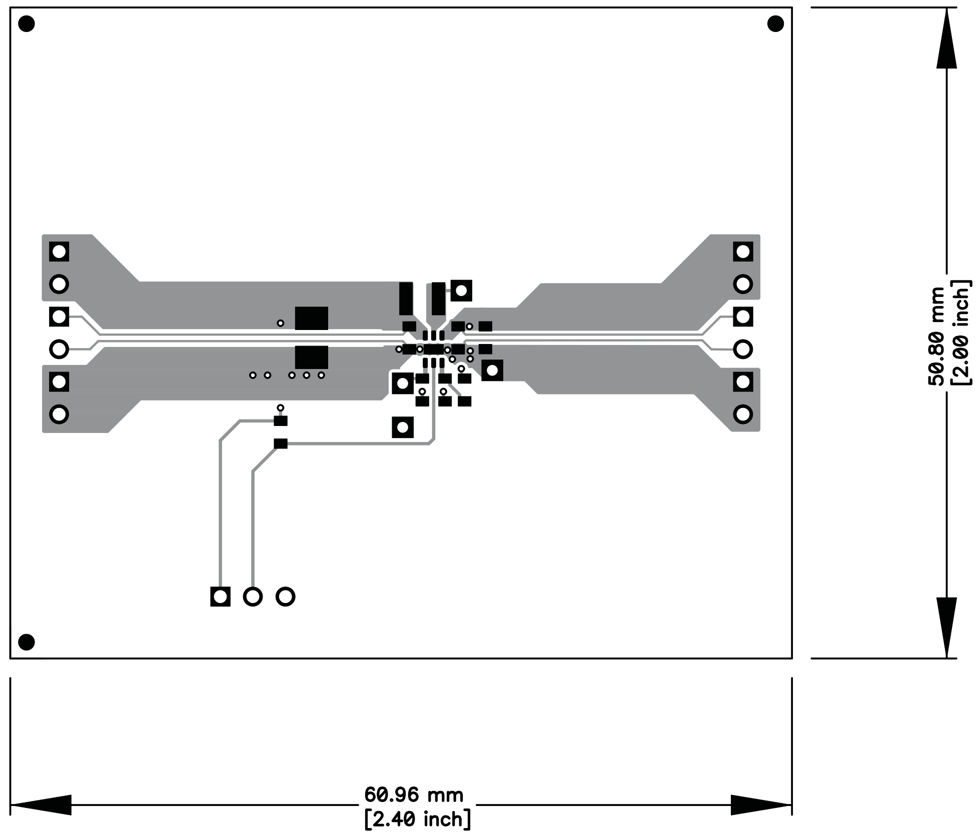

Figure 7. Top Layer

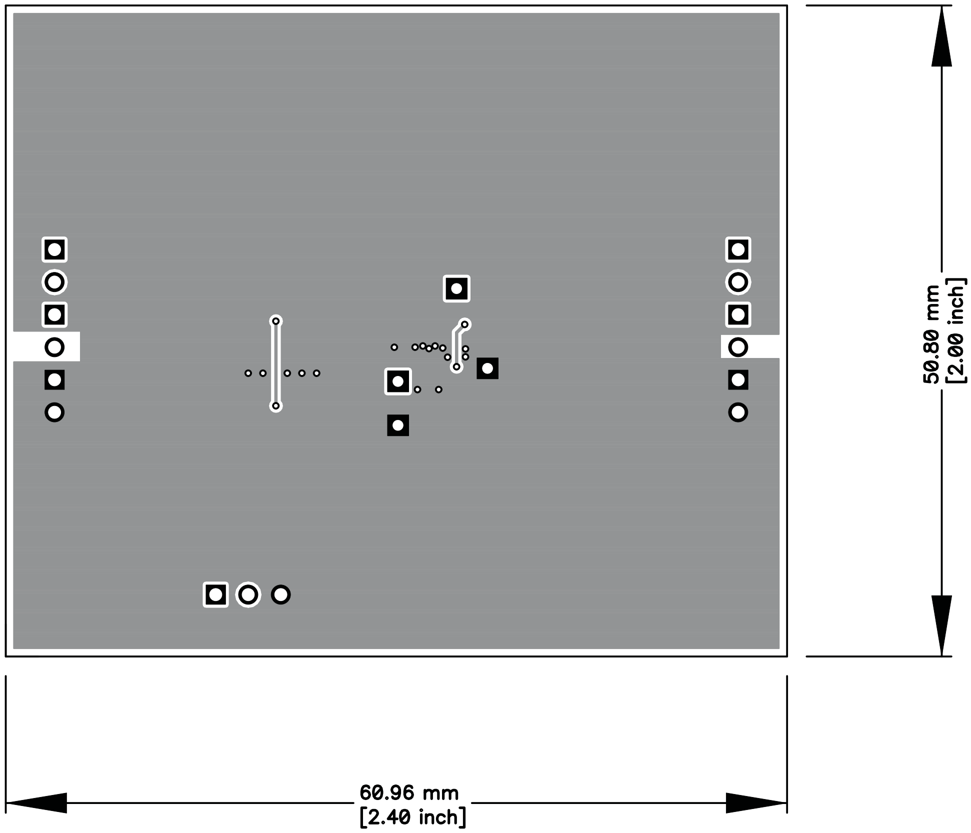

Figure 8. Bottom Layer

5.3 Bill of Materials

Table 2. HPA673A Bill of Materials

~001						
Count	**RefDes**	**Value**	**Description**	**Size**	**Part Number**	**MFR**
2	C1, C2	10uF	Capacitor, Ceramic, Low Inductance, 6.3V, X5R, 20%	0603	GRM188R60J106ME47D	Murata
1	C3	150uF	Capacitor, Tantalum, 6.3V, 25milliohm, 20%	3528(B)	T520B157M006ATE025	Kemet
0	C4		Capacitor, Ceramic, Low Inductance, 6.3V, X5R, 20%	0603		Murata
6	J1, J2, J3, J4, J5, J6	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	JP1	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
1	L1	4.7uH	Inductor, Power, 1.1 A, 138 milliohms	2.5 x 2.0 mm	LQM2HPN4R7MG0	Murata
2	R1, R4	1.00M	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	182k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	2.00k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS61260DRV	IC, Tiny Low Input Voltage Boost Converter	SON	TPS61260DRV	TI
1	--		PCB, 2.4 In x 2 In x 0.031 In		HPA673	Any
1			Label - See note 5	1.25 x 0.25 inch	THT-13-457-10	Brady
1	Apply on: JP1-ON		Shunt, 100-mil, Black	0.1	929950-00	3M

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0.8 V to 4 V and the output voltage range of 1.8 V to 4 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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