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# FAN2558/FAN2559 180mA Low Voltage CMOS LDO

#### **Features**

- Fixed 1.0V, 1.2V, 1.3V, 1.5V, 1.8V, 2.5V, 3.3V, 3.5V, 3.6V, 3.8V and Adjustable Output
- Power Good Indicator with Open Drain Output
- 180mA Output Current
- 100µA Ground Current
- C<sub>bypass</sub> for Low Noise Operation
- Fast Enable for CDMA Applications
- High Ripple Rejection
- · Current Limit
- · Thermal Shutdown
- Excellent Line and Load Regulation
- Requires Only 1µF Output Capacitor
- Stable with 0 to  $300 \text{m}\Omega$  ESR
- TTL-level Compatible Enable Input
- · Active Output Discharge

# **Applications**

- Processor Power-up sequencing
- PDAs, Cell Phones
- Portable Electronic Equir ...
- PCMCIA Vcc and Vpp gulation/swice...ing

# **General Description**

The FAN2558/9 low voltage CMOS LDOs feature fixed or adjustable output voltage, 180mA load current, delayed power good output (open drain) and 1% output accuracy with excellent line and load regulation external bypass capacitor provides ultra-low nois operation.

The FAN2558/9 low vo'  $_{2}$ e LPOs in  $_{3}$ rr ate both thermal shutdown and short  $_{4}$ rcu. ... ection. Catput is stalle with a  $1\mu$ F, low ESR capaci  $_{4}$ Th.  $_{5}$ AN  $_{5}$ 58/9 family is available in 5-Lead SO1  $_{3}$ , 6-La  $_{4}$ SC  $_{2}$ 3 and  $_{2}$ 2. am MLP-6 packages.

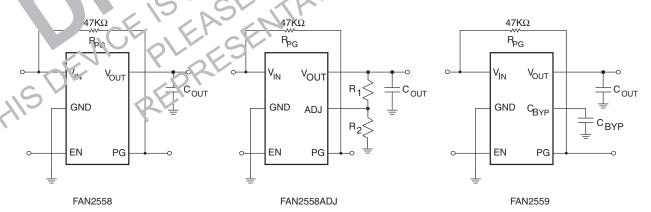
\N. 58: Output LDO with Power Good output

FA: 558ADJ. Adjustable Ou mu LDO with Power Good output

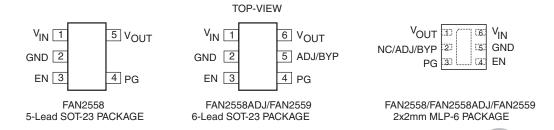
FAN2559: Fixed Cutput LLO with Power Good output, Lov Noise

Available standard output voltages are 1.0, 1.2V, 1.3V, 1.5V, 1.8V, 2.5V 3 37/3.5V, 3.6V, and 3.8V. Custom output voltage options are also available.

# nob. ...lo A' ... avn



# **Pin Assignments**



	Pin Name					OF	
Pin no.	FAN	FAN2558		FAN2558ADJ		.FAN2559	
	5SOT-23	2x2mm MLP-6	6SOT-23	2x2mm / P-6	6と ノ「-23	2x2mm MLP-6	
1	V <sub>IN</sub>	V <sub>OUT</sub>	V <sub>IN</sub>	V, 'T	Λ'N	V <sub>OUT</sub>	
2	GND.	NC	GND.		GND.	BYP	
3	EN	PG	F'	PG	EN	PG	
4	PG	EN	PG	EN	49	EN	
5	V <sub>OUT</sub>	GND	ADJ	GND	O BYP	GND	
6		Vie	T	V <sub>IN</sub>	Voot	V <sub>IN</sub>	

# Pin Descriptions

Symbol	Pin Function Description
V <sub>IN</sub>	nwer^nop., γut
V <sub>OUT</sub>	Regulate Voltage Ou put
aNL	round Connection
PG	Power Good Output, Open Drain
7	Ratio of potential divider from Vout to ADJ determines output voltage
BYP	Reference Noise Bypass
EN	Chip Enable Input The regulator is fully enabled when TTL "H" is applied to this input. The regulator enters into shu down mode when TTL "L" is applied to this input.

# **Absolute Maximum Ratings**

Parameter		Min.	Max.	Units
V <sub>IN</sub> to GND		6	V	
Voltage on any other pin to GND	-0.3	V <sub>IN</sub> + 0.3	V	
Junction Temperature (T <sub>J</sub> )		-55	150	°C
Storage Temperature		-65	150	°C
Lead Soldering Temperature, 10 seconds		300	°C	
Power Dissipation (P <sub>D</sub> )		Internally "ted	W	
Electrostatic Discharge (ESD) Protection (Note1)	HBM	4		kV
	CDM			(5)

# **Recommended Operating Conditions**

Parameter	Λ .	Typ.	Max.	Units
Supply Voltage Range, V <sub>IN</sub> for V <sub>OUT</sub> < 2.0V		0	5.5	V
Supply Voltage Range, V <sub>IN</sub> for V <sub>OUT</sub> ≥ 2.0V	TUI VDROPCUT	-6	5.5	V
Load Current		703	180	mA
Enable Input Voltage V <sub>EN</sub>	100	0, "	V <sub>IN</sub>	V
Power Good Output Voltage Range V	0	7/27	V <sub>IN</sub>	V
Junction Temperature	1-10		125	°C
Thermal Resistance-Jun to mbien 3OT-23 (Note	2)		235	
Thermal Resistance-J ction to Case, 2mm x 2mm 6-lead MLP	PUZOR		75	°C/W
Notes:  1. Using Mil. d. 883E, r., thod 3015.7 (Human Body Model) a				

# **Electrical Characteristics**

 $V_{IN}$  =  $V_{IN}$  min (note 5) to 5.5V,  $V_{EN}$  =  $V_{IN}$ ,  $I_{LOAD}$  = 100 $\mu$ A,  $T_A$  = -40°C to +85°C, unless otherwise noted. Typical values are at 25°C.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
V <sub>OUT</sub>	Output Voltage Accuracy (Note 3)	I <sub>LOAD</sub> = 100μA	-2	1	2	%
V <sub>OUT(ADJ)</sub>	Output Voltage Range (Adjustable)	$I_{LOAD} = 100 \mu A$	1		V <sub>IN</sub>	V
$\Delta V_{OUT\_LNR}$	Line Regulation	$V_{IN}$ min $< V_{IN} < 5.5V$	-0.3		0.3	%/V
$\Delta V_{OUT\_LDR}$	Load Regulation (Note 4)	$I_{LOAD} = 0.1 \text{mA} \text{ to } 150 \text{mA}$		2.5	1	%
I <sub>SD</sub>	Supply Current in Shutdown Mode	$V_{EN} < 0.4V$ PG = No Connection		.1		IA
I <sub>GND</sub>	Ground Pin Current (Note 4)	$I_{LOAD} = 0mA, V_{IN} = 5.5V$		90	150	μΑ
		$I_{LOAD} = 150 \text{mA}, V_{IN} = 5.5 \text{V}$			150	μΑ
I <sub>LIM</sub>	Current Limit	V <sub>OUT</sub> = 0V	60	350	500	mA
T <sub>SD</sub>	Thermal Shutdown Temperature			15.0		°C
	Thermal Shutdown Hysteresis			10		°C
$V_{ENL}$	Enable Input Low	\ = 5.5 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		103	7.4	V
V <sub>ENH</sub>	Enable Input High	V <sub>II</sub> = 5.5V, inabled	1.6	0.		V
IE	Enable Input Current	$V_{ENL}$ 4V, $V_{I,I} = 5.5V$ $V_{IH} \ge 1.6 \text{ V} V_{I,I} = 5.5V$	2015	0.01		μΑ
V <sub>PG</sub>	Low Threshol	% of VOUT PG ON	(35)			%
	High Thres old	% of V <sub>OUT</sub> PG OFF	2		97	%
V <sub>PGL</sub>	PG uput L v Vol ge	I <sub>PG SINK</sub> = 100μ΄A. Faul. Condition		0.02	0.1	V
I <sub>PC</sub>	'G Leakar Current	PG off, V <sub>PG</sub> =5.5V		0.01		μА
.N	Encole Response Time	$C_{OUT} = 1\mu F$ $C_{BYPASS} = 10nF$		30	300	μS
Ton	Power ON" Delay Time	$\begin{split} C_{OUT} &= 1 \mu F \\ C_{BYPASS} &= 10 n F \\ V_{ENL} &\geq 1.6 V, \\ V_{IN} &= 0 V \text{ to } V_{OUT} + 1 V \end{split}$		300	500	μS
$\nu_{PG}$	PG Delay time		1		5	mS
V <sub>DROP-OUT</sub>	Dropout Voltage (For Adjustable Output Version)	V <sub>OUT</sub> > 2.7V and I <sub>LOAD</sub> = 180mA		400		mV
V <sub>FB_ADJ</sub>	Feedback Voltage (For Adjustable Output Version)			0.59		V

### Note:

- 3. Guaranteed ±1% output voltage accuracy parts are available on customer request.
- 4. Measured at constant junction temperature using low duty cycle pulse testing.
- 5.  $V_{IN}$  min = 2.7V or ( $V_{OUT}$  + 1V), whichever is greater.

# DC Electrical Characteristics (Continued)

 $V_{IN}$  =  $V_{IN}$  min (note 5) to 5.5V,  $V_{EN}$  =  $V_{IN}$ ,  $I_{LOAD}$  = 100 $\mu$ A,  $T_A$  = -40°C to +85°C, unless otherwise noted. Typical values are at 25°C.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
PSRR	Power Supply Rejection Ratio	DC to 100kHz $C_{OUT} = 1 \mu F$ $C_{BYPASS} = 10 nF$ $I_{LOAD} = 0 \text{ to } 150 \text{mA}$ $V_{OUT} \leq 1.8 \text{V}$		50		dB
e <sub>N</sub>	Output Noise	BW: 300Hz to 50kHz $C_{OUT}$ =1 $\mu$ F $C_{BYPASS}$ = 10nF $I_{LOAD}$ = 0 to 150mA		30		μV <sub>RM</sub> ς
No DE	S NOT R NOT R NOE PLEASE REPRESE	ECONINE NO CONTAC FOR	ED F	OR NI ORNI	in or	



# **Functional Description**

Utilizing BiCMOS technology, the FAN2525/FAN2559 product family is optimized for use in compact battery powered systems. These LDOs offer a unique combination of high ripple rejection, low noise, low power consumption, high tolerance for a variety of output capacitors, and less than  $1\mu A$  "OFF" current. In the circuit, a differential current sense amplifier controls a series-pass P-Channel MOSFET to achieve high ripple rejection. A separate error amplifier compares the load voltage at the output with an onboard trimmed low voltage bandgap reference for output regulation.

Thermal shutdown and current limit circuits protect the device under extreme conditions. When the device temperature reaches 150°C, the output is disabled. When the device cools down by 10°C, it is re-enabled. The user can shut down the device using the Enable control pin at any time. The current limit circuit is trimmed, which leads to consistent power on /enable delays, and provides safe short circuit current densities even in narrow traces of the PCB.

A carefully optimized control loop accommodates a vice range of ESR values in the output bypass capacitor, at ving the user to optimize space, cost, and performation.

An Enable pin shuts down the regular output of conserve power, reducing supply current of less on 1.

The fixed-voltage 255 as a r se bypass on Power Good is available as a roos. Inction to indicate that the output voltage has reduce vithin 5% of the nominal value.

T six pin dju ble-voltage version utilizes pin 5 to connect pan expression voltage divider which feeds back to the regular or amplifier, thus setting the output voltage to the desired value.

# Applications Information

### External Capacitors - Selection

The FAN2558/FAN2559 gives the user the flexibility to utilize a wide variety of capacitors compared to other LDOs. An innovative design approach offers significantly reduced sensitivity to ESR, which degrades regulator loop stability in older designs. While the improvements featured in the FAN2558/FAN2559 family greatly simplify the design task,

capacitor quality still must be considered if the designer is to achieve optimal circuit performance. In general, ceramic capacitors offer superior ESR performance, and a smaller case size than tantalum capacitors.

#### **Input Capacitor**

An input capacitor of  $2.2\mu F$  (nominal value) or greater, connected between the Input pin and Ground, placed in close proximity to the device, will improve transient response and ripple rejection. Higher values will further improve ripple rejection and transient response. An improve ripple rejection and transient response and ripple rejection. Higher values will further improve ripple rejection. An improve ripple rejection and transient response and ripple rejection. Higher values will improve transient response and ripple rejection. Higher values will further improve ripple rejection and transient response and ripple rejection. Higher values will further improve ripple rejection and transient response. An improve ripple rejection and transient response. An improve ripple rejection and transient response. An improve ripple rejection and transient response and ripple rejection. Higher values will further improve ripple rejection and transient response and ripple rejection. An improve ripple rejection and transient response and ripple rejection and ripple reject

#### Output pa 'tor

An  $\alpha$  citor is required to maintain regulator loop bill. Stat. peration will be achieved with a wide variety of calcitors with LSR values anging from 0 in  $\Omega$  up to 4001. Multilaver ceramic, take lum or alumnum electrolytic capacitors may be used. A nominal value of at least  $1\mu$ F is recommended. Note that the choice of output capacitor affects load transient response, apple rejection, and it has a alight effect on noise performance as well.

An internal resistor of approximately  $100\Omega$  is connected between  $V_{\rm OV}$  and GND in shutdown mode, to discharge the output capacitor at a faster rate.

#### Bypass Capacitor (FAN2559 Only)

In the fixed-voltage configuration, connecting a capacitor between the bypass pin and ground can significantly reduce output noise. Values ranging from 0pF to 47nF can be used, depending on the sensitivity to output noise in the application.

At the high-impedance Bypass pin, care must be taken in the PCB layout to minimize noise pickup, and capacitors must be selected to minimize current loading (leakage). Noise pickup from external sources can be considerable. Leakage currents into the Bypass pin will directly affect regulator accuracy and should be kept as low as possible; thus, high-quality ceramic and film types are recommended for their low leakage characteristics. Cost-sensitive applications not concerned with noise can omit this capacitor.

#### **Control Functions**

#### **Enable Pin**

Connecting 2V or greater to the Enable pin will enable the output, while 0.4V or less will disable it while reducing the quiescent current consumption to less than  $1\mu A$ . If this shutdown function is not needed, the pin can simply be connected permanently to the  $V_{IN}$  pin. Allowing this pin to float will cause erratic operation.

#### **Error Flag (Power Good)**

Fault conditions such as input voltage dropout (low  $V_{IN}$ ), overheating, or overloading (excessive output current), will set an error flag. The PG pin which is an open-drain output, will go LOW when  $V_{OUT}$  is less than 95% or the specified output voltage. When the voltage at  $V_{OUT}$  is greater than 95% of the specified output voltage, the PG pin is HIGH. A logic pull-up resistor of  $47 K\Omega$  is recommended at this output. The pin can be left disconnected if unused.

#### **Thermal Protection**

The FAN2558/FAN2559 is designed to supply high pear output currents for brief periods, however sustained cressive output load at high input - output voltage crence will increase the device's temperature and exceed meaning due to power dissipation. During atputer of deconditions, when the die temperature excells the shidown limit temperature of 150°C, an or the halproceion will disable the output until the imperature decorption is approximately 10°C below the limitation which point is output in 12-enabled. During a thermal inutdown, the may assert the power-down function at the principle power consumption to minimal.

#### Th. rmal naracteristics

The t N 2/8/FAN 25:9 is designed to supply 180 mA at the specified output voltage with an operating die (junction) temperature of up to 125°C. Once the power dissipation and thermal resistance is known, the maximum junction temperature of the device can be calculated. While the power dissipation is calculated from known electrical parameters, the actual thermal resistance depends on the thermal characteristics of the SOT23-5 surface-mount package and the surrounding PC board copper to which it is mounted.

The power dissipation is equal to the product of the input-tooutput voltage differential and the output current plus the ground current multiplied by the input voltage, or:

$$P_{D} = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

The ground pin current  $I_{\mbox{\footnotesize GND}}$  can be found in the charts provided in the Electrical Characteristics section.

The relationship describing the thermal behavior of the package is:

$$P_{D(max)} = \left\{ \frac{T_{J(max)} - T_A}{\theta_{JA}} \right\}$$

where  $T_{J(max)}$  is the maximum allowable junction temperature of the die, which is 125°C, and T<sub>A</sub> is the ambient operating temperature.  $\theta_{JA}$  is dependent on the surrounding PC board layout and can be empirical obtained. While the  $\theta_{JC}$ (junction-to-case) of the SOT 3-5 ckage specified at 130°C/W, the  $\theta_{JA}$  of the firmum in B fr sprint will be at least 235°C /W. This can sir proved providing a heat sink of surrounding per round the PWB. Depending on the size of  $\theta$  copp are. The resulting  $\theta_{JA}$  can range from appi ima. 'y 180° '/W for one aguare inch to nearly 130° W to 4 sq iches. The addition of backside cop--holes, stiffeners, and off er enhancements c als vid in reducing thermal resistance. The heat contribute. by the dissipation of other delices located nearby must be included in the design considerations. Once the limiting parameter, in these two relationships have been determined, the design can be modified to on use that the device remains within specified operating conditions. If overload conditions are not considered, it is possible for the device to enter a thermal cycling loop, in which the circuit enters a shutdown condition, ccol, re-enables, and then again overheats and thats dov/n repeatedly due to an unmanaged fault condition.

#### Adjustable Version

The FAN2558ADJ includes an input pin ADJ which allows the user to select an output voltage ranging from 1V to near  $V_{\rm IN}$ , using an external resistor divider. The voltage  $V_{\rm ADJ}$  presented to the ADJ pin is fed to the onboard error amplifier which adjusts the output voltage until  $V_{\rm ADJ}$  is equal to the onboard bandgap reference voltage of 1.00V(typ). The equation is:

$$V_{OUT} = 0.59V \times \left[1 + \frac{R_1}{R_2}\right]$$

Since the bandgap reference voltage is trimmed, 1% initial accuracy can be achieved. The total value of the resistor chain should not exceed 250KOhm total to keep the error amplifier biased during no-load conditions. Programming output voltages very near  $V_{IN}$  need to allow for the magnitude and variation of the dropout voltage  $V_{DO}$  over load, supply, and temperature variations. Note that the low-leakage FET input to the CMOS error amplifier induces no bias current error to the calculation.

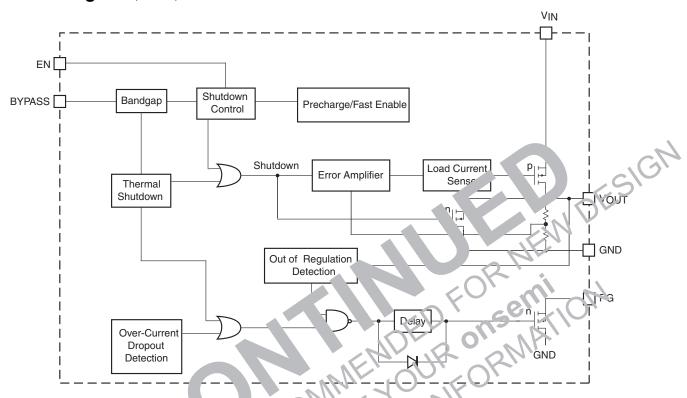
#### **General PCB Layout Considerations**

For optimum device performance, careful circuit layout and grounding techniques must be used. Establishing a small local ground, to which the GND pin, and the output and bypass capacitors are connected, is recommended. The input capacitor should be grounded to the main ground plane. The quiet local ground is then routed back to the main ground plane using feed through via. In general, the high-frequency compensation components (input, bypass, and output capacitors) should be located as close to the device as possible. Close proximity of the output capacitor is especially important to achieve optimum performance, especially during high

load conditions. A large copper area in the local ground serves as heat sink (as discussed above) when high power dissipation significantly increases device temperature. Component-side copper provides significantly better thermal performance. Added feed through connecting the device side ground plane to the back plane further reduces thermal resistance.

tant to achieve optimum performance, especially during high

# **Block Diagram** (Note 6)

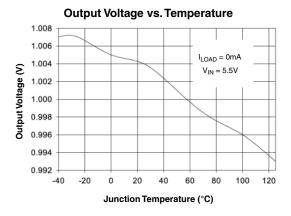


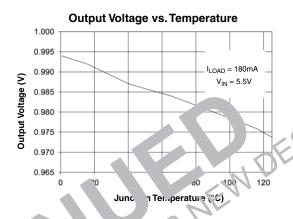
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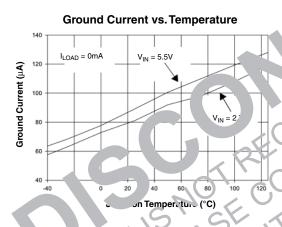
July for FAN2559 only

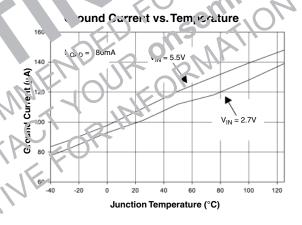
# **Typical Performance Characteristics**

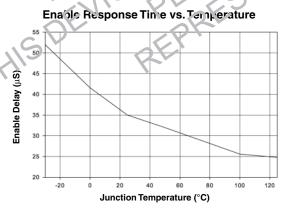
Unless otherwise specified,  $C_{IN}$  =  $C_{OUT}$  = 1 $\mu$ F,  $R_{PG}$  = 47k $\Omega$ ,  $T_A$  = 25°C, EN =  $V_{IN}$ 

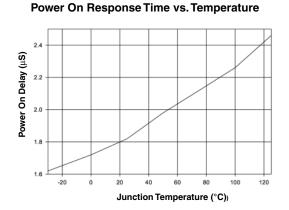






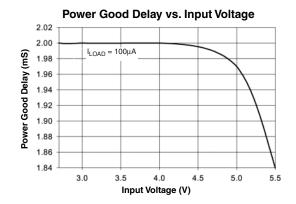






# **Typical Performance Characteristics** (Continued)

Unless otherwise specified,  $C_{IN}$  =  $C_{OUT}$  =  $1\mu F,~R_{PG}$  =  $47k\Omega,~T_{A}$  =  $25^{\circ}C,~EN$  =  $V_{IN}$ 



Output Voltage vs. Input Voltage 0.996 0.994 0.992 Output Voltage (V) 0.990 1<sub>LOAD</sub> =100μA 0.988 5.0 5.5 S 0.986 0.984 0.982 I<sub>LOAD</sub> =180mA 0.980 0.978 3.0 age

Output Voltage vs. Load Current

0.994

0.992

0.990

0.988

0.986

0.986

0.984

0.982

20

6

80

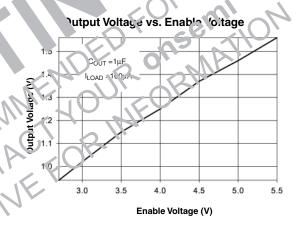
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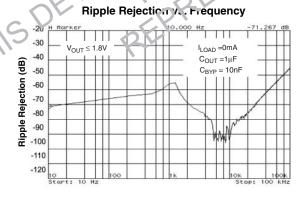
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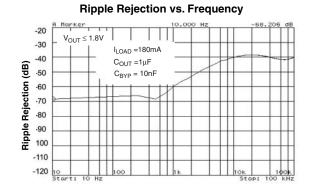
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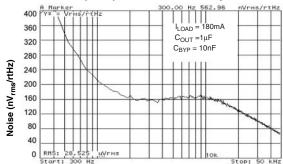


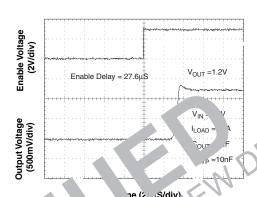


# **Typical Performance Characteristics** (Continued)

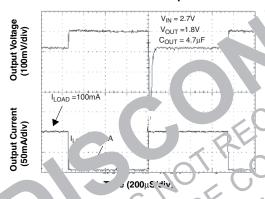
Unless otherwise specified,  $C_{IN}$  =  $C_{OUT}$  =  $1\mu F,~R_{PG}$  =  $47k\Omega,~T_{A}$  =  $25^{\circ}C,~EN$  =  $V_{IN}$ 

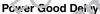


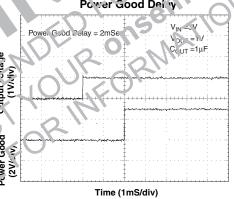




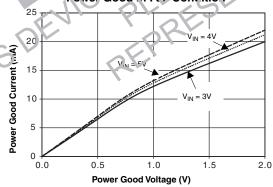
#### **Load Transient Response**





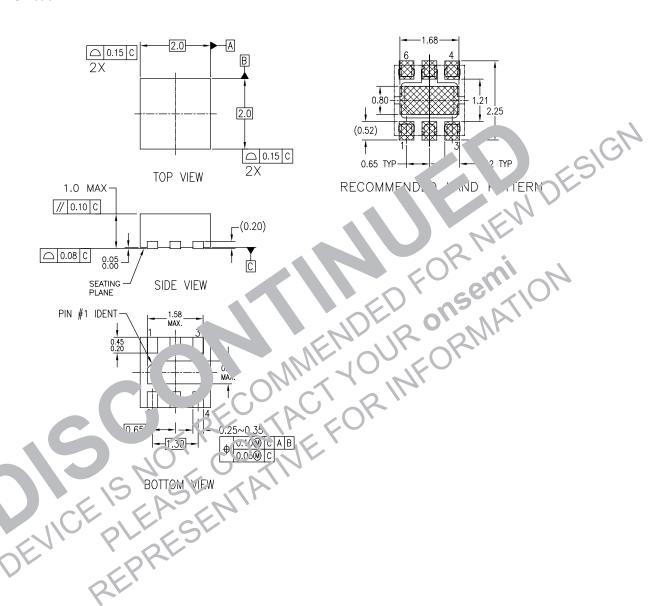


# Power Good in Fail Condition



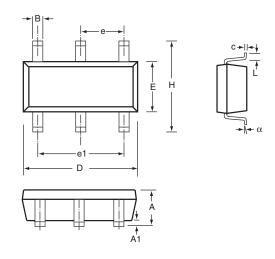
### **Mechanical Dimensions**

#### 2x2mm 6-Lead MLP

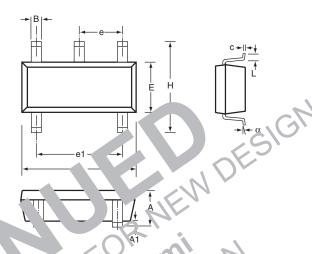


# **Mechanical Dimensions**

# 6-Lead SOT-23 Package



# 5-Lead SOT-23 Package



Symbol	Inc	hes	Millimet		Votes
	Min	Max	Min	// x	
Α	.035	.057	0	1.4.	1/2
A1	.000	.000	)	15	Ola.
В	.008	.( :(0	20	.50	7
С	.00	.0	08	25	177
D	.1	?2	2.70	3.10	2/2
F	59	71ر	1.50	1.80	1
е	37	BSC	.95	L'SC	
	.075	BSC	1.90	BSC	
Н	730.	.126	2.20	3.20	
L	.004	.024	.1ù	.60	
α	0°	10°	0°	10°	

#### Notes:

- 7. Package outline exclusive of mold flash & metal burr.
- 8. Packageoutline exclusive of solder plating.
- 9. EIAJ Ref Number SC\_74A

# **Ordering Information**

 $T_A = -40^{\circ}C$  to  $85^{\circ}C$ 

Part Number	Output Voltage	Package Marking	Package	Order Code
FAN2558	1.0V	58T	5-Lead SOT-23	FAN2558S10X
	1.2V	58U		FAN2558S12X
	1.3V	58X		FAN2558S13X
	1.5V	58V		FAN2558S15X
	1.8V	580		FAN2558S18X
	2.5V	58J		F^N2558S25X
	3.3V	58K		FAN. 58S33X
	3.5V	58P		FAN2 8S35X
	3.6V	58Q		1 N. 558836X
	3.8V	581		FAN2558\$35X
	1.0V	58T	2mm x 2mnLeac 'LP	FAN2558MP10X
	1.2V	58U		FA) !2558MP12X
	1.3V	58X		FAN2558MP13X
	1.5V	58V		FAR2558MP15X
	1.8V	580		FAN2558 MF)18X
	Adjustable	5 7	J-Lead SOT-23	FAI 12558SX
		581	2mm x 2nnm 6-Lead M. r	FAN2558MPX
FAN2559	1.0V	52	6 Lead SO 7-23	FAN2559S10X
	1.2V	Ur	MV.100.20	FAN2559S12X
	1.31/	59X	1/1/1/1/1	FAN2559S13X
	.5V	59V	C1 -2"	FAN2559S15X
	8V	590		FAN2559S18X
	1.	59T	2mm x 2mm 6-Lead MLP	FAN2559MP10X
	.2V	5.7U		FAN2559MP12X
	1.3V	59X	7	FAN2559MP13X
	1.50	597		FAN2559MP15X
	1.8V	590		FAN2559MP18X

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