CMOS 12-Bit Buffered Multiplying DAC

General Description

The AD7545 is a 12-bit CMOS multiplying digital-to-analog converter (DAC) with internal data latches. Input data is loaded as a single 12-bit word and latched under the control of CS and WR inputs. When CS and WR are low, the input data latches are transparent and the DAC output responds to any changes in the digital input.

AD7545 works with a single +5V or +15V power supply. Electrical characteristics are specified at both of these supply voltages. With a +5V supply, the digital inputs are +5V TTL and CMOS compatible while high voltage CMOS compatibility is maintained at +15V supply range.

Maxim AD7545 uses low tempco thin-film resistors which are laser-trimmed to result in linearity errors that are typically ±¼ LSB and gain errors of maximum ±1 LSB (G grade).

The digital inputs are designed with improved protection against electrostatic discharge (ESD) damage and can typically withstand to over 6,000V of ESD voltages.

The AD7545 is supplied in 20-lead narrow DIP and Small Outline packages.

Applications

Motion Control Systems

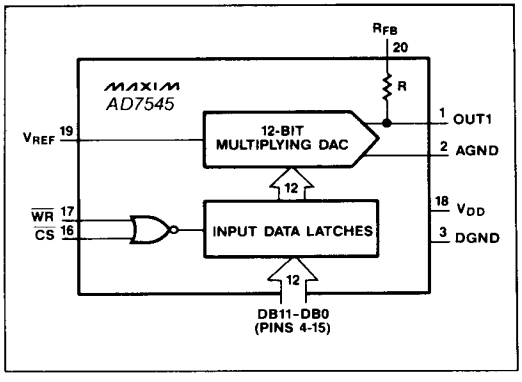
Automatic Test Equipment

μP Controlled Calibration Circuitry

Programmable Gain Amplifiers

Programmable Power Supplies

Functional Diagram



Features

- ◆ **12-Bit Resolution**
- ◆ **±1 LSB Gain Accuracy (G Grade)**
- ◆ **Single Supply Operation**
- ◆ **Improved ESD Protection**
- ◆ **CMOS/TTL Compatible for V_{DD} = +5V**
- ◆ **CMOS Compatible for V_{DD} = +15V**

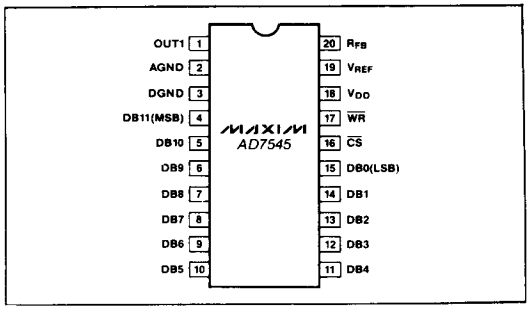
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7545JN	0°C to +70°C	Plastic DIP	±2 LSB
AD7545KN	0°C to +70°C	Plastic DIP	±1 LSB
AD7545LN	0°C to +70°C	Plastic DIP	±½ LSB
AD7545GLN	0°C to +70°C	Plastic DIP	±½ LSB
AD7545JCWP	0°C to +70°C	Small Outline	±2 LSB
AD7545KCWP	0°C to +70°C	Small Outline	±1 LSB
AD7545LCWP	0°C to +70°C	Small Outline	±½ LSB
AD7545GLCWP	0°C to +70°C	Small Outline	±½ LSB
AD7545JC/D	0°C to +70°C	Dice	±2 LSB
AD7545AQ	-25°C to +85°C	CERDIP**	±2 LSB
AD7545BQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7545CQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7545GCQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7545SD	-55°C to +125°C	Ceramic	±2 LSB
AD7545TD	-55°C to +125°C	Ceramic	±1 LSB
AD7545UD	-55°C to +125°C	Ceramic	±½ LSB
AD7545GUD	-55°C to +125°C	Ceramic	±½ LSB
AD7545SQ	-55°C to +125°C	CERDIP**	±2 LSB
AD7545TQ	-55°C to +125°C	CERDIP**	±1 LSB
AD7545UQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7545GUQ	-55°C to +125°C	CERDIP**	±½ LSB

** All devices—20 lead packages*

***Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Pin Configuration



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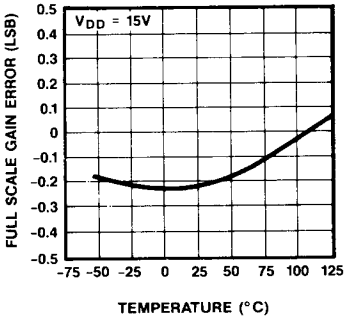
ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise stated.)

V_{DD} to DGND	-0.3 to +17V
Digital Input Voltage to DGND	-0.3 to V_{DD}
V_{RFB}, V_{REF} to DGND	±25V
V_{OUT1} to DGND	-0.3 to V_{DD}
AGND to DGND	-0.3 to V_{DD}
Power dissipation to +75°C (any package)	450mW
Derate above 75°C by	6mW/°C
Operating Temperature Ranges	
J, K, L, GL	0°C to +70°C
A, B, C, GC	-25°C to +85°C
S, T, U, GU	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering 10 seconds)	+300°C

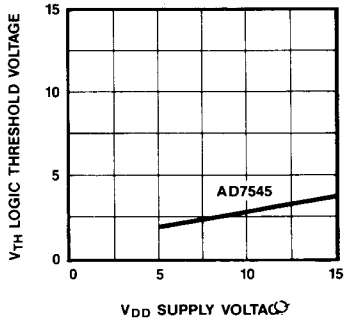
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

Typical Performance Characteristics

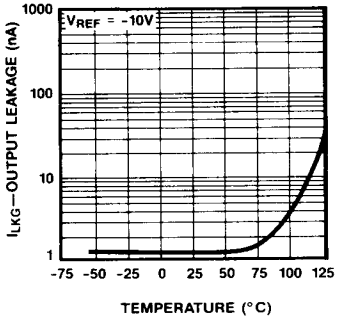
FULL-SCALE GAIN ERROR vs TEMPERATURE



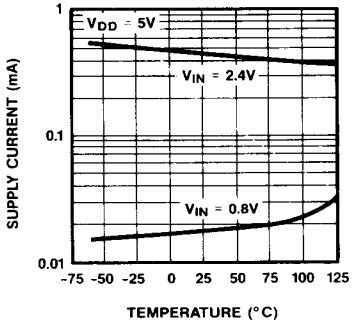
LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



OUTPUT LEAKAGE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND. Over specified temperature range unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N					12	Bits
Relative Accuracy	INL		J,A,S K,B,T L,C,U GL,GC,GU			±2 ±1 ±1/2 ±1/2	LSB LSB LSB LSB
Differential Non-Linearity	DNL	10-bit Monotonic 12-bit Monotonic 12-bit Monotonic 12-bit Monotonic	J,A,S K,B,T L,C,U GL,GC,GU			±4 ±1 ±1 ±1	LSB LSB LSB LSB
Gain Error (Note 1)	FSE		J,A,S K,B,T			±20 ±10	LSB LSB
			L,C,U T_A = +25°C Over Temp.			±5 ±6	LSB LSB
			GL,GC,GU T_A = +25°C Over Temp.			±1 ±2	LSB LSB
Gain Tempco ΔGain/ΔTemp. (Note 2)	TCFS				±2	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD} (Note 2)	PSR	ΔV_{DD} = ±5%	T_A = +25°C Over Temp.			0.015 0.03	%/% %/%
DYNAMIC PERFORMANCE							
Current Settling Time (Note 2)	t_S	To ±1/2 LSB. OUT1 Load is 100ohms. $\overline{CS}$ = 0V. DAC output measured from falling edge of $\overline{WR}$.				2	μs
Propagation Delay (Note 2)	t_{PD}	From digital inputs, DB11-DB0, change from V_{DD} to 0V or 0V to V_{DD}, to 90% of final analog output. OUT1 load is: R = 100ohms/C = 13pF.	T_A = +25°C			300	ns
Digital to Analog Glitch Impulse	Q	V_{REF} = AGND	T_A = +25°C		400		nV-s
AC Feedthrough at OUT1 (Note 3)	FTE	V_{REF} = ±10V, 10kHz sinewave, DB11-DB0 = 0V.			5		mVp-p
REFERENCE INPUT							
Input Resistance	R_{REF}	V_{REF} pin to AGND		7	11	25	kohms
Input Resistance Tempco	TCR				-300		ppm/°C

Note 1: Using internal feedback resistor, RFB. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 3, 4 and 8.
Note 2: Guaranteed by design but not tested.
Note 3: In ceramic packages the feedthrough can be further reduced by grounding the metal lid of the package.
Note 4: Sample tested at 25°C to ensure compliance.
Note 5: See timing diagram for definitions of the switching times.

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ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND. Over specified temperature range unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG OUTPUTS								
OUT1 Capacitance (Note 2)	C_{OUT1}	DB11-DB0 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V					70 200	pF pF
OUT1 Leakage Current	I_{LKG}	$\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = 0V	J,K,L,GL	T_A = +25°C Over Temp.			10 50	nA nA
			A,B,C,GC	T_A = +25°C Over Temp.			10 50	nA nA
			S,T,U,GU	T_A = +25°C Over Temp.			10 200	nA nA
DIGITAL INPUTS								
Input High Voltage	V_{IH}				2.4			V
Input Low Voltage	V_{IL}						0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}		T_A = +25°C Over Temp.		±0.001	±1 ±10	μA μA
Input Capacitance (Note 2)	C_{IN}	V_{IN} = 0V; DB11-DB0 V_{IN} = 0V; $\overline{WR}$, $\overline{CS}$					5 20	pF pF
SWITCHING CHARACTERISTICS (Notes 4, 5)								
Chip Select to Write Setup Time	t_{CS}			T_A = +25°C Over Temp.	280 380	200 270		ns ns
Chip Select to Write Hold Time	t_{CH}				0			ns
Write Pulse Width	t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$		T_A = +25°C Over Temp.	250 400	175 280		ns ns
Data Setup Time	t_{DS}			T_A = +25°C Over Temp.	140 210	100 150		ns ns
Data Hold Time	t_{DH}				10			ns
POWER SUPPLY								
Supply Current	I_{DD}	All digital inputs: V_{IL} or V_{IH} : 0V or V_{DD}, : 0V or V_{DD}		T_A = +25°C Over Temp.		10 10	2 100 500	mA μA μA

Note 1: Using internal feedback resistor, RFB. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 3, 4 and 8.
Note 2: Guaranteed by design but not tested.
Note 3: In ceramic packages the feedthrough can be further reduced by grounding the metal lid of the package.
Note 4: Sample tested at 25°C to ensure compliance.
Note 5: See timing diagram for definitions of the switching times.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND. Over specified temperature range unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE								
Resolution	N						12	Bits
Relative Accuracy	INL		J,A,S K,B,T L,C,U GL,GC,GU				±2 ±1 ±1/2 ±1/2	LSB LSB LSB LSB
Differential Non-Linearity	DNL	10-bit Monotonic 12-bit Monotonic 12-bit Monotonic 12-bit Monotonic	J,A,S K,B,T L,C,U GL,GC,GU				±4 ±1 ±1 ±1	LSB LSB LSB LSB
Gain Error (Note 1)	FSE		J,A,S K,B,T L,C,U				±25 ±15 ±10	LSB LSB LSB
			GL,GC,GU	T_A = +25°C Over Temp.			±6 ±7	LSB LSB
Gain Tempco ΔGain/ΔTemp. (Note 2)	TCFS					±2	±10	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD} (Note 2)	PSR	ΔV_{DD} = ±5%		T_A = +25°C Over Temp.			0.01 0.02	%/% %/%
DYNAMIC PERFORMANCE								
Current Settling Time (Note 2)	t_S	To ±1/2 LSB OUT1 Load is 100ohms. $\overline{CS}$ = 0V. DAC output measured from falling edge of $\overline{WR}$.					2	μs
Propagation Delay (Note 2)	t_{PD}	From digital inputs, DB11-DB0, change from V_{DD} to 0V or 0V to V_{DD}, to 90% of final analog output. OUT1 Load is: R = 100ohms/C = 13pF.		T_A = +25°C			250	ns
Digital to Analog Glitch Impulse	Q	V_{REF} = AGND		T_A = +25°C		250		nV-s
AC Feedthrough at OUT1 (Note 3)	FTE	V_{REF} = ±10V, 10kHz sinewave, DB11-DB0 = 0V.				5		mVp-p
REFERENCE INPUT								
Input Resistance	R_{REF}	V_{REF} pin to AGND			7	11	25	kohms
Input Resistance Tempco	TCR					-300		ppm/°C
ANALOG OUTPUTS								
OUT1 Capacitance (Note 2)	C_{OUT1}	DB11-DB0 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V					70 200	pF pF
OUT1 Leakage Current	I_{LKG}	$\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = 0V	J,K,L,GL	T_A = +25°C Over Temp.			10 50	nA nA
			A,B,C,GC	T_A = +25°C Over Temp.			10 50	nA nA
			S,T,U,GU	T_A = +25°C Over Temp.			10 200	nA nA
DIGITAL INPUTS								
Input High Voltage	V_{IH}				13.5			V
Input Low Voltage	V_{IL}						1.5	V

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ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND. Over specified temperature range unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (Continued)							
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	T_A = +25°C Over Temp.		±0.001	±1 ±10	μA μA
Input Capacitance (Note 2)	C_{IN}	V_{IN} = 0V; DB11-DB0 V_{IN} = 0V; WR, CS				5 20	pF pF
SWITCHING CHARACTERISTICS (Notes 4, 5)							
Chip Select to Write Setup Time	t_{CS}		T_A = +25°C Over Temp.	180 200	120 150		ns ns
Chip Select to Write Hold Time	t_{CH}			0			ns
Write Pulse Width	t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	T_A = +25°C Over Temp.	160 240	100 170		ns ns
Data Setup Time	t_{DS}		T_A = +25°C Over Temp.	90 120	60 80		ns ns
Data Hold Time	t_{DH}			10			ns
POWER SUPPLY							
Supply Current	I_{DD}	All digital inputs: V_{IL} or V_{IH} : 0V or V_{DD}. : 0V or V_{DD}	 T_A = +25°C Over Temp.		 10 10	2 100 500	mA μA μA

Note 1: Using internal feedback resistor, RFB. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 3, 4 and 8.
Note 2: Guaranteed by design but not tested.
Note 3: In ceramic packages the feedthrough can be further reduced by grounding the metal lid of the package.
Note 4: Sample tested at 25°C to ensure compliance.
Note 5: See timing diagram for definitions of the switching times.

Detailed Description

D/A Converter

The basic AD7545 DAC circuit consists of a laser trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or AGND depending on the status of each input bit. Although the current at OUT1 and AGND will depend on the digital input code, the sum of the two output currents is always equal to the input current at V_{REF}.

Either current output can be converted into a voltage externally by adding an output amplifier (Figure 3). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low temperature coefficient external resistor should be used for R_{FB} to minimize gain variation with temperature.

The internal feedback resistor R_{FB} is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent supply rejection and gain temperature coefficient.

The I_{OUT1} pin output capacitance, C_{OUT1}, is code dependent and is typically 70pF to 200pF, with all switches to AGND and I_{OUT1}, respectively.

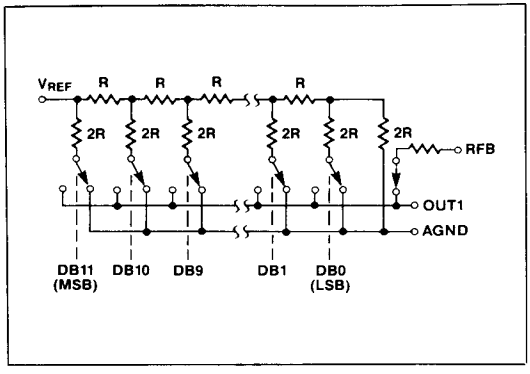


Figure 1. Simplified D/A Circuit of AD7545

Digital Circuit

The digital circuit for one bit is shown in Figure 2. The digital CONTROL signal is HIGH when $\overline{WR}$ and $\overline{CS}$ are both low. When $\overline{WR}$ and $\overline{CS}$ are tied low, the digital input directly controls the D/A switches.

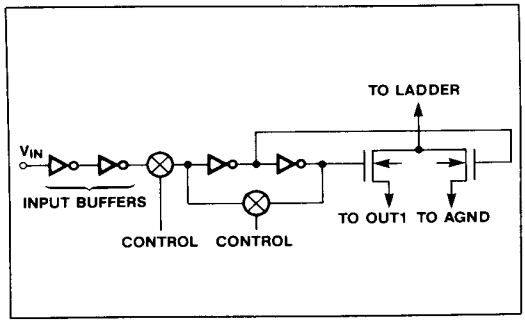
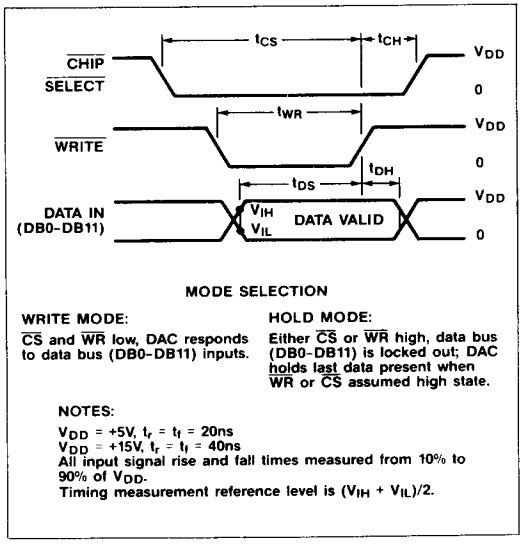


Figure 2. Digital Input Structure

The input buffer inverters act as a level shifter converting TTL levels into CMOS logic levels. These input buffers are CMOS/TTL compatible (0.8V and 2.4V) at V_{DD} = +5V. The AD7545 also works with V_{DD} = +15V where the input buffers are CMOS compatible (1.5V and 13.5V) only. With the digital input voltages at 1V to 6V the input buffers work in their linear regions drawing current from the power supply. Therefore to minimize high supply currents the digital input voltages should be kept as close to the supply and ground voltages (V_{DD} and DGND) as possible.

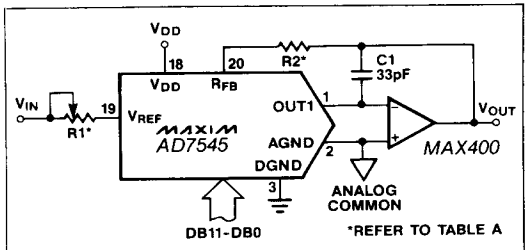
All digital inputs are ruggedized against electrostatic-discharge (ESD) sensitivity and can typically withstand ESD voltages of over 6kV.



Circuit Configurations

Unipolar Operation

The most common configuration for the AD7545 is shown in Figure 3. This circuit is used for unipolar binary operation or two-quadrant multiplication. The



TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

TABLE A. RECOMMENDED TRIM RESISTOR VALUES vs. GRADES FOR V_{DD} = +5V

Figure 3. Unipolar Binary Operation

Table 1. Unipolar Binary Code Table for Circuit of Figure 3

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{4095}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{1}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0

code table for this mode is given in Table 1. Note that the polarity of the output is the inverse of the reference voltage, V_{REF}.

In many applications the gain adjustment will not be necessary, especially when using the "G" suffix parts with guaranteed maximum ±1 LSB gain errors. In those cases and also when the gain is trimmed at the reference source, resistors R1 and R2 in Figure 3 can be omitted. However, if the trims are desired and the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used for R1 and R2.

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The capacitor C1 provides phase compensation and helps reduce the overshoot and ringing when using fast amplifiers at the output of the DACs.

Bipolar Operation

With the circuit configuration shown in Figure 4, the AD7545 operates in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors, R3, R4 and R5 are required. These resistors must be of the same material (preferably metal film or wire-wound) for good temperature characteristics, and they should match to 0.01% for 12-bit performance.

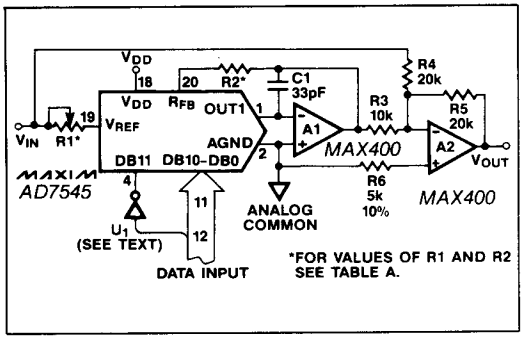

Figure 4. Bipolar Operation (2's Complement Code)

Table 2. 2's Complement Code Table for Circuit of Figure 4

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
0 1 1 1 1 1 1 1 1 1 1 1	$+V_{IN}\left(\frac{2047}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 1	$+V_{IN}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{2048}{2048}\right)$

The code table for the output, which is 2's complement is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude. The U1 inverter on the MSB line converts the 2's complement input code to offset-binary code. If this inversion is done in software using an exclusive-OR instruction or the input code is in offset binary, the U1 inverter can be omitted. Table 3 shows the code relationships to output voltage for the offset binary operation.

To adjust the circuit with offset binary code, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. In many applications the gain adjustment will not be necessary, especially when using the "G" suffix parts with guaranteed maximum ±1 LSB gain errors. In those cases and also when the gain is trimmed at the reference source, resistors R1 and R2 in Figure 4 can be omitted. However,if the trims are desired and the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used for R1 and R2.

(Voltage Mode) Single Supply

The AD7545 can be conveniently used in single supply (voltage mode) operation with OUT1 and AGND biased at any voltage between DGND and V_{DD}. This is possible since the ladder termination resistor is connected to AGND. OUT1 and AGND must not be allowed to go 0.3V lower or higher than the DGND or V_{DD}, respectively. Otherwise, internal diodes would turn on and a heavy current flow from the supply, possibly destroying the device.

Figure 5 shows the AD7545 connected as a voltage output DAC. OUT1 is connected to the reference input and AGND is grounded. V_{REF} pin, now the DAC output, is a voltage source with a constant impedance equal to the reference input resistance (typically 11kohms). This output should be buffered with an op-amp when a lower output impedance is required. R_{FB} pin is not used in this mode.

Table 3. Offset Binary Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{2048}\right)$

The input impedance of the reference input (OUT1) for this mode is code dependent, and the response time of the circuit depends on the behaviour of the reference source with changing load conditions.

Two advantages of the voltage mode operation are

single supply operation and that a negative reference is not required for a positive output. It should also be noted that the reference input (the voltage at OUT1) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded linearity and differential nonlinearity (DNL). Figures 6 and 7 show the typical dependence of DNL on supply voltage, V_{DD}, and the reference voltage, V_{REF}. If the DAC is offset from DGND by biasing OUT1 and AGND at a voltage above DGND, this will effect DNL and its effect will be the same as reducing V_{DD} by the amount of the offset.

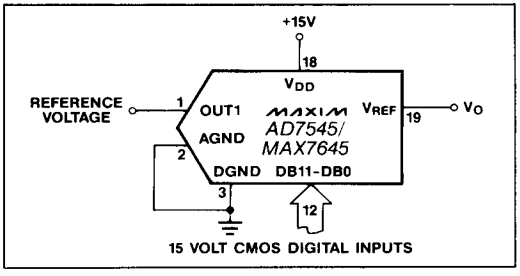

Figure 5. Single Supply Operating Using Voltage Switching Mode

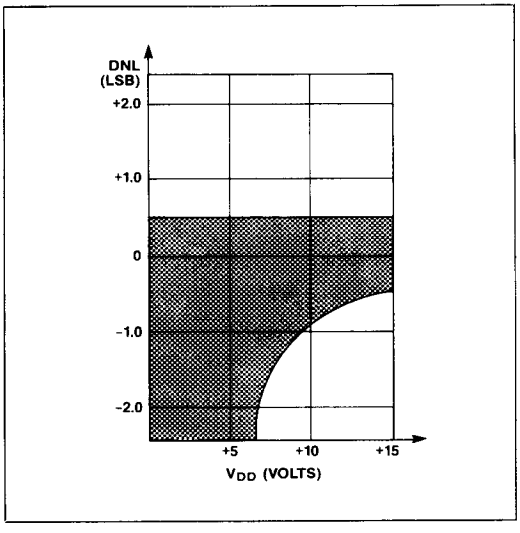

Figure 6. Differential Nonlinearity vs. V_{DD} for Figure 4 Circuit. Reference Voltage = 2.5 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C and U Grades.

The unipolar and bipolar circuits in Figures 3 and 4 can all be converted to voltage output mode. For example, Figure 8 shows the 2's complement bipolar circuit of Figure 4 modified to work with an output range of +2V to +8V around an offset ground potential of +5V from a single supply, V_{DD}, of +10V to 15V. The REF02 reference is used to bias the AGND at +5V. The R1 and R2 resistors form a voltage divider together

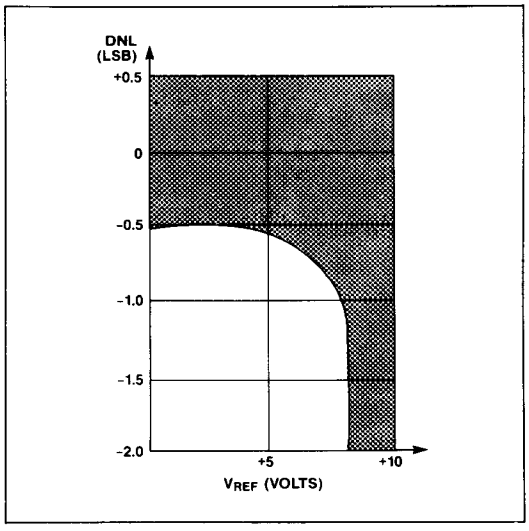

Figure 7. Differential Nonlinearity vs. Reference Voltage for Figure 4 Circuit. V_{DD} = 15 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C, and U Grades.

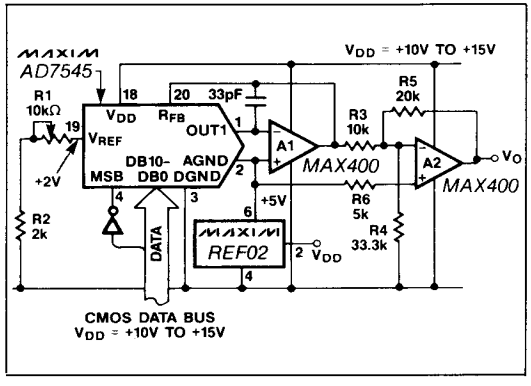

Figure 8. Single Supply "Bipolar" 2's Complement D/A Converter

CMOS 12-Bit Buffered Multiplying DAC

with the DAC reference input resistor, supplying the DAC with +2V input voltage. If the application requires a wide temperature range, the +2V should be generated with an op-amp to avoid drifts due to tempco matching of the DAC resistors to the external resistors. Output voltage ranges can be produced by changing R4 to change the offset, and (R1 + R2) to change the gain (slope) of the DAC transfer function. To ensure good linearity, the supply voltage, V_{DD}, must be kept at least +5V above the OUT1 voltage.

Microprocessor Interfacing

The AD7545 directly interfaces to 8- and 16-bit microprocessors using standard WR and CS control signals and its 12-bit data latch.

Figure 9 shows a typical interface circuit for an 8-bit processor. This application uses two memory addresses for the lower 8 bits and the upper 4 bits of data to the DAC. A 4-bit external latch is required to facilitate the interface.

For processors with 16-bit wide address busses and 8-bit data busses, such as 6800, 8080 and Z80, the 12 lower address lines can be used to supply data to the DAC, as shown in Figure 10. The upper 4 bits contain the address of the DAC that is selected. This arrangement takes 4k bytes of address locations for each DAC and the data is written with a single instruction cycle into the DAC.

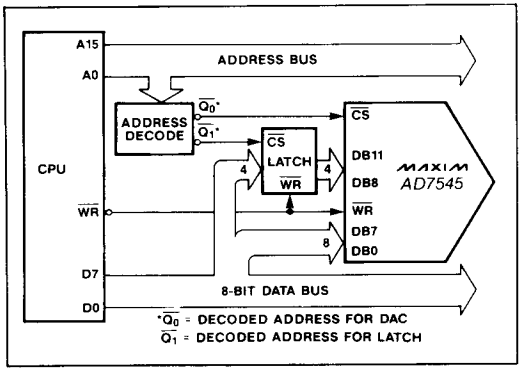

Figure 9. 8-Bit Processor to AD7545 Interface

Application Information

Output Amplifier Offset

For best linearity, OUT1 and AGND should be terminated at exactly 0V. In most applications OUT1 is connected to the summing junction of an inverting op-amp. The input offset voltage of the amplifier can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}\ (1 + R_{FB}/R_O)$$

where V_{OS} is the op-amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code and varies from approximately 11kohms to 33kohms. The error voltage range is then typically 4/3 V_{OS} to 2 V_{OS}, a change of 2/3 V_{OS}. An amplifier with 3mV of offset will therefore degrade the

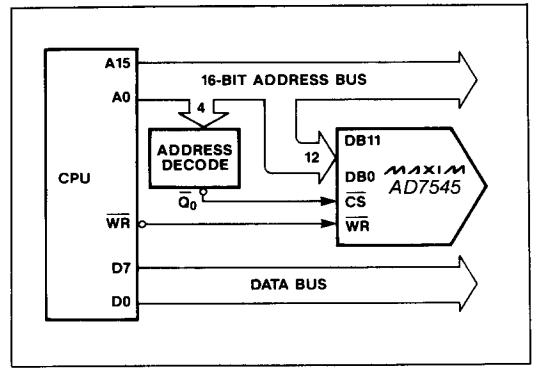

Figure 10. Connecting the AD7545 to 8-Bit Processors via the Address Bus

linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 LSBs.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error. I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier noninverting input is grounded through a "bias current compensation resistor". This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} pin to OUT1. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs V_{REF} and OUT1 pins.

The DAC output follows the digital inputs when the $\overline{WR}$ and $\overline{CS}$ pins are low. In those systems where the data is not valid for the full period where $\overline{WR}$ is low, invalid outputs and voltage glitches can appear at the DAC output. Adjusting the timing of the $\overline{WR}$ signal so that it is low only when data is valid eliminates this problem.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high-speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance C_{OUT1} and the internal feedback resistor, R_{FB}. Its value depends on the type of op-amp used but typically ranges from 10pF to 3pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized and the output voltage settling time improved by keeping the circuit board trace and stray capacitance at OUT1 as small as possible.

Grounding and Bypassing

Since OUT1, AGND and noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, low resistance (less than 0.2ohms) connection. The current at OUT1 and AGND varies with input code, creating a code dependent error if these terminals are connected to ground (or a "virtual ground") through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic capacitor, should be connected as close to the DAC V_{DD} and DGND pins as possible.

The AD7545 has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or DGND when not used. It is also a good practice to connect active inputs to V_{DD} or DGND through high valued resistors (1Mohms) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

It is also recommended that two back-to-back diodes be connected between the DGND and AGND pins in those systems where these pins tie on the backplane.

Chip Topology