UHF ASK/FSK Receiver T5760/T5761

Introduction

Technical Features

- **Low-cost Solution Due to High Integration Level with Minimum External Circuitry Requirements**
- **Fully Integrated PLL Including LC-VCO and Loop Filter**
- **Very High Sensitivity with Power-matched LNA**
- **30 dB Image Rejection**
- **High System IIP3 (-16 dBm), System 1-dB Compression Point (-25 dBm)**
- **High Large-signal Capability at GSM Band (Blocking = -30 dBm at +20 MHz, IIP3 = -12 dBm at + 20 MHz)**
- **5 V to 20 V Automotive-compatible Data Interface**
- **Data Clock Available for Manchester-coded and Bi-phase-coded Signals**
- **Programmable Digital Noise Suppression**
- **Receiving Bandwidth B_{IF} = 600 kHz Allowing Low Cost 90 ppm Crystals**
- **Low Power Consumption Due to Self Configurable Polling**
- **Temperature Range -40°C to +105°C**
- **ESD Protection Circuit: 2 kV HBM (Human Body Model)/200 V MM (Machine Model)**
- **Communication to a Microcontroller Possible Via a Single Bi-directional Data Line**

Description

The T5760/T5761 is a multi-chip PLL receiver device supplied in an SO20 package. It has been specially developed for the demands of low-cost RF data transmission systems with data rates from 1 kBaud to 10 kBaud in Manchester or Bi-phase code. The receiver is well suited to operate with Atmel's PLL RF transmitter T5750. It can be used in the frequency receiving range of f_0 = 868 MHz to 870 MHz (T5760) or f_0 = 902 MHz to 928 MHz (T5761) for ASK or FSK data transmission. All the statements made below refer to 868.3 MHz and 915.0 MHz applications.

Typical Applications

- **Short Range Data Links**
- **Remote Keyless Entry (RKE) Systems**
- **Wireless Keyboard**
- **Telemetry**
- **Consumption Metering**
- **Alarm Systems**
- **Garage Door Openers**

T5760/T5761

Application Note

Preliminary

Rev. 4658B–RKE–04/03

Functional Description

General Operation

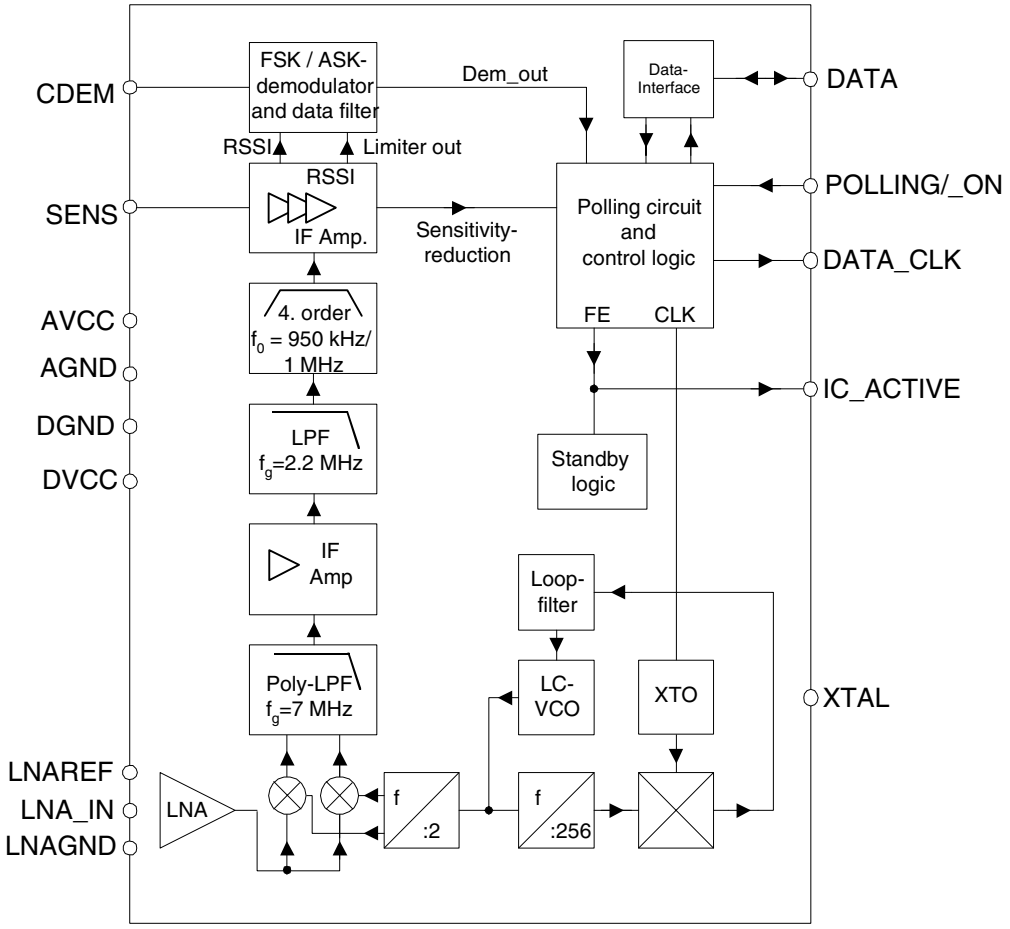
The T5760/T5761 is a low-IF super-heterodyne receiver that can be subdivided into two main functional units (see Figure 1):

- the RF front end
- the signal processing and control unit

The RF front end consists of a low noise amplifier (LNA), I/Q mixer, polyphase lowpass filter (Poly-LPF), IF amplifier (IF Amp), lowpass filter (LPF), a fully integrated PLL synthesizer, a crystal oscillator (XTO) and standby logic.

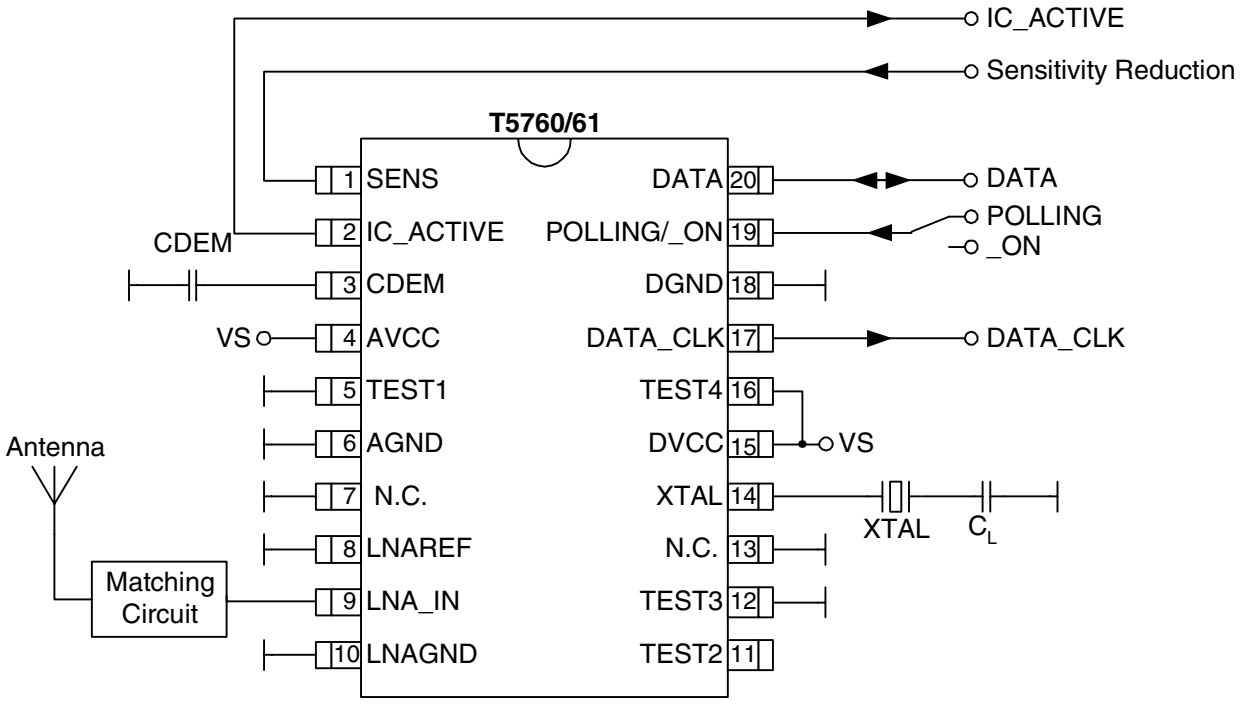
The signal processing and control unit contains a bandpass filter, RSSI amplifier, FSK/ASK demodulator, data filter, data interface and a polling circuit and control logic.

Figure 1. Block Diagram



Due to the high integration level only a few external components are necessary to operate the receiver (see Figure 2). In the RF path a matching network is needed to adapt the antenna to the LNA input. The cut-off frequency of the data filter is defined by the external capacitor CDEM. The reference frequency f_{XTO} for the PLL and the control logic is set by a crystal (XTAL) and its corresponding load capacitor C_L. The supply voltages should be decoupled using capacitors (not represented in Figure 2).

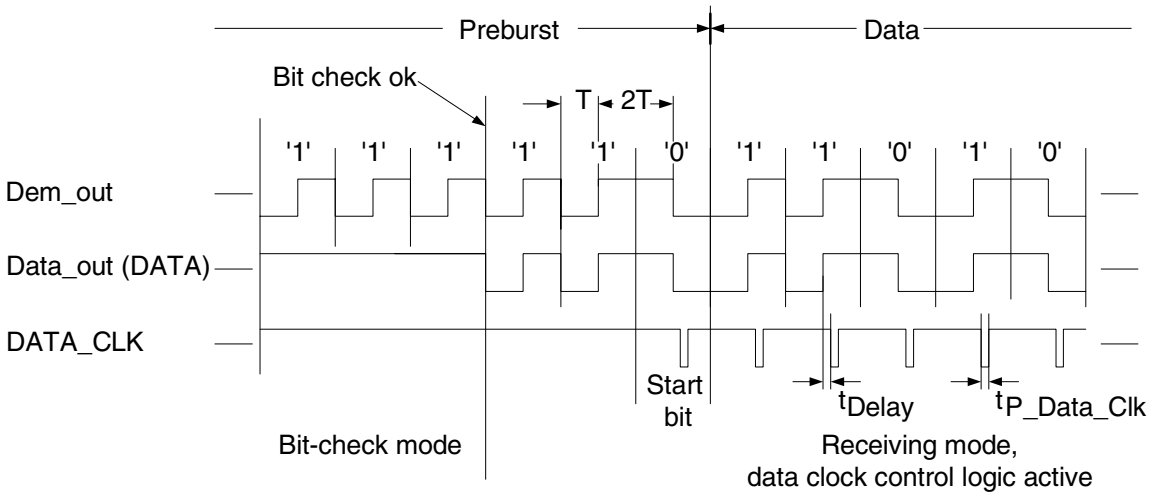
Figure 2. Simplified Application Circuit



Polling Concept

For low current consumption a polling concept is implemented to reduce the duty cycle. In polling mode the receiver is enabled periodically in configurable time intervals T_{Sleep} for a time $T_{Bit\text{-}check}$. During this bit-check time the integrated logic verifies if an occurred transmitter signal is valid. The criteria for a valid signal are the number of bits to be checked $N_{Bit\text{-}check}$ and the programmed bit-check limits T_{Lim_min} and T_{Lim_max} for time frame check. If no valid signal is detected the receiver is set back to sleep mode to save current. In case of a valid signal the receiver remains active and the demodulated data stream Dem_out is available at pin DATA. As soon as the receiver detects the start bit, a data clock signal appears on pin DATA_CLK as illustrated in Figure 3. Using this data clock a connected microcontroller can synchronise and evaluate the following data stream. For this the microcontroller only has to read in the logical level at pin DATA during every low pulse of the data clock.

Figure 3. Timing Diagram for $N_{Bit\text{-}check}$=3



After the end of the data transmission the receiver remains active until the receiver is commanded back to polling mode. This can be done by means of pin DATA or pin POLLING/_ON as described in the datasheet.

Architecture of the Registers

Description

The T5760/T5761 contains two 12-bit RAM registers, the OPMODE and the LIMIT register. Both registers can be configured by means of the serial bi-directional data line (DATA).

Bit 1 of Table 1/Table 2 represents the start bit and bit 2 is used for register identification. Bit 15 represents the stop bit to ensure that the desired values will be written into the selected register. A more detailed description of the registers is given in the data sheet and the following chapters.

OPMODE Register

The OPMODE register, as illustrated in Table 1, is used to configure the following parameters:

- Baud rate range (BR_Range): Bit 3 and Bit 4
- Number of bits to be checked ($N_{Bit\text{-}check}$): Bit 4 and Bit 5
- Modulation scheme (Modulation): Bit 7
- Sleep time (Sleep): Bit 8 ... Bit 12
- Sleep time extension (X_{Sleep}): Bit 13
- Automatic noise suppression (Noise Suppression): Bit 14

Table 1. OPMODE Register

		OPMODE Register												
Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
0	1	BR_Range		$N_{Bit\text{-}check}$		Modulation	Sleep					X_{Sleep}	Noise Suppression	0
		Baud 1	Baud 0	BitChk 1	BitChk 2	ASK/ _FSK	Sleep 4	Sleep 3	Sleep 2	Sleep1	Sleep 0	$X_{Sleep\ Std}$	Noise_ Disable	
Default values of Bit 3...14		0	0	0	1	0	0	0	1	1	0	0	1	

LIMIT register

The LIMIT register, see Table 2, serves to set the limits for time frame check. It is used to configure the following parameters:

- Lower limit value for bit check (T_{Lim_min}): Bit 3 ... Bit 8
- Upper limit value for bit check (T_{Lim_max}): Bit 9 ... Bit 14

Table 2. LIMIT Register

		LIMIT Register												
Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
0	0	Lim_min						Lim_max						0
		Lim_ min5	Lim_ min4	Lim_ min3	Lim_ min2	Lim_ min1	Lim_ min0	Lim_ max5	Lim_ max4	Lim_ max3	Lim_ max2	Lim_ max1	Lim_ max0	
Default values of Bit 3...14		0	1	0	1	0	1	1	0	1	0	0	1	

Application Hints

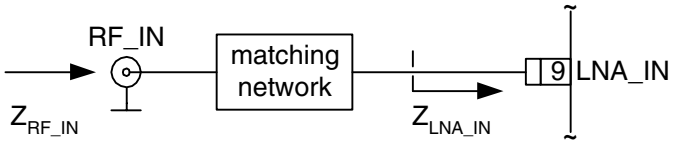
Input Matching

General Description

To achieve a high sensitivity the low noise amplifier (LNA) of the receiver T5760/T5761 has to be matched to the antenna input RF_IN. This is done as in Figure 4 by means of a matching network to adapt the LNA input impedance Z_{LNA_IN} to the RF input impedance Z_{RF_IN}.

The best noise figure NF of the LNA is achieved with power matching due to an integrated degeneration inductance.

Figure 4. RF Input Matching



The simplest matching network as shown in Figure 12 consists of two capacitors and a shunt inductor for the matching to 50 Ω without the use of a SAW front-end filter.

SAW Matching

Although the receiver T5760/T5761 can be operated with and without a SAW front-end filter, SAW filters may be used to increase the system selectivity and large signal handling capability.

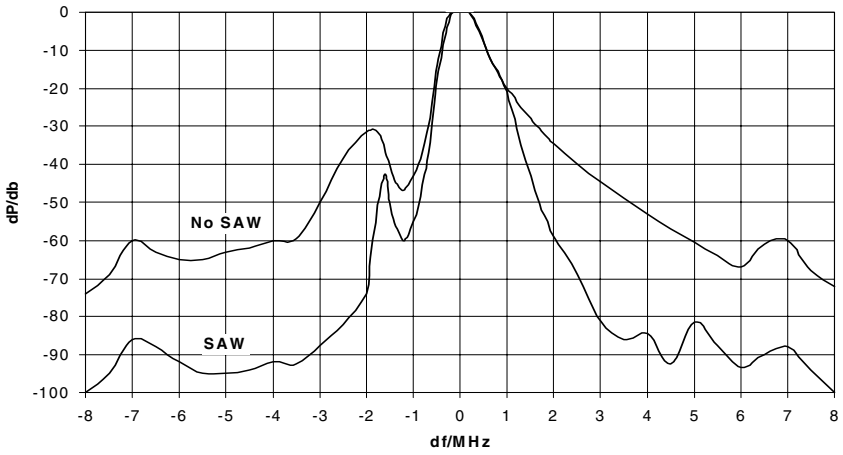
The SAW filter has to be power-matched to the source and to the load impedance for a low insertion loss, flat passband and for a good ultimate rejection. The source and the load impedance depends on the SAW type and is supplied by the manufacturer. Furthermore the cross talk of the SAW filter has to be minimized for a optimize rejection. The cross talk mainly depends on grounding. Hence it is recommended to use the suggested RF layout of the respective application.

Figure 5 shows the selectivity performance of the Receiver Application Board ATAB5760/ATAB5761 with and without a SAW front-end filter for 868.3 MHz in ASK mode. FSK mode exhibit similar behavior. The curves are shown such that the peak of the 'with SAW' response is aligned to that of the 'no SAW' response. If a SAW filter is used, an insertion loss of 3 dB has to be considered.

Printed Whip Receiving Antenna

For testing purposes a whip antenna is printed on the Receiver Application Board ATAB5760/ATAB5761. Normally a whip is a quarter wavelength long. Depending on the dielectric constant and the thickness of the PCB the length could be reduced. On the Receiver Application Board ATAB5760/ATAB5761 the length corresponds to about one fifth of the wavelength.

Figure 5. Receiving Frequency Response



Crystal Oscillator

Selection of the Crystal

The local oscillator frequency f_{LO}, determined by the integrated crystal oscillator (XTO) and a corresponding crystal (XTAL), is given by:

$$f_{LO} = f_{RF} - f_{IF} \qquad (1)$$

with f_{IF} according Table 3.

The crystal frequency is calculated in using the following formula:

$$f_{XTAL} = \frac{f_{LO}}{128} \qquad (2)$$

The intermediate frequency f_{IF} is given in Table 3.

Table 3. Intermediate Frequency

Parameter	Symbol	f_{RF} = 868.3 MHz Typ.	f_{RF} = 915 MHz Typ.	Variable Oscillator Typ.	Unit
Receiving Mode					
Intermediate frequency	f_{IF}	950	1000	$f_{IF} = \frac{f_{RF}}{915}$	kHz

The XTO is a single-pin series resonant oscillator so that only one capacitor together with a crystal connected in series to GND are needed as external elements.

Determination of the Crystal Load Capacitance

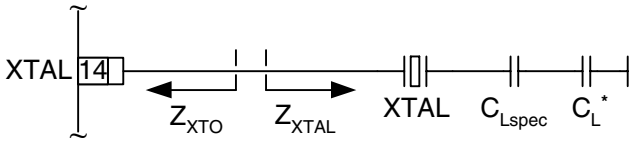
The series connection of a crystal and a corresponding load capacitor results in an impedance of Z_{XTAL}. For a series connection with a load capacitor of C_{Lspec} the impedance is pure real, i. e. $Im\{Z_{XTAL}\} = 0\ \Omega$. Moreover, the crystal nominally oscillates on the load resonance frequency f_L. Both values, C_{Lspec} and f_L, are specified by the crystal's manufacturer.

Z_{XTO} is the large signal input impedance of the crystal oscillator XTO seen into Pin XTAL in steady-state oscillation. For reliable oscillation start-up, the following conditions, according to Figure 6, have to be met:

$$Re\{Z_{XTO} + Z_{XTAL}\} < 0 \qquad (3)$$

$$Re\{Z_{XTO} + Z_{XTAL}\} = 0 \qquad (4)$$

Figure 6. Condition for Oscillation Startup



To fulfill condition (4) at the specified frequency f_L the load capacitance C_L* (only auxiliary value for calculation) is determined as:

$$C_L = \frac{1}{2 \times \pi \times f_L \times |Im\{Z_{XTO}\}|} \qquad (5)$$

In any application board there are additional parasitic board capacitances, C_{Stray1} and C_{Stray2}, according Figure 7. To determine the crystal load capacitance, C_L, that has to be mounted, the specified crystal capacitance C_{Lspec} as well as the board capacitances, C_{Stray1} and C_{Stray2}, have to be taken into account.

$$C_L = \frac{C_L \times C_{Lspec}}{C_L + C_{Lspec}} - (C_{Stray1} + C_{Stray2}) \qquad (6)$$

Figure 7. Determination of the Load Capacitor C_L

The start-up condition (3) is always met as long as the series resonance resistance of the crystal $Re\{Z_{XTAL}\}$ does not exceed the negative resistance of the oscillator $Re\{Z_{XTO}\}$ (a maximum value of 120 Ω as specified in the data sheet).

Using (6) the resulting load capacitance C_L can be calculated.

Calculation example for Receiver Application Board ATAB5760/ATAB5761 V2.0:

f_{RF} = 868.3 MHz (required RF frequency)

f_{IF} = 0.95 MHz (see Table 3)

f_{LO} = 867.35 MHz using (1),

$f_{XTAL} = f_L$ = 6.776172 MHz using (2)

$|(Im)\{Z_{XTO}\}|$ = 175Ω(design parameter)

C_{Lspec} = 16 pF (data from crystal manufacturer)

$C_{Stray1} = C_{Stray2}$ = 1.0 pF (estimated)

C_L = 134 pF using (5)

C_L = 12.3 pF using (6)

On the Receiver Application Board T5760/T5761 V2.0 for the frequency of 868.3 MHz a crystal load capacitance C_L = C9 = 12 pF is mounted.

Frequency Accuracy

Besides the production and temperature tolerances of the XTO the tolerances of the crystal have also to be considered. The tolerance calculation for the XTO using the ACAL 4730007678 crystal (4730007821 crystal for f_{RF} = 915 MHz respectively) results in:

Table 4. Frequency Tolerances

	Tolerance/ppm
XTO	±30
Crystal frequency over production margin	±30
Crystal frequency over ambient temperature (-40°C to +105°C)	±50
Aging of the crystal (15 years)	±10
Receiver tolerance in total	±120

Measurement of the LO Frequency

The frequency of the local oscillator (LO) can be determined by measuring the LO spurious emissions IS_{LORF} (see electrical characteristics of datasheet T5760/T5761). For this measurement a spectrum analyzer has to be connected to the RF input port. The typical value is -70 dBm for the No SAW version and -82 dBm for the SAW version.

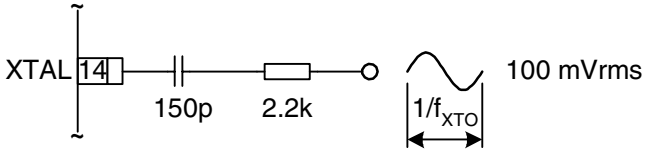
Receiving Frequency Shifting

To operate the receiver at different frequencies in the specified frequency range, the receiving frequency has to be shifted. Changing the XTO frequency, f_{XTO}, causes such a shift.

For example, for test purposes the frequency f_{XTO} can be shifted by feeding a sine wave into pin XTAL. For this purpose a signal generator with low phase noise should be used.

Figure 8 shows the circuit to feed the desired frequency into the XTO.

Figure 8. XTO Feed Circuit



Peripheral Circuit

DATA Interface

The DATA interface (see Figure 9) is used both for programming of the registers and as output of a received data stream.

A detailed programming description of the configuration registers by means of the data interface is given in chapter “Programming of the Configuration Registers” on page 22 The usable input levels are illustrated in Table 5.

The data interface have been designed for automotive requirements, i.e., it can be connected via the pull-up resistor R_{pup} to a voltage up to 20 V and is short-circuit protected. The applicable pull-up resistor depends on the load capacity C_L at Pin DATA and the selected baud rate range (see data sheet T5760/T5761, Table 12).

Figure 9. Data Interface

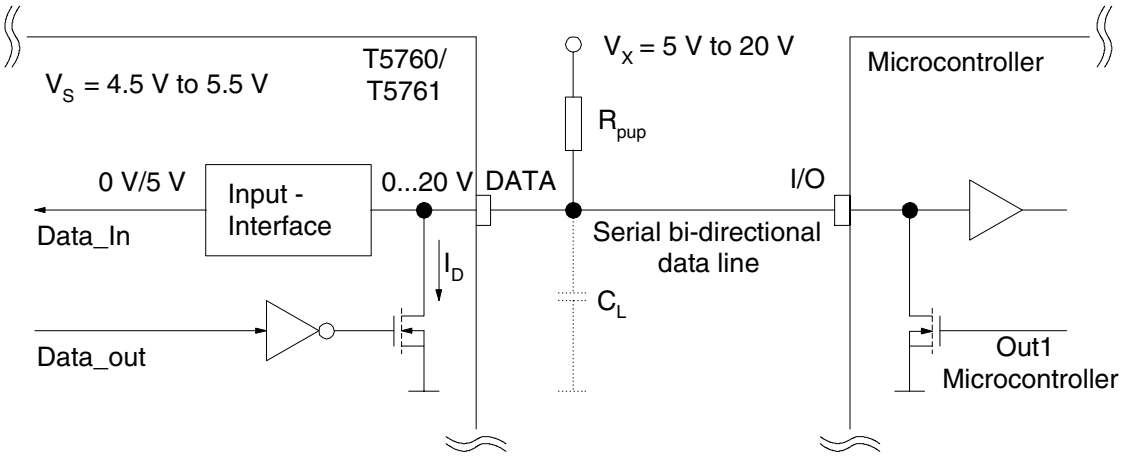


Table 5. Margins of the DATA Interface

Parameter	Test Condition	Symbol	Min.	Typ.	Max.	Unit
DATA output						
– Saturation voltage Low	$I_{ol} \leq 12$ mA	V_{ol}		0.35	0.8	V
	I_{ol} = 2 mA	V_{ol}		0.08	0.3	V
– maximum voltage at Pin DATA		V_{oh}			20	V
– quiescent current	V_{oh} = 20 V	I_{qu}			20	µA
– short-circuit current	V_{ol} = 0.8 V to 20 V	I_{ol_lim}	13	30	45	mA
– ambient temperature in case of permanent short-circuit	V_{oh} = 0 V to 20 V	t_{amb_sc}			85	°C
DATA input						
– Low level input voltage		V_{Il}			0.35 x V_S	V
– High level input voltage		V_{Ih}	0.65 x V_S			V

POLLING/_ON

Using pin POLLING/_ON it is possible to switch the receiver from polling mode to receiving mode or vice versa. According to Table 6 a high level results in polling mode and a low level in receiving mode.

Table 6. POLLING/_ON Level Margins

Parameter	Test Condition	Symbol	Min.	Typ.	Max.	Unit
POLLING/_ON input						
– Low level input voltage	Receiving mode	V_{Il}			0.2 x V_S	V
– High level input voltage	Polling mode	V_{Ih}	0.8 x V_S			V

If the receiver is in the receiving mode POLLING/_ON can be used to switch back to sleep mode and subsequently to polling mode as described in the data sheet.

Furthermore the receiver can be operated in a transparent mode where the integrated control logic is disabled and the receiver is controlled via a connected microcontroller. After a power-on reset, an initial programming of the OPMODE register is necessary in this case.

$N_{Bit\text{-}check,}$ Sleep and X_{Sleep} are programmed to 0 then BR_Range, Modulation and Noise Suppression have to be selected accordingly.

DATA_CLK

As soon as the receiver detects the start bit, a data clock signal appears on pin DATA_CLK as illustrated in Table 4 on page 9. Using this data clock, an incoming data stream can be strobed into a shift register. A connected microcontroller can easily synchronise and evaluate this data stream.

The DATA_CLK can only be used for Manchester- and Bi-phase coded signals. The level margins are given in Table 7.

Table 7. DATA_CLK Level Margins

Parameter	Test Condition	Symbol	Min.	Typ.	Max.	Unit
DATA_CLK output						
- Saturation voltage low	IDATA_CLK = 1 mA	V_{ol}		0.1	0.4	V
- Saturation voltage high	IDATA_CLK = -1 mA	V_{oh}	V_S - 0.4 V	V_S - 0.15 V		V

Note: If the DATA_CLK is used, it should be connected to the microcontroller via a resistor of 2.2 kΩ directly at pin DATA_CLK.

CDEM

The capacitor CDEM defines the high-pass cut-off frequency of the data filter and should be selected according to Table 8. A more detailed description of the data filter is given in the data sheet.

Table 8. Recommended Values for CDEM

Parameter	Test Condition	Symbol	Min.	Typ.	Max.	Unit
Recommended CDEM for best performance	BR_Range0 (default) BR_Range1 BR_Range2 BR_Range3	CDEM		39 22 12 8.2		nF nF nF nF

IC_ACTIVE

Pin IC_ACTIVE is an IC condition indicator. In sleep mode the output level is low. For start-up, bit-check and receiving mode the output level is high. The level margins are given in Table 9.

This pin can be used to control different functions, e.g., an additional LNA, an antenna switch, etc. or simply to indicate a successful bit-check.

Table 9. IC_ACTIVE Level Margins

Parameter	Test Condition	Symbol	Min.	Typ.	Max.	Unit
IC_ACTIVE output - Saturation voltage low - Saturation voltage high	 IIC_ACTIVE = 1 mA IIC_ACTIVE = -1 mA	 V_{ol} V_{oh}	 V_S - 0.4 V	 0.1 V_S - 0.15 V	 0.4 	 V V

Test Pins

The pins Test 1 to Test 4 are only used for testing purpose. In operation these pins have to be connected according the following Table 10.

Table 10. Obligatory Connections of the Test Pins During Operation

Pin	Symbol	Connected to
5	Test 1	GND
11	Test 2	Not connected
12	Test 3	GND
16	Test 4	DVCC

Sensitivity Reduction

For full sensitivity Pin SENS should be connected to GND directly or over an external resistor, R_{Sens}.

A sensitivity reduction can be performed in connecting R_{Sens} to V_S. The reduced sensitivity is defined by the value of R_{Sens} according to Table 11.

By connecting R_{Sens} to V_S or GND via a microcontroller the receiver can be switched from full sensitivity to reduced sensitivity or vice versa at any time.

Table 11. R_{SENS} for Reduced Sensitivity

Parameter	Test Condition	Symbol	Min.	Typ.	Max.	Unit
Reduced sensitivity	R_{Sens} connected from pin SENS to V_S, input matched according to Figure 12/ Figure 13, f_{IN} = 868.3 MHz / 915 MHz					dBm (peak level)
	R_{Sens} = 56 kΩ	P_{Ref_Red}	-63	-68	-73	dBm
	R_{Sens} = 100 kΩ	P_{Ref_Red}	-72	-77	-82	dBm
Reduced sensitivity variation over full operating Range	$P_{Red} = P_{Ref\_Red} + DP_{Red}$					
	R_{Sens} = 56 kΩ	DP_{Red}	5	0	0	dB
	R_{Sens} = 100 kΩ	DP_{Red}	5	0	0	dB
Reduced sensitivity variation for different values of R_{Sens}	Values relative to R_{Sens} = 56 kΩ $P_{Red} = P_{Ref\_Red} + DP_{Red}$					
	R_{Sens} = 56 kΩ	DP_{Red}		0		dB
	R_{Sens} = 68 kΩ	DP_{Red}		-3.5		dB
	R_{Sens} = 82 kΩ	DP_{Red}		-6.0		dB
	R_{Sens} = 100 kΩ	DP_{Red}		-9.0		dB
	R_{Sens} = 120 kΩ	DP_{Red}		-11.0		dB
	R_{Sens} = 150 kΩ	DP_{Red}		-13.5		dB

Decoupling

Concerning the PCB layout, attention must be paid to the decoupling components in order to minimize ripples on the power supply.

For the supply voltage input port two decoupling capacitors C_6 and C_7 (approximately 10 nF, NP0 and 4.7 µF, Tantal) are recommended to prevent voltage break-in and ripples. Make sure that every different supply voltage (AVCC, DVCC) on any application PCB is lead separately from the supply voltage input port and is properly decoupled by further capacitors ,C_5 and C_8 (approximately 10 nF, NP0), to its ground (AGND, DGND).

Always try to layout a ground plane on the reverse side and use vias for decoupling. In mixed signal layout's the separation of digital and analog groups is obligatory. Try to design the microcontroller part separately from the RF part of the receiver.

Calculation of Receiver Parameters

Bit Check Limits

During bit check the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter and signals due to noise. This is done by subsequent time frame checks where the distance between two signal edges are continuously compared to a programmable time window.

The limits of the time window, T_{Lim_min} and T_{Lim_max}, must be programmed by the microcontroller depending on the signal baud rate. Generally we recommend the limits:

T_{Lim_min} = 0.7 x (the shortest distance)

T_{Lim_max} = 1.3 x (the longest distance)

between the two signal edges of the transmitter preburst during the bit check.

Calculation of T_{Lim_min} and T_{Lim_max} for modulation schemes like Bi-phase and Manchester where the duty cycle is 50 % and the preburst consists of a row of ‘1’ or a row of ‘0’:

$$T_{Lim\_min} = \frac{0.7}{2 \times \text{signal baud rate}} \quad (7)$$

$$T_{Lim\_max} = \frac{1.3}{2 \times \text{signal baud rate}} \quad (8)$$

The bit-check limits, which have to be programmed into the limit register, are determined by means of the following formulas:

$$Lim\_min = \frac{T_{Lim\_min}}{T_{XClk}} \quad (9)$$

$$Lim\_max = \frac{T_{Lim\_max}}{T_{XClk}} + 1 \quad (10)$$

The distribution of t_{ee} (edge-to-edge output at pin DATA) due to noise shows that the short t_{ee} occurs more often than the long t_{ee}. This means that the lower limit Lim_min has an essential influence regarding wake-up of the receiver. To prevent the wake-up of the T5760/T5761 due to noise, Lim_min should not be programmed below ’Lower limit of Lim_min’ as illustrated in Table 12. The ’Lower limit of Lim_min’ depends on the selected baud rate range (BR_range) and on the number of bits to be checked.

Generally, a wake-up due to noise becomes more unlikely if a smaller time window is selected or the number of bits to be checked is increased.

Table 12. Lower Limits of Lim_min

BR_range	Number of Bits to Be Checked	Lower Limit of Lim_min
B0 (1.0 to 1.8 kBaud)	3	14
	6	11
	9	11
B1 (1.8 to 3.2 kBaud)	3	15
	6	11
	9	11
B2 (3.2 to 5.6 kBaud)	3	15
	6	11
	9	11
B3 (5.6 to 10.0 kBaud)	3	15
	6	11
	9	11

To facilitate selecting the lower and upper limit values for the bit check Table 13 and Table 14 are given. If the values of T_{Lim_min} and T_{Lim_max} have already been calculated the limits Lim_min and Lim_max in decimal format can be read from the tables as follows:

1. Take the calculated value of T_{Lim_min} (e.g., 350 µs for f_{Sig} = 1 kBd) and search this value for the desired frequency f_{RF} and the baud rate range (BR0 .. BR3).
2. Choose the closest lower value (e.g., 347 µs for f_{RF} = 868.3 MHz and BR0).
3. Simply read out the corresponding value Lim_min (e.g., 21 for T_{Lim_min} = 347 µs).
4. Take the calculated value of T_{Lim_max} (e.g., 650 µs for f_{Sig} = 1 kBd) and search this value for the desired frequency f_{RF} and the baud rate range (BR0 .. BR3).
5. Choose the closest higher value (e.g., 661 µs for f_{RF} = 868.3 MHz and BR0).
6. Simply read out the corresponding value Lim_max (e.g., 41 for T_{Lim_max} = 661 µs).
7. Convert the determined values into binary format for programming of the LIMIT register.

Table 13. Lower Limit Value for Bit-check

	T_{Lim_min} in µs							
	f_{RF} = 868.3 MHz				f_{RF} = 915 MHz			
Lim_min	BR0	BR1	BR2	BR3	BR0	BR1	BR2	BR3
10	165	83	41	21	157	78	39	20
11	182	91	45	23	173	86	43	22
12	198	99	50	25	188	94	47	24
13	215	107	54	27	204	102	51	25
14	231	116	58	29	220	110	55	27
15	248	124	62	31	235	118	59	29
16	264	132	66	33	251	125	63	31
17	281	141	70	35	267	133	67	33
18	298	149	74	37	282	141	71	35
19	314	157	79	39	298	149	75	37
20	331	165	83	41	314	157	78	39
21	347	174	87	43	329	165	82	41
22	364	182	91	45	345	173	86	43
23	380	190	95	48	361	180	90	45
24	397	198	99	50	376	188	94	47
25	413	207	103	52	392	196	98	49
26	430	215	107	54	408	204	102	51
27	446	223	112	56	424	212	106	53
28	463	231	116	58	439	220	110	55
29	479	240	120	60	455	227	114	57
30	496	248	124	62	471	235	118	59
31	512	256	128	64	486	243	122	61
32	529	264	132	66	502	251	125	63
33	545	273	136	68	518	259	129	65
34	562	281	141	70	533	267	133	67
35	579	289	145	72	549	274	137	69
36	595	298	149	74	565	282	141	71
37	612	306	153	76	580	290	145	73
38	628	314	157	79	596	298	149	75
39	645	322	161	81	612	306	153	76
40	661	331	165	83	627	314	157	78
41	678	339	169	85	643	322	161	80
42	694	347	174	87	659	329	165	82
43	711	355	178	89	674	337	169	84
44	727	364	182	91	690	345	173	86
45	744	372	186	93	706	353	176	88
46	760	380	190	95	722	361	180	90
47	777	388	194	97	737	369	184	92

Table 13. Lower Limit Value for Bit-check (Continued)

	T_{Lim_min} in µs							
	f_{RF} = 868.3 MHz				f_{RF} = 915 MHz			
Lim_min	BR0	BR1	BR2	BR3	BR0	BR1	BR2	BR3
48	793	397	198	99	753	376	188	94
49	810	405	202	101	769	384	192	96
50	826	413	207	103	784	392	196	98
51	843	422	211	105	800	400	200	100
52	860	430	215	107	816	408	204	102
53	876	438	219	110	831	416	208	104
54	893	446	223	112	847	424	212	106
55	909	455	227	114	863	431	216	108
56	926	463	231	116	878	439	220	110
57	942	471	236	118	894	447	224	112
58	959	479	240	120	910	455	227	114
59	975	488	244	122	925	463	231	116
60	992	496	248	124	941	471	235	118
61	1008	504	252	126	957	478	239	120
62	1025	512	256	128	973	486	243	122
63	1041	521	260	130	988	494	247	124

Table 14. Upper Limit Value for Bit-check

	T_{Lim_max} in µs							
	f_{RF} = 868.3 MHz				f_{RF} = 915 MHz			
Lim_max	BR0	BR1	BR2	BR3	BR0	BR1	BR2	BR3
12	182	91	45	23	173	86	43	22
13	198	99	50	25	188	94	47	24
14	215	107	54	27	204	102	51	25
15	231	116	58	29	220	110	55	27
16	248	124	62	31	235	118	59	29
17	264	132	66	33	251	125	63	31
18	281	141	70	35	267	133	67	33
19	298	149	74	37	282	141	71	35
20	314	157	79	39	298	149	75	37
21	331	165	83	41	314	157	78	39
22	347	174	87	43	329	165	82	41
23	364	182	91	45	345	173	86	43
24	380	190	95	48	361	180	90	45
25	397	198	99	50	376	188	94	47
26	413	207	103	52	392	196	98	49
27	430	215	107	54	408	204	102	51
28	446	223	112	56	424	212	106	53
29	463	231	116	58	439	220	110	55
30	479	240	120	60	455	227	114	57
31	496	248	124	62	471	235	118	59
32	512	256	128	64	486	243	122	61
33	529	264	132	66	502	251	125	63
34	545	273	136	68	518	259	129	65
35	562	281	141	70	533	267	133	67
36	579	289	145	72	549	274	137	69
37	595	298	149	74	565	282	141	71
38	612	306	153	76	580	290	145	73
39	628	314	157	79	596	298	149	75
40	645	322	161	81	612	306	153	76
41	661	331	165	83	627	314	157	78
42	678	339	169	85	643	322	161	80
43	694	347	174	87	659	329	165	82
44	711	355	178	89	674	337	169	84
45	727	364	182	91	690	345	173	86
46	744	372	186	93	706	353	176	88
47	760	380	190	95	722	361	180	90
48	777	388	194	97	737	369	184	92
49	793	397	198	99	753	376	188	94

Table 14. Upper Limit Value for Bit-check (Continued)

	T_{Lim_max} in µs							
	f_{RF} = 868.3 MHz				f_{RF} = 915 MHz			
Lim_max	BR0	BR1	BR2	BR3	BR0	BR1	BR2	BR3
50	810	405	202	101	769	384	192	96
51	826	413	207	103	784	392	196	98
52	843	422	211	105	800	400	200	100
53	860	430	215	107	816	408	204	102
54	876	438	219	110	831	416	208	104
55	893	446	223	112	847	424	212	106
56	909	455	227	114	863	431	216	108
57	926	463	231	116	878	439	220	110
58	942	471	236	118	894	447	224	112
59	959	479	240	120	910	455	227	114
60	975	488	244	122	925	463	231	116
61	992	496	248	124	941	471	235	118
62	1008	504	252	126	957	478	239	120
63	1025	512	256	128	973	486	243	122

Sleep Time

In increasing the sleep time, T_{Sleep}, the average current consumption, I_{Spoll}, of the receiver can be reduced significantly (according to formula (13)). In this case the preburst length, $T_{Preburst}$, of the transmitter telegram has to be adapted to:

$$T_{Preburst} \geq T_{Sleep} + T_{Startup} + T_{Bit\text{-}check} + T_{Start\_microcontroller} \quad (11)$$

To calculate the obligatory preburst length $T_{Preburst}$ the maximum bit-check time $T_{Bit\text{-}check}$ (given in the data sheet, chapter Electrical Characteristics) for a valid input signal is inserted in formula (11).

For a selected sleep time T_{Sleep} the 5-bit word (start value for the sleep counter) defined by Sleep0 to Sleep4 in the OPMODE register is given by:

$$Sleep = \frac{T_{Sleep}}{X_{Sleep} \times 1024 \times T_{Clk}} \quad (12)$$

The start value for the sleep counter can be determined by means of Table 15 in the following order:

1. Select a sleep time T_{Sleep} (e.g., 12.695 ms for f_{RF} = 868.3 MHz and X_{Sleep} = 1)
2. Simply read out the corresponding value Sleep (e.g. 6 for T_{Sleep} = 12.695 ms)
3. Convert the value determined into binary format to program the 5-bit word into the OPMODE register

For a further decrease of the average current consumption according to formula (13) an extension factor, X_{Sleep}, for the sleep time is available. X_{Sleep} can be set to ‘1’ or ‘8’ (see also data sheet T5760/T5761, Table 8). Setting X_{Sleep} to ‘8’ results in an 8 times longer sleep time T_{Sleep} compared to the default configuration.

Table 15. Start Value for Sleep Counter

Sleep	T_{Sleep} in ms			
	f_{RF} = 868.3 MHz		f_{RF} = 915 MHz	
	X_{Sleep} =		X_{Sleep} =	
	1	8	1	8
0	Receiver is continuously polling until a valid signal occurs			
1	2.116	16.926	2.008	16.062
2	4.232	33.853	4.016	32.124
3	6.347	50.779	6.023	48.186
4	8.463	67.705	8.031	64.248
5	10.579	84.632	10.039	80.310
6	12.695	101.558	12.047	96.372
7	14.811	118.484	14.054	112.434
8	16.926	135.410	16.062	128.496
9	19.042	152.337	18.070	144.558
10	21.158	169.263	20.078	160.621
11	23.274	186.189	22.085	176.683
12	25.389	203.116	24.093	192.745
13	27.505	220.042	26.101	208.807
14	29.621	236.968	28.109	224.869
15	31.737	253.895	30.116	240.931
16	33.853	270.821	32.124	256.993
17	35.968	287.747	34.132	273.055
18	38.084	304.674	36.140	289.117
19	40.200	321.600	38.147	305.179
20	42.316	338.526	40.155	321.241
21	44.432	355.453	42.163	337.303
22	46.547	372.379	44.171	353.365
23	48.663	389.305	46.178	369.427
24	50.779	406.231	48.186	385.489
25	52.895	423.158	50.194	401.551
26	55.011	440.084	52.202	417.613
27	57.126	457.010	54.209	433.675
28	59.242	473.937	56.217	449.738
29	61.358	490.863	58.225	465.800
30	63.474	507.789	60.233	481.862
31	Permanent sleep mode			

Average Supply Current in Polling Mode

The average current consumption in polling mode, I_{Spoll}, depends on the duty cycle of the active mode and can be determined by:

$$I_{Spoll} = \frac{I_{Soff} \times T_{Sleep} + I_{Son} \times (T_{Startup} + T_{Bit\text{-}check})}{T_{Sleep} + T_{Startup} + T_{Bit\text{-}check}} \quad (13)$$

In formula (13) $T_{Bit\text{-}check}$ is the typical bit-check time for no RF signal (given in the data sheet, chapter 'Electrical Characteristics').

Calculation Examples

Table 16 gives six calculation examples for different settings

Table 16. Calculation Examples

Parameter	Setting for	Ex. 1	Ex. 2	Ex. 3	Ex. 4	Ex. 5	Ex. 6	Unit
Selected Parameters and Values Arising from								
Output frequency f_{RF}	Tx, Rx	868.3	868.3	868.3	915	915	868.3	MHz
Signal baud rate f_{Sig}	Tx	1.0	1.0	1.0	2.4	4.8	9.6	kBd
BR_Range	Rx	0	0	0	1	2	3	
$N_{Bit\text{-}check}$	Rx	3	3	3	6	6	9	
Modulation	Tx, Rx	FSK	ASK	FSK	ASK	FSK	FSK	
T_{Sleep}	Rx	12.695	12.695	50.779	60.233	24.093	50.779	ms
T_{Clk}	Rx	2.0662	2.0662	2.0662	1.9607	1.9607	2.0662	µs
T_{XClk}	Rx	16.53	16.53	16.53	7.84	3.92	2.07	µs
$T_{Startup}$	Rx	1852	1852	1852	1049	1049	662	µs
$T_{Bit\text{-}check}$ typ. (no RF applied)	Rx	0.45	0.45	0.45	0.24	0.14	0.08	ms
$T_{Bit\text{-}check}$ max. (valid input signal)	Rx	3.5	3.5	3.5	2.71	1.35	0.99	ms
$T_{Start\_microcontroller}$	Rx	1	1	1	1	1	1	ms
I_{Soff} typ.	Rx	170	170	170	170	170	170	µA
I_{Son} typ.	Rx	7.8	7.4	7.8	7.4	7.8	7.8	mA
Calculated Parameters								
T_{Lim_min}	Rx	350.0	350.0	350.0	145.8	72.9	36.5	µs
T_{Lim_max}	Rx	650.0	650.0	650.0	270.8	135.4	67.7	µs
Lim_min	Rx	21	21	21	18	18	17	
Lim_max	Rx	41	41	41	36	36	34	
Sleep	Rx	6	6	24	30	12	24	
X_{Sleep}	Rx	1	1	1	1	1	1	
I_{Spoll} typ.	Rx	1341	1280	501	321	529	280	µA
$T_{Preburst}$ min.	Tx	19.05	19.05	57.13	64.99	27.49	53,43	ms

Programming of the Configuration Registers

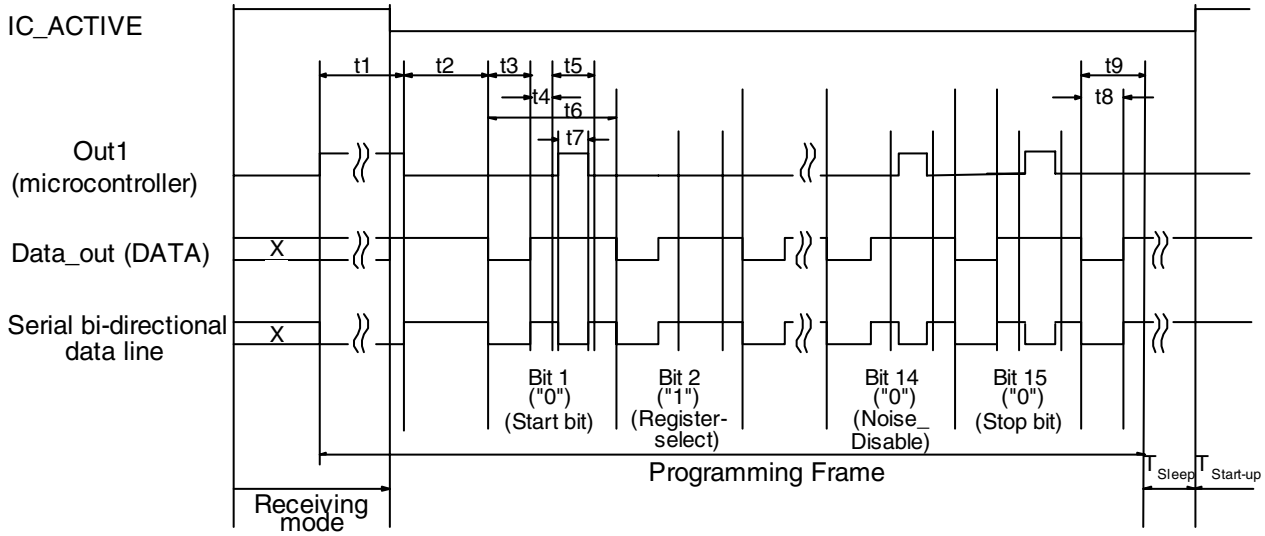
The programming of configuration registers is performed via the single-wire bi-directional data interface (see Figure 9) which is also used to transfer a received data stream to a connected microcontroller.

Programming of a register is possible in sleep-mode as well as in the active-mode of the receiver. Figure 10 illustrates the programming timing exemplary of the OPMODE register and Table 17 the obligatory time intervals.

The programming start pulse ,t1, initiates the programming of the configuration registers and is generated by a connected microcontroller. By means of this start pulse the serial data line ,DATA, is pulled down for the time period, t1. After DATA has been released the receiver becomes the master device. When the programming delay period ,t2, is elapsed the receiver emits 15 subsequent synchronization pulses with the pulse length, t3. After each of these pulses a programming window ,t5, occurs with a starting delay of t4. Within the programming window, t5, the individual bits are set. If the microcontroller pulls down the serial data line, DATA, for the time period, t7, during t5 the according bit is set to '0'. If no programming pulse, t7, is issued this bit is set to '1'. All 15 bits of the register are subsequently programmed in this way. The time frame to program a bit is defined by t6.

Bit 15 is followed by the equivalent time window t9. If the just programmed bit sequence is equivalent with the already stored register content the equivalent acknowledge pulse t8 (E_Ack) occurs during t9. In programming the respective register twice E_Ack should be used to verify the register content. Both the OPMODE register and the LIMIT register can be programmed sequentially in the described way.

Figure 10. Programming Timing of OPMODE Register



If bit 1 is set to '1' the OFF-command is executed to set the receiver back to polling mode simultaneously. The usable pulse length, t1, depends on the selected baud rate range (see Table 17).

In applying a programming start pulse of $t1_{min} < t1 < 5632 \times T_{Clk}$ the OFF-command will only be performed if the receiver is not in reset mode. In reset mode, the OFF-command will not be executed and the reset marker (RM) will not be deleted. Hence the reset marker (RM) is still present at pin DATA. This period is generally used to switch the receiver to polling mode or to start programming of a register.

After a power on reset (POR) an extended time t1 > 7936 x T_{Clk} is needed. In this case the OFF-command will definitely be performed, a possible present reset marker (RM) will be deleted and the registers OPMODE and LIMIT will be set back to the default values.

Table 17. Programming Time Intervals

Parameter	Test Condition	Symbol	f_{RF}= 868.3 MHz 6.776172 MHz Oscillator		f_{RF}= 915 MHz 7.140625 MHz Oscillator		Variable Oscillator		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Configuration of the Receiver									
Frequency of the reset marker	Frequency is stable within 50 ms after POR	f_{RM}	118.2	118.2	124.5	124.5	$\frac{1}{4096 \times T_{Clk}}$	$\frac{1}{4096 \times T_{Clk}}$	Hz
Programming start pulse	BR_Range0	t1	3355	11637	3184	11043	1624 x T_{Clk}	5632 x T_{Clk}	µs
	BR_Range1		2273	11637	2168	11043	1100 x T_{Clk}	5632 x T_{Clk}	µs
	BR_Range2		1731	11637	1643	11043	838 x T_{Clk}	5632 x T_{Clk}	µs
	BR_Range3		1461	11637	1386	11043	707 x T_{Clk}	5632 x T_{Clk}	µs
	after POR		16397		15560		7936 x T_{Clk}		µs
Programming delay period		t2	795	797	754	756	384.5 x T_{Clk}	385.5 x T_{Clk}	µs
Synchronization pulse		t3	264	264	251	251	128 x T_{Clk}	128 x T_{Clk}	µs
Delay to the start of the program window		t4	131	131	125	125	63.5 x T_{Clk}	63.5 x T_{Clk}	µs
Programming window		t5	529	529	502	502	256 x T_{Clk}	256 x T_{Clk}	µs
Time frame of a bit		t6	1058	1058	1004	1004	512 x T_{Clk}	512 x T_{Clk}	µs
Programming pulse		t7	132	529	125	502	64 x T_{Clk}	256 x T_{Clk}	µs
Equivalent acknowledge pulse (E_Ack)		t8	264	264	251	251	128 x T_{Clk}	128 x T_{Clk}	µs
Equivalent time window		t9	533	533	506	506	258 x T_{Clk}	258 x T_{Clk}	µs
OFF-bit programming window		t10	929	929	881	881	449.5 x T_{Clk}	449.5 x T_{Clk}	µs

Additional information about the programming of the configuration registers is given in datasheet T5760/T5761.

Receiver Application Board ATAB5760/ATAB5761 V2.0

General Description

The Receiver Application Board ATAB5760/ATAB5761 V2.0 is a programmable RF remote control receiver for both ASK and FSK modulation. The essential component of the PCB is the receiver IC T5760 (868.3 MHz) or T5761 (915 MHz) respectively. Atmel provides three different types of Receiver Application Board in the frequency band from 868 MHz to 928 MHz (see Table 18).

Table 18. Ordering Information

Extended Type Number	Receiver IC	Frequency	Version (Printed on PCB)	Remarks
ATAB5760-S	T5760	868.3 MHz	T5760 V2.0 (SAW)	including SAW front end filter
ATAB5760-N	T5760	868.3 MHz	T5760/T5761 V2.0 (No SAW)	without SAW front end filter
ATAB5761-N	T5761	915 MHz	T5760/T5761 V2.0 (No SAW)	without SAW front end filter

Technical Features for Default Settings

- Power supply: 4.5 V to 5.5 V
- Typical quiescent supply current: 170 µA
- Typical polling supply current: 1.76 mA (including current through LED D1)
- Typical receiving supply current: 10.5 mA (including current through LED D1)
- Receiving frequency: ≈ 868.3 MHz (ATAB5760) / ≈ 915 MHz (ATAB5761)
- Input sensitivity (BER ≤ 10^{-3}): ≈ -103 dBm (SAW) / ≈ -106 dBm (No SAW)
- Reduced sensitivity can be set by means of resistor R2. For more information see chapter “Sensitivity Reduction” on page 13.
- Printed monopole receiving antenna can be connected through solderable jumper BR2. Jumper BR1 has to be unsoldered in this case. Assuming an effective radiated power (ERP) of -11 dBm with a corresponding transmitter a free space link range of larger than 150 m is achieved in default mode.

Operation of the Receiver Application Board

Default Software Settings

- BR_Range: 1.0 kBaud to 1.8 kBaud
- $N_{Bit\text{-}check}$: 3
- Modulation: FSK
- T_{Sleep}: 12.695 ms (868.3 MHz)/12.047 ms (915 MHz)
- X_{Sleep}: 1
- Noise suppression: active
- T_{Lim_min} 347 µs (868.3 MHz)/329 µs (915 MHz)
- T_{Lim_max} 661 µs (868.3 MHz)/627 µs (915 MHz)
- Testword: F09AF09A

Getting Started

The Receiver Application Board ATAB5760/ATAB5761 can either be operated in conjunction with the Basic Application Board as described in the Hardware Description ATAK57xx or stand-alone. The stand-alone mode is operated as follows:

1. Apply +5 V between pin VCC and GND; a power-on reset (POR) is generated automatically.
2. Delete the reset marker at pin DATA by means of a debounced low pulse ($t1 \geq 16.4$ ms).
3. Feed an FSK-modulated RF signal into the SMB connector X3 or use the printed receiving antenna in conjunction with the corresponding Transmitter Application Board ATAB5750 to transmit a valid signal.
4. If a low level is applied to pin POLLING/_ON, the receiver is permanently in receiving mode. In case of applying a high level, the receiver is in polling mode.
5. In polling mode the receiver switches to the receiving mode if the bit check was successful. To set the receiver back to polling mode either apply a debounced low pulse ($ton2 \geq 16.5$ ms) at pin POLLING/_ON or use the pin DATA as described in the data sheet.

Configuration of the Receiver

1. Power up the PC and start the operating system.
2. Plug the Receiver Application Board ATAB5760/ATAB5761 onto the Basic Application Board as described in the Hardware Description ATAK57xx.
3. Switch on the 5 V power supply of the Basic Application Board.
4. Connect the serial link cable (RS232) to an unused serial port (Com1, Com2).
5. Start the RF Design Kit Software as described in the Software Description ATAK57xx.
6. Program the receiver with the target values.

For reprogramming of the transmitter repeat steps 5 and 6.

Application Board Circuit

Figure 11. Application Schematic 868.3 MHz (SAW)

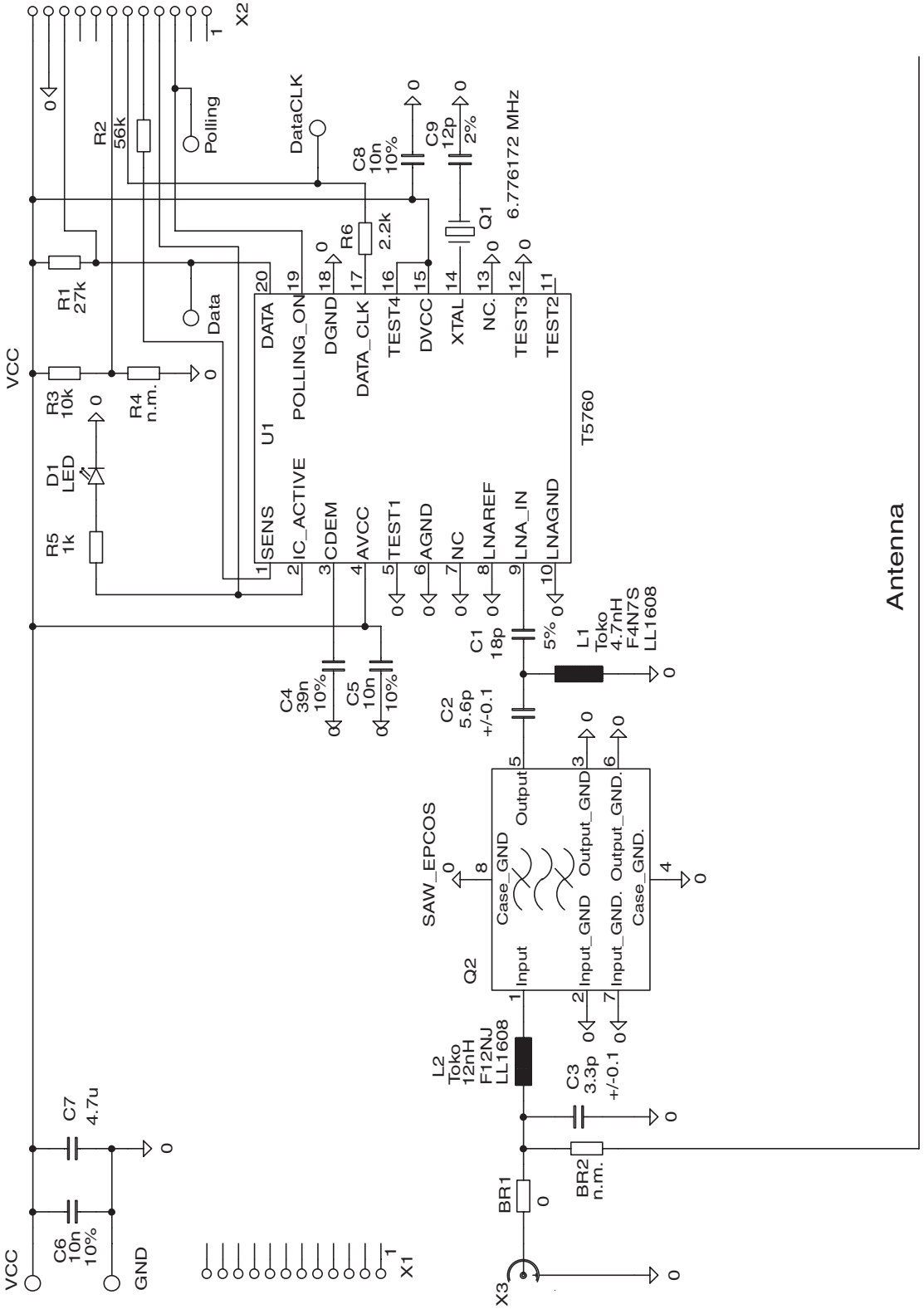


Figure 12. Application Schematic 868.3 MHz (No SAW)

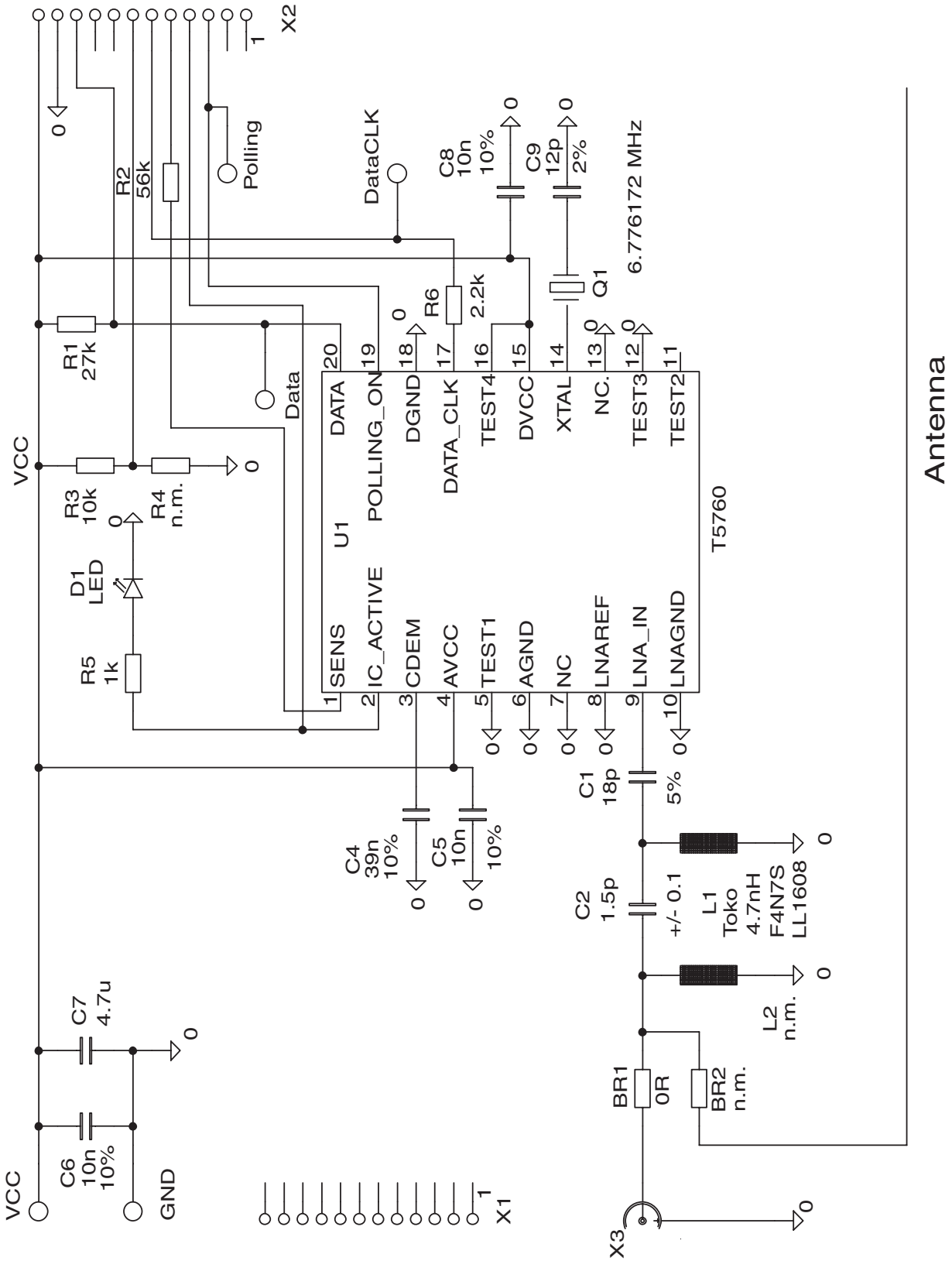
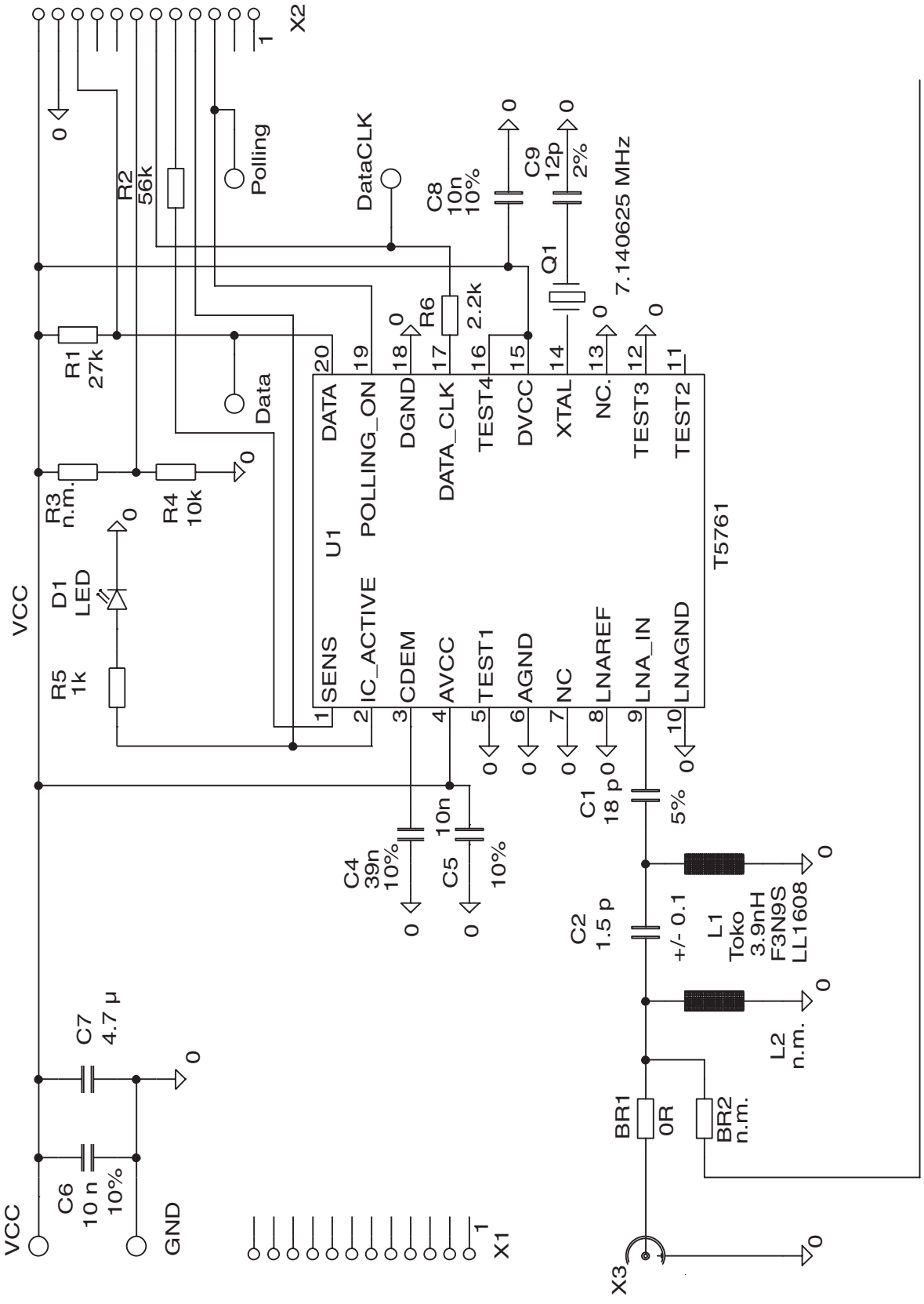


Figure 13. Application Schematic 915 MHz (No SAW)



Application Board Layout

Figure 14. Component Placement of Top Layer (SAW)

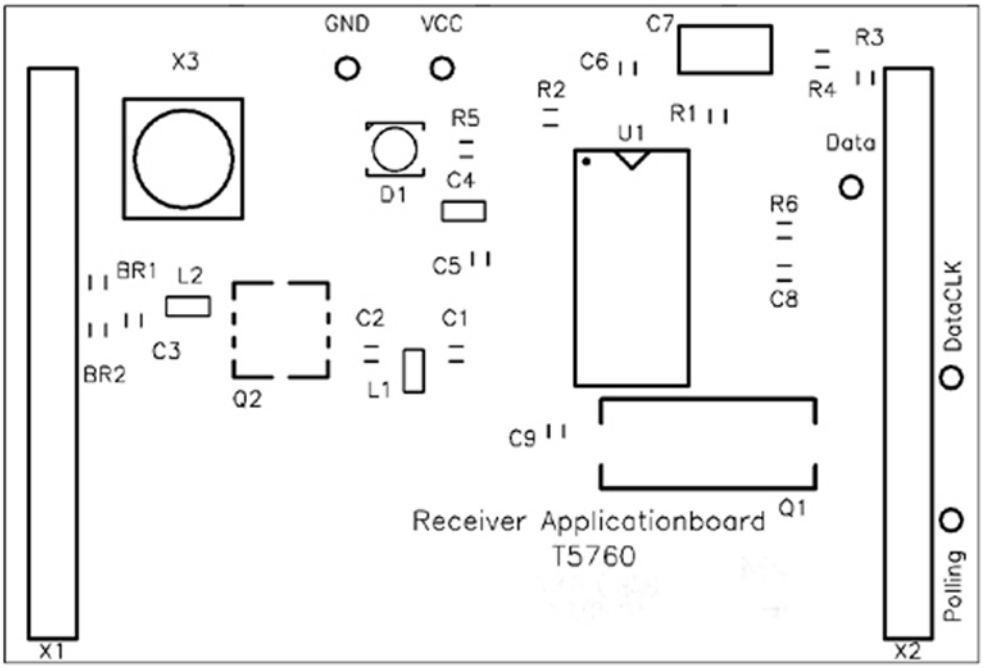


Figure 15. Layout of Top Layer (SAW)

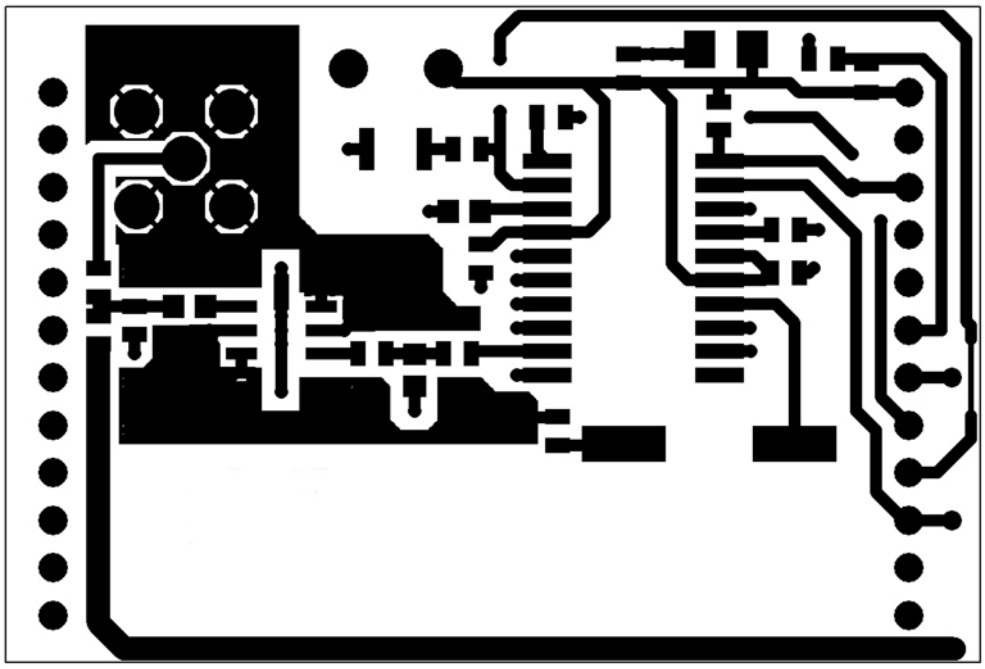


Figure 16. Layout of Bottom Layer (SAW)

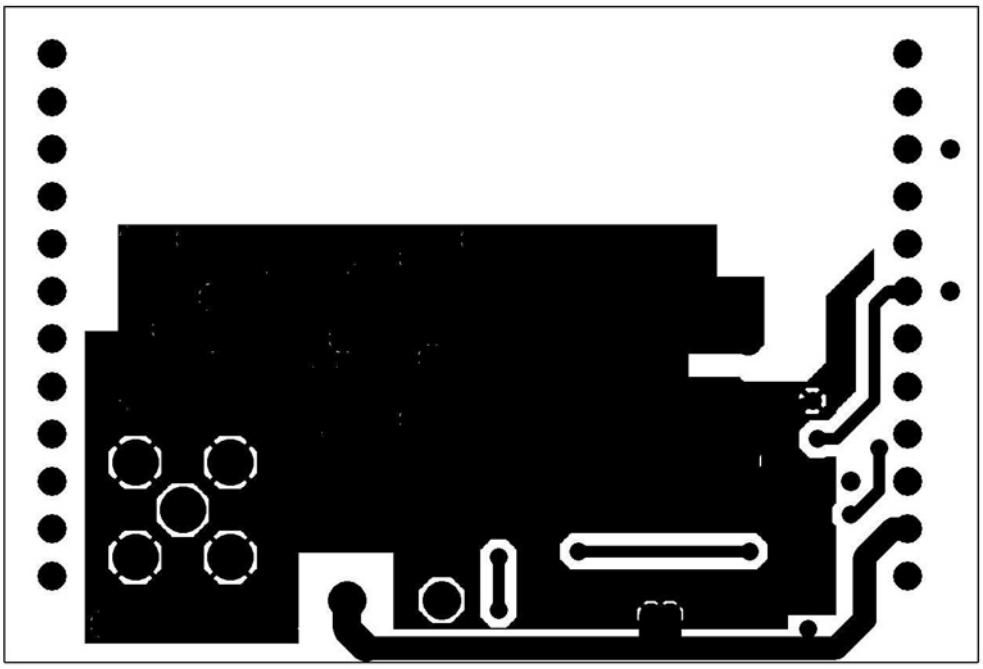


Figure 17. Components Placement of Top Layer (No SAW)

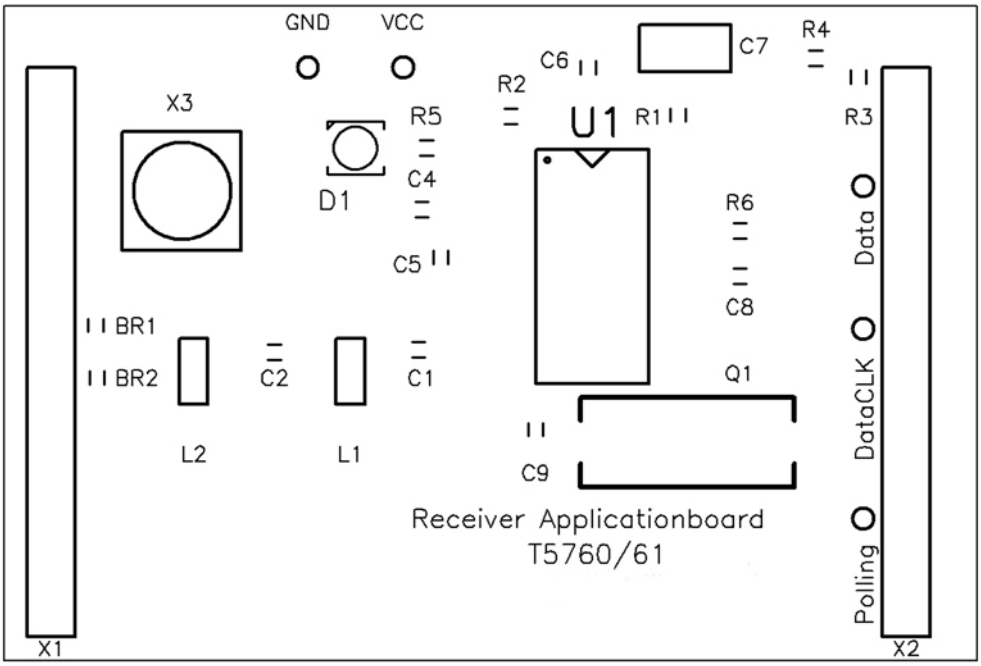


Figure 18. Layout of Top Layer (No SAW)

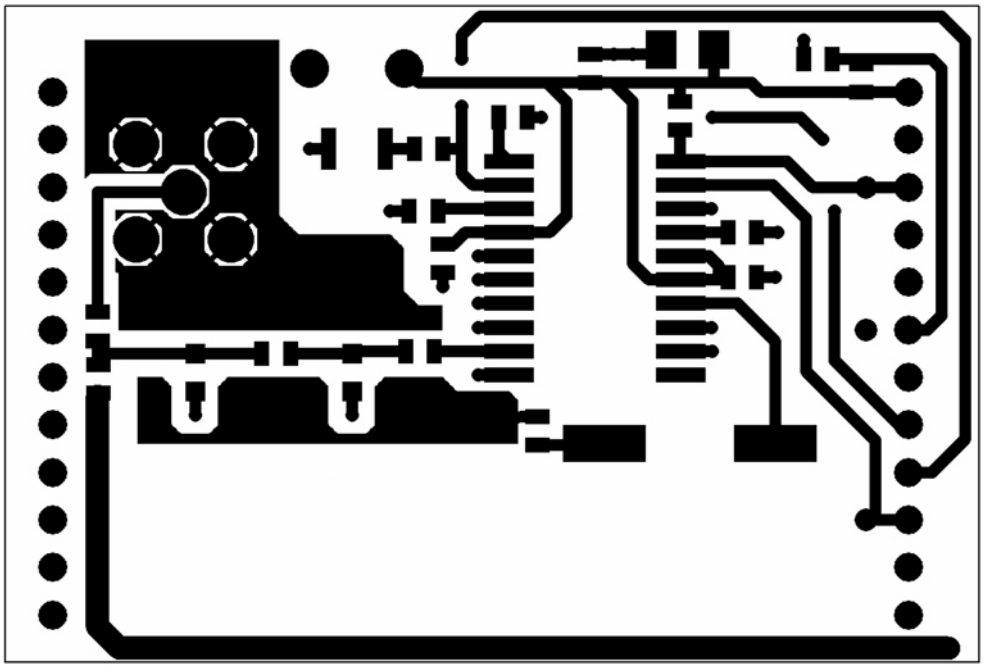


Figure 19. Layout of Bottom Layer (No SAW)

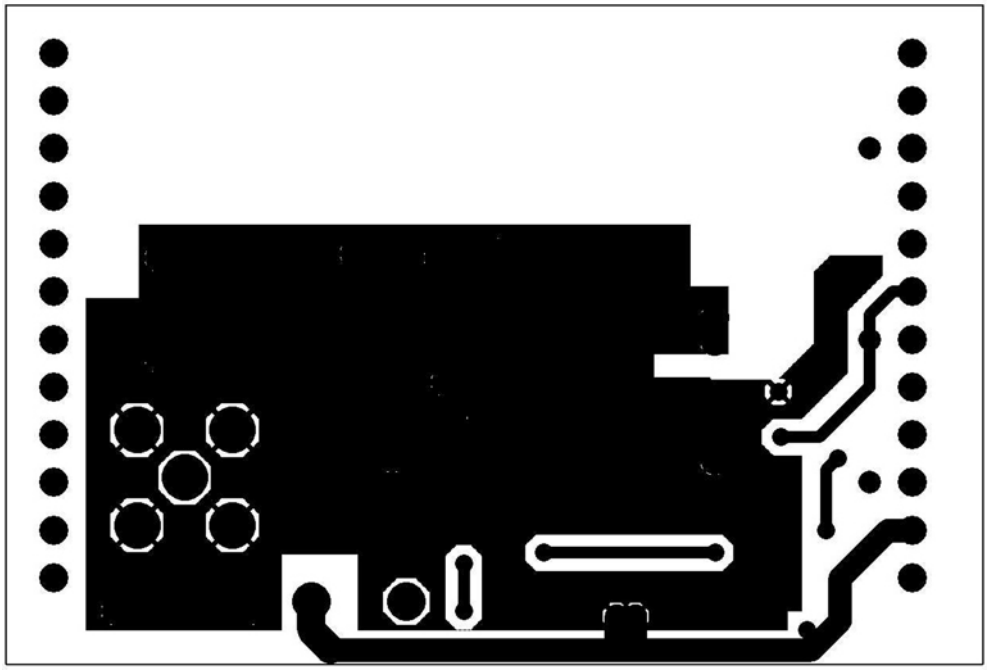


Table 19. Components List Receiver Application Board ATAB5760/ATAB5761 V2.0

Components	PCS	868.3 MHz (No SAW)	868.3 MHz (SAW)	915 MHz (No SAW)	Value	Tol.	Material/ Series	Package	Manufacturer/ Distributor
U1	1	X	X	X	T5760 T5761			SO20	Atmel
Q1	1	X	X	X	6.776172 MHz 7.140625 MHz		Order No.: 4730007678 Order No.: 4730007821	HC-49 / U4B	ACAL
Q2	1		X		SAW Filter B3570		B39871-B3570-U310	QCC8C	EPCOS
C1	1	X	X	X	18 pF/50 V	5%	GRM1885C1H180J	Size 0603	muRata
C2	1	X	X	X	1.5 pF/50 V 5.6 pF/50 V	0.1 pF	GRM1885C1H1R5B GRM1885C1H5R6B	Size 0603	muRata
C3	1		X		3.3 pF/50 V	0.1 pF	GRM1885C1H3R3B	Size 0603	muRata
C4	1	X	X	X	39 nF/25 V	10%	GRM1885C1E393K	Size 0603	muRata
C5, C6, C8	3	X	X	X	10 nF/50 V	10%	GRM1885C1H103K	Size 0603	muRata
C7	1	X	X	X	4.7 µF/10 V	20%	Tantal	Size 1206	e.g., Vishay
C9	1	X	X	X	12 pF/50 V	2%	GRM1885C1H120G	Size 0603	muRata
R1	1	X	X	X	27 kΩ/0.1 W	5%		Size 0603	e.g., Vishay
R2	1	X	X	X	56 kΩ/0.1 W	5%		Size 0603	e.g., Vishay
R3	1	X	X		10 kΩ/0.1 W	5%		Size 0603	e.g., Vishay
R4	1			X	10 kΩ/0.1 W	5%		Size 0603	e.g. Vishay
R5	1	X	X	X	1 kΩ/0.1 W	5%		Size 0603	e.g., Vishay
R6	1	X	X	X	2.2 kΩ/0.1 W	5%		Size 0603	e.g., Vishay
BR1	1	X	X	X	0 Ω/100 V			Size 0603	e.g., Vishay
BR2					n. m.				
L1	1	X	X	X	4.7 nH 3.9 nH	0.3 nH	LL1608-FS4N7S LL1608-FS3N9S	Size 0603	TOKO
L2	1		X		12nH	5%	LL1608-FS12NJ	Size 0603	TOKO
D1	1	X	X	X	SMD LED red		TLMD3100	P-LCC-2	Vishay
X1, X2	2	X	X	X	Row connector		Order No.: 800-10-012-10-001	12 pins / 0.1 " pitch	CAB
X3	1	X	X	X	SMB connector		R114 426 000		Radiall
VCC	1	X	X	X	Pin connector		Order No.: 240-345	Single pin	Farnell
GND, Data, DataCLK, Polling	4	X	X	X	Pin connector		Order No.: 240-333	Single pin	Farnell
PCB	1	X	X	X	T5760/61 V2.0 (No SAW) T5760 V2.0 (SAW)	FR4	Thickness 1.5 mm		

Photographs

Figure 20. Component Side of Receiver Application Board (SAW)

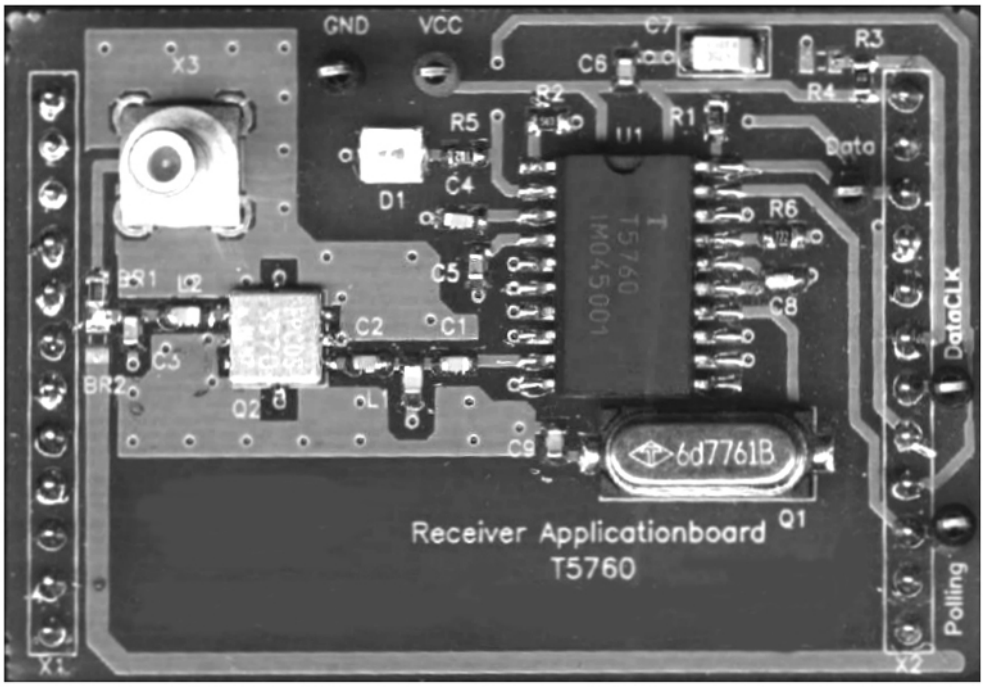


Figure 21. Solder Side of Receiver Application Board (SAW)

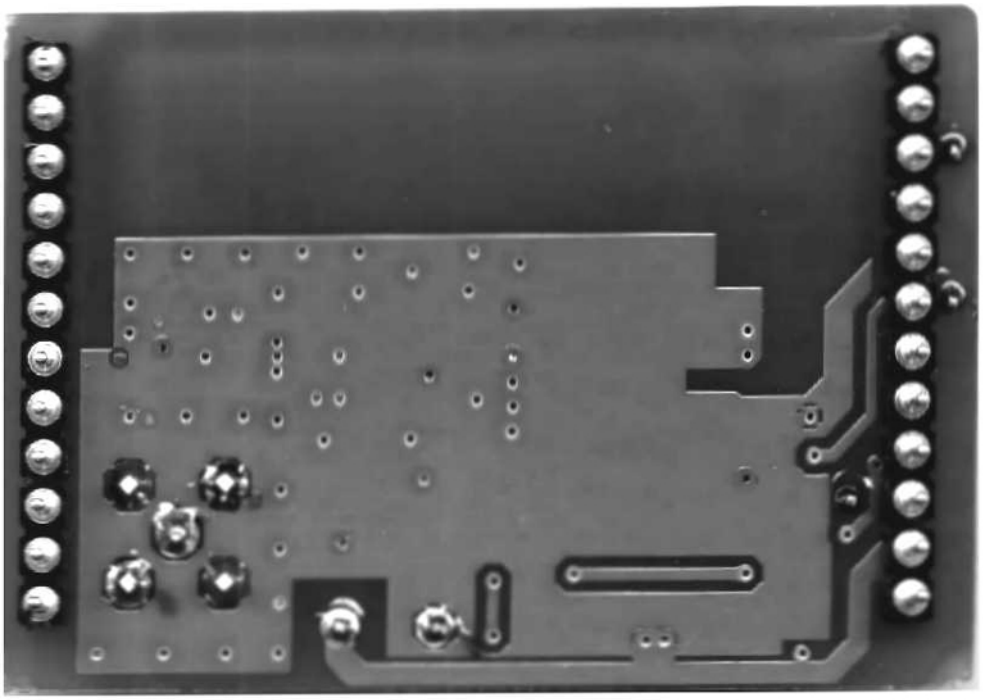


Figure 22. Component side of Receiver Application Board (No SAW)

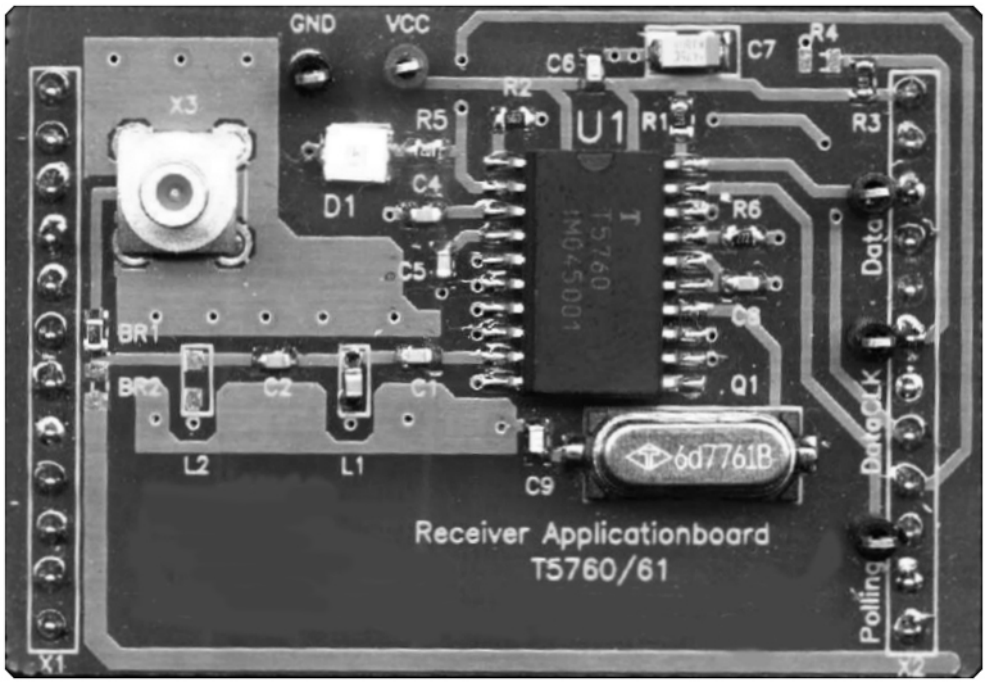
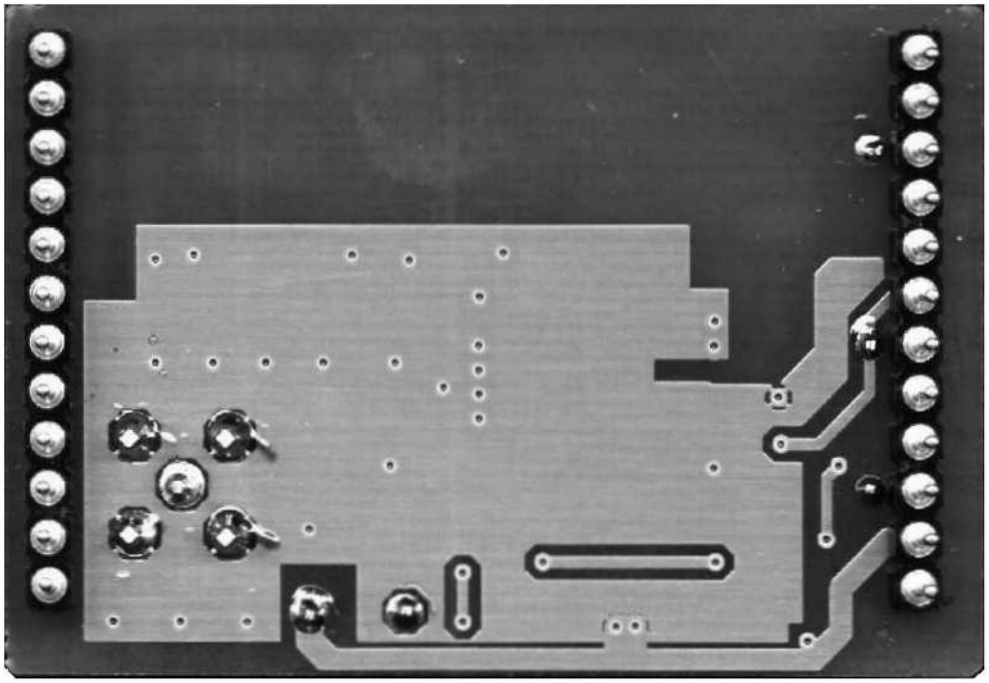


Figure 23. Solder Side of Receiver Application Board (No SAW)



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