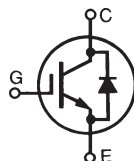


High Voltage, High Frequency, BiMOSFET™ Monolithic Bipolar MOS Transistor

IXBF10N300C



$$V_{CES} = 3000V$$

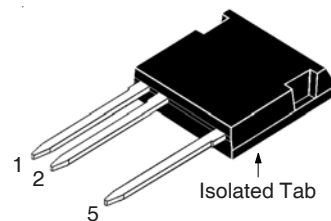
$$I_{C110} = 10A$$

$$V_{CE(sat)} \leq 6.0V$$

(Electrically Isolated Tab)

mbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ C$ to $150^\circ C$	3000	V
V_{CGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GE} = 1M\Omega$	3000	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ C$	29	A
I_{C110}	$T_C = 110^\circ C$	10	A
I_{CM}	$T_C = 25^\circ C$, 1ms	240	A
SSOA (RBSOA)	$V_{GE} = 15V$, $T_{VJ} = 125^\circ C$, $R_G = 10\Omega$ Clamped Inductive Load	$I_{CM} = 80$	A
		$V_{CES} \leq 1500$	V
T_{SC} (SCSOA)	$V_{GE} = 15V$, $T_J = 125^\circ C$, $R_G = 52\Omega$, $V_{CE} = 1500V$, Non-Repetitive	10	μs
P_C	$T_C = 25^\circ C$	240	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	Plastic Body for 10s	260	$^\circ C$
F_C	Mounting Force	20..120 / 4.5..27	N/lb.
V_{ISOL}	50/60Hz, 5 Seconds	4000	V~
Weight		5	g

ISOPLUS i4-Pak™



1 = Gate
2 = Emitter
5 = Collector

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- High Blocking Voltage
- High Frequency Operation

Advantages

- Low Gate Drive Requirement
- High Power Density

Applications

- Switch-Mode and Resonant-Mode Power Supplies

Symbol	Test Conditions ($T_J = 25^\circ C$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$	3000		V
$V_{GE(th)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = V_{CES}$, $V_{GE} = 0V$ Note 2, $T_J = 125^\circ C$			25 μA 3 mA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 200 nA
$V_{CE(sat)}$	$I_C = 10A$, $V_{GE} = 15V$, Note 1 $T_J = 125^\circ C$		4.6 4.8	6.0 V V

Symbol Test Conditions

($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Characteristic Values

Min. Typ. Max.

g_{fs}	$I_C = 10\text{A}, V_{CE} = 10\text{V}$, Note 1	13	22	S
C_{ies}	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$		4580	pF
C_{oes}			204	pF
C_{res}			75	pF
$Q_{g(on)}$	$I_C = 10\text{A}, V_{GE} = 15\text{V}, V_{CE} = 1000\text{V}$		208	nC
Q_{ge}			23	nC
Q_{gc}			80	nC
$t_{d(on)}$	Inductive load, $T_J = 25^\circ\text{C}$ $I_C = 10\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 1500\text{V}, R_G = 10\Omega$ Note 2		32	ns
t_{ri}			10	ns
E_{on}			7.20	mJ
$t_{d(off)}$			390	ns
t_{fi}			84	ns
E_{off}			1.04	mJ
$t_{d(on)}$	Inductive load, $T_J = 125^\circ\text{C}$ $I_C = 10\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 1500\text{V}, R_G = 10\Omega$ Note 2		28	ns
t_{ri}			16	ns
E_{on}			6.15	mJ
$t_{d(off)}$			450	ns
t_{fi}			165	ns
E_{off}			1.40	mJ
R_{thJC}				0.52 $^\circ\text{C/W}$
R_{thCS}		0.15		$^\circ\text{C/W}$

Reverse Diode

Symbol Test Conditions

($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

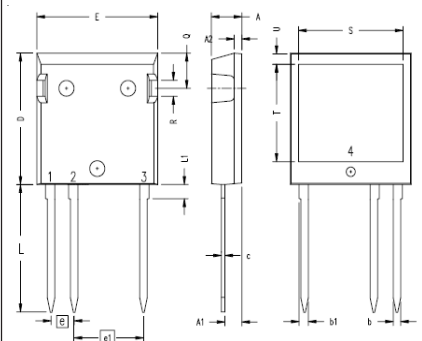
Characteristic Values

Min. Typ. Max.

V_F	$I_F = 10\text{A}, V_{GE} = 0\text{V}$, Note 1		5.0	V
t_{rr}	$I_F = 10\text{A}, V_{GE} = 0\text{V}, -di_F/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GE} = 0\text{V}$		700	ns
I_{RM}			21	A
Q_{RM}			7.4	μC

- Notes: 1. Pulse test, $t < 300\mu\text{s}$, duty cycle, $d < 2\%$.
2. Device must be heatsunk for high-temperature leakage current measurements to avoid thermal runaway.

ISOPLUS i4-Pak™ (HV) Outline



Pin 1 = Gate
Pin 2 = Emitter
Pin 3 = Collector
Tab 4 = Isolated

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.085	1.17	2.16
b	.045	.055	1.14	1.40
b1	.058	.068	1.47	1.73
C	.020	.029	0.51	0.74
D	.819	.840	20.80	21.34
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.840	19.81	21.34
L1	.083	.102	2.11	2.59
Q	.210	.244	5.33	6.20
R	.100	.180	2.54	4.57
S	.660	.690	16.76	17.53
T	.590	.620	14.99	15.75
U	.065	.080	1.65	2.03

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

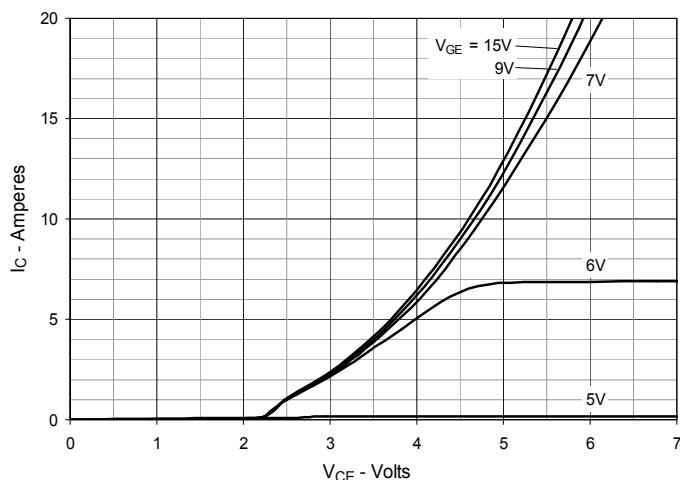
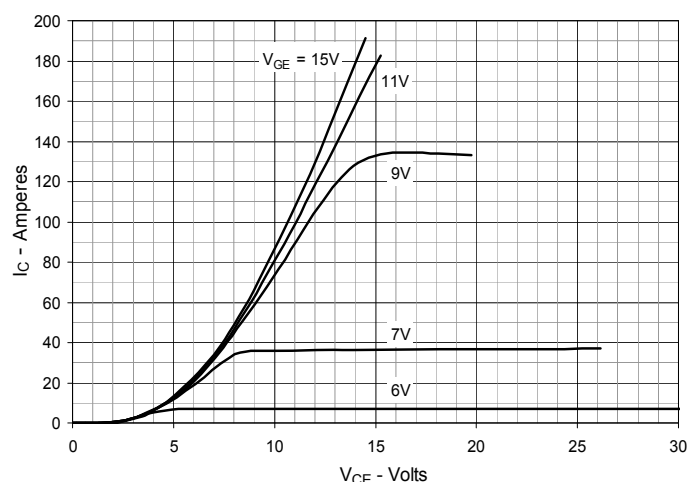
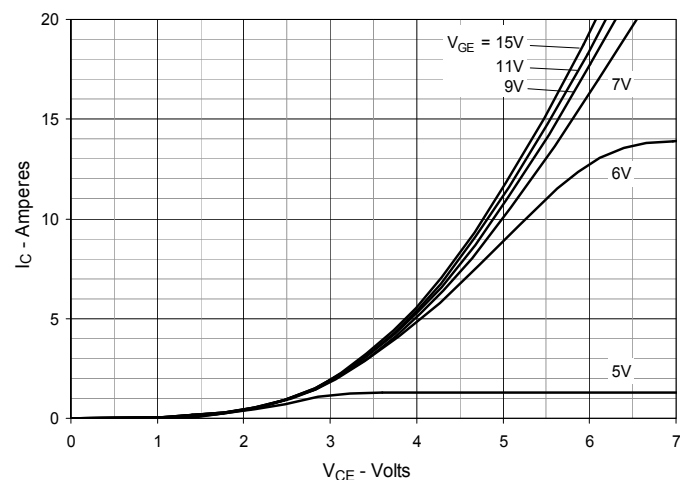
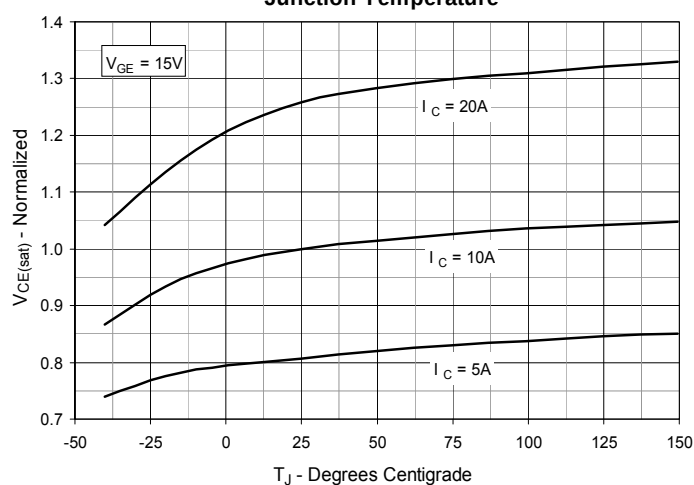
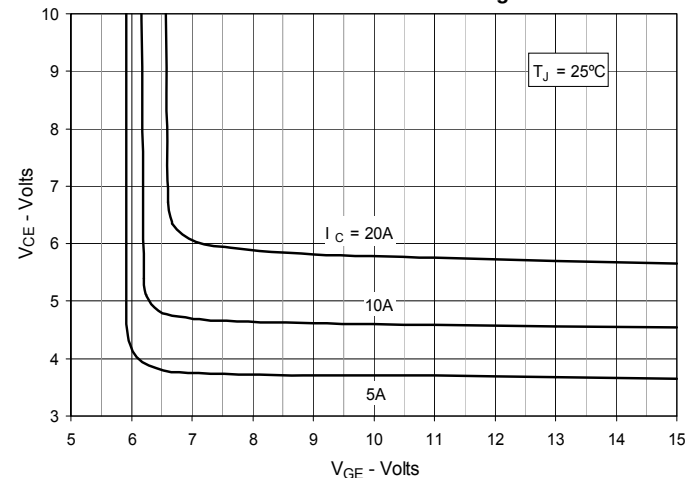
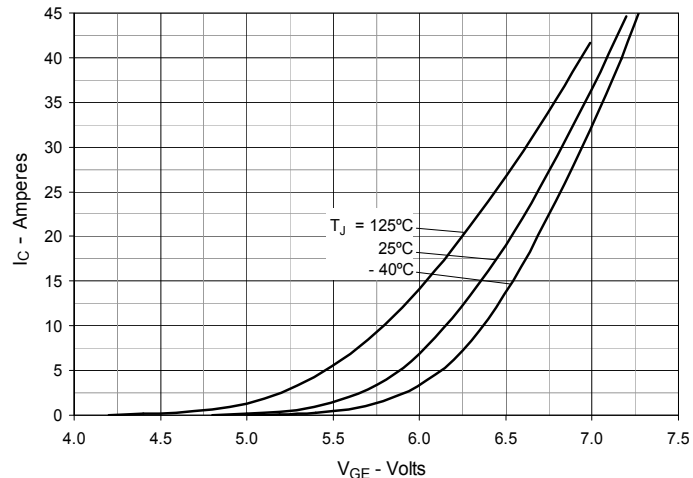
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

Fig. 6. Input Admittance


Fig. 7. Transconductance

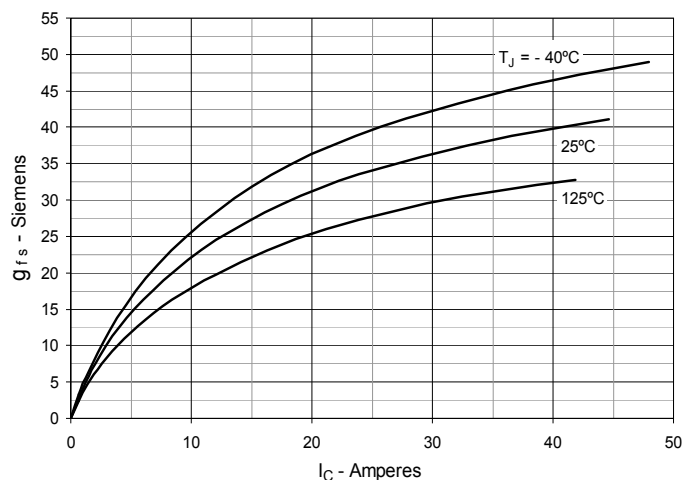


Fig. 8. Gate Charge

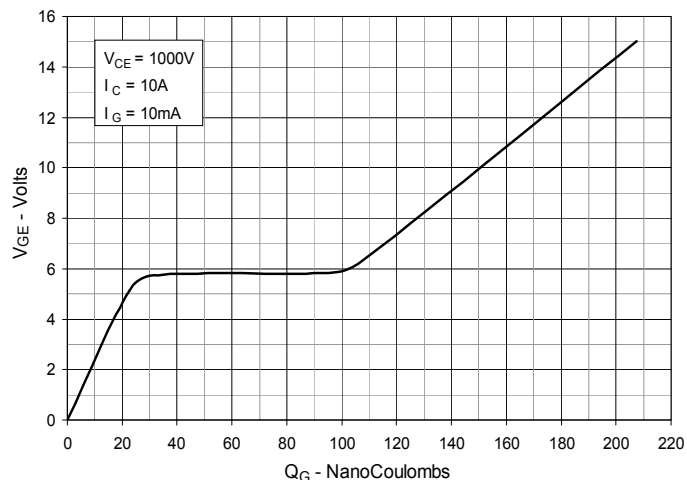


Fig. 9. Forward Voltage Drop of Intrinsic Diode

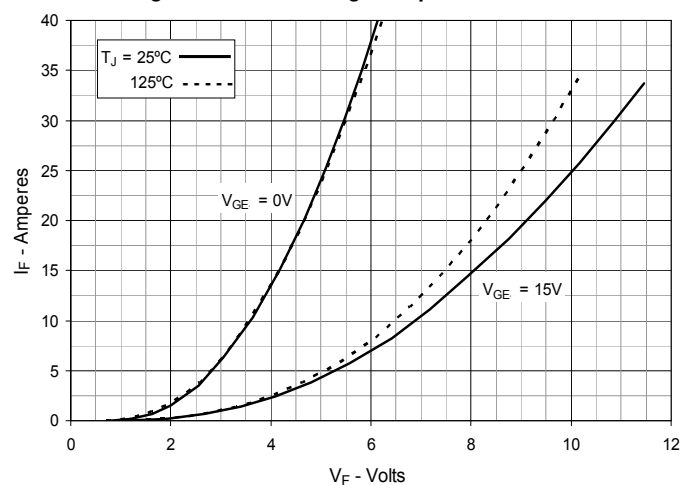


Fig. 10. Capacitance

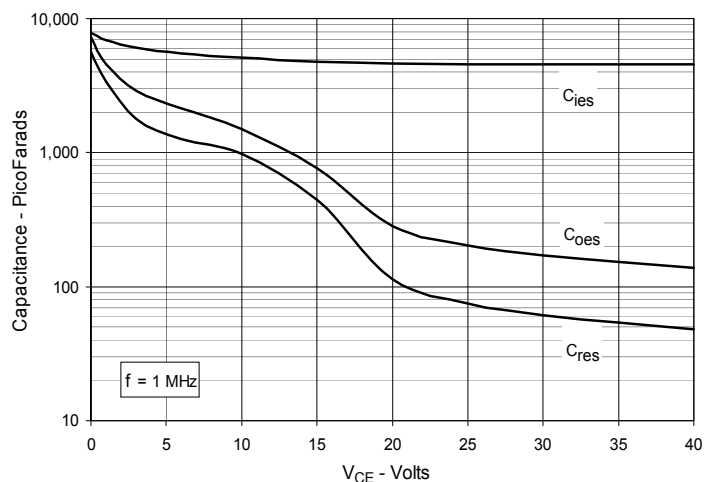


Fig. 11. Reverse-Bias Safe Operating Area

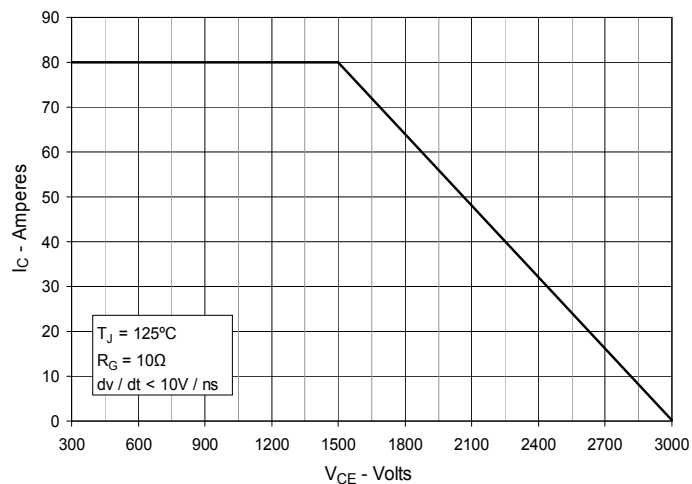


Fig. 12. Maximum Transient Thermal Impedance

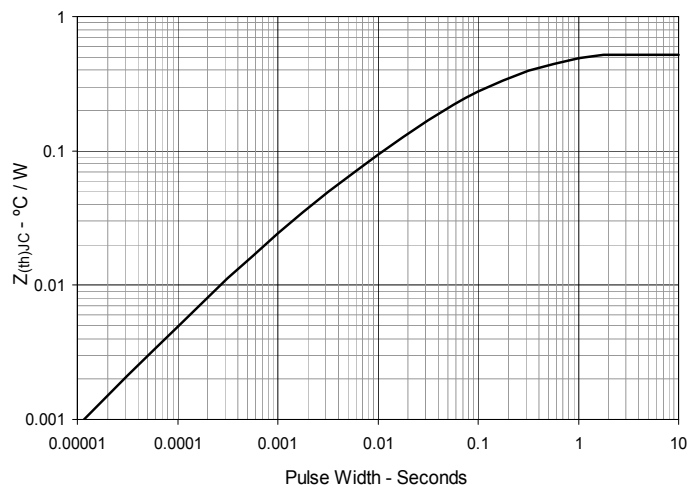


Fig. 13. Forward-Bias Safe Operating Area @ $T_C = 25^\circ\text{C}$

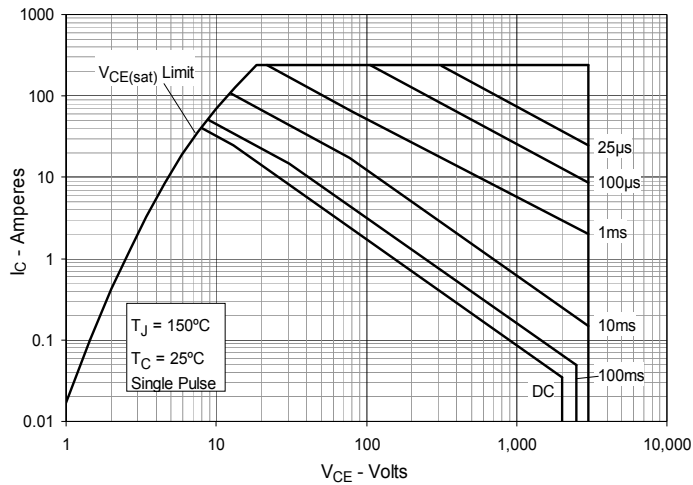


Fig. 14. Forward-Bias Safe Operating Area @ $T_C = 75^\circ\text{C}$

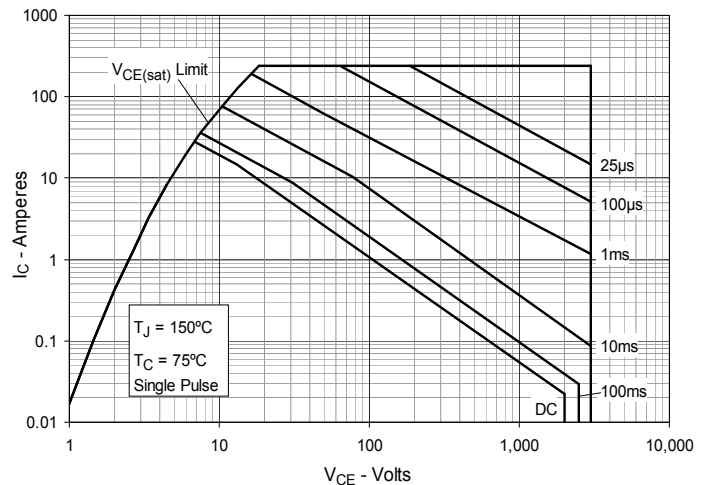


Fig. 15. Inductive Switching Energy Loss vs. Gate Resistance

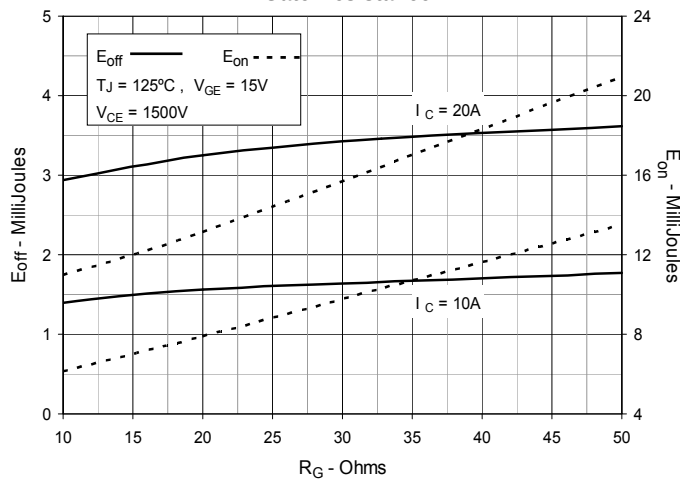


Fig. 16. Inductive Switching Energy Loss vs. Collector Current

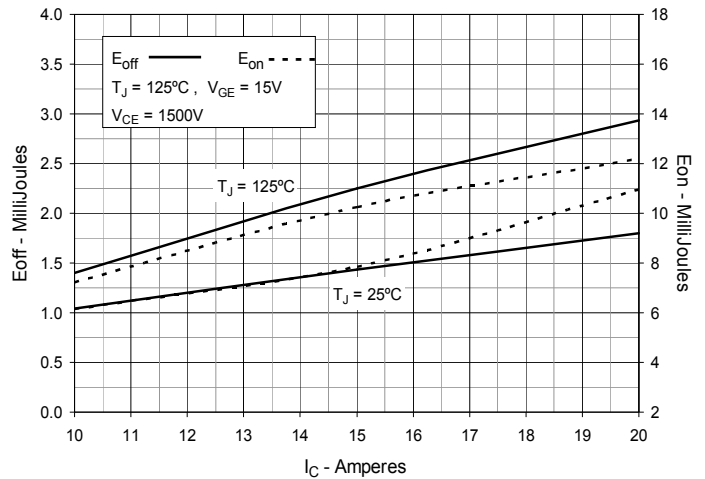


Fig. 17. Inductive Switching Energy Loss vs. Junction Temperature

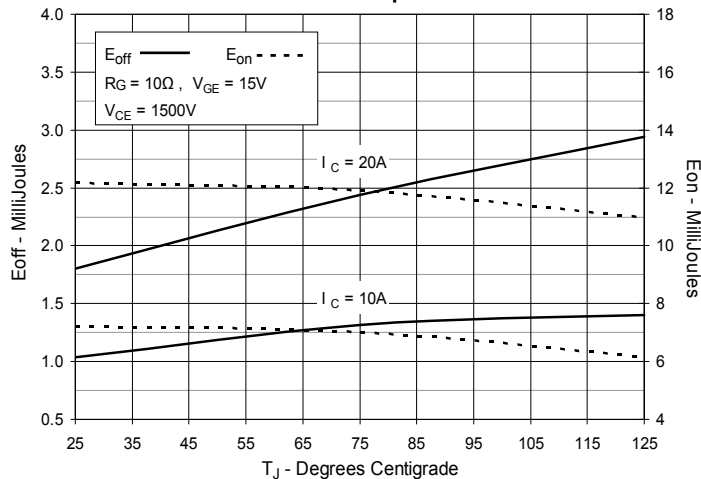


Fig. 18. Inductive Turn-off Switching Times vs. Gate Resistance

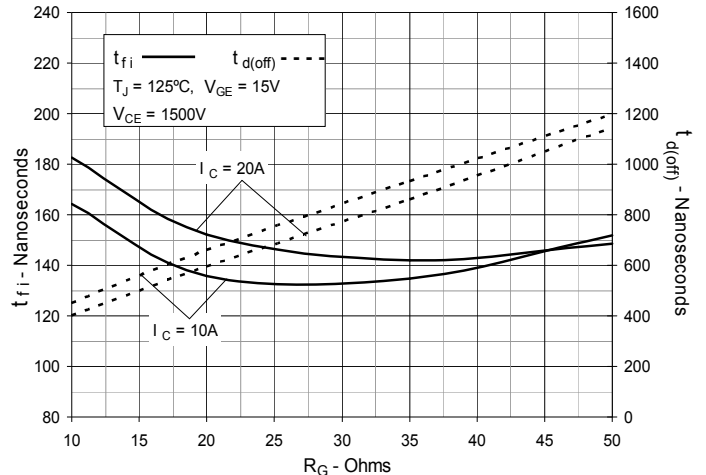


Fig. 19. Inductive Turn-off Switching Times vs. Collector Current

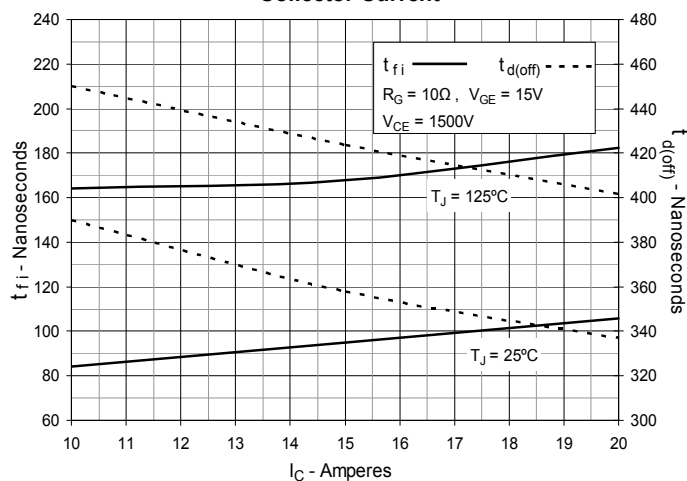


Fig. 20. Inductive Turn-off Switching Times vs. Junction Temperature

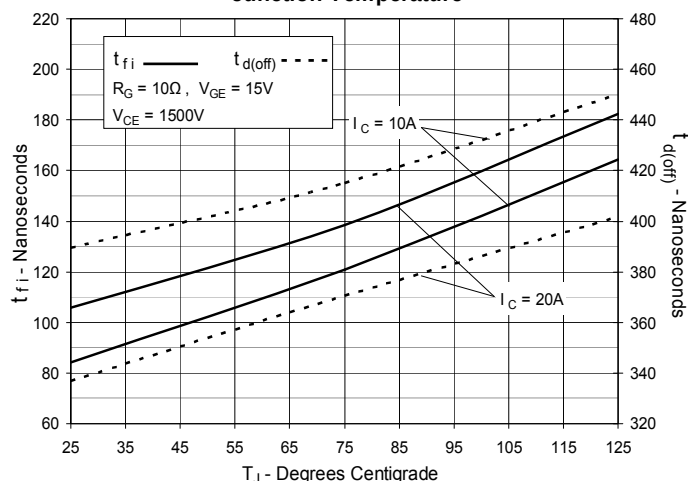


Fig. 21. Inductive Turn-on Switching Times vs. Gate Resistance

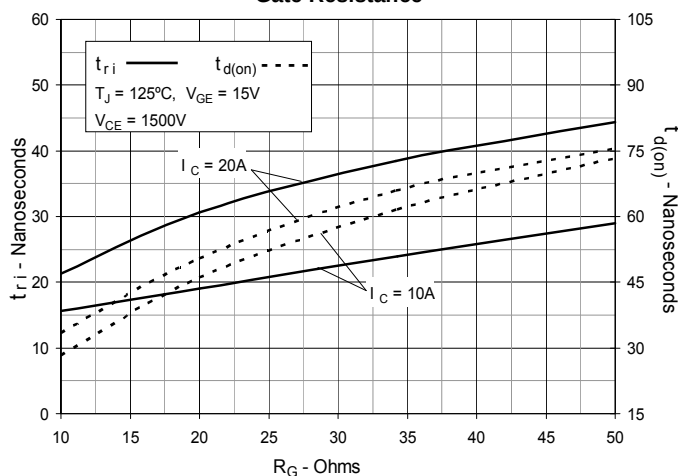


Fig. 22. Inductive Turn-on Switching Times vs. Collector Current

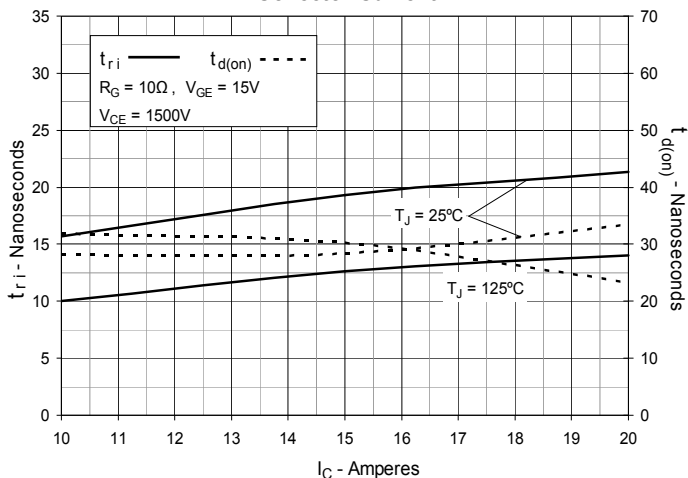


Fig. 23. Inductive Turn-on Switching Times vs. Junction Temperature

