12-BIT 40-KSPS LOW POWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH INTERNAL REFERENCE AND PARALLEL/SERIAL INTERFACE

FEATURES

- **40-kHz Min Sampling Rate**
- **4-V, 5-V, and ±10-V Input Ranges**
- **73.9-dB SINAD with 10-kHz Input**
- **±0.45 LSB Max INL**
- **±0.45 LSB Max DNL, 12-Bit No Missing Codes**
- **±5-mV BPZ, ±0.5 PPM/°C BPZ Drift**
- **SPI Compatible Serial Output With Daisy-Chain (TAG), SPI Master/Slave Feature**
- **Single 5-V Analog Supply**
- **Pin-Compatible With ADS7806 and 16-Bit ADS7807/8507**
- **Uses Internal or External 2.5-V Reference**
- **Low Power Dissipation**
  - **24 mW Typ, 30 mW Max at 40 KSPS**
- **50-μW Max Power Down Mode**
- **28-Pin SO Package**
- **Full Parallel Interface**
- **2's Comp or BTC Output Code**

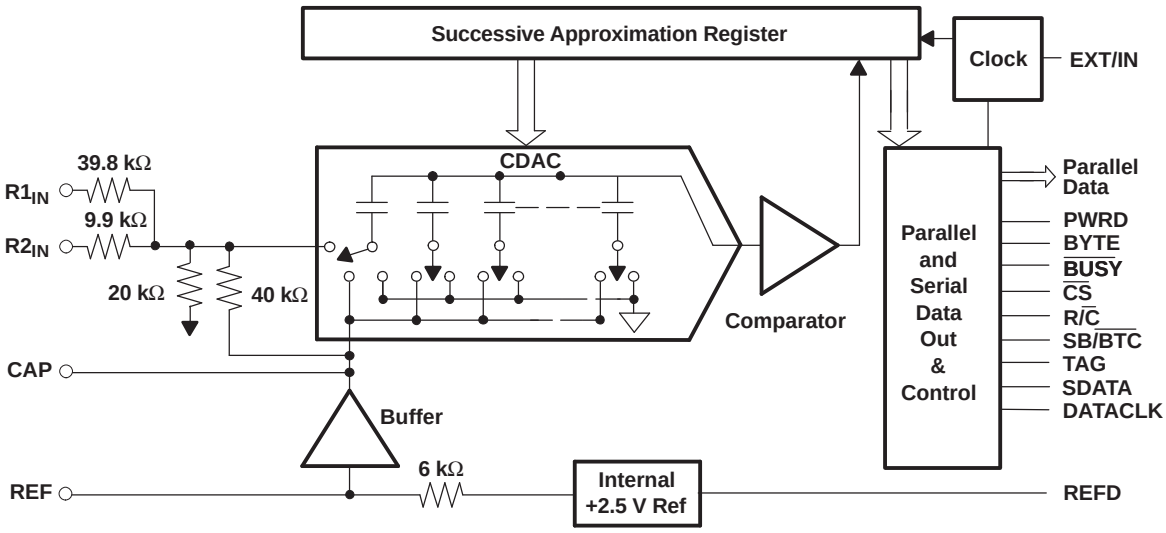
APPLICATIONS

- **Industrial Process Control**
- **Test Equipment**
- **Medical Equipment**
- **Data Acquisition Systems**
- **Digital Signal Processing**
- **Instrumentation**

DESCRIPTION

The ADS8506 is a complete low power, single 5-V supply, 12-bit sampling analog-to-digital (A/D) converter. It contains a complete 12-bit capacitor-based, successive approximation register (SAR) A/D converter with sample and hold, clock, reference, and data interface. The converter can be configured for a variety of input ranges including ±10 V, 4 V, and 5 V. For most input ranges, the input voltage can swing to 25 V or –25 V without damage to the converter.

A SPI compatible serial interface allows data to be synchronized to an internal or external clock. A full parallel interface with BYTE select is also provided to allow the maximum system design flexibility. The ADS8506 is specified at 40 kHz sampling rate over the industrial -40°C to 85°C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MINIMUM INL (LSB)	NO MISSING CODE	FULL-SCALE ERROR (%)	SPECIFICATION TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QTY
ADS8506IB	±0.45	12	±0.25	-40°C to 85°C	SO-28	DW	ADS8506IBDW	Tube, 20
							ADS8506IBDWR	Tape and Reel, 1000
ADS8506I	±0.9	12	±0.5	-40°C to 85°C	SO-28	DW	ADS8506IDW	Tube, 20
							ADS8506IDWR	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Analog inputs	$R1_{IN}$	±25 V
	$R2_{IN}$	±25 V
	REF	$+V_{ANA}$ + 0.3 V to AGND2 - 0.3 V
Ground voltage differences	DGND, AGND2	±0.3 V
	V_{ANA}	6 V
	V_{DIG} to V_{ANA}	0.3 V
	V_{DIG}	6 V
Digital inputs		-0.3 V to $+V_{DIG}$ + 0.3 V
Maximum junction temperature		165°C
Storage temperature range		–65°C to 150°C
Internal power dissipation		700 mW
Lead temperature (soldering, 1.6 mm from case 10 seconds)		260°C

(1) All voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

At T_A = -40°C to 85°C, f_S = 40 kHz, V_{DIG} = V_{ANA} = 5 V, and using internal reference and fixed resistors, (see Figure 43) unless otherwise specified.

PARAMETER		TEST CONDITIONS	ADS8506IB			ADS8506I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution					12			12	Bits
ANALOG INPUT									
Voltage ranges		See Table 1	-10		10	-10		10	V
			0		5	0		5	
			0		4	0		4	
Impedance									
Capacitance				45			45		pF
THROUGHPUT SPEED									
Conversion time		Acquire and convert			15			15	µs
Complete cycle					25			25	
Throughput rate			40						kHz
DC ACCURACY									
INL	Integral linearity error		-0.45	±0.15	0.45	-0.9	±0.15	0.9	LSB(1)

(1) LSB means Least Significant Bit. One LSB for the ±10-V input range is 305 µV.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = -40°C to 85°C, f_S = 40 kHz, V_{DIG} = V_{ANA} = 5 V, and using internal reference and fixed resistors, (see Figure 43) unless otherwise specified.

PARAMETER		TEST CONDITIONS	ADS8506IB			ADS8506I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DNL	Differential linearity error		-0.45	±0.15	0.45	-0.9	±0.15	0.9	LSB
	No missing codes		12			12			Bits
	Transition noise(2)			0.1			0.1		LSB
	Gain Error			±0.1			±0.2		%
	Full scale error(3)(4)		-0.25		0.25	-0.5		0.5	%
	Full scale error drift			±5			±7		ppm/°C
	Full scale error(3)(4)	Ext. 2.5-V Ref	-0.25		0.25	-0.5		0.5	%
	Full scale error drift	Ext. 2.5-V Ref		±0.5			±0.5		ppm/°C
	Bipolar zero error(3)	±10 V Range	-10		10	-10		10	mV
	Bipolar zero error drift	±10 V Range		±0.5			±0.5		ppm/°C
	Unipolar zero error(3)	0 V to 5 V, 0 V to 4 V Ranges	-3		3	-3		3	mV
	Unipolar zero error drift	0 V to 5 V, 0 V to 4 V Ranges		±0.5			±0.5		ppm/°C
	Recovery time to rated accuracy from power down(5)	2.2-µF Capacitor to CAP		1			1		ms
	Power supply sensitivity (V_{DIG} = V_{ANA} = V_S)	+4.75 V < V_S < +5.25 V			±0.5			±0.5	LSB
AC ACCURACY									
SFDR	Spurious-free dynamic range	f_{IN} = 10 kHz, ±10 V	80	98		80	98		dB(6)
THD	Total harmonic distortion	f_{IN} = 10 kHz, ±10 V		-96	-80		-96	-80	dB
SINAD	Signal-to-(noise+distortion)	f_{IN} = 10 kHz, ±10 V	72	73.9		70	73.9		dB
		-60 dB Input		32			32		
SNR	Signal-to-noise	f_{IN} = 10 kHz, ±10 V	72	74		70	74		dB
	Usable bandwidth(7)			130			130		kHz
	Full-power bandwidth (-3 dB)			600			600		kHz
SAMPLING DYNAMICS									
	Aperture delay			40			40		ns
	Aperture jitter			20			20		ps
	Transient response	FS Step			5			5	µs
	Overvoltage recovery(8)			750			750		ns
REFERENCE									
	Internal reference voltage	No load	2.48	2.5	2.52	2.48	2.5	2.52	V
	Internal reference source current (must use external buffer)			1			1		µA
	Internal reference drift			8			8		ppm/°C
	External reference voltage range for specified linearity		2.3	2.5	2.7	2.3	2.5	2.7	V
	External reference current drain	Ext. 2.5-V Ref			100			100	µA
DIGITAL INPUTS									
V_{IL}	Low-level input voltage		-0.3		+0.8	-0.3		+0.8	V
V_{IH}	High-level input voltage		2.0		V_D +0.3 V	2.0		V_D +0.3 V	V
I_{IL}	Low-level input current	V_{IL} = 0 V			±10			±10	µA
I_{IH}	High-level input current	V_{IH} = 5 V			±10			±10	µA
DIGITAL OUTPUTS									

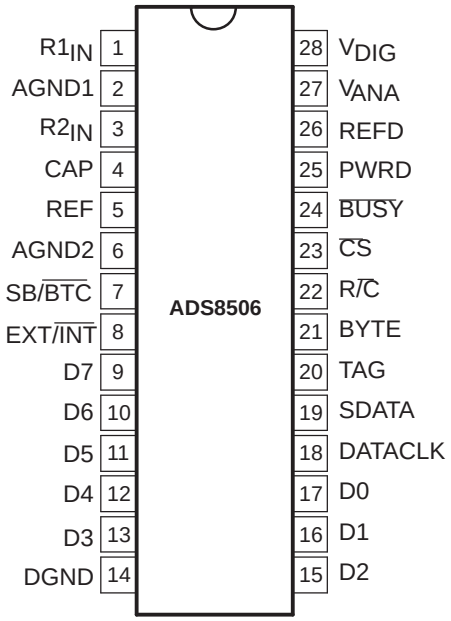
(2) Typical rms noise at worst case transitions.
(3) As measured with fixed resistors, see Figure 43. Adjustable to zero with external potentiometer.
(4) Full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error.
(5) This is the time delay after the ADS8506 is brought out of Power-Down mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert command after this delay will yield accurate results.
(6) All specifications in dB are referred to a full-scale input.
(7) Usable bandwidth defined as full-scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60 dB.
(8) Recovers to specified performance after 2 x FS input overvoltage.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = -40°C to 85°C, f_S = 40 kHz, V_{DIG} = V_{ANA} = 5 V, and using internal reference and fixed resistors, (see Figure 43) unless otherwise specified.

PARAMETER		TEST CONDITIONS	ADS8506IB			ADS8506I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Data format - Parallel 12-bits in 2-bytes								
	Data coding - Serial binary 2s complement or straight binary								
V_{OL}	Low-level output voltage	I_{SINK} = 1.6 mA			0.4			0.4	V
V_{OH}	High-level output voltage	I_{SOURCE} = 500 µA	4			4			V
	Leakage Current	High-Z state, V_{OUT} = 0 V to V_{DIG}			±5			±5	µA
	Output capacitance	High-Z state			15			15	pF
DIGITAL TIMING									
	Bus access time	R_L = 3.3 kΩ, C_L = 50 pF			83			83	ns
	Bus relinquish time	R_L = 3.3 kΩ, C_L = 10 pF			83			83	ns
POWER SUPPLIES									
V_{DIG}	Digital I/O voltage	Must be ≤ V_{ANA}	4.75	5	5.25	4.75	5	5.25	V
V_{ANA}	ADC core voltage		4.75	5	5.25	4.75	5	5.25	V
I_{DIG}	Digital current			0.6			0.6		mA
I_{ANA}	Analog current			4.2			4.2		mA
	Power dissipation	V_{ANA} = V_{DIG} = 5 V, f_S = 40 kHz		24	30		24	30	mW
		REFD High		20			20		mW
		PWRD and REFD High		50			50		µW
TEMPERATURE RANGE									
	Specified performance		-40		85	-40		85	°C
	Derated performance		-55		125	-55		125	°C
	Storage temperature		-65		150	-65		150	°C
SO	Thermal resistance (Θ_{JA})			46			46		°C/W

DEVICE INFORMATION



Terminal Functions

TERMINAL		DIGITAL I/O	DESCRIPTION
NO.	NAME		
1	$R1_{IN}$		Analog Input.
2	AGND1		Analog sense ground. Used internally as ground reference point. Minimal current flow
3	$R2_{IN}$		Analog Input.
4	CAP		Reference buffer output. 2.2-µF Tantalum capacitor to ground.
5	REF		Reference input/output. Outputs internal 2.5-V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2-µF tantalum capacitor.
6	AGND2		Analog ground
7	SB/$\overline{BTC}$	I	Selects straight binary or binary 2's complement for output data format. if high, data is output in a straight binary format. If low, data is output in a binary 2's complement format.
8	EXT/$\overline{INT}$	I	Selects external/Internal data clock for transmitting data. If high, data is output synchronized to the clock input on DATACLK. If low, a convert command initiates the transmission of the data from the previous conversion, along with 12-clock pulses output on DATACLK.
9	D7	O	Data bit 3 if BYTE is high. Data bit 11 (MSB) if BYTE is low. Hi-Z when CS is high and/or R/$\overline{C}$ is low. Leave unconnected when using serial output.
10	D6	O	Data bit 2 if BYTE is high. Data bit 10 if BYTE is low. Hi-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
11	D5	O	Data bit 1 if BYTE is high. Data bit 9 if BYTE is low. Hi-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
12	D4	O	Data bit 0 (LSB) if BYTE is high. Data bit 8 if BYTE is low. Hi-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
13	D3	O	Ground if BYTE is high. Data bit 7 if BYTE is low. Hi-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
14	DGND		Digital ground
15	D2	O	Ground if BYTE is high. Data bit 6 if BYTE is low. Hi-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
16	D1	O	Ground if BYTE is high. Data bit 5 if BYTE is low. Hi-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
17	D0	O	Ground if BYTE is high. Data bit 4 if BYTE is low. Hi-Z when $\overline{CS}$ is high and/or R/$\overline{C}$ is low.
18	DATACLK	I/O	Either an input or an output depending on the EXT/$\overline{INT}$ level. Output data is synchronized to this clock. If EXT/$\overline{INT}$ is low, DATACLK transmits 12 pulses after each conversion, and then remains low between conversions.
19	SDATA	O	Serial data output. Data is synchronized to DATACLK, with the format determined by the level of SB/$\overline{BTC}$. In the external clock mode, after 12 bits of data, the ADC outputs the level input on TAG as long as $\overline{CS}$ is low and R/$\overline{C}$ is high. If EXT/$\overline{INT}$ is low, data is valid on both the rising and falling edges of DATACLK, and between conversions SDATA stays at the level of the TAG input when the conversion was started.
20	TAG	I	Tag input for use in the external clock mode. If EXT is high, digital data input from TAG is output on DATA with a delay that is dependent on the external clock mode.
21	BYTE	I	Selects 8 most significant bits (low) or 8 least significant bits (high) on parallel output pins.
22	R/$\overline{C}$	I	Read/convert input. With $\overline{CS}$ low, a falling edge on R/$\overline{C}$ puts the internal sample-and-hold into the hold state and starts a conversion. When EXT/$\overline{INT}$ is low, this also initiates the transmission of the data results from the previous conversion.
23	$\overline{CS}$	I	Internally ORed with R/$\overline{C}$. If R/$\overline{C}$ is low, a falling edge on $\overline{CS}$ initiates a new conversion. If EXT/$\overline{INT}$ is low, this same falling edge will start the transmission of serial data results from the previous conversion.
24	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes low and stays low until the conversion is completed and the digital outputs have been updated.
25	PWRD	I	Power down input. If high, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
26	REFD	I	REFD High shuts down the internal reference. External reference will be required for conversions.
27	V_{ANA}		ADC Core Supply. Nominally +5 V. Decouple with 0.1-µF ceramic and 10-µF tantalum capacitors.
28	V_{DIG}		Digital Interface Supply. Nominally +5 V. Connect directly to pin 27. Must be ≤ V_{ANA}.

Table 1. Input Range Connections (see Figure 42 and Figure 43)

ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200 Ω TO	CONNECT $R2_{IN}$ VIA 100 Ω TO	IMPEDANCE
±10 V	V_{IN}	CAP	45.7 kΩ
0 V to 5 V	AGND	V_{IN}	20.0 kΩ
0 V to 4 V	V_{IN}	V_{IN}	21.4 kΩ

TYPICAL CHARACTERISTICS

POWER SUPPLY CURRENT vs FREE-AIR TEMPERATURE

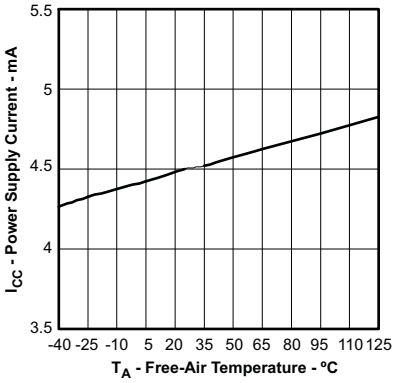


Figure 1.

INTERNAL REFERENCE vs FREE-AIR TEMPERATURE

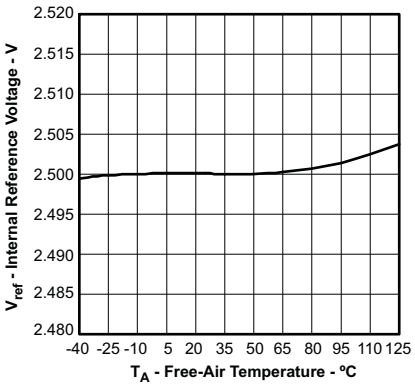


Figure 2.

POWER SUPPLY CURRENT vs SAMPLING FREQUENCY

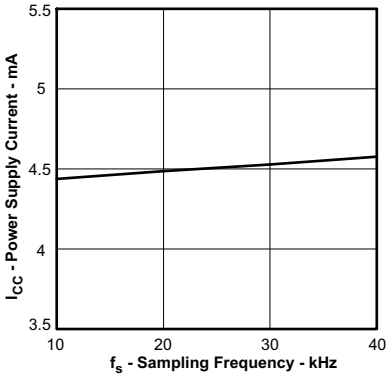


Figure 3.

BIPOLAR OFFSET ERROR vs FREE-AIR TEMPERATURE

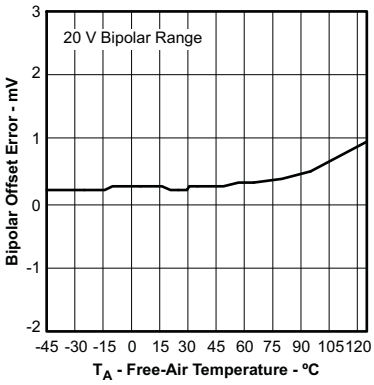


Figure 4.

BIPOLAR POSITIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

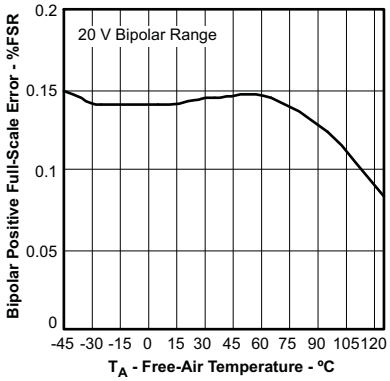


Figure 5.

BIPOLAR NEGATIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

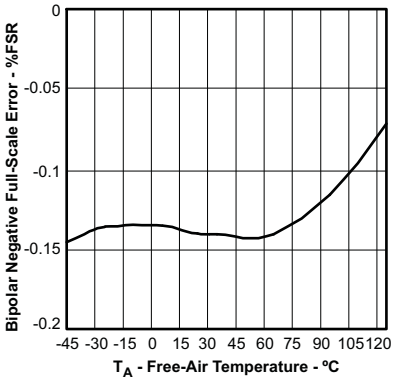


Figure 6.

TYPICAL CHARACTERISTICS (continued)

UNIPOLAR OFFSET ERROR vs FREE-AIR TEMPERATURE

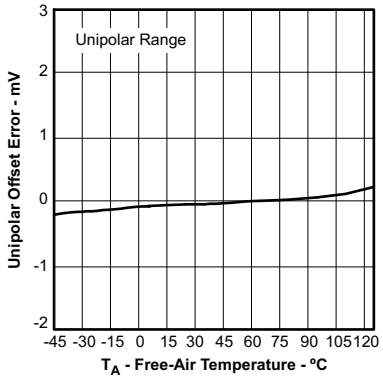


Figure 7.

UNIPOLAR FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

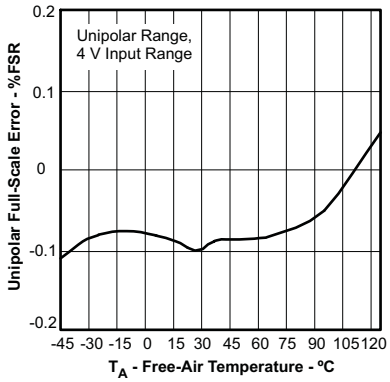


Figure 8.

UNIPOLAR FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

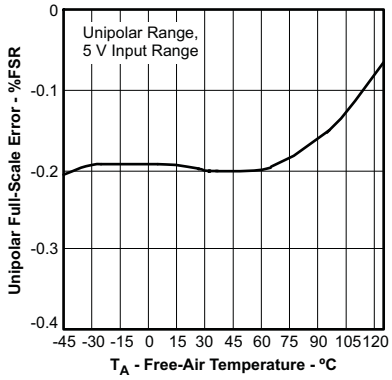


Figure 9.

SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE

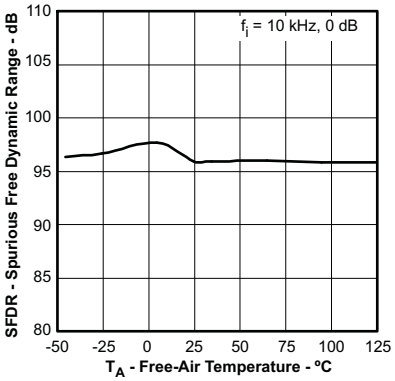


Figure 10.

TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE

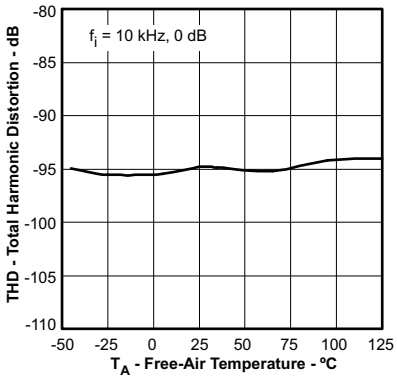


Figure 11.

SIGNAL-TO-NOISE RATIO vs FREE-AIR TEMPERATURE

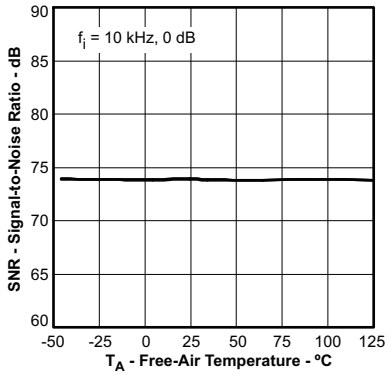


Figure 12.

SIGNAL-TO-NOISE AND DISTORTION vs FREE-AIR TEMPERATURE

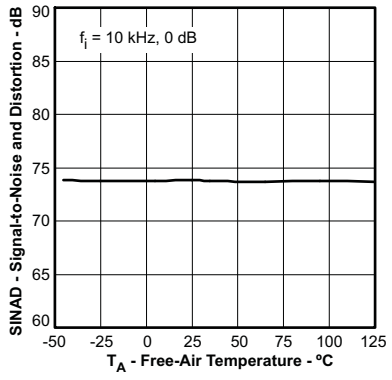


Figure 13.

SIGNAL-TO-NOISE AND DISTORTION vs FREQUENCY

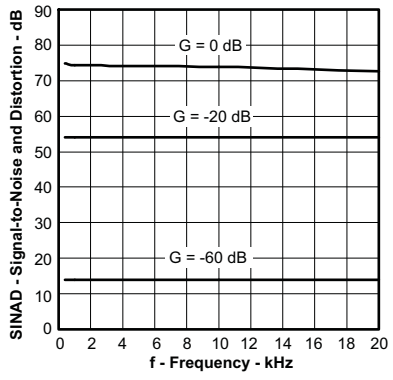


Figure 14.

SIGNAL-TO-NOISE AND DISTORTION vs FREE-AIR TEMPERATURE

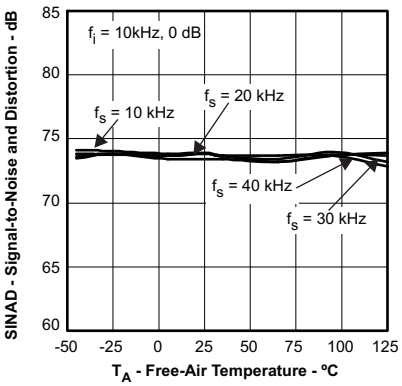


Figure 15.

TYPICAL CHARACTERISTICS (continued)

SIGNAL-TO-NOISE RATIO vs FREQUENCY

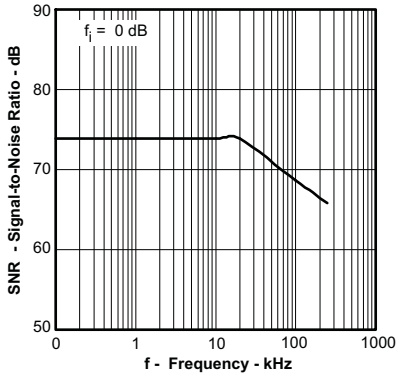


Figure 16.

SIGNAL-TO-NOISE AND DISTORTION vs FREQUENCY

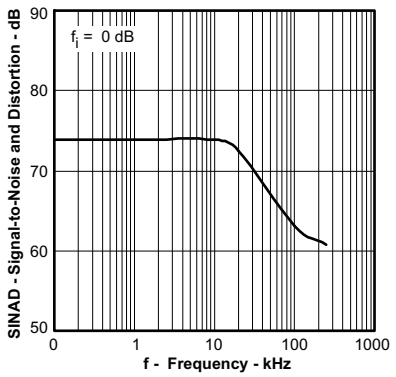


Figure 17.

SPURIOUS FREE DYNAMIC RANGE vs FREQUENCY

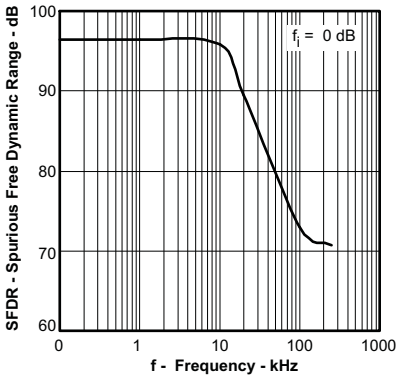


Figure 18.

TOTAL HARMONIC DISTORTION vs FREQUENCY

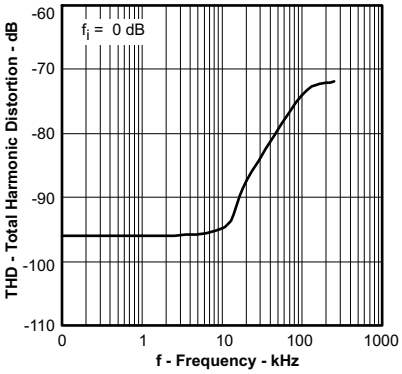


Figure 19.

SPURIOUS FREE DYNAMIC RANGE vs EQUIVALENT SERIES RESISTOR

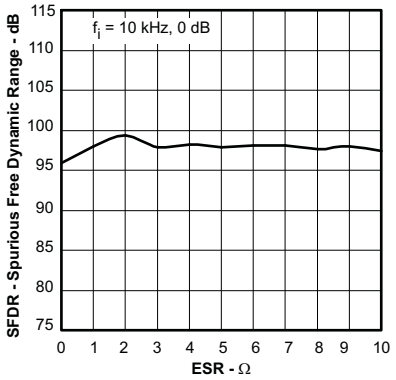


Figure 20.

TOTAL HARMONIC DISTORTION vs EQUIVALENT SERIES RESISTOR

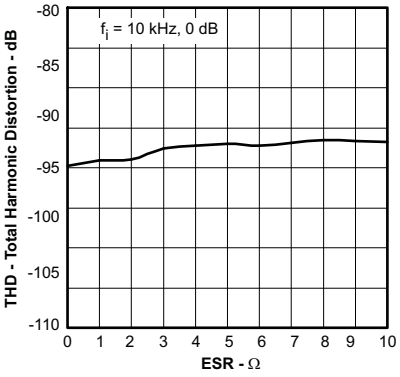


Figure 21.

SIGNAL-TO-NOISE RATIO vs EQUIVALENT SERIES RESISTOR

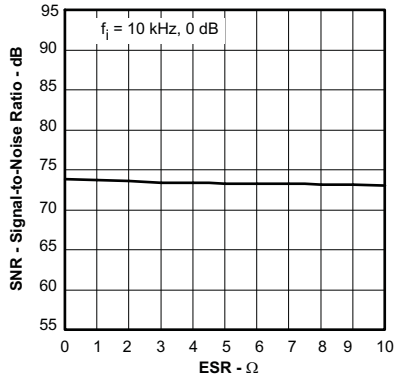


Figure 22.

SIGNAL-TO-NOISE AND DISTORTION vs EQUIVALENT SERIES RESISTOR

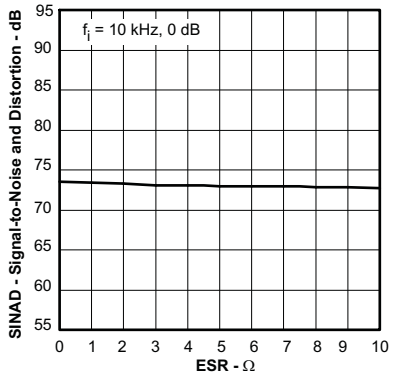


Figure 23.

OUTPUT REJECTION vs POWER-SUPPLY RIPPLE FREQUENCY

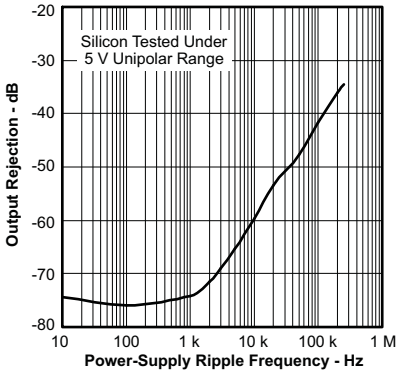


Figure 24.

TYPICAL CHARACTERISTICS (continued)

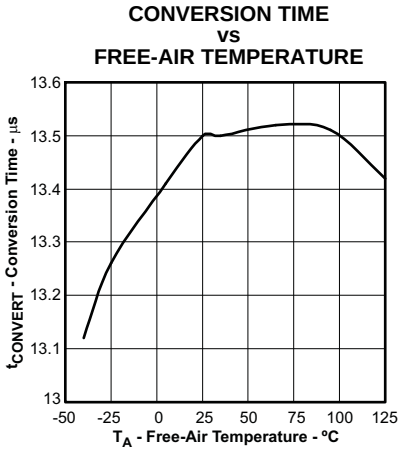


Figure 25.

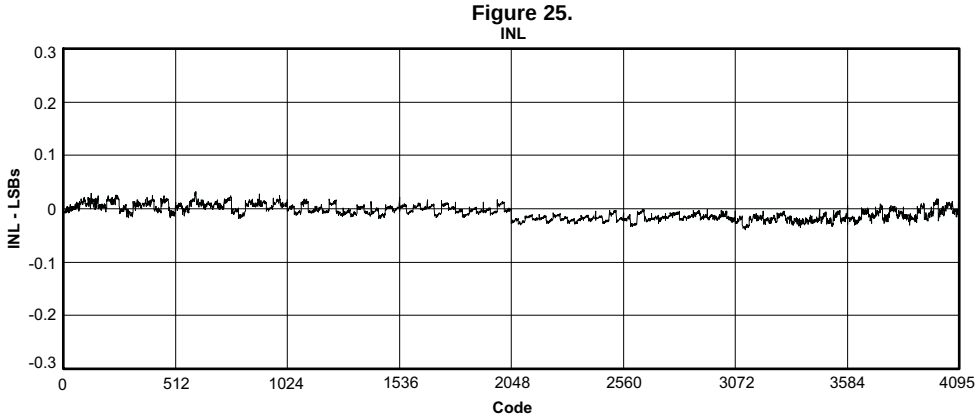


Figure 26.

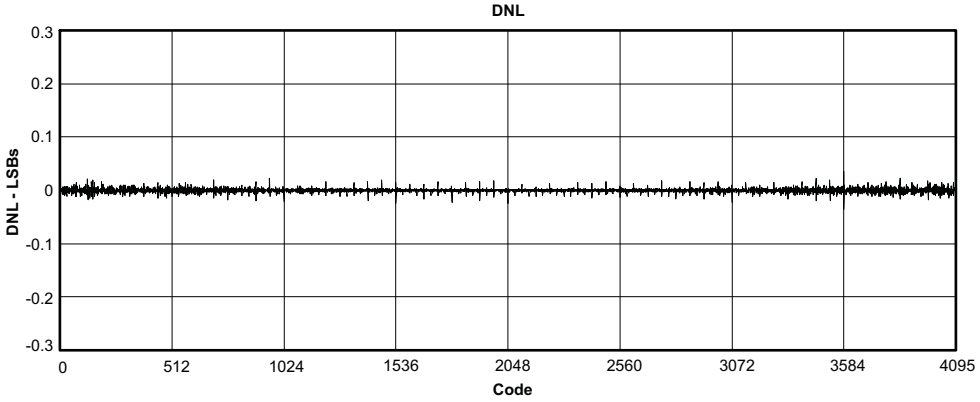


Figure 27.

TYPICAL CHARACTERISTICS (continued)

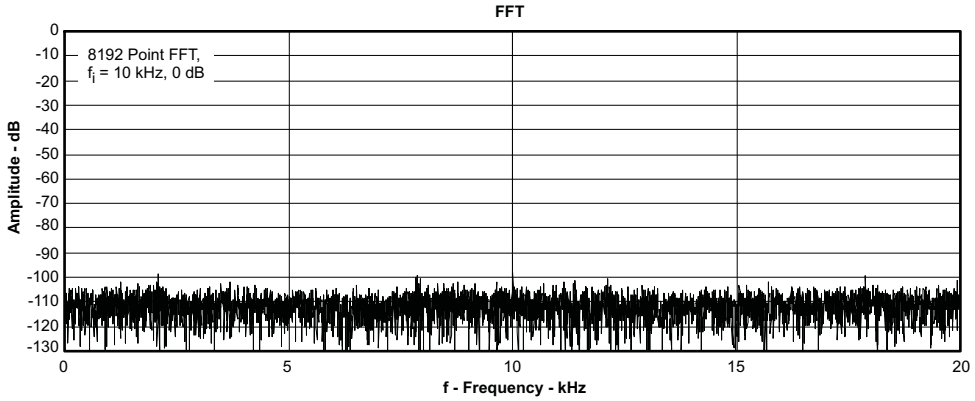


Figure 28.

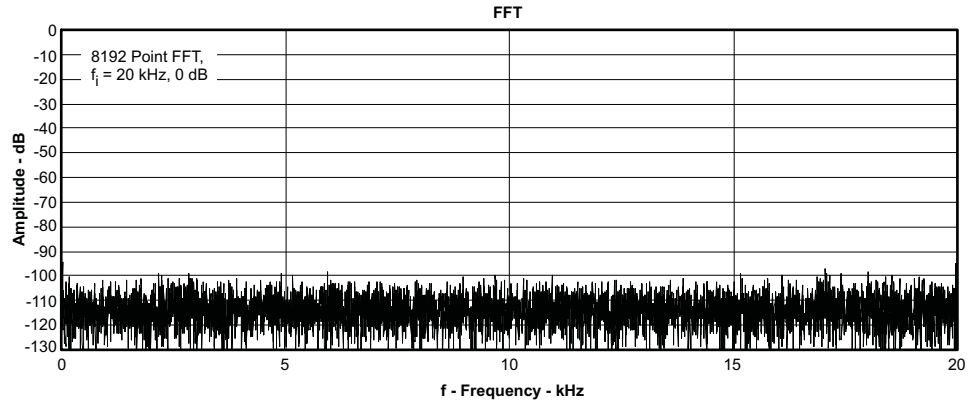


Figure 29.

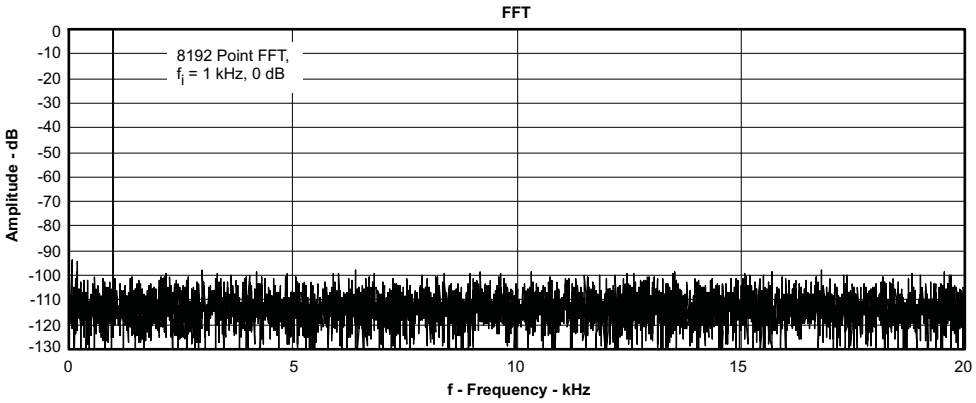


Figure 30.

BASIC OPERATION

PARALLEL OUTPUT

Figure 31 shows a basic circuit to operate the ADS8506 with a ±10-V input range and parallel output. Taking R/$\overline{C}$ (pin 22) LOW for a minimum of 40 ns (12 µs max) will initiate a conversion. $\overline{BUSY}$ (pin 24) will go LOW and stay

LOW until the conversion is completed and the output register is updated. If BYTE (pin 21) is LOW, the eight most significant bits (MSBs) will be valid when $\overline{BUSY}$ rises; if BYTE is HIGH, the four least significant bits (LSBs) will be valid when $\overline{BUSY}$ rises. Data will be output in binary 2's complement (BTC) format. $\overline{BUSY}$ going HIGH can be used to latch the data. After the first byte has been read, BYTE can be toggled allowing the remaining byte to be read. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS8506 begins tracking the input signal at the end of the conversion. Allowing 25 µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the Calibration section).

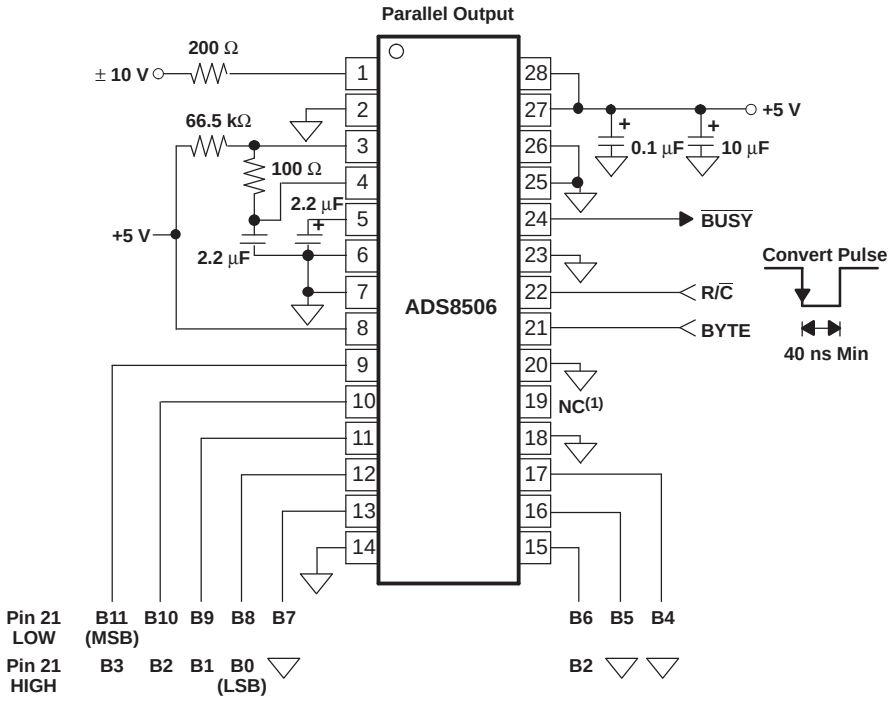


Figure 31. Basic ±10-V Operation, Both Parallel and Serial Output

SERIAL OUTPUT

Figure 32 shows a basic circuit to operate the ADS8506 with a ±10-V input range and serial output. Taking R/$\overline{C}$ (pin 22) LOW for 40 ns (12 µs max) will initiate a conversion and output valid data from the previous conversion on SDATA (pin 19) synchronized to 12 clock pulses output on DATACLK (pin 18). $\overline{BUSY}$ (pin 24) will go LOW and stay LOW until the conversion is completed and the serial data has been transmitted. Data will be output in BTC format, MSB first, and will be valid on both the rising and falling edges of the data clock. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS8506 begins tracking the input signal at the end of the conversion. Allowing 25 µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain are corrected in software (refer to the Calibration section).

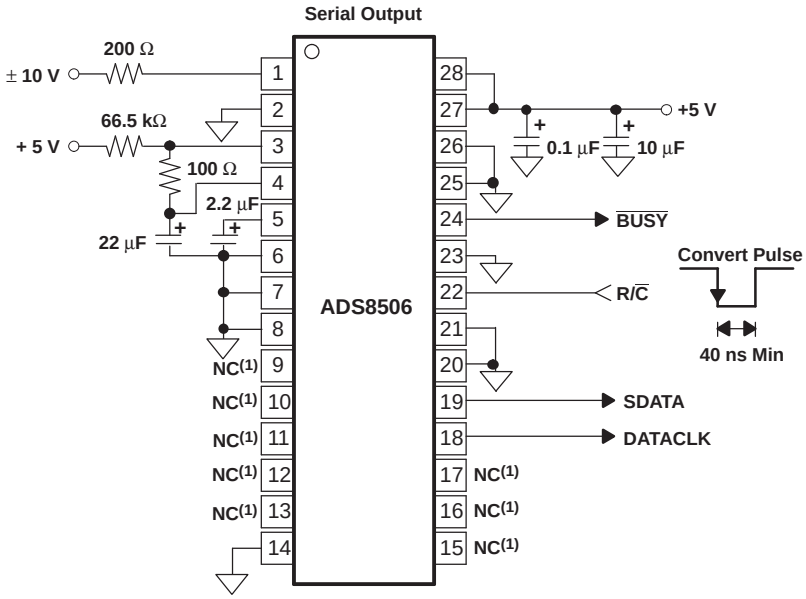


Figure 32. Basic ±10-V Operation With Serial Output

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 23) and R/$\overline{C}$ (pin 22) low for a minimum of 40 ns puts the sample-and-hold of the ADS8506 in the hold state and starts conversion *N*. $\overline{BUSY}$ (pin 24) goes low and stays low until conversion *N* is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ low are ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go high before $\overline{BUSY}$ goes high, or a new conversion is initiated without sufficient time to acquire a new signal.

The ADS8506 begins tracking the input signal at the end of the conversion. Allowing 25 µs between convert commands assures accurate acquisition of a new signal. Refer to Table 2 and Table 3 for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states, and Figure 33, Figure 34, Figure 35, Figure 36, Figure 37, Figure 38, and Figure 39 for timing diagrams.

Table 2. Control Functions When Using Parallel Output (DATACLK Tied Low, EXT/$\overline{INT}$ Tied High)

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Data bus is in Hi-Z state.
↓	0	1	Initiates conversion *N*. Data bus remains in Hi-Z state.
0	↓	1	Initiates conversion *N*. Databus enters Hi-Z state.
0	1	↑	Conversion *N* completed. Valid data from conversion *N* on the databus.
↓	1	1	Enables databus with valid data from conversion *N*.
↓	1	0	Enables databus with valid data from conversion *N–1*(1). Conversion *N* in progress.
0	↑	0	Enables databus with valid data from conversion *N–1*(1). Conversion *N* in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion *N* in progress.

(1) See Figure 33 and Figure 34 for constraints on data valid from conversion N–1.

$\overline{CS}$ and R/$\overline{C}$ are internally ORed and level triggered. It is not a requirement which input goes low first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion *N*, be sure the less critical input is low at least t_{su2} ≥ 10 ns prior to the initiating input. If EXT/$\overline{INT}$ (pin 8) is low when initiating conversion *N*, serial data from conversion *N–1* is output on SDATA (pin 19) following the start of conversion *N*. See Internal Data Clock in the Reading Data section.

To reduce the number of control pins, $\overline{CS}$ can be tied low using R/$\overline{C}$ to control the read and convert modes. This has no effect when using the internal data clock in the serial output mode. The parallel output and the serial output (only when using an external data clock), however, is affected whenever R/$\overline{C}$ goes high and the external clock is active. Refer to the Reading Data section. In the internal clock mode data is clocked out every convert cycle regardless of the states of $\overline{CS}$ and R/$\overline{C}$. The conversion result is available as soon as BUSY returns to high therefore, data always represents the conversion previously completed even when it is read during a conversion.

READING DATA

The ADS8506 outputs serial or parallel data in straight binary (SB) or binary 2's complement data output format. If SB/$\overline{BTC}$ (pin 7) is high, the output is in SB format, and if low, the output is in BTC format. Refer to Table 4 for ideal output codes. The first conversion immediately following a power-up does not produce a valid conversion result.

The parallel output can be read without affecting the internal output registers; however, reading the data through the serial port shifts the internal output registers one bit per data clock pulse. As a result, data can be read on the parallel port prior to reading the same data on the serial port, but data cannot be read through the serial port prior to reading the same data on the parallel port.

Table 3. Control Functions When Using Serial Output(1)

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	OPERATION
↓	0	1	0	Output	Initiates conversion *N*. Valid data from conversion *N–1* clocked out on SDATA.
0	↓	1	0	Output	Initiates conversion *N*. Valid data from conversion *N–1* clocked out on SDATA.
↓	0	1	1	Input	Initiates conversion *N*. Internal clock still runs conversion process.
0	↓	1	1		Initiates conversion *N*. Internal clock still runs conversion process.
↓	1	1	1	Input	Conversion *N* completed. Valid data from conversion *N* clocked out on SDATA synchronized to external data clock.
↓	1	0	1	Input	Valid data from conversion *N–1* output on SDATA synchronized to external data clock. Conversion *N* in progress.
0	↑	0	1	Input	Valid data from conversion *N–1* output on SDATA synchronized to external data clock. Conversion *N* in progress.
0	0	↑	X	Input	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	X	X	New convert commands ignored. Conversion *N* in progress..

(1) See Figure 37, Figure 38, and Figure 39 for constraints on data valid from conversion *N–1*.

Table 4. Output Codes and Ideal Input Voltages

DESCRIPTION	ANALOG INPUT			DIGITAL OUTPUT			
				BINARY 2's COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
Full-scale range	±10	0 V to 5 V	0 V to 4 V	BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Least significant bit (LSB)	305 µV	76 µV	61 µV				
+Full-Scale (FS - 1LSB)	9.999695 V	4.999924 V	3.999939 V	0111 1111 1111	7FF	1111 1111 1111	FFF
Midscale	0 V	2.5 V	2 V	0000 0000 0000	000	1000 0000 0000	800
One LSB Below Midscale	305 µV	2.499924 V	1.999939 V	1111 1111 1111	FFF	0111 1111 1111	7FF
-Full-Scale	-10 V	0 V	0 V	1000 0000 0000	800	0000 0000 0000	000

PARALLEL OUTPUT

To use the parallel output, tie EXT/$\overline{INT}$ (pin 8) high and DATACLK (pin 18) low. SDATA (pin 19) should be left unconnected. The parallel output is active when R/$\overline{C}$ (pin 22) is high and $\overline{CS}$ (pin 23) is low. Any other combination of $\overline{CS}$ and R/$\overline{C}$ 3-states the parallel output. Valid conversion data can be read in two 8-bit bytes on D7-D0 (pins 9-13 and 15-17). When BYTE (pin 21) is low, the 8 most significant bits will be valid with the MSB on D7. When BYTE is high, the 4 least significant bits are valid with the LSB on D4. BYTE can be toggled to read both bytes within one conversion cycle.

Upon initial power up, the parallel output contains indeterminate data.

PARALLEL OUTPUT (After a Conversion)

After conversion *N* is completed and the output registers have been updated, $\overline{BUSY}$ (pin 24) goes high. Valid data from conversion *N* is available on D7-D0 (pin 9-13 and 15-17). $\overline{BUSY}$ going high can be used to latch the data. Refer to Table 5 and Figure 33 and Figure 34 for timing specifications.

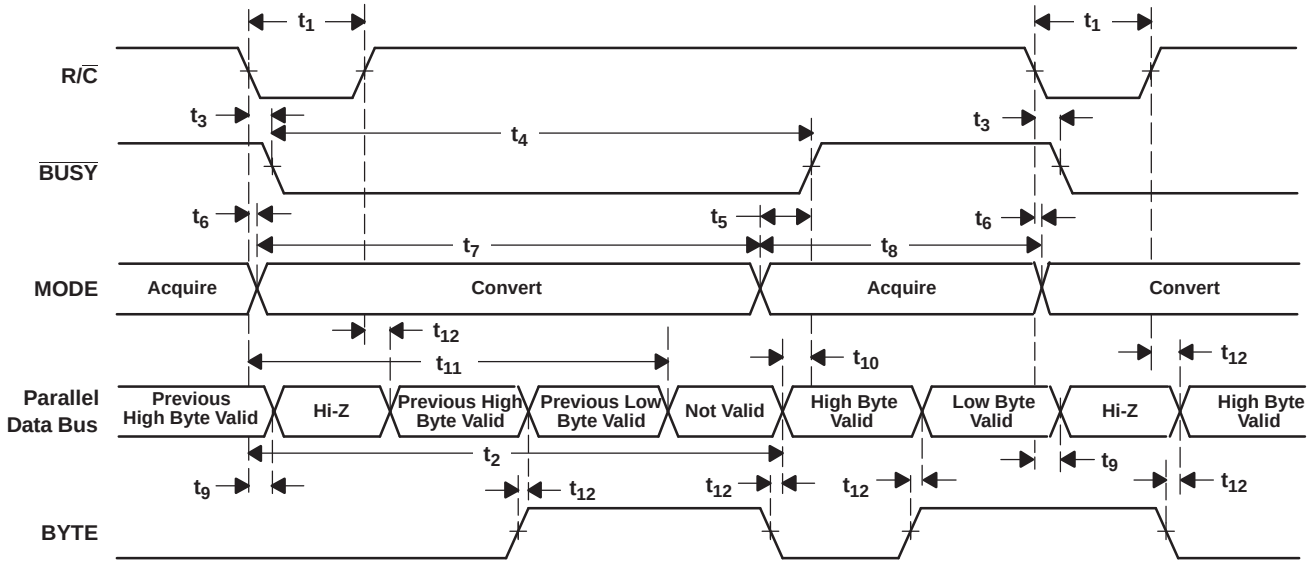


Figure 33. Conversion Timing With Parallel Output ($\overline{CS}$ and DATACLK Tied Low, EXT/INT Tied High)

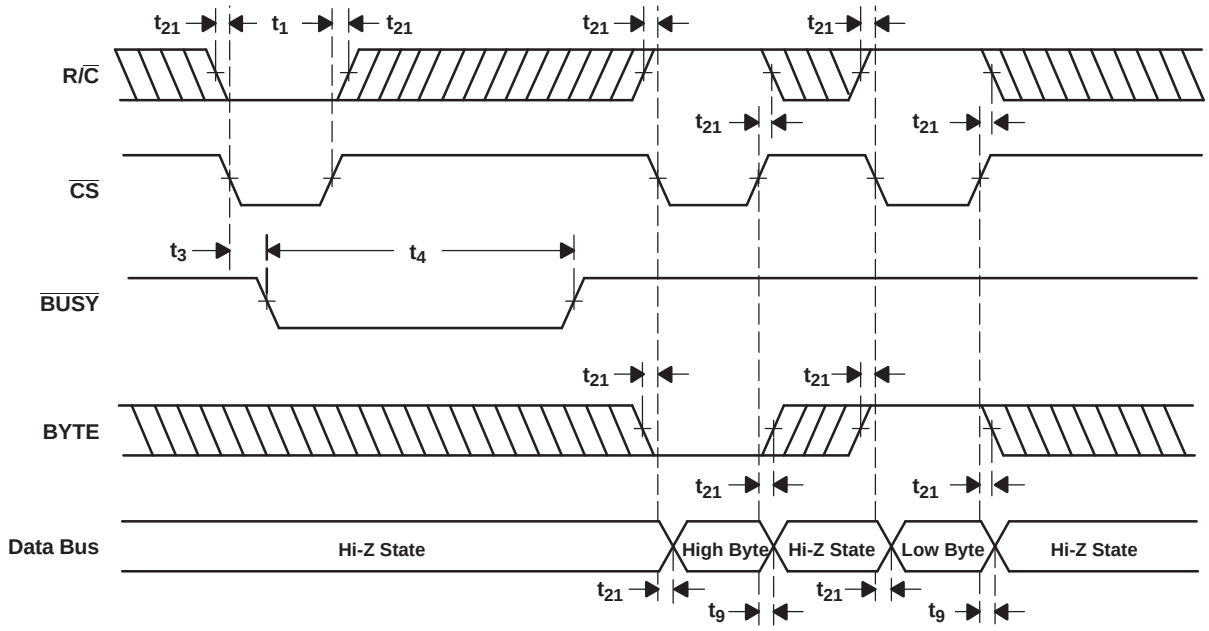


Figure 34. $\overline{CS}$ to Control Conversion and Read Timing With Parallel Outputs

PARALLEL OUTPUT (During a Conversion)

After conversion *N* has been initiated, valid data from conversion *N–1* can be read and is valid up to 12 µs after the start of conversion *N*. Do not attempt to read data beyond 12 µs after the start of conversion *N* until $\overline{BUSY}$ (pin 24) goes high; this may result in reading invalid data. Refer to Table 5 and Figure 33 and Figure 34 for timing constraints.

Table 5. Parallel Conversion and Data Timing, T_A = -40°C to 85°C

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert pulse width	0.04		12	µs
t_2	Data valid delay after R/$\overline{C}$ low		13.5	15	µs
t_3	$\overline{BUSY}$ delay from start of conversion			85	ns
t_4	$\overline{BUSY}$ Low		13.5	15	µs
t_5	$\overline{BUSY}$ delay after end of conversion		90		ns
t_6	Aperture delay		40		ns
t_7	Conversion time		13.5	15	µs
t_8	Acquisition time		11.5		µs
t_9	Bus relinquish time	10		83	ns
t_{10}	$\overline{BUSY}$ delay after data valid	20	60		ns
t_{11}	Previous data valid after start of conversion		13.5	15	µs
t_{12}	Bus access time and BYTE delay		10	83	ns
t_{21}	R/$\overline{C}$ to $\overline{CS}$ setup time	10			ns
$t_7 + t_8$	Throughput time			25	µs

SERIAL OUTPUT

Data can be clocked out with the internal data clock or an external data clock. When using serial output, be careful with the parallel outputs, D7-D0 (pins 9-13 and 15-17), as these pins come out of Hi-Z state whenever $\overline{CS}$ (pin 23) is low and R/$\overline{C}$ (pin 22) is high. The serial output cannot be 3-stated and is always active. Refer to the Applications Information section for specific serial interfaces. If external clock is used, the TAG input can be used to daisy-chain multiple ADS8506 data pins together.

INTERNAL DATA CLOCK (During a Conversion)

To use the internal data clock, tie EXT/$\overline{INT}$ (pin 8) low. The combination of R/$\overline{C}$ (pin 22) and CS (pin 23) low initiates conversion *N* and activates the internal data clock (typically 900-kHz clock rate). The ADS8506 outputs 12 bits of valid data, MSB first, from conversion *N–1* on SDATA (pin 19), synchronized to 12 clock pulses output on DATACLK (pin 18). The data is valid on both the rising and falling edges of the internal data clock. The rising edge of $\overline{BUSY}$ (pin 24) can be used to latch the data. After the 12th clock pulse, DATACLK remains low until the next conversion is initiated, while SDATA returns to the state of the TAG pin input sensed at the start of transmission. Refer to Table 6 and Figure 36.

EXTERNAL DATA CLOCK

To use an external data clock, tie EXT/$\overline{INT}$ (pin 8) high. The external data clock is not and cannot be synchronized with the internal conversion clock; care must be taken to avoid corrupting the data. To enable the output mode of the ADS8506, CS (pin 23) must be low and R/$\overline{C}$ (pin 22) must be high. DATACLK must be high for 20% to 70% of the total data clock period; the clock rate can be between DC and 10 MHz. Serial data from conversion *N* can be output on SDATA (pin 19) after conversion *N* is completed or during conversion *N+1*.

An obvious way to simplify control of the converter is to tie $\overline{CS}$ low and use R/$\overline{C}$ to initiate conversions.

While this is perfectly acceptable, there is a possible problem when using an external data clock. At an indeterminate point from 12 µs after the start of conversion *N* until $\overline{BUSY}$ rises, the internal logic shifts the results of conversion *N* into the output register. If $\overline{CS}$ is low, R/$\overline{C}$ high, and the external clock is high at this point, data is lost. So, with $\overline{CS}$ low, either R/$\overline{C}$ and/or DATACLK must be low during this period to avoid losing valid data.

EXTERNAL DATA CLOCK (After a Conversion)

After conversion *N* is completed and the output registers have been updated, $\overline{\text{BUSY}}$ (pin 24) goes high. With $\overline{\text{CS}}$ low and R/$\overline{\text{C}}$ high, valid data from conversion *N* is output on SDATA (pin 19) synchronized to the external data clock input on DATACLK (pin 18). The MSB is valid on the first falling edge and the second rising edge of the external data clock. The LSB is valid on the 12th falling edge and 13th rising edge of the data clock. TAG (pin 20) inputs a bit of data for every external clock pulse. The first bit input on TAG is valid on SDATA on the 13th falling edge and the 14th rising edge of DATACLK; the second input bit is valid on the 14th falling edge and the 15th rising edge, etc. With a continuous data clock, TAG data is output on SDATA until the internal output registers are updated with the results from the next conversion. Refer to Table 6 and Figure 38.

EXTERNAL DATA CLOCK (During a Conversion)

After conversion *N* has been initiated, valid data from conversion *N–1* can be read and is valid up to 12 μs after the start of conversion *N*. Do not attempt to clock out data from 12 μs after the start of conversion *N* until BUSY (pin 24) rises; this results in data loss. NOTE: For the best possible performance when using an external data clock, data should not be clocked out during a conversion. The switching noise of the asynchronous data clock can cause digital feedthrough degrading the converter's performance. Refer to Table 6 and Figure 39.

Table 6. Serial Timing Requirements, T_A = –40°C to 85°C

PARAMETER		MIN	TYP	MAX	UNIT
t_{w1}	Pulse duration, convert	0.04		12	µs
t_{d1}	Delay time, $\overline{BUSY}$ from R/$\overline{C}$ low		12	20	ns
t_{w2}	Pulse duration, $\overline{BUSY}$ low		13.5	15	µs
t_{d2}	Delay time, $\overline{BUSY}$, after end of conversion		5		ns
t_{d3}	Delay time, aperture		5		ns
t_{conv}	Conversion time		13.5	15	µs
t_{acq}	Acquisition time	10	11.5		µs
$t_{conv} + t_{acq}$	Cycle time			25	µs
t_{d4}	Delay time, R/$\overline{C}$ low to internal DATACLK output		204		ns
t_{c1}	Cycle time, internal DATACLK	600	820	850	ns
t_{d5}	Delay time, data valid to internal DATACLK high	150	204		ns
t_{d6}	Delay time, data valid after internal DATACLK low	150	208		ns
t_{c2}	Cycle time, external DATACLK	35			ns
t_{w3}	Pulse duration, external DATACLK high	15			ns
t_{w4}	Pulse duration, external DATACLK low	15			ns
t_{su1}	Setup time, R/$\overline{C}$ rise/fall to external DATACLK high	15			ns
t_{su2}	Setup time, R/$\overline{C}$ transition to $\overline{CS}$ transition	10			ns
t_{d8}	Delay time, data valid from external DATCLK high	2		20	ns
t_{d9}	Delay time, $\overline{CS}$ rising edge to external DATACLK rising edge	10			ns
t_{d10}	Delay time, previous data available after $\overline{CS}$, R/$\overline{C}$ low	12			µs
t_{su4}	Setup time, $\overline{BUSY}$ transition to first external DATACLK	5			ns
t_{d11}	Delay time, final external DATACLK to $\overline{BUSY}$ rising edge			2	µs
t_{su3}	Setup time, TAG valid to rising DATACLK	0			ns
t_{h1}	Hold time, TAG valid after rising edge of DATACLK	2			ns

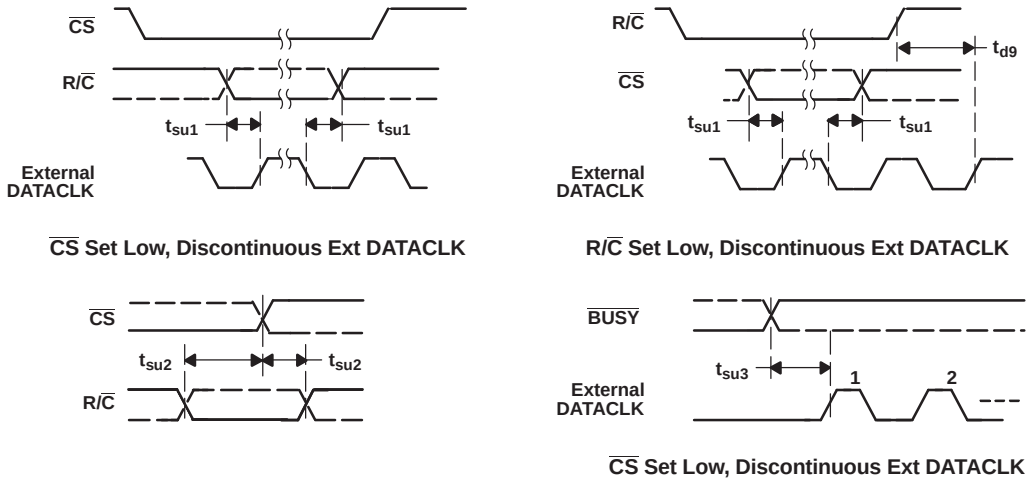
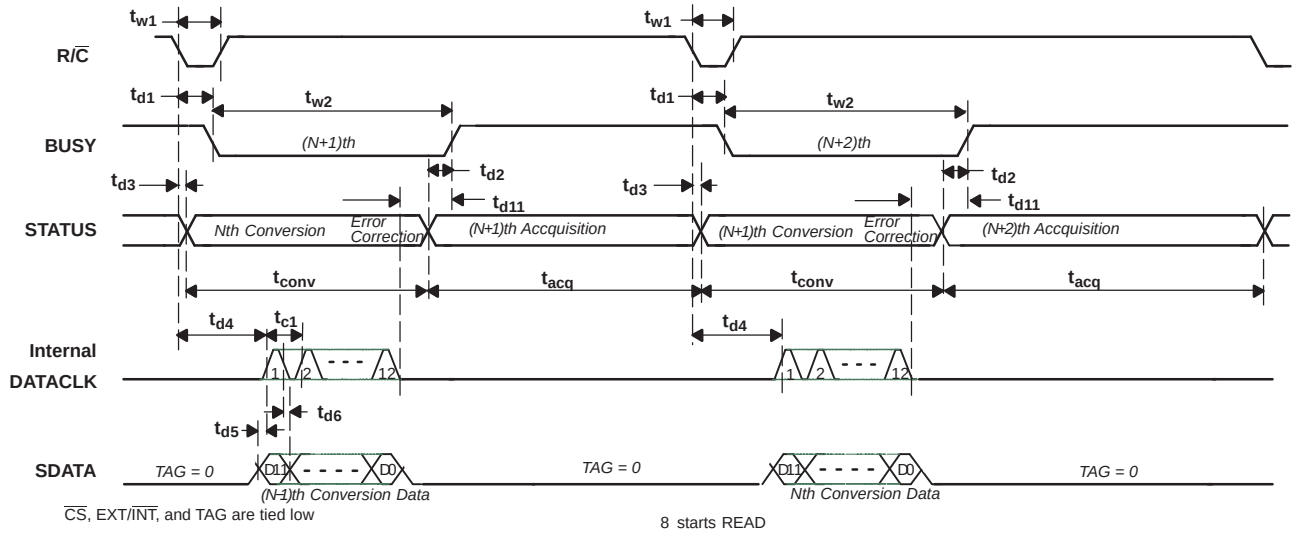


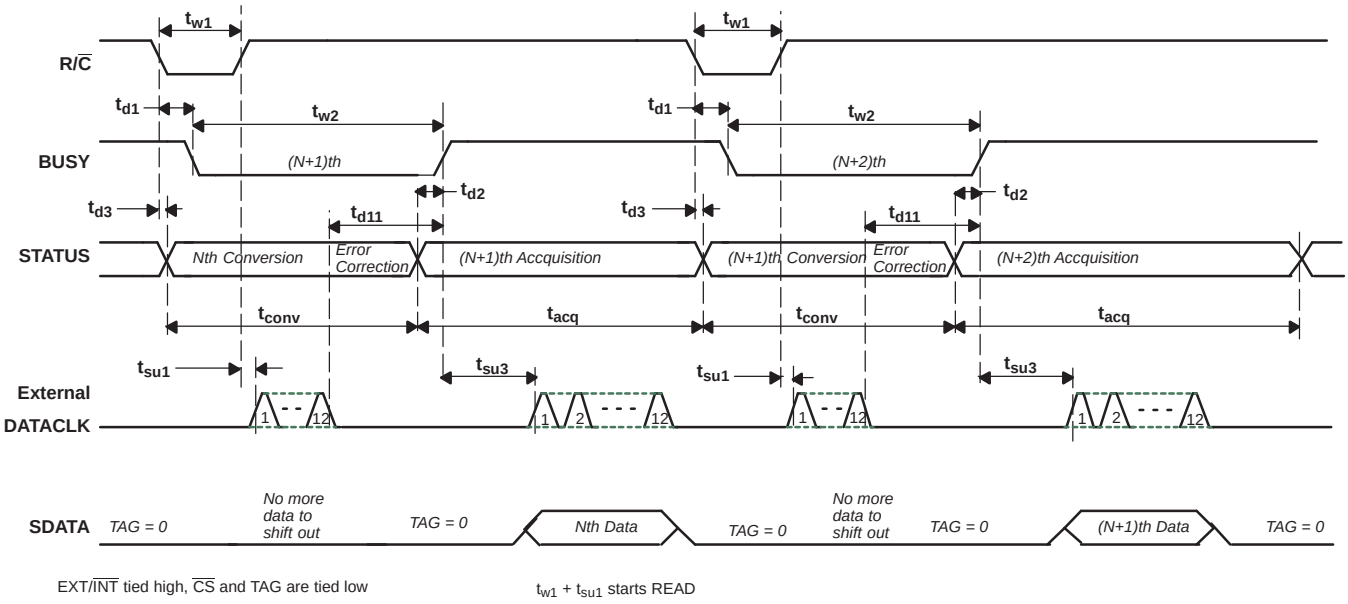
Figure 35. Critical Timing



CS, EXT/INT, and TAG are tied low

8 starts READ

Figure 36. Basic Conversion Timing - Internal DATACLK (Read Previous Data During Conversion)



EXT/INT tied high, CS and TAG are tied low

$t_{w1} + t_{su1}$ starts READ

Figure 37. Basic Conversion Timing - External DATACLK

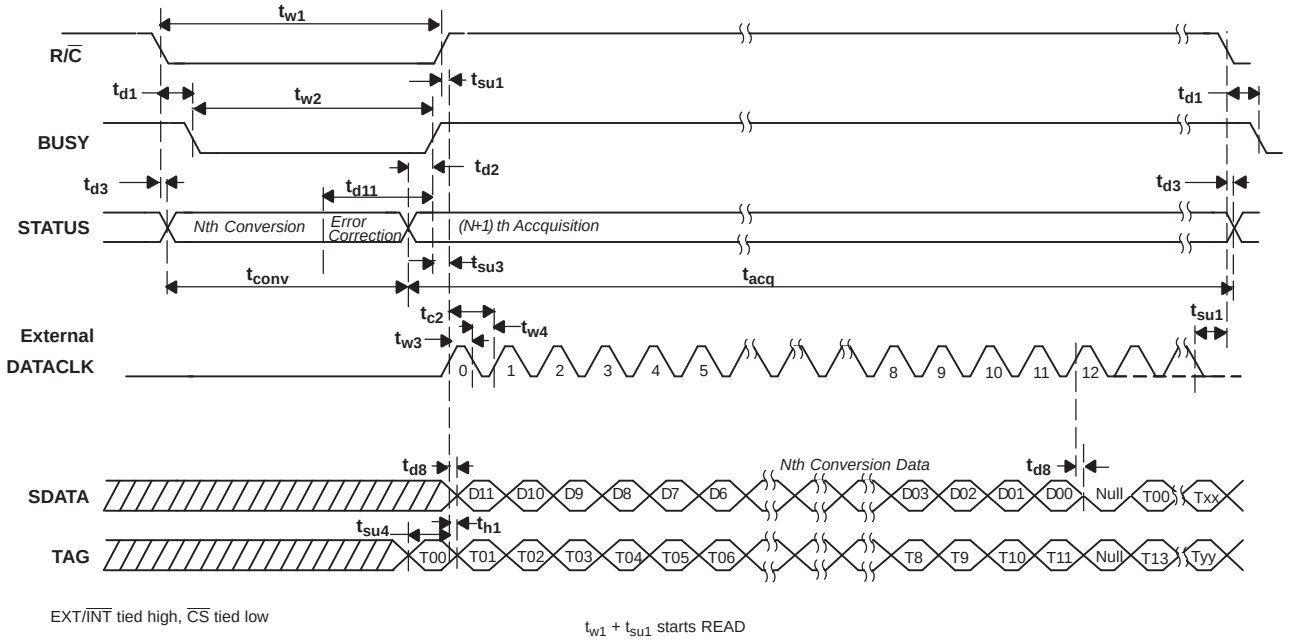


Figure 38. Read After Conversion (Discontinuous External DATACLK)

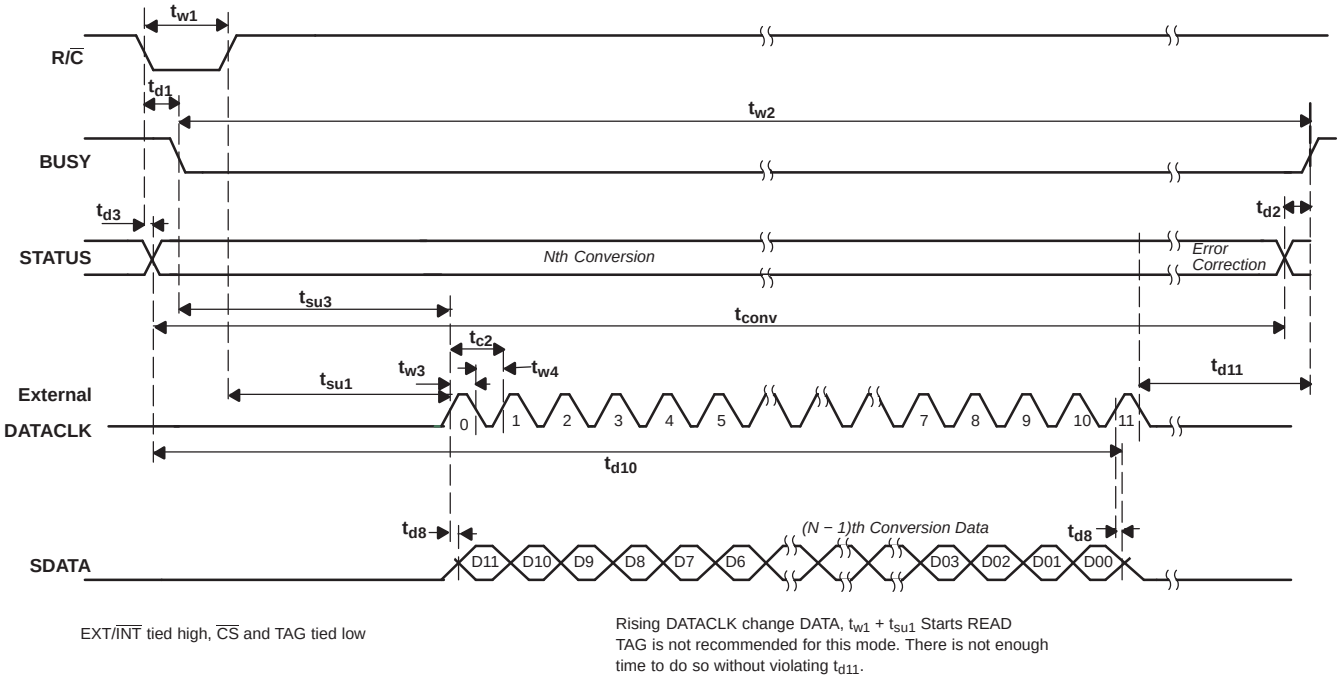


Figure 39. Read During Conversion (Discontinuous External DATACLK)

TAG FEATURE

The TAG feature allows the data from multiple ADS8506 converters to be read on a single serial line. The converters are cascaded together using the DATA pins as outputs and the TAG pins as inputs as illustrated in Figure 40. The DATA pin of the last converter drives the processor's serial data input. Data is then shifted through each converter, synchronous to the externally supplied data clock, onto the serial data line. The internal clock cannot be used for this configuration.

The preferred timing uses the discontinuous, external, data clock during the sampling period. Data must be read during the sampling period because there is not sufficient time to read data from multiple converters during a conversion period without violating the t_{d11} constraint (see the EXTERNAL DATACLOCK section). The sampling period must be sufficiently long to allow all data words to be read before starting a new conversion.

Note, in Figure 40, that a NULL bit separates the data word from each converter. The state of the DATA pin at the end of a READ cycle reflects the state of the TAG pin at the start of the cycle. This is true in all READ modes, including the internal clock mode. For example, when a single converter is used in the internal clock mode the state of the TAG pin determines the state of the DATA pin after all 12 bits have shifted out. When multiple converters are cascaded together this state forms the NULL bit that separates the words. Thus, with the TAG pin of the first converter grounded as shown in Figure 40 the NULL bit becomes a zero between each data word.

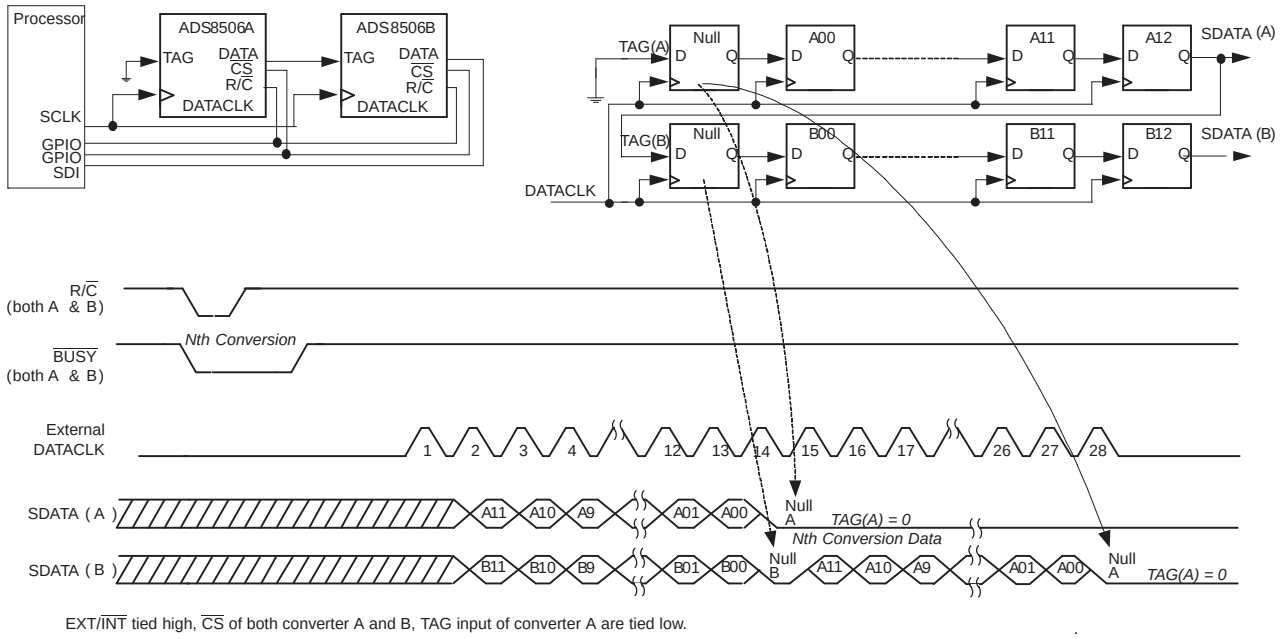


Figure 40. Timing of TAG Feature With Single Conversion (Using External DATACLK)

INPUT RANGES

The ADS8506 offers three input ranges: standard ±10-V and 0-V to 5-V ranges, and a 0-V to 4-V range for complete, single-supply systems. See Figure 42 and Figure 43 for the necessary circuit connections for implementing each input range and optional offset and gain adjust circuitry. Offset and full-scale error specifications are tested with the fixed resistors, see Figure 43 (full-scale error includes offset and gain errors measured at both +FS and -FS). Adjustments for offset and gain are described in the Calibration section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain are corrected in software (refer to the Calibration section).

The input impedance, summarized in Table 1, results from the combination of the internal resistor network (see the front page of this product data sheet) and the external resistors used for each input range (see Figure 44). The input resistor divider network provides inherent over-voltage protection to at least ±5.5 V for $R2_{IN}$ and ±12 V for $R1_{IN}$.

Analog inputs above or below the expected range yields either positive full-scale or negative full-scale digital outputs, respectively. Wrapping or folding over for analog inputs outside the nominal range does not occur.

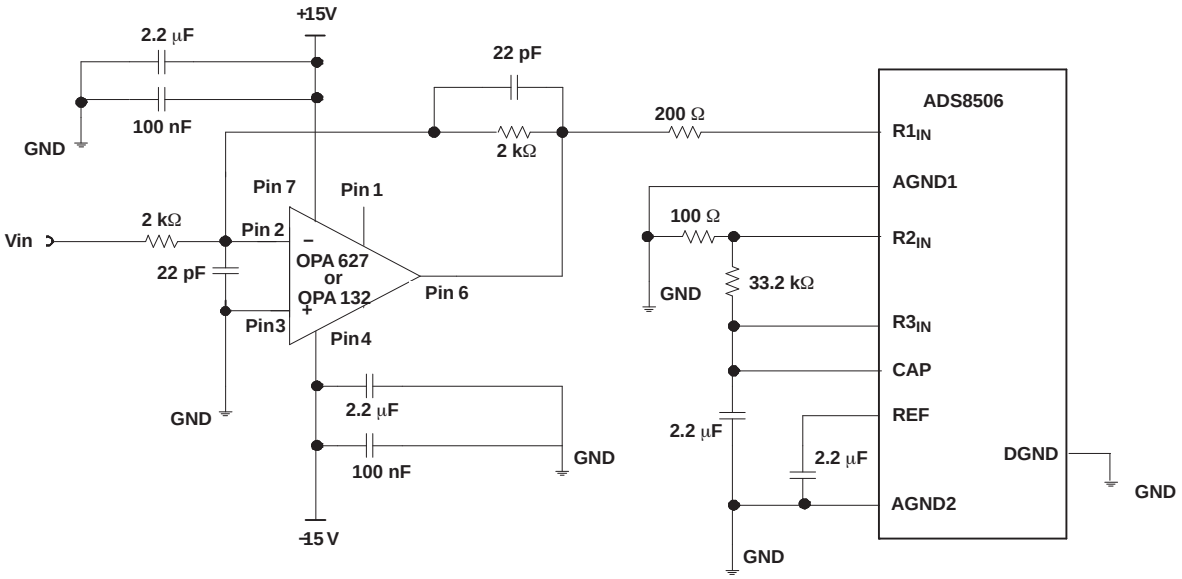


Figure 41. Typical Driving Circuit (±10 V, No Trim)

CALIBRATION

Hardware Calibration

To calibrate the offset and gain of the ADS8506 in hardware, install the resistors shown in Figure 42. Table 7 lists the hardware trim ranges relative to the input for each input range.

Table 7. Offset and Gain Adjust Ranges for Hardware Calibration (see Figure 42)

INPUT RANGE	OFFSET ADJUST RANGE (mV)	GAIN ADJUST RANGE (mV)
±10 V	±15	±60
0 V to 5 V	±4	±30
0 V to 4 V	±3	±30

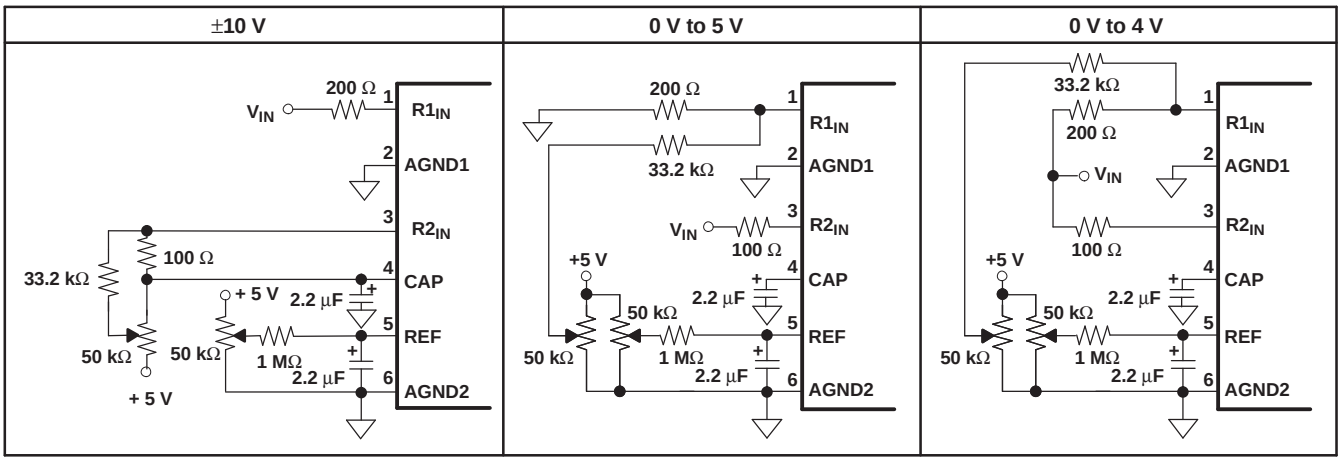


Figure 42. Circuit Diagrams (With Hardware Trim)

Software Calibration

To calibrate the offset and gain in software, no external resistors are required. However, to get the data sheet specifications for offset and gain, the resistors shown in Figure 43 are necessary. See the No Calibration section for more details on the external resistors. Refer to Table 8 for the range of offset and gain errors with and without the external resistors.

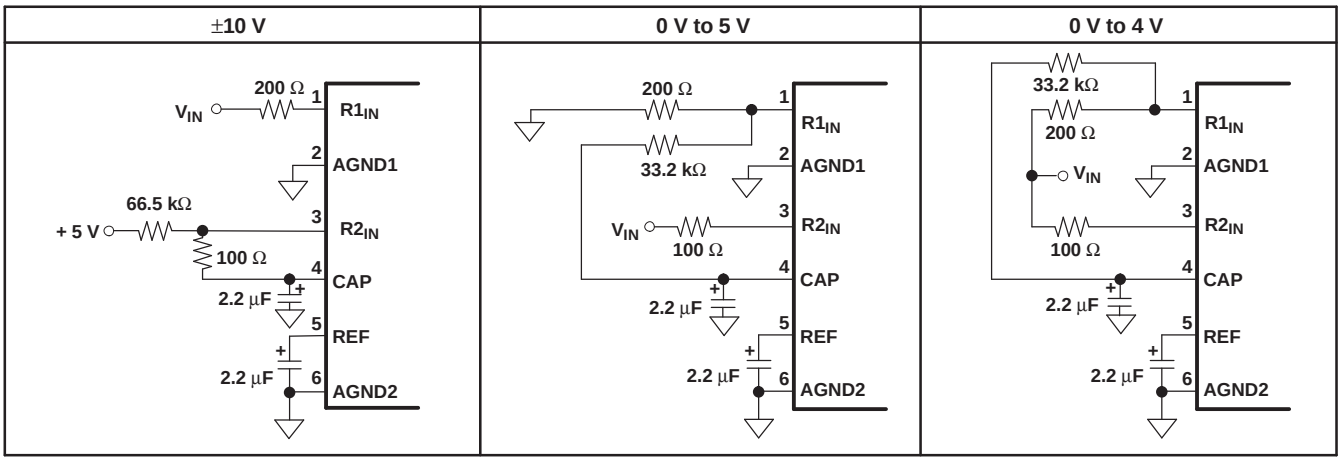


Figure 43. Circuit Diagrams (Without Hardware Trim)

Table 8. Range of Offset and Gain Errors With and Without External Resistors

INPUT RANGE (V)	OFFSET ERROR			GAIN ERROR		
	WITH RESISTORS	WITHOUT RESISTORS		WITH RESISTORS	WITHOUT RESISTORS	
	RANGE (mV)	RANGE (mV)	TYP (mV)	RANGE (% FS)	RANGE (% FS)	TYP
±10	-10 ≤ BPZ ≤ 10	0 ≤ BPZ ≤ 35	15	-0.4 ≤ G ≤ 0.4	-0.3 ≤ G ≤ 0.5	0.05
				0.15 ≤ G(1) ≤ 0.15	-0.1 ≤ G(1) ≤ 0.2	0.05
0 to 5	-3 ≤ UPO ≤ 3	-12 ≤ UPO ≤ -3	-7.5	-0.4 ≤ G ≤ 0.4	-1.0 ≤ G ≤ 0.1	-0.2
				0.15 ≤ G(1) ≤ 0.1	-0.55 ≤ G(1) ≤ -0.05	-0.2
0 to 4	-3 ≤ UPO ≤ 3	-10.5 ≤ UPO ≤ -1.5	-6	-0.4 ≤ G ≤ 0.4	-1.0 ≤ G ≤ 0.1	-0.2
				-0.15 ≤ G(1) ≤ 0.15	-0.55 ≤ G(1) ≤ -0.05	-0.2

(1) High grade

No Calibration

Figure 43 shows circuit connections. Note that the actual voltage dropped across the external resistors is at least two orders of magnitude lower than the voltage dropped across the internal resistor divider network. This should be considered when choosing the accuracy and drift specifications of the external resistors. In most applications, 1% metal-film resistors are sufficient.

The external resistors, see Figure 43, may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. Not using the external resistors results in offset and gain errors in addition to those listed in the electrical characteristics section. Offset refers to the equivalent voltage of the digital output when converting with the input grounded. A positive gain error occurs when the equivalent output voltage of the digital output is larger than the analog input. Refer to Table 8 for nominal ranges of gain and offset errors with and without the external resistors. Refer to Figure 44 for typical shifts in the transfer functions which occur when the external resistors are removed.

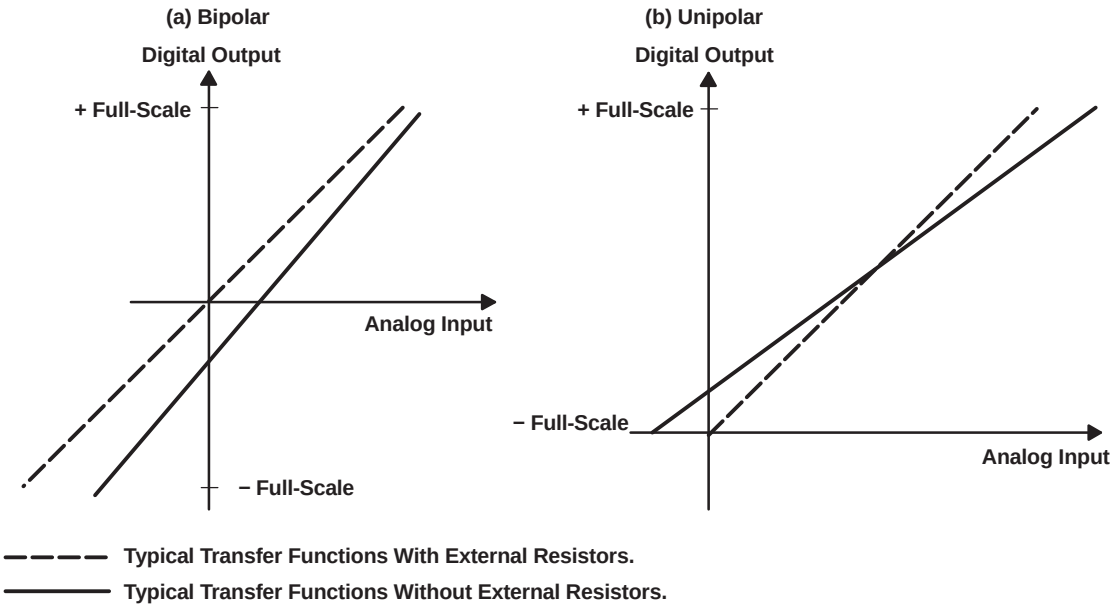


Figure 44. Typical Transfer Functions With and Without External Resistors

To further analyze the effects of removing any combination of the external resistors, consider Figure 45. The combination of the external and the internal resistors form a voltage divider which reduces the input signal to a 0.3125-V to 2.8125-V input range at the capacitor digital-to-analog converter (CDAC). The internal resistors are laser trimmed to high relative accuracy to meet full-scale specifications. The actual input impedance of the internal resistor network looking into pin 1 or pin 3 however, is only accurate to ±20% due to process variations. This should be taken into account when determining the effects of removing the external resistors.

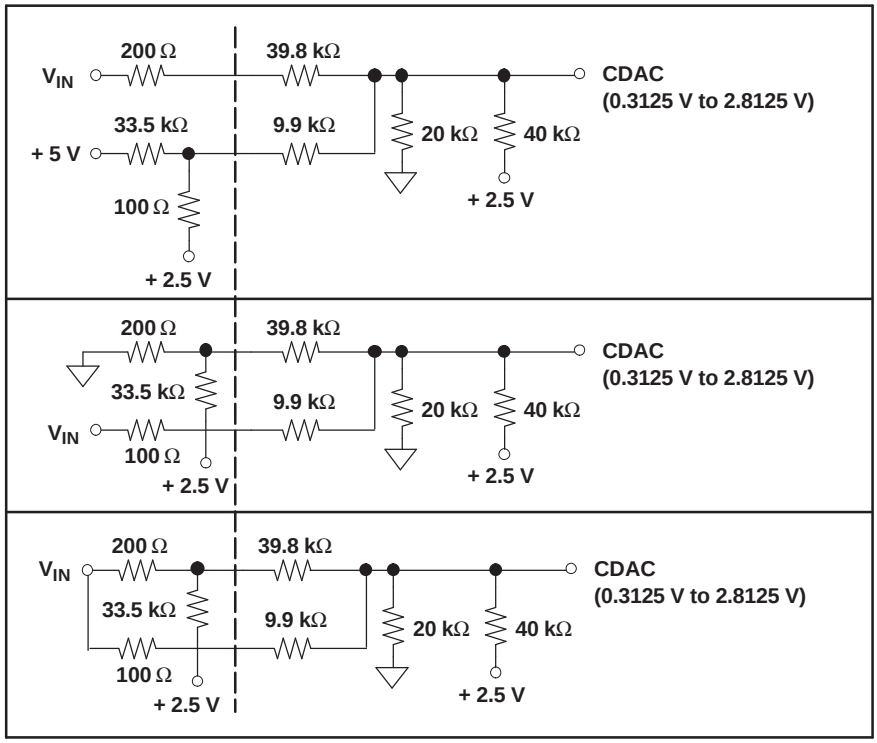


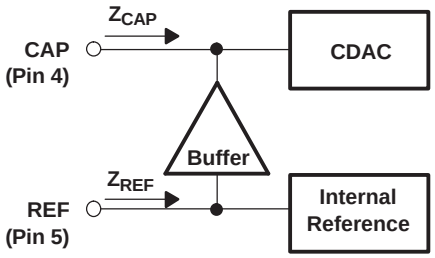
Figure 45. Circuit Diagrams Showing External and Internal Resistors

REFERENCE

The ADS8506 can operate with its internal 2.5-V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full-scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

The ADS8506 also has an internal buffer for the reference voltage. Figure 46 shows characteristic impedances at the input and output of the buffer with all combinations of powerdown and reference down.



	PWRD 0 REFD 0	PWRD 0 REFD 1	PWRD 1 REFD 0	PWRD 1 REFD 1
Z_{CAP} Ω	1	1	200	200
Z_{REF} Ω	6 k	100 M	6 k	100 M

Figure 46. Characteristic Impedances of the Internal Buffer

REF

REF (pin 5) is an input for an external reference or the output for the internal 2.5-V reference. A 2.2-µF tantalum capacitor should be connected as close as possible to the REF pin from ground. This capacitor and the output resistance of REF create a low-pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference, degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads, as shown in Figure 46.

The range for the external reference is 2.3 V to 2.7 V and determines the actual LSB size. Increasing the reference voltage increases the full-scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2-µF tantalum capacitor should be placed as close as possible to the CAP pin from ground to provide optimum switching currents for the CDAC throughout the conversions cycle. This capacitor also provides compensation for the output of the buffer. Using a capacitor any smaller than 1 µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2 µF have little affect on improving performance. ESR is the total equivalent series resistance of the compensation capacitor (CAP pin). See Figure 46 and Figure 47.

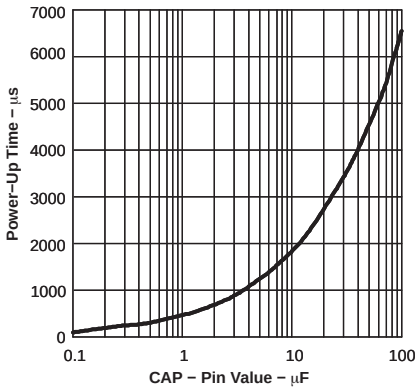


Figure 47. Power-Down to Power-Up Time vs Capacitor Value on CAP

The output of the buffer is capable of driving up to 1 mA of current to a DC load. Using an external buffer allows the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This causes performance degradation of the converter.

REFERENCE AND POWER-DOWN

The ADS8506 has analog power-down and reference power down capabilities via PWRD (pin 25) and REFD (pin 26), respectively. PWRD and REFD high powers down all analog circuitry maintaining data from the previous conversion in the internal registers, provided that the data has not already been shifted out through the serial port. Typical power consumption in this mode is 50 µW. Power recovery is typically 1 ms, using a 2.2-µF capacitor connected to CAP. Figure 47 shows power-down to power-up recovery time relative to the capacitor value on CAP. With +5 V applied to V_{DIG}, the digital circuitry of the ADS8506 remains active at all times, regardless of PWRD and REFD states.

PWRD

PWRD high powers down all of the analog circuitry except for the reference. Data from the previous conversion is maintained in the internal registers and can still be read. With PWRD high, a convert command yields meaningless data.

REFD

REFD high powers down the internal 2.5-V reference. All other analog circuitry, including the reference buffer, is active. REFD should be high when using an external reference to minimize power consumption and the loading effects on the external reference. See Figure 46 for the characteristic impedance of the reference buffer's input for both REFD high and low. The internal reference consumes approximately 5 mW.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5-V power supply and tie the analog and digital grounds together. As noted in the electrical characteristics, the ADS8506 uses 90% of its power for the analog circuitry. The ADS8506 should be considered as an analog component.

The +5-V power for the A/D converter should be separate from the +5 V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise

from the digital logic. For best performance, the +5-V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12-V or +15-V supplies are present, a simple +5-V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5-V source.

GROUNDING

Three ground pins are present on the ADS8506. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground to which all analog signals internal to the A/D converter are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D converter should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the *system* ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch on the ADS8506 is approximately 5% to 10% of the amount on similar A/D converters with the charge redistribution digital-to-analog converter (DAC) CDAC architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D converter. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS8506.

The resistive front end of the ADS8506 also provides a specified ±25-V overvoltage protection. In most cases, this eliminates the need for external over-voltage protection circuitry.

INTERMEDIATE LATCHES

The ADS8506 does have 3-state outputs for the parallel port, but intermediate latches should be used if the bus is active during conversions. If the bus is not active during conversion, the 3-state outputs can be used to isolate the A/D converter from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS8506 has an internal LSB size of 38 μV. Transients from fast switching signals on the parallel port, even when the A/D converter is 3-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

APPLICATION INFORMATION

AVERAGING

The noise of the converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise is reduced by a factor of $1/\sqrt{Hz}$ where n is the number of averages. For example, averaging four conversion results reduces the TN by to 0.4 LSBs. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to low-pass filter and decimate the output codes. This works in a similar manner to averaging: for every decimation by 2, the signal-to-noise ratio improves 3 dB.

QSPI™ INTERFACE

Figure 48 shows a simple interface between the ADS8506 and any QSPI equipped microcontroller. This interface assumes that the convert pulse does not originate from the microcontroller and that the ADS8506 is the only serial peripheral.

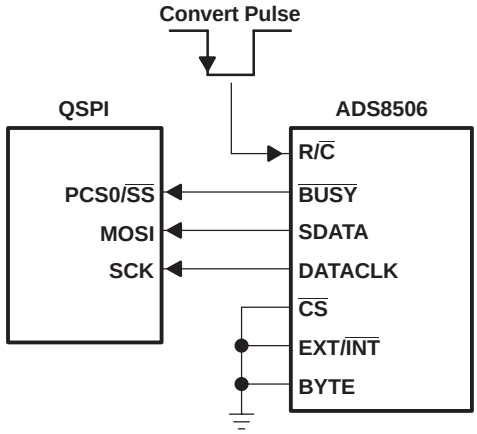


Figure 48. QSPI Interface to the ADS8506

Before enabling the QSPI interface, the microcontroller must be configured to monitor the slave select line. When a transition from high to low occurs on slave select ($\overline{SS}$) from $\overline{BUSY}$ (indicating the end of the current conversion), the port can be enabled. If this is not done, the microcontroller and the A/D converter may be *out-of-sync*.

SPI™ INTERFACE

The SPI interface is generally only capable of 8-bit data transfers. For some microcontrollers with SPI interfaces, it might be possible to receive data in a similar manner as shown for the QSPI interface in Figure 48. The microcontroller needs to fetch the 8 most significant bits before the contents are overwritten by the least significant bits.

Revision History

Changes from Revision A (OCTOBER 2007) to Revision B **Page**

- Changed minimum INL for ADS8506I from ±0.45 to ±0.9 LSB in ordering information table 2
- Changed INL min value for ADS8506I from -0.45 to -0.9 LSB in the electrical characteristics 2
- Changed INL max value for ADS8506I from 0.45 to 0.9 LSB in the electrical characteristics 2
- Added DNL min value for ADS8506I of -0.9 LSB in the electrical characteristics 3
- Changed DNL max value for ADS8506I from 0.45 to 0.9 LSB in the electrical characteristics 3
- Changed gain error typ value for ADS8506I from ±0.1% to ±0.2% 3
- Changed full scale error drift typ value for ADS8506I from ±5 to ±7 3
- Changed power supply sensitivity value for ADS8506I from typ to max 3
- Added spurious-free dynamic range min value for ADS8506IB of 80 dB 3
- Added spurious-free dynamic range min value for ADS8506I of 80 dB 3
- Changed SINAD min value for ADS8506I from 72 to 70 dB 3
- Changed SNR min value for ADS8506I from 72 to 70 dB 3
- Changed delay time t_{d10} min value from 2 to 12 µs. 17
- Changed delay time t_{d11} max value from 1 to 2 µs 17
- Changed t_{su3} to t_{su4} and t_{su4} description 17
- Changed t_{h1} description 17
- Added t_{d9} to critical timing diagram 17
- Changed t_{su3} to t_{su4} in Figure 38 19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8506IBDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8506I B	Samples
ADS8506IBDWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8506I B	Samples
ADS8506IBDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8506I B	Samples
ADS8506IDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8506I	Samples
ADS8506IDWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8506I	Samples
ADS8506IDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8506I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

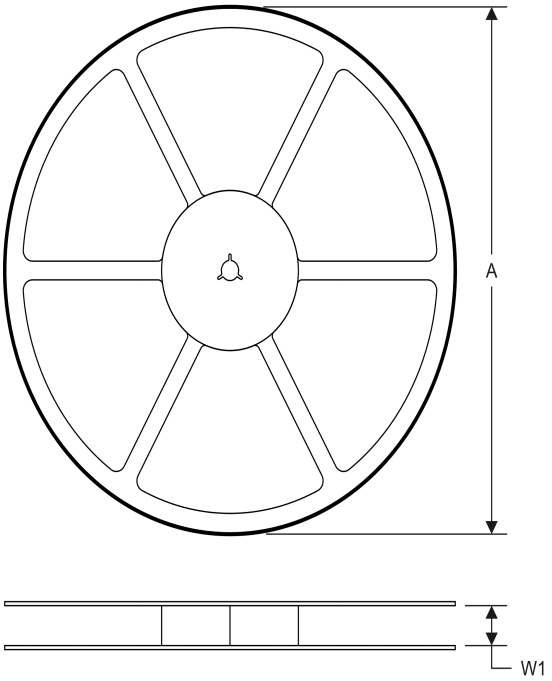
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

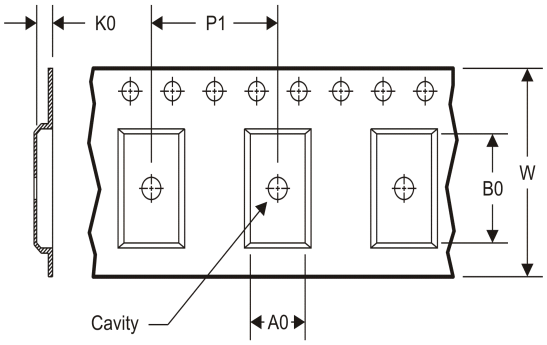
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



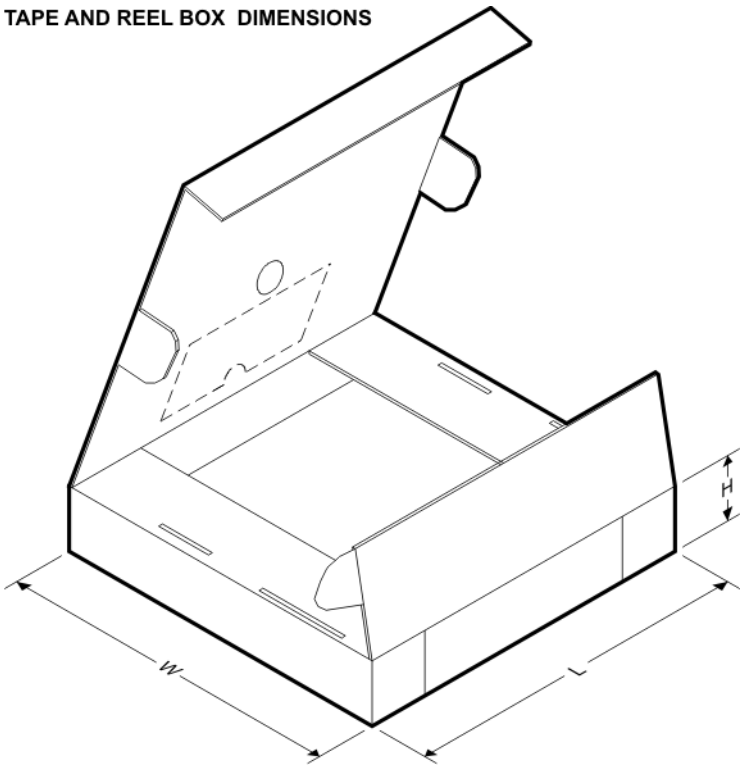
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8506IBDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
ADS8506IDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

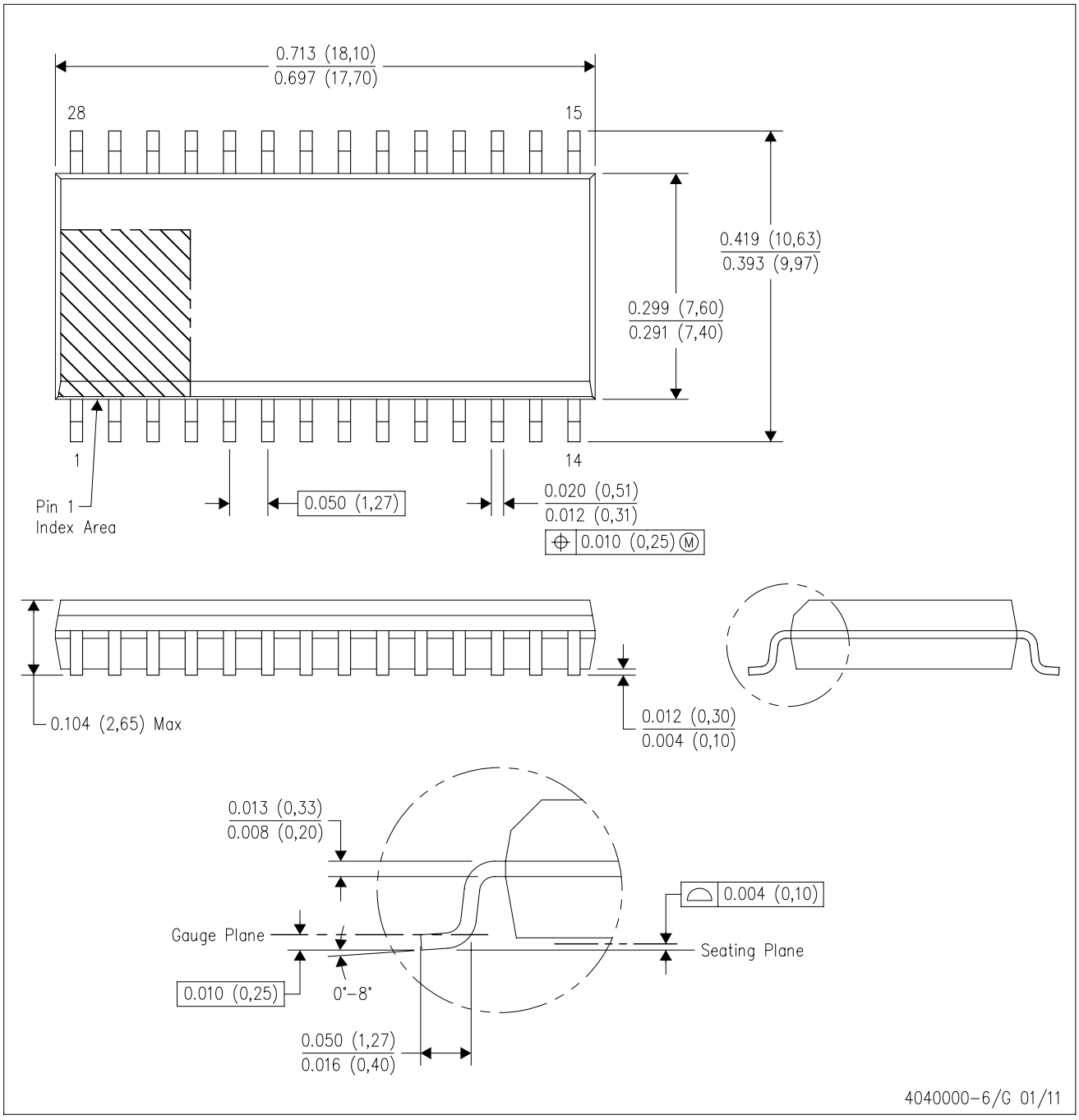
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

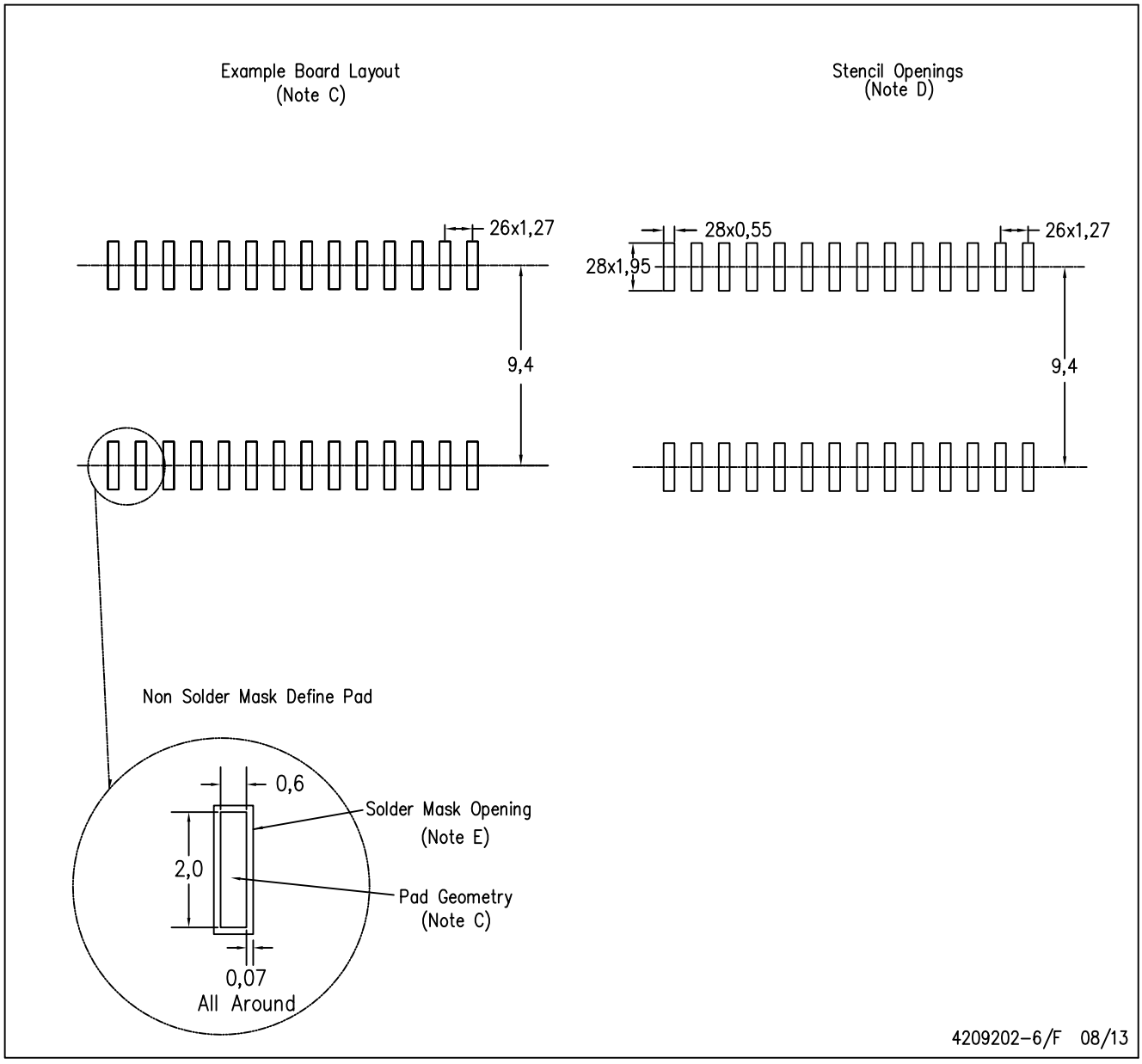
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8506IBDWR	SOIC	DW	28	1000	367.0	367.0	55.0
ADS8506IDWR	SOIC	DW	28	1000	367.0	367.0	55.0

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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