FAIRCHILD SEMICONDUCTOR™

HGT1S14N41G3VLS, HGTP14N41G3VL

Data Sheet | **September 2000** | **File Number 4887**

14A, 410V N-Channel, Logic Level, Voltage Clamping IGBTs

This N-Channel IGBT is a MOS gated, **logic level** device which is intended to be used as an ignition coil driver in **automotive ignition circuits**. Unique features include an active voltage clamp between the collector and the gate which provides **Self Clamped Inductive Switching (SCIS)** capability in ignition circuits. Internal diodes provide **ESD protection** for the logic level gate. Both a series resistor and a shunt resister are provided in the gate circuit

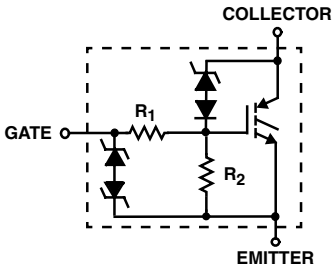
Formerly Developmental Type TA49360.

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGT1S14N41G3VLS	TO-263AB	14N41GVL
HGTP14N41G3VL	TO-220AB	14N41GVL

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB in tape and reel, i.e. HGT1S14N41G3VLS9A

Symbol

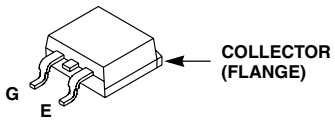


Features

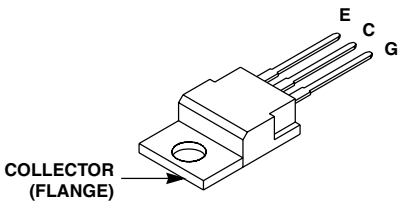
- Ignition Energy = 340mJ at $T_{J\ (STARTING)} = 25^{o}C$
- Typical Internal Clamp Voltage = 410V at $T_J = 25^{o}C$
- Logic Level Gate Drive
- ESD Gate Protection
- $T_J = 175^{o}C$
- Internal Series and Shunt Gate Resistors
- 24V Reverse Battery Capability
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Packaging

JEDEC TO-263AB



JEDEC TO-220AB



INTERSIL CORPORATION IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,587,713
4,598,461	4,605,948	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162	4,644,637
4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690	4,794,432	4,801,986
4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606	4,860,080	4,883,767
4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951	4,969,027	

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGT1S14N41G3VLS, HGTP14N41G3VL	UNITS
Collector to Emitter Breakdown Voltage	BV_{CER}	430	V
Collector to Emitter Breakdown Voltage	BV_{CES}	445	V
Emitter to Collector Breakdown Voltage	BV_{ECS}	24	V
Collector Current Continuous at $V_{GE} = 5V$, $T_C = 25^oC$	I_{C25}	25	A
at $V_{GE} = 5V$, $T_C = 110^oC$	I_{C110}	18	A
Gate to Emitter Voltage (Note 1)	V_{GEM}	±10	V
Inductive Switching Current at L = 3 mH, $T_C = 25^oC$	I_{SCIS}	15	A
at L = 3 mH, $T_C = 150^oC$	I_{SCIS}	11.5	A
Collector to Emitter Avalanche Energy at L = 3 mH, $T_C = 25^oC$	E_{AS}	340	mJ
Power Dissipation Total at $T_C = 25^oC$	P_D	136	W
Power Dissipation Derating $T_C > 25^oC$		0.91	$W/^oC$
Storage Junction Temperature Range	T_{STG}	-55 to 175	^oC
Operating Junction Temperature Range	T_J	-55 to 175	^oC
Electrostatic Discharge Voltage HBM at 250pF, 1500Ω All Pin Configurations	ESD	5	kV
Electrostatic Discharge Voltage MM at 200pF, 0Ω All Pin Configurations	ESD	2	kV
Maximum Lead Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{PKG}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. May be exceeded if I_{GEM} is limited to 10mA.

Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector to Emitter Breakdown Voltage	BV_{CER}	$I_C = 10mA$, $R_G = 1k\Omega$, $V_{GE} = 0V$, $T_J = -40^oC$ to 150^oC (Figure 17)		380	410	430	V
Collector to Emitter Breakdown Voltage	BV_{CES}	$I_C = 10mA$, $V_{GE} = 0V$, $T_J = -40^oC$ to 150^oC		395	425	445	V
Gate to Emitter Plateau Voltage	V_{GEP}	$I_C = 10A$, $V_{CE} = 12V$		-	3	-	V
Gate Charge	$Q_{G(ON)}$	$I_C = 10A$, $V_{CE} = 12V$, $V_{GE} = 5V$ (Figure 16)		-	26	-	nC
Collector to Emitter Clamp Breakdown Voltage	$BV_{CE(CL)}$	$I_C = 15A$, $R_G = 1k\Omega$		380	410	430	V
Emitter to Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$		24	28	-	V
Collector to Emitter Leakage Current	I_{CES}	$V_{CE} = 350V$, $V_{GE} = 0V$ (Figure 13)	$T_J = 25^oC$	-	-	40	μA
			$T_J = 150^oC$	-	-	200	μA
		$V_{CE} = 15V$, $V_{GE} = 0V$	$T_J = 25^oC$	-	-	10	μA
			$T_J = 150^oC$	-	-	50	μA
Emitter to Collector Leakage Current	I_{ECS}	$V_{EC} = 24V$, $V_{GE} = 0V$ (Figure 13)	$T_J = 25^oC$	-	-	1	mA
			$T_J = 150^oC$	-	-	40	mA
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 1mA$, $V_{CE} = V_{GE}$ (Figure 12)		1.3	1.8	2.2	V
Collector to Emitter On-State Voltage	$V_{CE(ON)}$	$I_C = 10A$, $V_{GE} = 3.7V$ (Figures 3 to 9)	$T_J = 25^oC$	-	1.6	2.65	V
			$T_J = 150^oC$	-	1.7	2.75	V
Collector to Emitter On-State Voltage	$V_{CE(ON)}$	$I_C = 6A$, $V_{GE} = 4.0V$ (Figures 3 to 9)	$T_J = -40^oC$	-	1.3	1.7	V
			$T_J = 25^oC$	-	1.25	1.6	V
		$I_C = 10A$, $V_{GE} = 4.5V$ (Figures 3 to 9)	$T_J = 25^oC$	-	1.45	1.7	V
			$T_J = 150^oC$	-	1.55	1.8	V
		$I_C = 14A$, $V_{GE} = 5V$ (Figures 3 to 9)	$T_J = 25^oC$	-	1.65	2.0	V
			$T_J = 175^oC$	-	1.8	2.3	V
Gate Series Resistance	R_1			-	80	-	Ω
Gate to Emitter Resistance	R_2			10	18	26	kΩ

Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Gate to Emitter Leakage Current	I_{GES}	$V_{GE} = \pm10V$		±384	±555	±1000	µA
Gate to Emitter Breakdown Voltage	BV_{GES}	$I_{GES} = \pm5mA$		±12	±14	-	V
Current Turn-On Delay Time - Resistive Load	$t_{d(ON)I}$	$V_{DD} = 14V$, $R_G = 1k\Omega$, $V_{GE} = 5V$ (Figure 14)	$I_C = 11.5A$, $T_J = 25^oC$	-	0.9	1.5	µs
			$I_C = 6.5A$, $T_J = 150^oC$	-	0.75	1.6	µs
Current Turn-On Rise Time - Resistive Load	t_{rI}	$V_{DD} = 14V$, $R_G = 1k\Omega$, $V_{GE} = 5V$ (Figure 14)	$I_C = 11.5A$, $T_J = 25^oC$	-	3.2	4.5	µs
			$I_C = 6.5A$, $T_J = 150^oC$	-	2.7	3.8	µs
Current Turn-Off Time - Inductive Load	$t_{d(OFF)I} + t_{fI}$	$I_C = 6.5A$, $R_G = 1k\Omega$, $V_{GE} = 5V$, $L = 300\mu H$, $V_{DD} = 300V$, $T_J = 150^oC$ (Figure 14)		-	9	20	µs
Current Turn-Off Time - Resistive Load	$t_{d(OFF)I} + t_{fI}$	$I_C = 6.5A$, $R_G = 1k\Omega$, $V_{GE} = 5V$, $R_L = 46\Omega$, $V_{DD} = 300V$, $T_J = 25^oC$ (Figure 14)		-	10	15	µs
Inductive Use Test	I_{SCIS}	$L = 3mH$, $V_G = 5V$, $R_G = 1k\Omega$ (Figures 1, 2)	$T_C = 150^oC$	11.5	-	-	A
			$T_C = 25^oC$	15	-	-	A
Thermal Resistance	$R_{\theta JC}$	(Figure 18)		-	-	1.1	$^oC/W$

Typical Performance Curves Unless Otherwise Specified

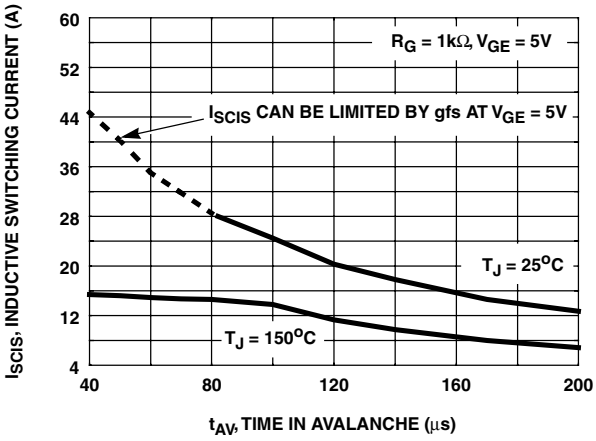


FIGURE 1. SELF CLAMPED INDUCTIVE SWITCHING CURRENT vs TIME IN AVALANCHE

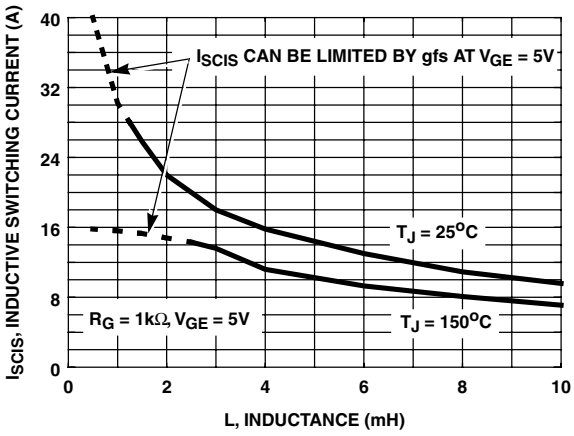


FIGURE 2. SELF CLAMPED INDUCTIVE SWITCHING CURRENT vs. INDUCTANCE

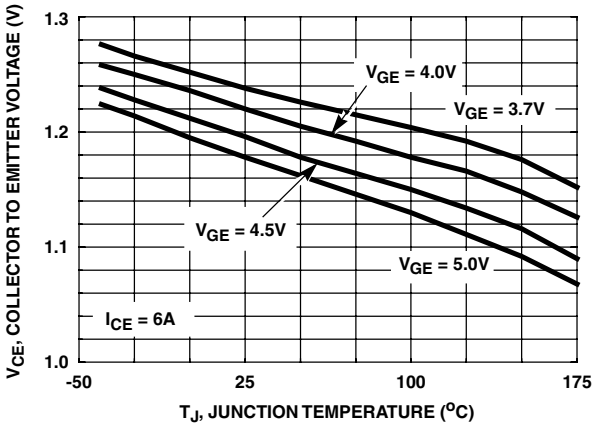


FIGURE 3. COLLECTOR TO EMITTER ON-STATE VOLTAGE vs JUNCTION TEMPERATURE

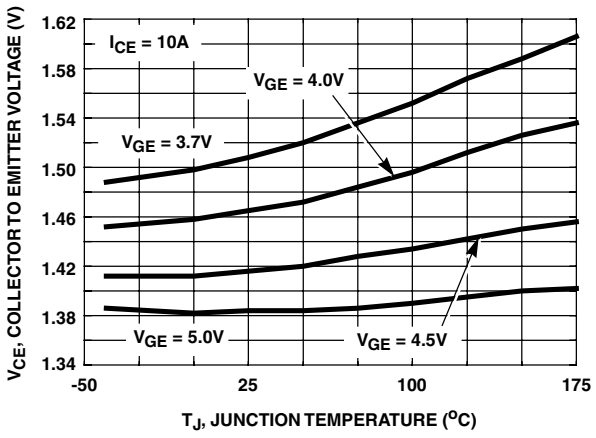


FIGURE 4. COLLECTOR TO EMITTER ON-STATE VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

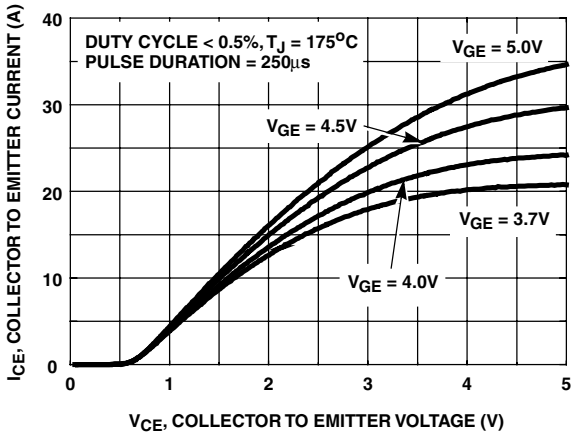


FIGURE 5. COLLECTOR TO EMITTER ON-STATE VOLTAGE

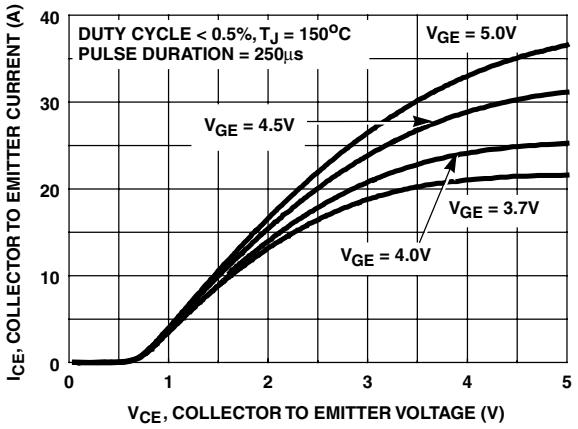


FIGURE 6. COLLECTOR TO EMITTER ON-STATE VOLTAGE

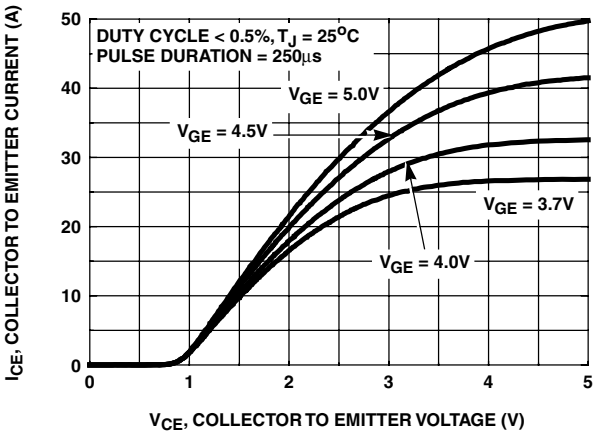


FIGURE 7. COLLECTOR TO EMITTER ON-STATE VOLTAGE

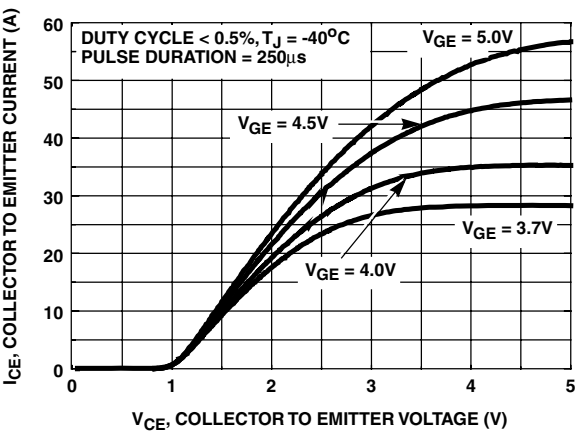


FIGURE 8. COLLECTOR TO EMITTER ON-STATE VOLTAGE

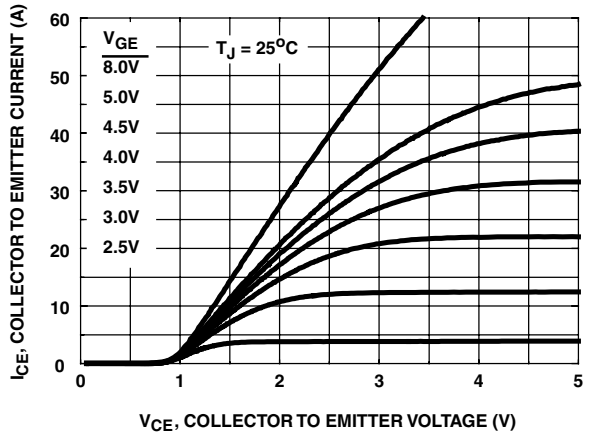


FIGURE 9. COLLECTOR TO EMITTER ON-STATE VOLTAGE

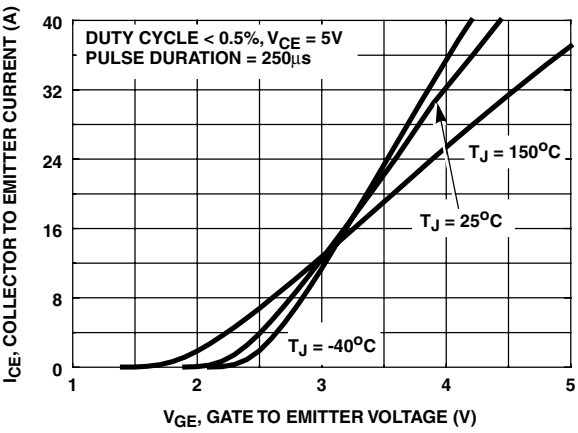


FIGURE 10. TRANSFER CHARACTERISTIC

Typical Performance Curves Unless Otherwise Specified (Continued)

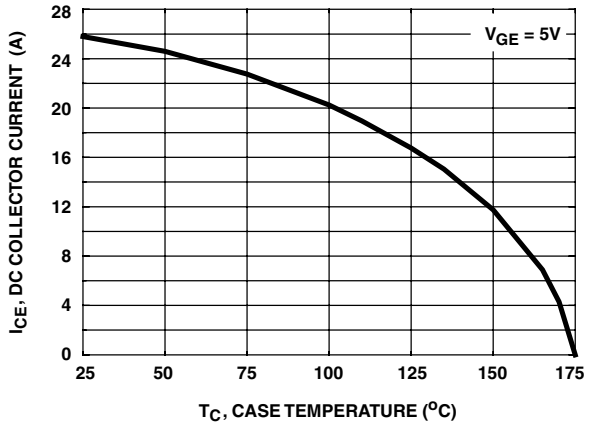


FIGURE 11. DC COLLECTOR CURRENT vs CASE TEMPERATURE

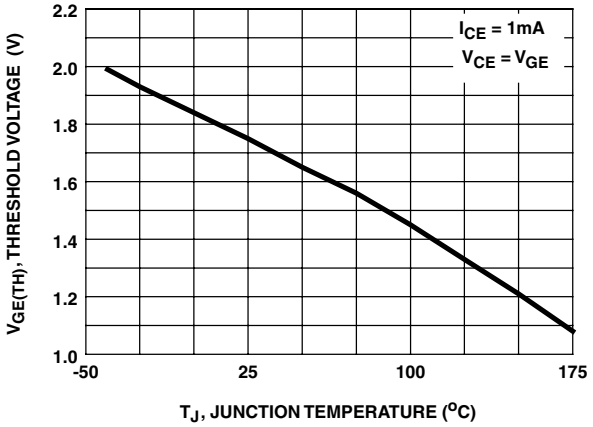


FIGURE 12. THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

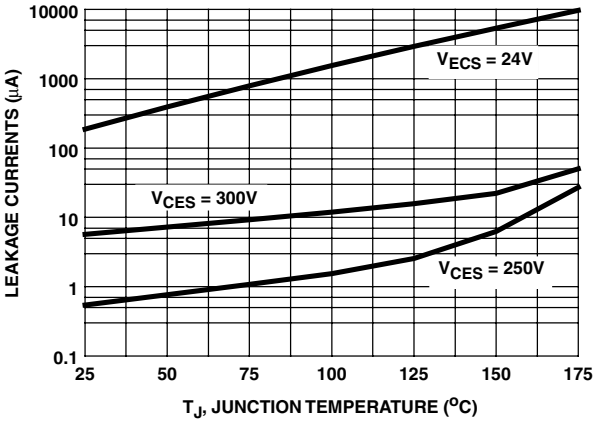


FIGURE 13. LEAKAGE CURRENT vs JUNCTION TEMPERATURE

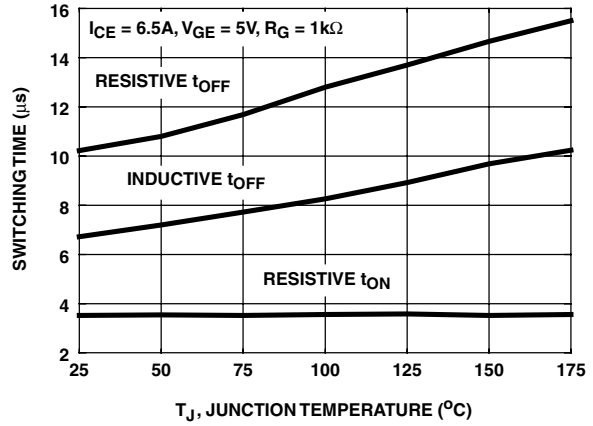


FIGURE 14. SWITCHING TIME vs JUNCTION TEMPERATURE

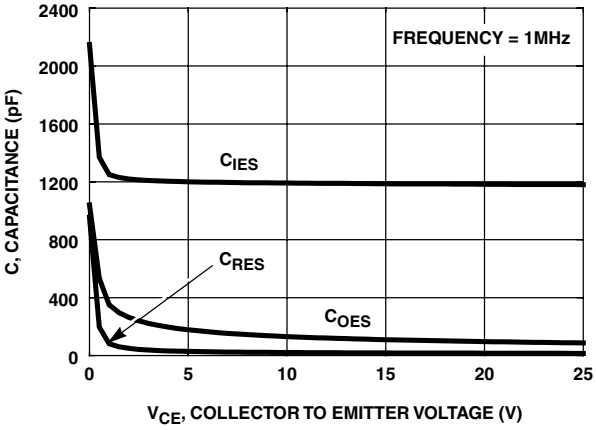


FIGURE 15. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE

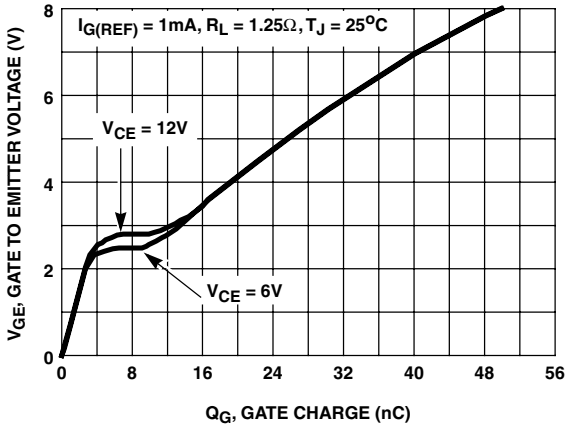


FIGURE 16. GATE CHARGE WAVEFORMS

Typical Performance Curves Unless Otherwise Specified (Continued)

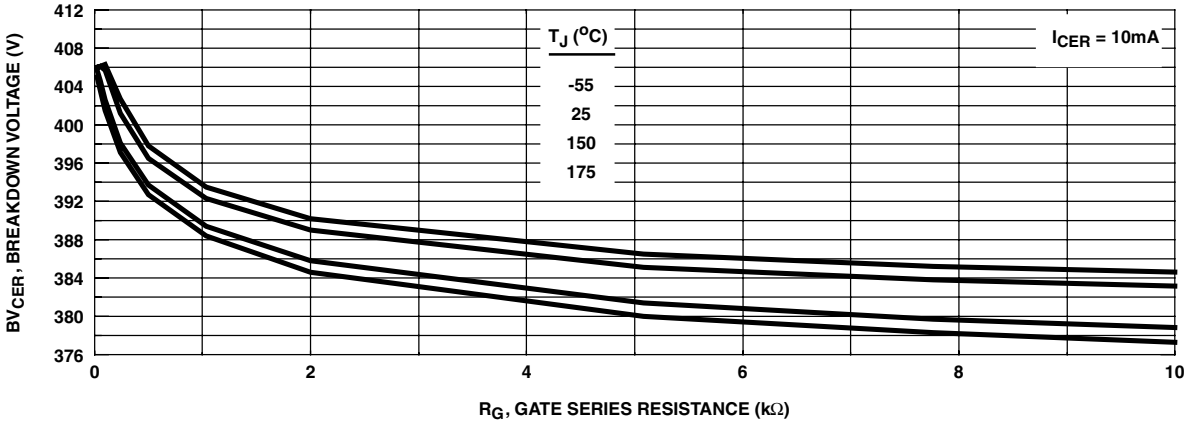


FIGURE 17. BREAKDOWN VOLTAGE vs SERIES GATE RESISTANCE

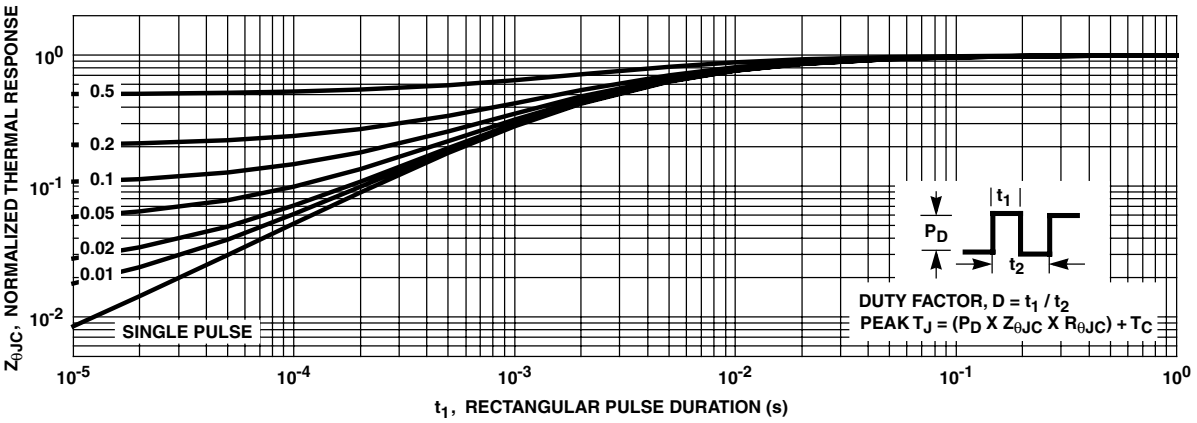


FIGURE 18. IGBT NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

Test Circuit and Waveforms

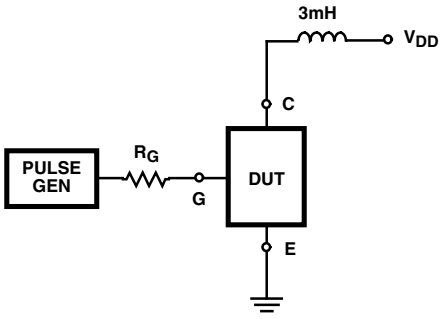


FIGURE 19. INDUCTIVE SWITCHING TEST CIRCUIT

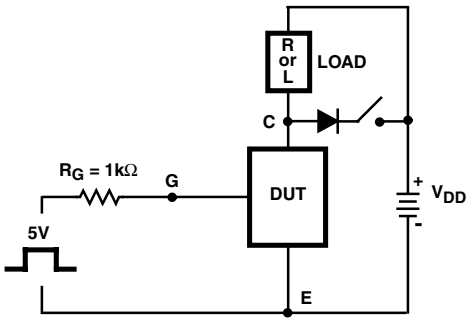
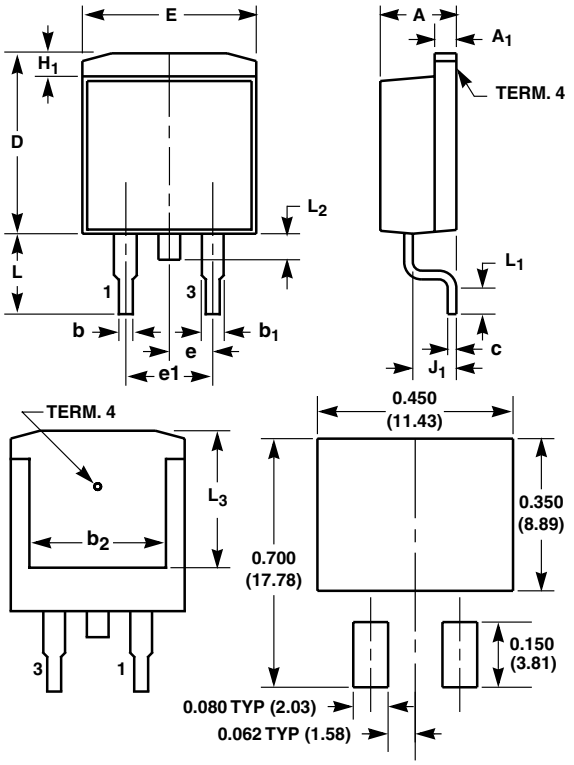


FIGURE 20. t_{ON} AND t_{OFF} SWITCHING TEST CIRCUIT

TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



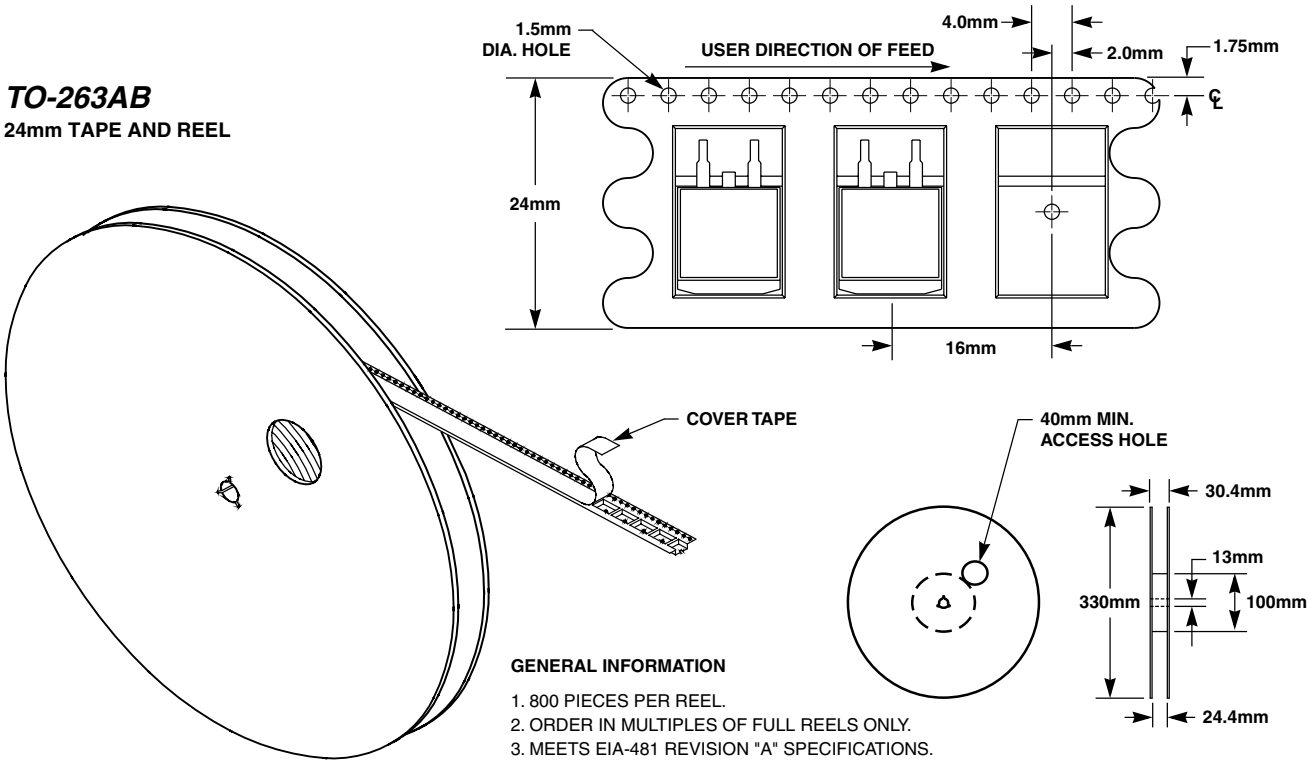
MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b_1	0.045	0.055	1.15	1.39	4, 5
b_2	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e_1	0.200 BSC		5.08 BSC		7
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L_1	0.090	0.110	2.29	2.79	4, 6
L_2	0.050	0.070	1.27	1.77	3
L_3	0.315	-	8.01	-	2

NOTES:
1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 10 dated 5-99.

TO-263AB

24mm TAPE AND REEL

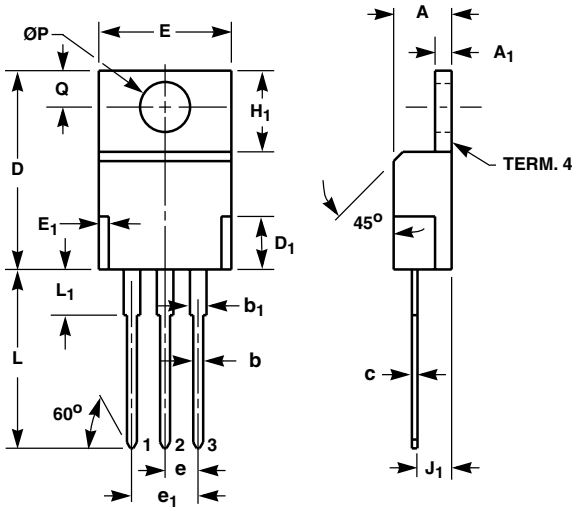


GENERAL INFORMATION

1. 800 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

FAIRCHILD SEMICONDUCTOR TM

FRM240D, FRM240R, FRM240H

16A, 200V, 0.24 Ohm, Rad Hard, N-Channel Power MOSFETs

June 1998

Features

- 16A, 200V, RDS(on) = 0.24Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 5.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2

Description

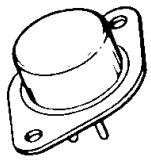
The Intersil Corporation has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^o) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

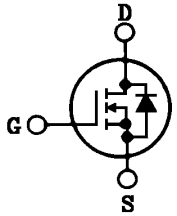
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Intersil High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA



Symbol



Absolute Maximum Ratings (T_C = +25^{o}C) Unless Otherwise Specified

		FRM240D, R, H	UNITS
Drain-Source Voltage	VDS	200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	200	V
Continuous Drain Current			
TC = +25^{o}C	ID	16	A
TC = +100^{o}C	ID	10	A
Pulsed Drain Current	IDM	48	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25^{o}C	PT	125	W
TC = +100^{o}C	PT	50	W
Derated Above +25^{o}C		1.00	W/^{o}C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	48	A
Continuous Source Current (Body Diode)	IS	16	A
Pulsed Source Current (Body Diode)	ISM	48	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	^{o}C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	^{o}C

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 200V, VGS = 0 VDS = 160V, VGS = 0 VDS = 160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	48	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 16A	-	4.03	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 10A	-	0.240	Ω
Turn-On Delay Time	td(on)	VDD = 100V, ID = 16A	-	52	ns
Rise Time	tr	Pulse Width = 3µs	-	264	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	280	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	148	
Gate-Charge Threshold	QG(th)	VDD = 100V, ID = 16A IGS1 = IGS2 0 ≤ VGS ≤ 20	1.5	8	nc
Gate-Charge On State	QG(on)		29	116	
Gate-Charge Total	QGM		57	228	
Plateau Voltage	VGP		3	16	V
Gate-Charge Source	QGS		7	28	nc
Gate-Charge Drain	QGD		15	60	
Diode Forward Voltage	VSD	ID = 16A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 16A; di/dt = 100A/µs	-	400	ns
Junction-To-Case	Rθjc		-	1.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

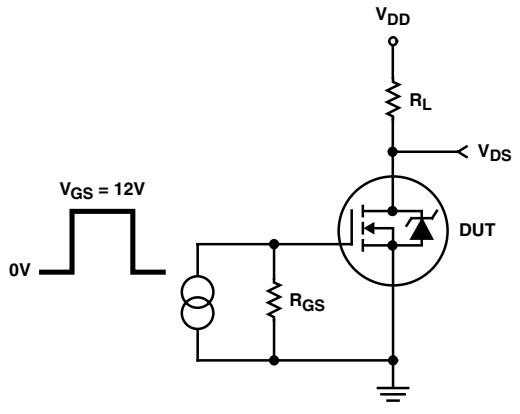


FIGURE 1. RESISTIVE SWITCHING TEST CIRCUIT

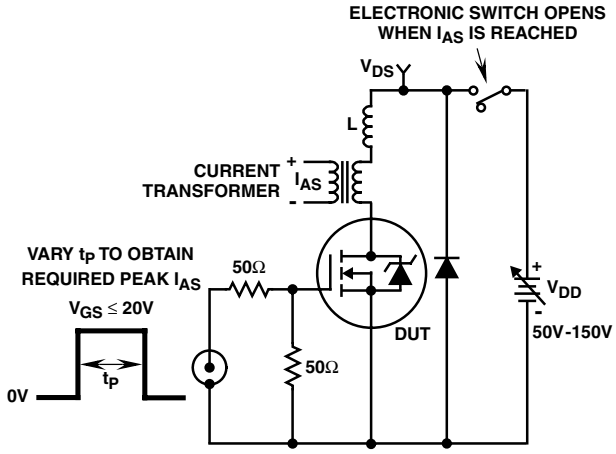


FIGURE 2. UNCLAMPED ENERGY TEST CIRCUIT

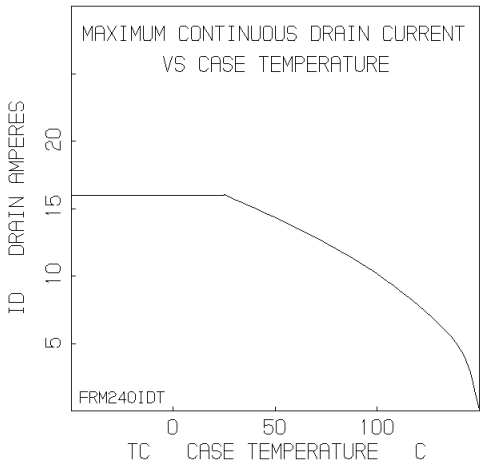
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

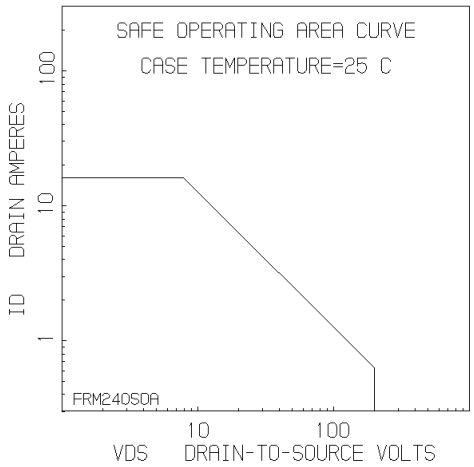
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS		UNITS
					MIN	MAX	
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	FRM240D, R	VGS = 0, ID = 1mA	200	-	V
	(Note 5, 6)	BVDSS	FRM240H	VGS = 0, ID = 1mA	190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	FRM240D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	FRM240H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	FRM240D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	FRM240H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	FRM240D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	FRM240H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	FRM240D, R	VGS = 0, VDS = 160V	-	25	μA
	(Note 5, 6)	IDSS	FRM240H	VGS = 0, VDS = 160V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	FRM240D, R	VGS = 10V, ID = 16A	-	4.03	V
	(Note 1, 5, 6)	VDS(on)	FRM240H	VGS = 16V, ID = 16A	-	6.05	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	FRM240D, R	VGS = 10V, ID = 10A	-	0.240	Ω
	(Note 1, 5, 6)	RDS(on)	FRM240H	VGS = 14V, ID = 10A	-	0.360	Ω

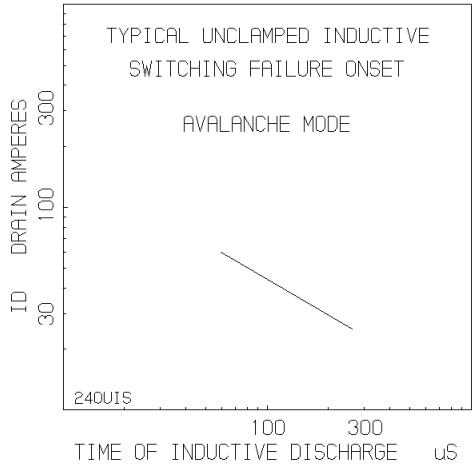
NOTES:

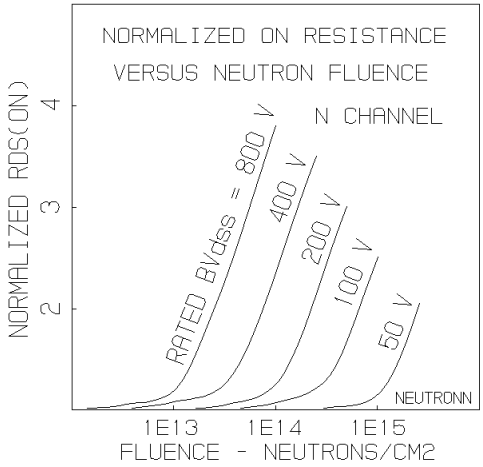
1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for “D”, 100KRAD(Si) for “R”. Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 7/9/90 on TA 17642 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, Intersil Application note AN-8831, Oct. 1988

Typical Performance Characteristics

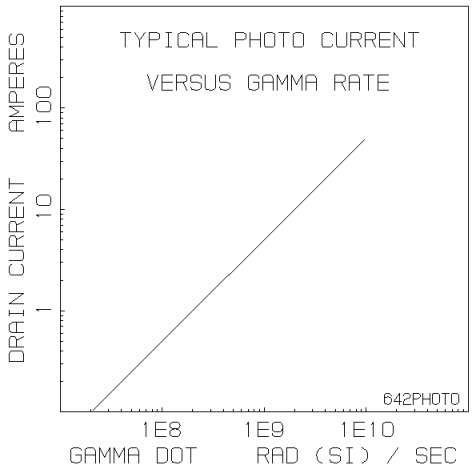


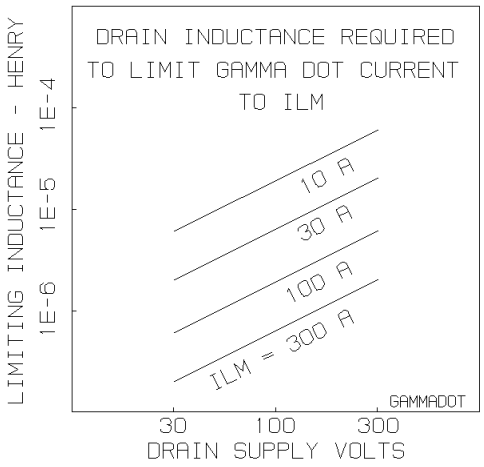






Typical Performance Characteristics (Continued)





Rad Hard Data Packages - Intersil Power Transistors

TXV Equivalent

1. Rad Hard TXV Equivalent - Standard Data Package

A. Certificate of Compliance

B. Assembly Flow Chart

C. Preconditioning - Attributes Data Sheet

D. Group A - Attributes Data Sheet

E. Group B - Attributes Data Sheet

F. Group C - Attributes Data Sheet

G. Group D - Attributes Data Sheet

2. Rad Hard TXV Equivalent - Optional Data Package

A. Certificate of Compliance

B. Assembly Flow Chart

C. Preconditioning
- Attributes Data Sheet
- Precondition Lot Traveler
- Pre and Post Burn-In Read and Record Data

D. Group A
- Attributes Data Sheet
- Group A Lot Traveler

E. Group B
- Attributes Data Sheet
- Group B Lot Traveler
- Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup B3)
- Bond Strength Data (Subgroup B3)
- Pre and Post High Temperature Operating Life Read and Record Data (Subgroup B6)

F. Group C
- Attributes Data Sheet
- Group C Lot Traveler
- Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup C6)
- Bond Strength Data (Subgroup C6)

G. Group D
- Attributes Data Sheet
- Group D Lot Traveler
- Pre and Post RAD Read and Record Data

Class S - Equivalents

1. Rad Hard "S" Equivalent - Standard Data Package

A. Certificate of Compliance

B. Serialization Records

C. Assembly Flow Chart

D. SEM Photos and Report

E. Preconditioning Attributes Data Sheet
Hi-Rel Lot Traveler
HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data

F. Group A - Attributes Data Sheet

G. Group B - Attributes Data Sheet

H. Group C - Attributes Data Sheet

I. Group D - Attributes Data Sheet

2. Rad Hard Max. "S" Equivalent - Optional Data Package

A. Certificate of Compliance

B. Serialization Records

C. Assembly Flow Chart

D. SEM Photos and Report

E. Preconditioning
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
- HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
- X-Ray and X-Ray Report

F. Group A
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- Subgroups A2, A3, A4, A5 and A7 Data

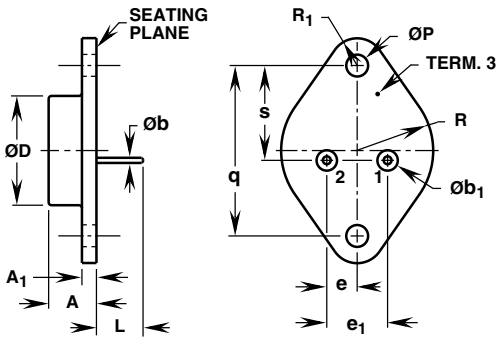
G. Group B
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- Subgroups B1, B3, B4, B5 and B6 Data

H. Group C
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- Subgroups C1, C2, C3 and C6 Data

I. Group D
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- Pre and Post Radiation Data

TO-204AA

JEDEC TO-204AA HERMETIC STEEL PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.310	0.330	7.88	8.38	-
A_1	0.060	0.065	1.53	1.65	-
Øb	0.038	0.042	0.97	1.06	2, 3
$Øb_1$	0.138	0.145	3.51	3.68	-
ØD	-	0.800	-	20.32	-
e	0.215 TYP		5.46 TYP		4
e_1	0.430 BSC		10.92 BSC		4
L	0.430	-	10.93	-	-
ØP	0.155	0.160	3.94	4.06	-
q	1.187 BSC		30.15 BSC		-
R	0.495	0.525	12.58	13.33	-
R_1	0.131	0.185	3.33	4.69	-
s	0.655	0.675	16.64	17.14	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-204AA outline dated 11-82.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of seating plane.
5. Controlling dimension: Inch.
6. Revision 2 dated 6-93.

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EnSigna™	MICROWIRE™	SMART START™	
FACT™	OPTOLOGIC™	Star* Power™	
FACT Quiet Series™	OPTOPLANAR™	Stealth™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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