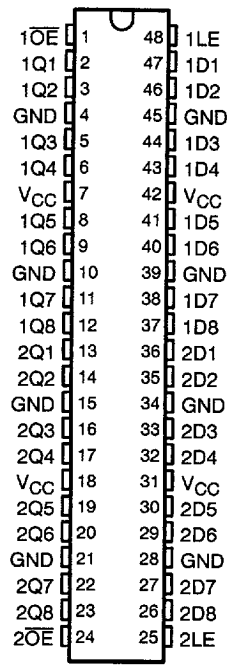
- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16373 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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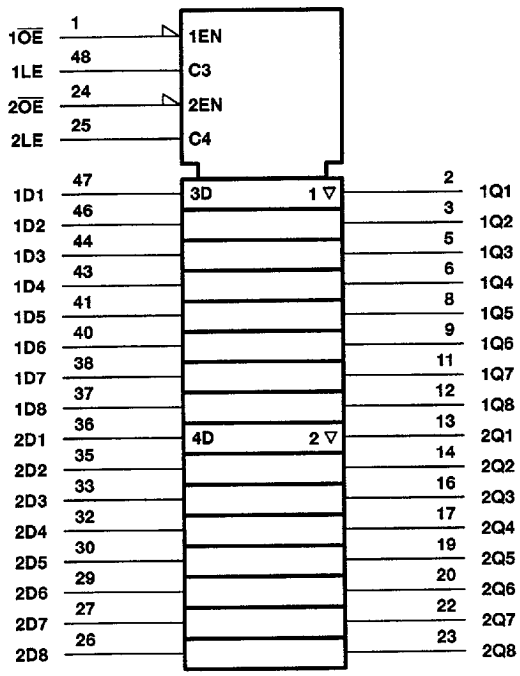
FUNCTION TABLE
(each 8-bit section)

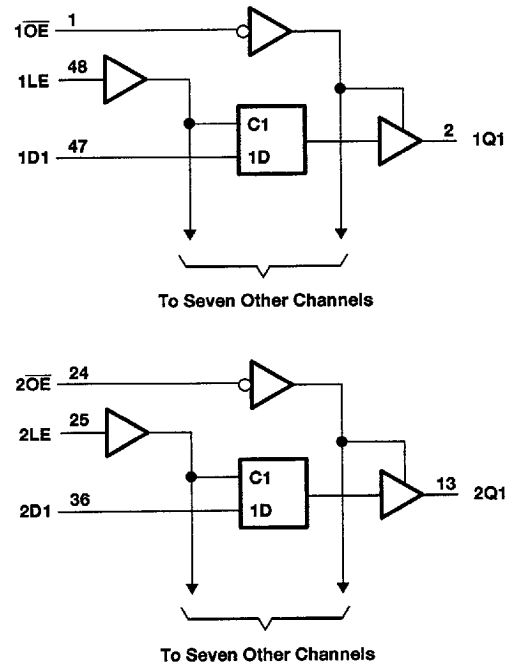
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = −12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = −24 mA		3 V	2		
V_{OL}	I_{OL} = 100 μA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	V_I = V_{CC} or GND		3.6 V		±5	μA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75		μA
	V_I = 2 V			−75		
I_{OZ}	V_O = V_{CC} or GND		3.6 V		±10	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			750	μA
C_i	V_I = V_{CC} or GND		3.3 V			pF
C_o	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

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