



FSA2271T

Low-Voltage, Dual-SPDT (0.4Ω) Analog Switch with Negative Swing Audio Capability

Features

- 0.4Ω Typical On Resistance for +3.0V Supply
- 0.25Ω Maximum R_{ON} Flatness for +3.0V Supply
- -3db Bandwidth: > 50MHz
- Low I_{CCT} Current Over Expanded Control Input Range
- Packaged in 10-Lead UMLP
- Power-off Protection on Common Ports
- Broad V_{CC} Operating Range: 1.65 to 4.3V
- Noise Immunity Termination Resistors
- ESD JEDEC: JESD22-A114 Human Body Model:
 - Power to GND: 16kV
 - I/O to GND: 10kV
 - All other Pins: 7kV
- ESD JEDEC: JESD22-A101 Charged Device Model:
 - CDM: 2kV

Applications

- Cell phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

Description

The FSA2271T is a high-performance, dual - single pole double throw (SPDT) analog switch with negative swing audio capability. It features ultra-low R_{ON} of 0.4Ω (typical) at 3.0V V_{CC} . The FSA2271T operates over a wide V_{CC} range of 1.65V to 4.3V and is fabricated with sub-micron CMOS technology to achieve fast switching speeds. Designed for break-before-make operation, the FSA2271T select input is TTL level compatible.


The FSA2271T features very low quiescent current, even when the control voltage is lower than the V_{CC} supply. This feature is optimized for the mobile handset applications, allowing direct interface with baseband processor general-purpose I/Os with minimal battery consumption.

The FSA2271T includes termination resistors that improve noise immunity during overshoot excursions, “pop-minimization,” or off-isolation coupling.

IMPORTANT NOTE:

For additional information, please contact analogswitch@fairchildsemi.com.

Ordering Information

Part Number	Termination Resistors	Operating Temperature Range	 Eco Status	Package
FSA2271TUMX	Yes	-40°C to 85°C	Green	10-Lead Quad Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8mm, 0.4mm pitch

 For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Analog Symbol

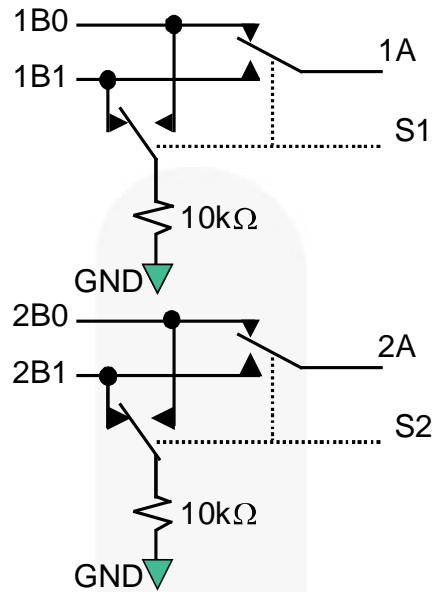


Figure 1. FSA2271T

Pin Configuration

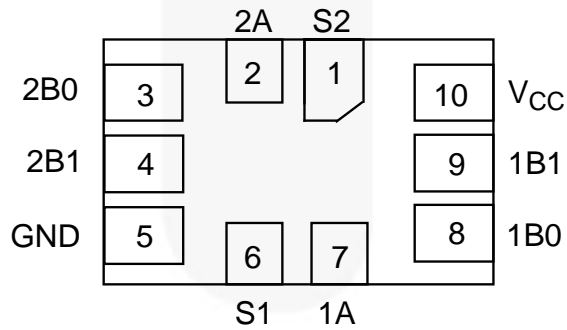


Figure 2. Pin Configuration

Pin Definitions

Pin#	Name	Description
1, 6	S2, S1	Switch Select Pins
2, 7	2A, 1A	Data Points
3, 8	2B0, 1B0	Data Points
4, 9	2B1, 1B1	Data Ports
5	GND	Ground
10	V _{CC}	Supply Voltage Data Ports

Truth Table

Control Input, S _n	Function
LOW Logic Level	nB0 connected to nA; nB1 terminated to GND
HIGH Logic Level	nB1 connected to nA; nB0 terminated to GND

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage		-0.5	5.5	V
V_{SW}	Switch Voltage ⁽¹⁾	1B0, 1B1, 2B0, 2B1, 1A, 2A Pins	$V_{CC} - 4.3V$	$V_{CC} + 0.3V$	V
V_{CNTRL}	Control Input Voltage ⁽¹⁾	S1, S2	-0.5	$V_{CC} + 0.3V$	V
I_{IK}	Input Clamp Diode Current			-50	mA
I_{SW}	Switch I/O Current	Continuous		350	mA
I_{SWPEAK}	Peak Switch Current	Pulsed at 1ms Duration, <10% Duty Cycle		500	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature	Soldering 10 seconds		+260	°C
ESD	Human Body Model, JEDEC: JESD22-A114	I/O to GND	10		kV
		All Other Pins	7		
		Power to GND	16		
	Charged Device Model, JEDEC-JESD-C101		2		

Note:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.65	4.30	V
$V_{S1,S2}$	Control Input Voltage	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	$V_{CC} - 4.3$	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C

DC Electrical Characteristics

All typical values are for $V_{CC}=3.3V$ at $25^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A=+25^{\circ}C$			$T_A=-40$ to $+85^{\circ}C$		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	Input Voltage High		3.60 to 4.30				1.7		V
			2.70 to 3.60				1.5		
			2.30 to 2.70				1.4		
			1.65 to 1.95				0.9		
V_{IL}	Input Voltage Low		3.60 to 4.30					0.7	V
			2.70 to 3.60					0.5	V
			2.30 to 2.70					0.4	
			1.65 to 1.95					0.4	
I_{IN}	Control Input Leakage (S1,S2)	$V_{IN}=0$ to V_{CC}	1.65 to 4.30				-0.5	0.5	μA
$I_{A(ON)}$	On Leakage Current of Port nA	nA=0.3V, $V_{CC}=0.3V$; nB0 or nB1 (on)=nA or Floating; nB0 or nB1 (off)=0V or floating Figure 5	1.95 to 4.30				-1	1	μA
I_{OFF}	Power Off Leakage Current (Common Port Only 1A, 2A)	Common Port (1A, 2A); $V_{IN}=0V$ to $4.3V$, $V_{CC}=0V$; nB0, nB1=0V or Floating	0					± 45	μA
R_{ON}	Switch On Resistance ⁽²⁾	$I_{ON}=100mA$, nB0 or nB1=0V, 0.7V, 3.6V, 4.3V Figure 3	4.30		0.3				Ω
		$I_{ON}=100mA$, nB0 or nB1=0V, 0.7V, 2.3V, 3.0V Figure 3	3.00		0.4			0.8	
		$I_{ON}=100mA$, nB0 or nB1=0V, 0.7V, 1.6V, 2.3V Figure 3	2.30		0.52				
		$I_{ON}=100mA$, nB0 or nB1=0V, 0.7V, 1.65V Figure 3	1.65		1.00				
ΔR_{ON}	On Resistance Matching Between Channels ⁽³⁾	$I_{ON}=100mA$, nB0 or nB1=0.7V	4.30		0.04			0.13	Ω
			3.00		0.06			0.13	
			2.30		0.12				
			1.65		1.00				
$R_{FLAT(ON)}$	On Resistance Flatness ⁽⁴⁾	$I_{OUT}=100mA$, nB0 or nB1=0V to V_{CC}	4.30					0.25	Ω
			3.00					0.25	
			2.30		0.5				
			1.65		0.6				
R_{TERM}	Internal Termination Resistors ⁽⁵⁾				10				k Ω
I_{CC}	Quiescent Supply Current	$V_{IN}=0$ or V_{CC} , $I_{OUT}=0$	4.30	-100		100	-500	500	nA
I_{CCT}	Increase in I_{CC} per Input	Input at 2.6V	4.30		3.0			10.0	μA
		Input at 1.8V			7.0			15.0	

Notes:

- On resistance is determined by the voltage drop between the A and B pins at the indicated current through the switch.
- $\Delta R_{ON}=R_{ON\ max}-R_{ON\ min}$ measured at identical V_{CC} , temperature, and voltage.
- Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
- Guaranteed by characterization, not production tested.

AC Electrical Characteristics

All typical value are for $V_{CC}=3.3V$ at $25^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A=+25^{\circ}C$			$T_A=-40^{\circ}C$ to $+85^{\circ}C$		Units
				Min.	Typ.	Max.	Min.	Max.	
t_{ON}	Turn-On Time	nB0 or nB1=1.5V; $R_L=50\Omega$, $C_L=35pF$ Figure 4, Figure 10	3.60 to 4.30			60	15	65	ns
			2.70 to 3.60			65	15	70	
			2.30 to 2.70			80	15	85	
			1.65 to 1.95		100				
t_{OFF}	Turn-Off Time	nB0 or nB1=1.5V; $R_L=50\Omega$, $C_L=35pF$ Figure 4, Figure 10	3.60 to 4.30			55	5	60	ns
			2.70 to 3.60			60	5	65	
			2.30 to 2.70			65	5	70	
			1.65 to 1.95		65				
t_{BBM}	Break-Before-Make Time	nB0 or nB1=1.5V; $R_L=50\Omega$, $C_L=35pF$ Figure 11	3.60 to 4.30		3		1		ns
			2.70 to 3.60		5		2		
			2.30 to 2.70		10		2		
			1.65 to 1.95		15		2		
Q	Charge Injection	$C_L=1.0nF$, $V_S=0V$; $R_S=0\Omega$ Figure 14	1.65 to 4.30		25				pC
OIRR	Off Isolation	$f=100kHz$, $R_L=50\Omega$, $C_L=0pF$ Figure 12	1.65 to 4.30		-70				dB
Xtalk	Crosstalk	$f=100kHz$, $R_L=50\Omega$; $C_L=0pF$ Figure 13	1.65 to 4.30		-70				dB
BW	-3db Bandwidth	$R_L=50\Omega$; $C_L=0pF$ Figure 9	1.65 to 4.30		>50				MHz
THD	Total Harmonic Distortion	$R_L=32\Omega$, $V_{SW}=2V_{PP}$, $f=20Hz$ to 20kHz, $V_{BIAS}=0V$ Figure 15	1.65 to 4.30		.06				%

Capacitance

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A=+25^{\circ}C$			$T_A=-40^{\circ}C$ to $+85^{\circ}C$		Units
				Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Control Pin Input Capacitance	$f=1MHz$ Figure 7	0		2.5				pF
C_{OFF}	B port Off Capacitance	$f=1MHz$ Figure 7	3.3		30				pF
C_{ON}	A port On Capacitance	$f=1MHz$ Figure 8	3.3		120				pF

Test Diagrams

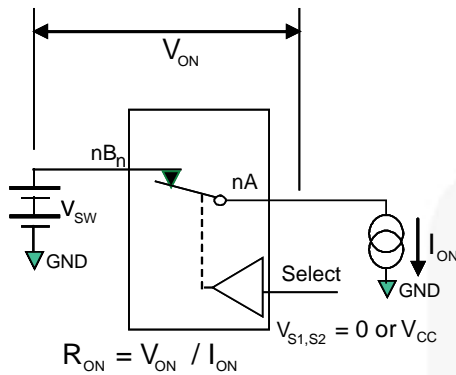


Figure 3. On Resistance

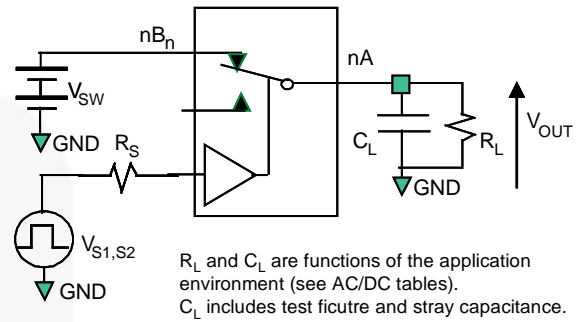


Figure 4. Test Circuit Load

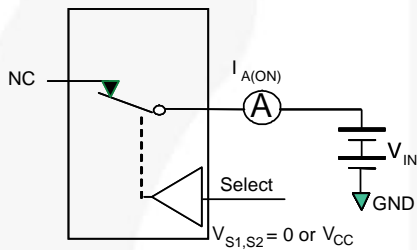
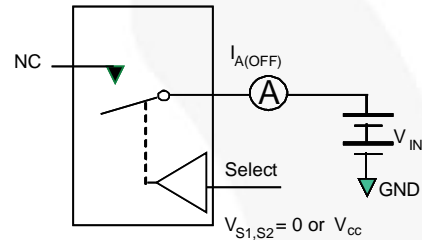


Figure 5. On Leakage



Each switch port is tested separately.

Figure 6. Off Leakage (Each Port Tested Separately)

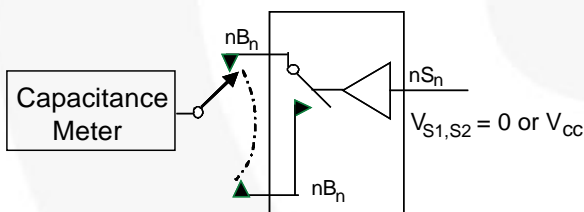


Figure 7. Off Capacitance

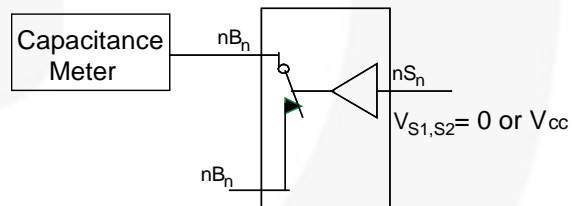


Figure 8. On Capacitance

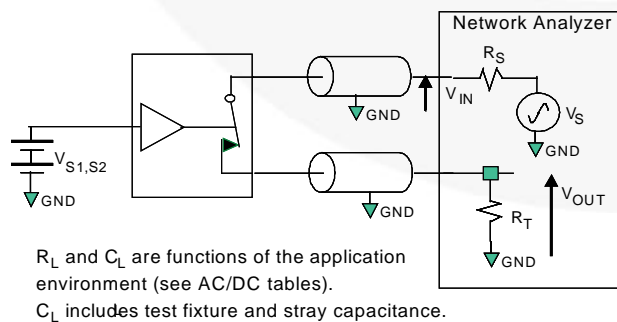


Figure 9. Bandwidth

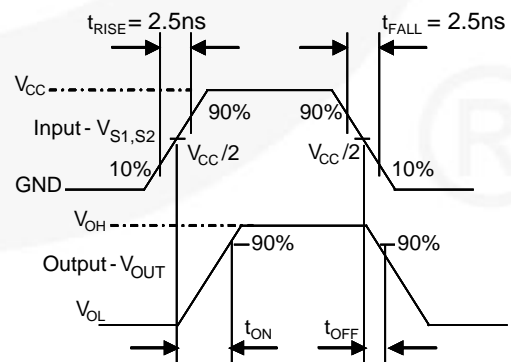


Figure 10. Turn-On / Turn-Off Waveforms

Test Diagrams (Continued)

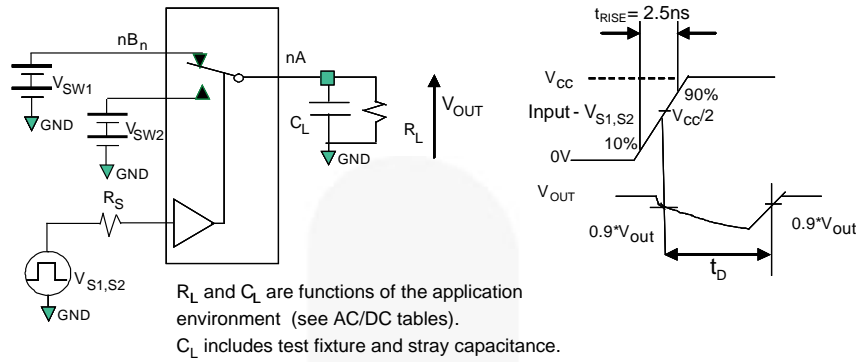


Figure 11. Break-Before-Make Timing

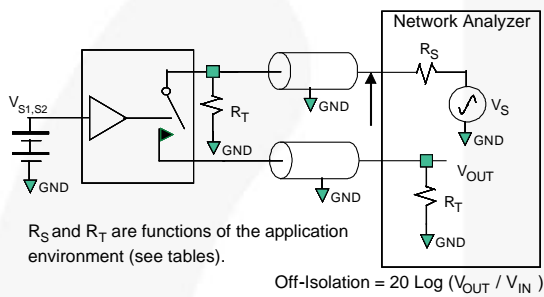


Figure 12. Channel Off Isolation

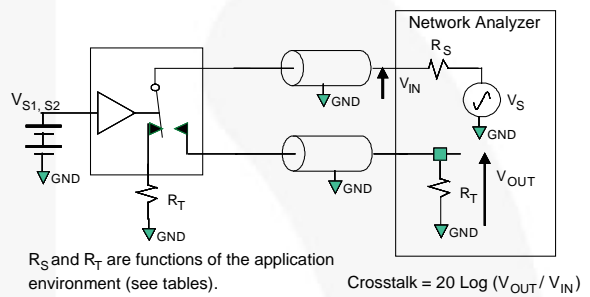


Figure 13. Adjacent Channel Crosstalk

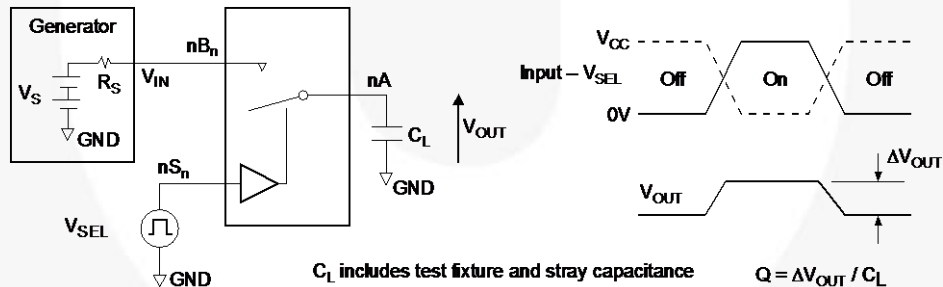


Figure 14. Charge Injection Test

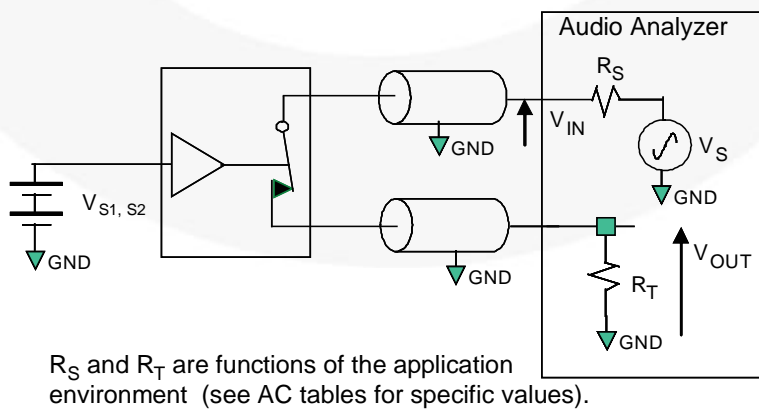
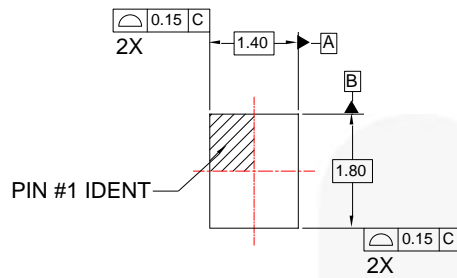
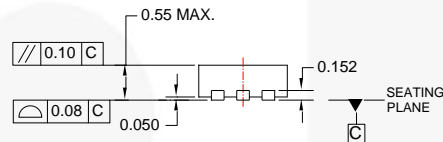


Figure 15. Total Harmonic Distortion

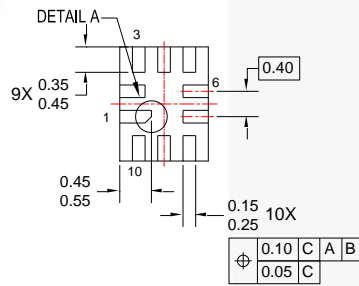
Physical Dimensions



TOP VIEW



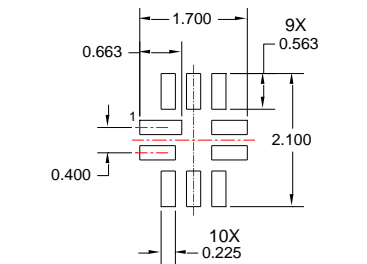
SIDE VIEW



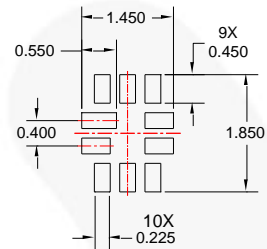
BOTTOM VIEW

NOTES:

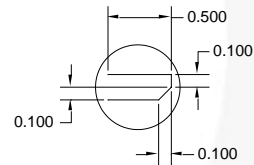
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- B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- C. DRAWING FILENAME: UMLP10Arev2



RECOMMENDED LAND PATTERN



OPTIONAL MINIMAL TOE LAND PATTERN



DETAIL A
PIN #1 TERMINAL
SCALE: 2X

Figure 16. 10-Lead, Quad Ultrathin Molded Leadless Package (UMLP)

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