

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

DESCRIPTION

The M35074-XXXSP is a character pattern display control IC can display on the digital camera, the digital video, the digital television, the CRT display, the liquid crystal display and the plasma display.

A character color and a character background color can be chosen from 128 kinds of colors per character.

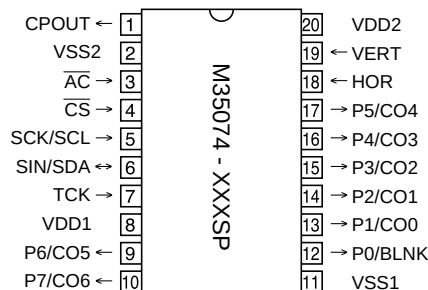
It uses a silicon gate CMOS process and it housed in a 20-pin shrink DIP package (M35074-XXXSP).

For M35074-002SP that is a standard ROM version of M35074-XXXSP respectively, the character pattern is also mentioned.

FEATURES

- Screen composition 24 characters X 12 lines
- Number of characters displayed 288 (Max.)
- Character composition 12 X 18 dot matrix
- Characters available ROM character:511 characters
- Character sizes available 4 (vertical) X 4 (horizontal)
- Display locations available
 - Horizontal direction 4055 locations
 - Vertical direction 2047 locations
- Data input By 24-bit serial input function
..... By the I²C-BUS serial input function (At only V_{DD} = 5V)
- Coloring for character
 - Character color 128 colors (Character unit)
 - Background coloring 128 colors (Character unit)
 - Border (shadow) coloring 128 colors (unit of screen / character unit)
 - Raster coloring 128 colors (unit of screen)
- Blanking for character
 - Character size blanking
 - Border size blanking
 - Matrix-outline blanking
 - All blanking (all raster area)
- Output ports
 - 8 shared output ports (toggled between CO0-CO6 and BLNK output)
- Display oscillation stop function
<At V_{DD} = 5V>
- Display input frequency range
 - External clock mode 1 Fosc = 6.3 MHz to 80 MHz
 - External clock mode 2 Fosc = 20 MHz to 120 MHz
 - Internal clock mode Fosc = 20 MHz to 120 MHz
- Horizontal synchronous input frequency range
..... H.sync = 15 kHz to 130 kHz
<At V_{DD} = 3.3V>
- Display input frequency range
 - External clock mode 1 Fosc = 6.3 MHz to 40 MHz
- Horizontal synchronous input frequency range
..... H.sync = 15 kHz to 60 kHz

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B

APPLICATION

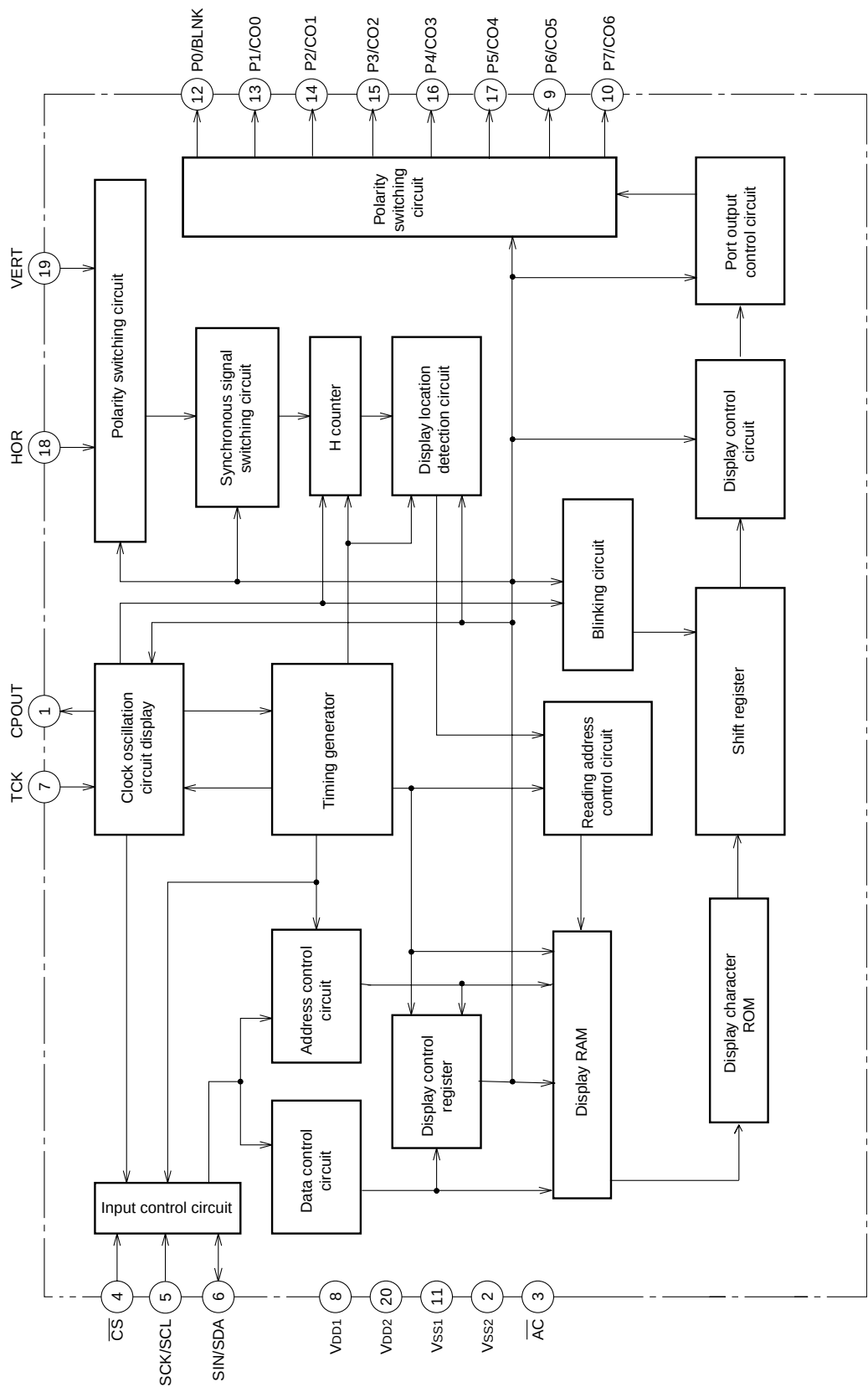
Digital camera, Digital video, Digital television, CRT display, Liquid crystal display, Plasma display

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

PIN DESCRIPTION

Symbol	Pin name	Input/ Output	Function
CPOUT	Filter output	Output	Filter output. Connect loop filter to this pin.
Vss2	Earthing pin	–	Connect to GND.
$\overline{AC}$	Auto-clear input	Input	When "L", this pin resets the internal IC circuit. Hysteresis input. Built-in pull-up resistor.
$\overline{CS}$	Chip select input	Input	<At 24-bit serial communication> This is the pin for chip select. Set to "L" level at serial data transmission. Hysteresis input. Built-in pull-up resistor. ----- <At I²C-BUS communication> Connect to "H."
SCK/SCL	Clock input	Input	<At 24-bit serial communication> SIN pin serial data is taken in when SCK rises at $\overline{CS}$ pin "L" level. Hysteresis input. ----- <At I²C-BUS communication> SDA pin serial data is taken in when SCL rises.
SIN/SDA	Data I/O	Input I/O	<At 24-bit serial communication> This is the pin for serial input of display control register and display RAM data. Hysteresis input. ----- <At I²C-BUS communication> Hysteresis input. This is the pin for serial input of display control register and display RAM data. Also, this pin output acknowledge signal.
TCK	External clock input	Input	This is the pin for external clock input.
VDD1	Power pin	–	Digital power pin. Connect to +5V with the power pin.
P6/CO5	Port P6 output	Output	This pin can be toggled between port pin output and CO5 signal pin.
P7/CO6	Port P7 output	Output	This pin can be toggled between port pin output and CO6 signal pin.
Vss1	Earthing pin	–	Connect to GND using circuit earthing pin.
P0/BLNK	Port P0 output	Output	This pin can be toggled between port pin output and BLNK signal output.
P1/CO0	Port P1 output	Output	This pin can be toggled between port pin output and CO0 signal output.
P2/CO1	Port P2 output	Output	This pin can be toggled between port pin output and CO1 signal output.
P3/CO2	Port P3 output	Output	This pin can be toggled between port pin output and CO2 signal output.
P4/CO3	Port P4 output	Output	This pin can be toggled between port pin output and CO3 signal output.
P5/CO4	Port P5 output	Output	This pin can be toggled between port pin output and CO4 signal output.
HOR	Horizontal synchronous signal input	Input	This pin inputs the horizontal synchronous signal. Hysteresis input.
VERT	Vertical synchronous signal input	Input	This pin inputs the vertical synchronous signal. Hysteresis input.
VDD2	Power pin	–	Analog power pin. Connect to +5V with the power pin.

BLOCK DIAGRAM



SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

MEMORY CONSTITUTION

INPUT EXAMPLE". Memory constitution is shown in Figure 1.

Address 000₁₆ to 11F₁₆ are assigned to the display RAM, address 120₁₆ to 128₁₆ are assigned to the display control registers. The internal circuit is reset and all display control registers (address 120₁₆ to 128₁₆) are set to "0" when the AC pin level is "L". And then, RAM is not erased and be undefined. For detail, see "DATA

Address	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	
000 ₁₆	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	CC6	CC5	CC4	CC3	CC2	CC1	CC0	C8	C7	C6	C5	C4	C3	C2	C1	C0	
001 ₁₆	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	CC6	CC5	CC4	CC3	CC2	CC1	CC0	C8	C7	C6	C5	C4	C3	C2	C1	C0	
⋮	⋮	Background color							Character color							Character code									
11E ₁₆	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	CC6	CC5	CC4	CC3	CC2	CC1	CC0	C8	C7	C6	C5	C4	C3	C2	C1	C0	
11F ₁₆	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	CC6	CC5	CC4	CC3	CC2	CC1	CC0	C8	C7	C6	C5	C4	C3	C2	C1	C0	
120 ₁₆	—	—	—	—	EXCK1	EXCK0	RSEL1	RSEL0	TEST24	DIVS2	DIVS1	DIVS0	DIV11	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	
121 ₁₆	—	—	—	—	—	—	TEST12	TEST11	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0	PTC7	PTC6	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0	
122 ₁₆	—	VP10	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	HP11	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	
123 ₁₆	—	—	—	SYAD	BEAT14	—	TEST19	—	—	BLK1	BLK0	BCOL	DSP11	DSP10	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0	
124 ₁₆	—	—	—	—	—	—	—	—	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2	
125 ₁₆	—	—	—	—	HSZ21	HSZ20	HSZ11	HSZ10	—	—	VSZ2H1	VSZ2H0	VSZ2L1	VSZ2L0	V18SZ1	V18SZ0	—	—	VSZ1H1	VSZ1H0	VS1L1Z	VSZ1L0	V1SZ1	V1SZ0	
126 ₁₆	—	—	—	—	—	—	—	—	—	FC6	FC5	FC4	FC3	FC2	FC1	FC0	—	RC6	RC5	RC4	RC3	RC2	RC1	RC0	
127 ₁₆	—	—	—	—	—	—	—	—	—	SPACE2	SPACE1	SPACE0	RAMERS	DSPON	TEST30	TEST17	TEST16	TEST15	TEST14	TEST13	POLH	POLV	VMASK	B/F	
128 ₁₆	—	—	—	—	—	—	—	—	—	—	—	—	TEST20	TEST29	TEST22	TEST21	TEST28	TEST27	TEST26	TEST10	TEST3	TEST2	TEST1	TEST0	

Fig.1 Memory constitution (Display RAM, Display Control register)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM . The screen constitution is shown in Figure 2.

Row Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	000 ₁₆	001 ₁₆	002 ₁₆	003 ₁₆	004 ₁₆	005 ₁₆	006 ₁₆	007 ₁₆	008 ₁₆	009 ₁₆	00A ₁₆	00B ₁₆	00C ₁₆	00D ₁₆	00E ₁₆	00F ₁₆	010 ₁₆	011 ₁₆	012 ₁₆	013 ₁₆	014 ₁₆	015 ₁₆	016 ₁₆	017 ₁₆
2	018 ₁₆	019 ₁₆	01A ₁₆	01B ₁₆	01C ₁₆	01D ₁₆	01E ₁₆	01F ₁₆	020 ₁₆	021 ₁₆	022 ₁₆	023 ₁₆	024 ₁₆	025 ₁₆	026 ₁₆	027 ₁₆	028 ₁₆	029 ₁₆	02A ₁₆	02B ₁₆	02C ₁₆	02D ₁₆	02E ₁₆	02F ₁₆
3	030 ₁₆	031 ₁₆	032 ₁₆	033 ₁₆	034 ₁₆	035 ₁₆	036 ₁₆	037 ₁₆	038 ₁₆	039 ₁₆	03A ₁₆	03B ₁₆	03C ₁₆	03D ₁₆	03E ₁₆	03F ₁₆	040 ₁₆	041 ₁₆	042 ₁₆	043 ₁₆	044 ₁₆	045 ₁₆	046 ₁₆	047 ₁₆
4	048 ₁₆	049 ₁₆	04A ₁₆	04B ₁₆	04C ₁₆	04D ₁₆	04E ₁₆	04F ₁₆	050 ₁₆	051 ₁₆	052 ₁₆	053 ₁₆	054 ₁₆	055 ₁₆	056 ₁₆	057 ₁₆	058 ₁₆	059 ₁₆	05A ₁₆	05B ₁₆	05C ₁₆	05D ₁₆	05E ₁₆	05F ₁₆
5	060 ₁₆	061 ₁₆	062 ₁₆	063 ₁₆	064 ₁₆	065 ₁₆	066 ₁₆	067 ₁₆	068 ₁₆	069 ₁₆	06A ₁₆	06B ₁₆	06C ₁₆	06D ₁₆	06E ₁₆	06F ₁₆	070 ₁₆	071 ₁₆	072 ₁₆	073 ₁₆	074 ₁₆	075 ₁₆	076 ₁₆	077 ₁₆
6	078 ₁₆	079 ₁₆	07A ₁₆	07B ₁₆	07C ₁₆	07D ₁₆	07E ₁₆	07F ₁₆	080 ₁₆	081 ₁₆	082 ₁₆	083 ₁₆	084 ₁₆	085 ₁₆	086 ₁₆	087 ₁₆	088 ₁₆	089 ₁₆	08A ₁₆	08B ₁₆	08C ₁₆	08D ₁₆	08E ₁₆	08F ₁₆
7	090 ₁₆	091 ₁₆	092 ₁₆	093 ₁₆	094 ₁₆	095 ₁₆	096 ₁₆	097 ₁₆	098 ₁₆	099 ₁₆	09A ₁₆	09B ₁₆	09C ₁₆	09D ₁₆	09E ₁₆	09F ₁₆	0A0 ₁₆	0A1 ₁₆	0A2 ₁₆	0A3 ₁₆	0A4 ₁₆	0A5 ₁₆	0A6 ₁₆	0A7 ₁₆
8	0A8 ₁₆	0A9 ₁₆	0AA ₁₆	0AB ₁₆	0AC ₁₆	0AD ₁₆	0AE ₁₆	0AF ₁₆	0B0 ₁₆	0B1 ₁₆	0B2 ₁₆	0B3 ₁₆	0B4 ₁₆	0B5 ₁₆	0B6 ₁₆	0B7 ₁₆	0B8 ₁₆	0B9 ₁₆	0BA ₁₆	0BB ₁₆	0BC ₁₆	0BD ₁₆	0BE ₁₆	0BF ₁₆
9	0C0 ₁₆	0C1 ₁₆	0C2 ₁₆	0C3 ₁₆	0C4 ₁₆	0C5 ₁₆	0C6 ₁₆	0C7 ₁₆	0C8 ₁₆	0C9 ₁₆	0CA ₁₆	0CB ₁₆	0CC ₁₆	0CD ₁₆	0CE ₁₆	0CF ₁₆	0D0 ₁₆	0D1 ₁₆	0D2 ₁₆	0D3 ₁₆	0D4 ₁₆	0D5 ₁₆	0D6 ₁₆	0D7 ₁₆
10	0D8 ₁₆	0D9 ₁₆	0DA ₁₆	0DB ₁₆	0DC ₁₆	0DD ₁₆	0DE ₁₆	0DF ₁₆	0E0 ₁₆	0E1 ₁₆	0E2 ₁₆	0E3 ₁₆	0E4 ₁₆	0E5 ₁₆	0E6 ₁₆	0E7 ₁₆	0E8 ₁₆	0E9 ₁₆	0EA ₁₆	0EB ₁₆	0EC ₁₆	0ED ₁₆	0EE ₁₆	0EF ₁₆
11	0F0 ₁₆	0F1 ₁₆	0F2 ₁₆	0F3 ₁₆	0F4 ₁₆	0F5 ₁₆	0F6 ₁₆	0F7 ₁₆	0F8 ₁₆	0F9 ₁₆	0FA ₁₆	0FB ₁₆	0FC ₁₆	0FD ₁₆	0FE ₁₆	0FF ₁₆	100 ₁₆	101 ₁₆	102 ₁₆	103 ₁₆	104 ₁₆	105 ₁₆	106 ₁₆	107 ₁₆
12	108 ₁₆	109 ₁₆	10A ₁₆	10B ₁₆	10C ₁₆	10D ₁₆	10E ₁₆	10F ₁₆	110 ₁₆	111 ₁₆	112 ₁₆	113 ₁₆	114 ₁₆	115 ₁₆	116 ₁₆	117 ₁₆	118 ₁₆	119 ₁₆	11A ₁₆	11B ₁₆	11C ₁₆	11D ₁₆	11E ₁₆	11F ₁₆

* The hexadecimal numbers in the boxes show the display RAM address.

Fig. 2 Screen constitution

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DISPLAY RAM

Address 000₁₆ to 11F₁₆

DA	Register	Contents		Remarks		
		Status	Function			
0	C0	0 1	Sets the displayed ROM character code. Select from 0000000002–1111111112 (512 types) and set up a character code.	Display character setting		
1	C1	0 1				
2	C2	0 1				
3	C3	0 1				
4	C4	0 1				
5	C5	0 1				
6	C6	0 1				
7	C7	0 1				
8	C8	0 1				
9	CC0	0 1			128 kinds of colors are set up by CC0–CC6. CC0–CC6 correspond to P1/CO0–P7/CO6 output, respectively.	Character color (character unit) setting
A	CC1	0 1				
B	CC2	0 1				
C	CC3	0 1				
D	CC4	0 1				
E	CC5	0 1				
F	CC6	0 1				
10	BC0	0 1	128 kinds of colors are set up by BC0–BC6 BC0–BC6 correspond to P1/CO0–P7/CO6 output, respectively.	Character background color (character unit) setting		
11	BC1	0 1				
12	BC2	0 1				
13	BC3	0 1				
14	BC4	0 1				
15	BC5	0 1				
16	BC6	0 1				
17	–	0 1			Fix to "0". Can not be used.	

Note: The display RAM is undefined state at the $\overline{AC}$ pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

REGISTERS DESCRIPTION

(1) Address 120₁₆

DA	Register	Contents		Remarks															
		Status	Function																
0	DIV0	① 1	Sets division value (multiply value) of horizontal oscillation frequency. $N1 = \sum_{n=0}^{11} (DIV_n \times 2^n)$ N1 : division value (multiply value)	Sets display frequency by division value (multiply value) setting. For detail, see "REGISTER SUPPLEMENTARY DESCRIPTION (1)". Also, set the display frequency range by registers DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1(address 120 ₁₆) in accordance with the display frequency. Any of this settings above is required only when EXCK1 = 0, EXCK0 = 1 and EXCK1 = 1, EXCK0 = 1.															
1	DIV1	① 1																	
2	DIV2	① 1																	
3	DIV3	① 1																	
4	DIV4	① 1																	
5	DIV5	① 1																	
6	DIV6	① 1																	
7	DIV7	① 1																	
8	DIV8	① 1																	
9	DIV9	① 1																	
A	DIV10	① 1																	
B	DIV11	① 1																	
C	DIVS0	① 1	For setting, see "REGISTER SUPPLEMENTARY DESCRIPTION (2)".	Sets display frequency range.															
D	DIVS1	① 1																	
E	DIVS2	① 1																	
F	TEST24	① 1	Fix to "0". Can not be used.																
10	RSEL0	① 1	For setting, see "REGISTER SUPPLEMENTARY DESCRIPTION (2)".	Sets display frequency range.															
11	RSEL1	① 1																	
12	EXCK0	① 1	<table><tr><td>EXCK1</td><td>EXCK0</td><td>Display clock input</td></tr><tr><td>0</td><td>0</td><td>External clock mode 1</td></tr><tr><td>0</td><td>1</td><td>Internal clock mode</td></tr><tr><td>1</td><td>0</td><td>Can not be used.</td></tr><tr><td>1</td><td>1</td><td>External clock mode 2</td></tr></table>	EXCK1	EXCK0	Display clock input	0	0	External clock mode 1	0	1	Internal clock mode	1	0	Can not be used.	1	1	External clock mode 2	Display clock setting See "REGISTER SUPPLEMENTARY DESCRIPTION (1)".
EXCK1	EXCK0	Display clock input																	
0	0	External clock mode 1																	
0	1	Internal clock mode																	
1	0	Can not be used.																	
1	1	External clock mode 2																	
13	EXCK1	① 1																	
14	—	① 1	Fix to "0". Can not be used.																
15	—	① 1	Fix to "0". Can not be used.																
16	—	① 1	Fix to "0". Can not be used.																
17	—	① 1	Fix to "0". Can not be used.																

Note: The mark ① around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

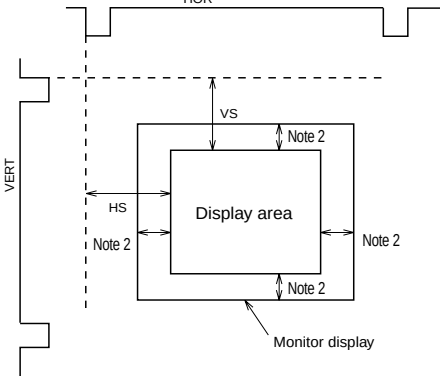
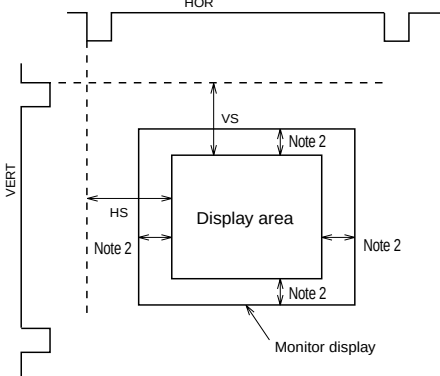
(2) Address 121₁₆

DA	Register	Contents		Remarks
		Status	Function	
0	PTC0	①	P0 output (port P0).	P0 pin output control.
		1	BLNK output	
1	PTC1	①	P1 output (port P1).	P1 pin output control.
		1	CO0 output	
2	PTC2	①	P2 output (port P2).	P2 pin output control.
		1	CO1 output	
3	PTC3	①	P3 output (port P3).	P3 pin output control.
		1	CO2 output	
4	PTC4	①	P4 output (port P4).	P4 pin output control.
		1	CO3 output	
5	PTC5	①	P5 output (port P5).	P5 pin output control.
		1	CO4 output	
6	PTC6	①	P6 output (port P6).	P6 pin output control.
		1	CO5 output	
7	PTC7	①	P7 output (port P7).	P7 pin output control.
		1	CO6 output	
8	PTD0	①	At the port output, it is "L" fixed. At the BLNK signal output, it is negative polarity.	P0 pin data control.
		1	At the port output, it is "L" fixed. At the BLNK signal output, it is negative polarity.	
9	PTD1	①	At the port output, it is "L" fixed. At the CO0 signal output, it is negative polarity.	P1 pin data control.
		1	At the port output, it is "L" fixed. At the CO0 signal output, it is negative polarity.	
A	PTD2	①	At the port output, it is "L" fixed. At the CO1 signal output, it is negative polarity.	P2 pin data control.
		1	At the port output, it is "L" fixed. At the CO1 signal output, it is negative polarity.	
B	PTD3	①	At the port output, it is "L" fixed. At the CO2 signal output, it is negative polarity.	P3 pin data control.
		1	At the port output, it is "L" fixed. At the CO2 signal output, it is negative polarity.	
C	PTD4	①	At the port output, it is "L" fixed. At the CO3 signal output, it is negative polarity.	P4 pin data control.
		1	At the port output, it is "L" fixed. At the CO3 signal output, it is negative polarity.	
D	PTD5	①	At the port output, it is "L" fixed. At the CO4 signal output, it is negative polarity.	P5 pin data control.
		1	At the port output, it is "L" fixed. At the CO4 signal output, it is negative polarity.	
E	PTD6	①	At the port output, it is "L" fixed. At the CO5 signal output, it is negative polarity.	P6 pin data control.
		1	At the port output, it is "L" fixed. At the CO5 signal output, it is negative polarity.	
F	PTD7	①	At the port output, it is "L" fixed. At the CO6 signal output, it is negative polarity.	P7 pin data control.
		1	At the port output, it is "L" fixed. At the CO6 signal output, it is negative polarity.	
10	TEST11	①	Set it as "0" at the time of the internal clock mode.	
		1	Set it as "0" at the time of the external clock mode1, 2.	
11	TEST12	①	Fix to "0".	
		1	Can not be used.	
12	-	①	Fix to "0".	
		1	Can not be used.	
13	-	①	Fix to "0".	
		1	Can not be used.	
14	-	①	Fix to "0".	
		1	Can not be used.	
15	-	①	Fix to "0".	
		1	Can not be used.	
16	-	①	Fix to "0".	
		1	Can not be used.	
17	-	①	Fix to "0".	
		1	Can not be used.	

Note: The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(3) Address 122₁₆

DA	Register	Contents		Remarks															
		Status	Function																
0	HP0	① 1	If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^{11} 2^n HPn + m \right)$ T: Period of display frequency 4055 settings are possible. m : offset value differ for the setting of the register EXCK0 and EXCK1. It shown below. <table><tr><td>EXCK1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>EXCK0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>m</td><td>13</td><td>13</td><td>Do not set</td><td>19</td></tr></table> 	EXCK1	0	0	1	1	EXCK0	0	1	0	1	m	13	13	Do not set	19	Horizontal display start location is specified using the 12 bits from HP11 to HP0. HP11 to HP0 = (000000000000₂) and (000000100111₂) setting is forbidden.
EXCK1	0	0		1	1														
EXCK0	0	1		0	1														
m	13	13		Do not set	19														
1	HP1	① 1																	
2	HP2	① 1																	
3	HP3	① 1																	
4	HP4	① 1																	
5	HP5	① 1																	
6	HP6	① 1																	
7	HP7	① 1																	
8	HP8	① 1																	
9	HP9	① 1																	
A	HP10	① 1																	
B	HP11	① 1																	
C	VP0	① 1	If VS is the vertical display start location, $VS = H \times \sum_{n=0}^{10} 2^n VPn$ H : Cycle with the horizontal synchronizing pulse 2047 settings are possible. 	The vertical start location is specified using the 11 bits from VP10 to VP0. VP10 to VP0 = (00000000000₂) setting is forbidden.															
D	VP1	① 1																	
E	VP2	① 1																	
F	VP3	① 1																	
10	VP4	① 1																	
11	VP5	① 1																	
12	VP6	① 1																	
13	VP7	① 1																	
14	VP8	① 1																	
15	VP9	① 1																	
16	VP10	① 1																	
17	—	① 1	Fix to "0".	HS*(shown left) shows horizontal display start location this is register B/F (address 127₁₆) = "0" is set.															
			Can not be used.																

Note 1: The mark ① around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

2: Set up the horizontal and vertical display start location so that display range may not exceed it.

Set the character code "1FF₁₆" (blank without background) for the display RAM of the part which the display range exceeds.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(4) Address 12316

DA	Register	Contents		Remarks																				
		Status	Function																					
0	DSP0	① 1	The display modes of display screen inside n+1 line by DSPn (n=0 to 11) The display mode decided by the combination with registers BLK1 and BLK0 (address 12316). Settings are given below. <table><tr><td>BLK1</td><td>BLK0</td><td>DSPn="0"</td><td>DSPn="1"</td></tr><tr><td>0</td><td>0</td><td>Matrix-outline border</td><td>Matrix-outline</td></tr><tr><td>0</td><td>1</td><td>Character</td><td>Border</td></tr><tr><td>1</td><td>0</td><td>Border</td><td>Matrix-outline</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline</td><td>Charcter</td></tr></table> (At register BCOL="0") For detail, see "DISPLAY FORM 1 (1)".	BLK1	BLK0	DSPn="0"	DSPn="1"	0	0	Matrix-outline border	Matrix-outline	0	1	Character	Border	1	0	Border	Matrix-outline	1	1	Matrix-outline	Charcter	Display mode settting of line 1.
BLK1	BLK0	DSPn="0"		DSPn="1"																				
0	0	Matrix-outline border		Matrix-outline																				
0	1	Character		Border																				
1	0	Border		Matrix-outline																				
1	1	Matrix-outline		Charcter																				
1	DSP1	① 1		Display mode settting of line 2.																				
2	DSP2	① 1		Display mode settting of line 3.																				
3	DSP3	① 1		Display mode settting of line 4.																				
4	DSP4	① 1		Display mode settting of line 5.																				
5	DSP5	① 1		Display mode settting of line 6.																				
6	DSP6	① 1		Display mode settting of line 7.																				
7	DSP7	① 1	Display mode settting of line 8.																					
8	DSP8	① 1	Display mode settting of line 9.																					
9	DSP9	① 1	Display mode settting of line 10.																					
A	DSP10	① 1	Display mode settting of line 11.																					
B	DSP11	① 1	Display mode settting of line 12.																					
C	BCOL	① 1	The blanking of BLK1 and BLK0 Sets all blanking (raster area)	All blanking (raster area) settting																				
D	BLK0	① 1	<table><tr><td>BLK1</td><td>BLK0</td><td>Blanking mode</td></tr><tr><td>0</td><td>0</td><td>Matrix-outline size</td></tr><tr><td>0</td><td>1</td><td>Character size</td></tr><tr><td>1</td><td>0</td><td>Border size</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline size</td></tr></table>	BLK1	BLK0	Blanking mode	0	0	Matrix-outline size	0	1	Character size	1	0	Border size	1	1	Matrix-outline size	Display mode (blanking mode) settting See "DISPLAY FORM 1 (1)".					
BLK1	BLK0	Blanking mode																						
0	0	Matrix-outline size																						
0	1	Character size																						
1	0	Border size																						
1	1	Matrix-outline size																						
E	BLK1	① 1																						
F	—	① 1	Fix to "0". Can not be used.																					
10	—	① 1	Fix to "0". Can not be used.																					
11	TEST19	① 1	Fix to "0". Can not be used.																					
12	—	① 1	Fix to "0". Can not be used.																					
13	BETA14	① 1	Matrix-outline display (12 × 18 dot) Matrix-outline display (14 × 18 dot)	Effective at the time of Matrix-outline displays and Matrix-outline border displays in the display mode.																				
14	SYAD	① 1	Border display of character Shadow display of character																					
15	—	① 1	Fix to "0". Can not be used.																					
16	—	① 1	Fix to "0". Can not be used.																					
17	—	① 1	Fix to "0". Can not be used.																					

Note: The mark ① around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(5) Address 124₁₆

DA	Register	Contents		Remarks									
		Status	Function										
0	LINE2	① 1	The vertical dot size for line n in the character dot lines (18 vertical lines) is set using LINn (n = 2 to 17). Dot size can be selected between 2 types for each dot line. For dot size, see the below registers. Line 1 and lines 2 to 2 can be set independent of one another. <table><tr><td></td><td>LINn = "0"</td><td>LINn = "1"</td></tr><tr><td>1st line</td><td>Refer to VSZ1L0 and VSZ1L1</td><td>Refer to VSZ1H0 and VSZ1H1</td></tr><tr><td>2nd to 12th line</td><td>Refer to VSZ2L0 and VSZ2L1</td><td>Refer to VSZ2H0 and VSZ2H1</td></tr></table>		LINn = "0"	LINn = "1"	1st line	Refer to VSZ1L0 and VSZ1L1	Refer to VSZ1H0 and VSZ1H1	2nd to 12th line	Refer to VSZ2L0 and VSZ2L1	Refer to VSZ2H0 and VSZ2H1	Character dot size setting in the vertical direction for the 2nd line.
	LINn = "0"	LINn = "1"											
1st line	Refer to VSZ1L0 and VSZ1L1	Refer to VSZ1H0 and VSZ1H1											
2nd to 12th line	Refer to VSZ2L0 and VSZ2L1	Refer to VSZ2H0 and VSZ2H1											
1	LINE3	① 1		Character dot size setting in the vertical direction for the 3rd line.									
2	LINE4	① 1		Character dot size setting in the vertical direction for the 4th line.									
3	LINE5	① 1		Character dot size setting in the vertical direction for the 5th line.									
4	LINE6	① 1		Character dot size setting in the vertical direction for the 6th line.									
5	LINE7	① 1		Character dot size setting in the vertical direction for the 7th line.									
6	LINE8	① 1		Character dot size setting in the vertical direction for the 8th line.									
7	LINE9	① 1		Character dot size setting in the vertical direction for the 9th line.									
8	LINE10	① 1		Character dot size setting in the vertical direction for the 10th line.									
9	LINE11	① 1		Character dot size setting in the vertical direction for the 11th line.									
A	LINE12	① 1		Character dot size setting in the vertical direction for the 12th line.									
B	LINE13	① 1		Character dot size setting in the vertical direction for the 13th line.									
C	LINE14	① 1		Character dot size setting in the vertical direction for the 14th line.									
D	LINE15	① 1		Character dot size setting in the vertical direction for the 15th line.									
E	LINE16	① 1	Character dot size setting in the vertical direction for the 16th line.										
F	LINE17	① 1	Character dot size setting in the vertical direction for the 17th line.										
10	—	① 1	Fix to "0". Can not be used.										
11	—	① 1	Fix to "0". Can not be used.										
12	—	① 1	Fix to "0". Can not be used.										
13	—	① 1	Fix to "0". Can not be used.										
14	—	① 1	Fix to "0". Can not be used.										
15	—	① 1	Fix to "0". Can not be used.										
16	—	① 1	Fix to "0". Can not be used.										
17	—	① 1	Fix to "0". Can not be used.										

Note: The mark ① around the status value means the reset status by the "L" level is input to AC pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(6) Address 125₁₆

DA	Register	Contents			Remarks															
		Status	Function																	
0	V1SZ0	①	H: Cycle with the horizontal synchronizing pulse			Character dot size setting in the vertical direction for the 1st line. (common to all lines)														
		1	<table><tr><th>V1SZ1</th><th>V1SZ0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	V1SZ1	V1SZ0		Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
V1SZ1	V1SZ0	Vertical direction size																		
0	0	1H/dot																		
0	1	2H/dot																		
1	0	3H/dot																		
1	1	4H/dot																		
1	V1SZ1	①																		
		1	<table><tr><th>V1SZ1</th><th>V1SZ0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	V1SZ1	V1SZ0		Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
V1SZ1	V1SZ0	Vertical direction size																		
0	0	1H/dot																		
0	1	2H/dot																		
1	0	3H/dot																		
1	1	4H/dot																		
2	VSZ1L0	①	H: Cycle with the horizontal synchronizing pulse			Character dot size setting in the vertical direction for the first line. (effective only at LINn = "0").														
		1	<table><tr><th>VSZ1L1</th><th>VSZ1L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	VSZ1L1	VSZ1L0		Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
VSZ1L1	VSZ1L0	Vertical direction size																		
0	0	1H/dot																		
0	1	2H/dot																		
1	0	3H/dot																		
1	1	4H/dot																		
3	VSZ1L1	①																		
		1	<table><tr><th>VSZ1L1</th><th>VSZ1L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	VSZ1L1	VSZ1L0		Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
VSZ1L1	VSZ1L0	Vertical direction size																		
0	0	1H/dot																		
0	1	2H/dot																		
1	0	3H/dot																		
1	1	4H/dot																		
4	VSZ1H0	①	H: Cycle with the horizontal synchronizing pulse			Character dot size setting in the vertical direction for the first line. (effective only at LINn = "1").														
		1	<table><tr><th>VSZ1H1</th><th>VSZ1H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	VSZ1H1	VSZ1H0		Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
VSZ1H1	VSZ1H0	Vertical direction size																		
0	0	1H/dot																		
0	1	2H/dot																		
1	0	3H/dot																		
1	1	4H/dot																		
5	VSZ1H1	①																		
		1	<table><tr><th>VSZ1H1</th><th>VSZ1H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	VSZ1H1	VSZ1H0		Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
VSZ1H1	VSZ1H0	Vertical direction size																		
0	0	1H/dot																		
0	1	2H/dot																		
1	0	3H/dot																		
1	1	4H/dot																		
6	-	①	Fix to "0".																	
		1	Can not be used.																	
7	-	①	Fix to "0".																	
		1	Can not be used.																	
8	V18SZ0	①	H: Cycle with the horizontal synchronizing pulse			Character dot size setting in the vertical direction for the 18th line. (common to all lines)														
		1	<table><tr><th>V18Z1</th><th>V18Z0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	V18Z1	V18Z0		Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
V18Z1	V18Z0	Vertical direction size																		
0	0	1H/dot																		
0	1	2H/dot																		
1	0	3H/dot																		
1	1	4H/dot																		
9	V18SZ1	①																		
		1	<table><tr><th>V18Z1</th><th>V18Z0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	V18Z1	V18Z0		Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
V18Z1	V18Z0	Vertical direction size																		
0	0	1H/dot																		
0	1	2H/dot																		
1	0	3H/dot																		
1	1	4H/dot																		
A	VSZ2L0	①	H: Cycle with the horizontal synchronizing pulse			Character dot size setting in the vertical direction (display monitor for 2nd to 12th line) (effective only at LINn = "0").														
		1	<table><tr><th>VSZ2L1</th><th>VSZ2L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	VSZ2L1	VSZ2L0		Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
VSZ2L1	VSZ2L0	Vertical direction size																		
0	0	1H/dot																		
0	1	2H/dot																		
1	0	3H/dot																		
1	1	4H/dot																		
B	VSZ2L1	①																		
		1	<table><tr><th>VSZ2L1</th><th>VSZ2L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	VSZ2L1	VSZ2L0		Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
VSZ2L1	VSZ2L0	Vertical direction size																		
0	0	1H/dot																		
0	1	2H/dot																		
1	0	3H/dot																		
1	1	4H/dot																		
C	VSZ2H0	①	H: Cycle with the horizontal synchronizing pulse			Character dot size setting in the vertical direction (display monitor for 2nd to 12th line) (effective only at LINn = "0").														
		1	<table><tr><th>VSZ2H1</th><th>VSZ2H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	VSZ2H1	VSZ2H0		Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
VSZ2H1	VSZ2H0	Vertical direction size																		
0	0	1H/dot																		
0	1	2H/dot																		
1	0	3H/dot																		
1	1	4H/dot																		
D	VSZ2H1	①																		
		1	<table><tr><th>VSZ2H1</th><th>VSZ2H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	VSZ2H1	VSZ2H0		Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot	
VSZ2H1	VSZ2H0	Vertical direction size																		
0	0	1H/dot																		
0	1	2H/dot																		
1	0	3H/dot																		
1	1	4H/dot																		
E	-	①	Fix to "0".																	
		1	Can not be used.																	
F	-	①	Fix to "0".																	
		1	Can not be used.																	
10	HSZ10	①	<table><tr><th>HSZ11</th><th>HSZ10</th><th>horizontal direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table>	HSZ11	HSZ10	horizontal direction size	0	0	1T/dot	0	1	2T/dot	1	0	3T/dot	1	1	4T/dot	Character size setting in the horizontal direction for the first line. T: Display frequency cycle.	
		HSZ11	HSZ10	horizontal direction size																
0	0	1T/dot																		
0	1	2T/dot																		
1	0	3T/dot																		
1	1	4T/dot																		
11	HSZ11	①	<table><tr><th>HSZ11</th><th>HSZ10</th><th>horizontal direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table>	HSZ11	HSZ10	horizontal direction size	0	0	1T/dot	0	1	2T/dot	1	0	3T/dot	1	1	4T/dot		
		HSZ11	HSZ10	horizontal direction size																
0	0	1T/dot																		
0	1	2T/dot																		
1	0	3T/dot																		
1	1	4T/dot																		
12	HSZ20	①	<table><tr><th>HSZ21</th><th>HSZ20</th><th>horizontal direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table>	HSZ21	HSZ20	horizontal direction size	0	0	1T/dot	0	1	2T/dot	1	0	3T/dot	1	1	4T/dot	Charcter size setting in the horizontal direction for the 2nd line to 12th line. T: Display frequency cycle.	
		HSZ21	HSZ20	horizontal direction size																
0	0	1T/dot																		
0	1	2T/dot																		
1	0	3T/dot																		
1	1	4T/dot																		
13	HSZ21	①	<table><tr><th>HSZ21</th><th>HSZ20</th><th>horizontal direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table>	HSZ21	HSZ20	horizontal direction size	0	0	1T/dot	0	1	2T/dot	1	0	3T/dot	1	1	4T/dot		
		HSZ21	HSZ20	horizontal direction size																
0	0	1T/dot																		
0	1	2T/dot																		
1	0	3T/dot																		
1	1	4T/dot																		
14	-	①	Fix to "0".																	
		1	Can not be used.																	
15	-	①	Fix to "0".																	
		1	Can not be used.																	
16	-	①	Fix to "0".																	
		1	Can not be used.																	
17	-	①	Fix to "0".																	
		1	Can not be used.																	

Note: The mark ① around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(7) Address 126₁₆

DA	Register	Contents		Remarks
		Status	Function	
0	RC0	① 1	RO0–RO6 correspond to CO0–CO6 output, respectively.	Raster color setting of all blankings.
1	RC1	① 1		
2	RC2	① 1		
3	RC3	① 1		
4	RC4	① 1		
5	RC5	① 1		
6	RC6	① 1		
7	–	① 1	Fix to "0". Can not be used.	
8	–	① 1	Fix to "0". Can not be used.	
9	FC0	① 1	FO0–FO6 correspond to CO0–CO6 output, respectively.	Color setting of the border display or the shadow display.
A	FC1	① 1		
B	FC2	① 1		
C	FC3	① 1		
D	FC4	① 1		
E	FC5	① 1		
F	FC6	① 1		
10	–	① 1	Fix to "0". Can not be used.	
11	–	① 1	Fix to "0". Can not be used.	
12	–	① 1	Fix to "0". Can not be used.	
13	–	① 1	Fix to "0". Can not be used.	
14	–	① 1	Fix to "0". Can not be used.	
15	–	① 1	Fix to "0". Can not be used.	
16	–	① 1	Fix to "0". Can not be used.	
17		① 1	Fix to "0". Can not be used.	

Note: The mark ① around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(8) Address 127₁₆

DA	Register	Contents		Remarks																																				
		Status	Function																																					
0	B/F	①	Synchronize with the leading edge of horizontal synchronization.	Synchronize with the front porch or back porch of the horizontal synchronization signal.																																				
		1	Synchronize with the trailing edge of horizontal synchronization.																																					
1	VMASK	①	Do not mask by VERT input signal.	Sets mask at phase comparison operating.																																				
		1	Mask by VERT input signal.																																					
2	POLV	①	VERT pin is negative polarity.	VERT pin polarity setting.																																				
		1	VERT pin is positive polarity.																																					
3	POLH	①	HOR pin is negative polarity.	HOR pin polarity setting.																																				
		1	HOR pin is positive polarity.																																					
4	TEST13	①	Fix to "0".																																					
		1	Can not be used.																																					
5	TEST14	①	Fix to "0".																																					
		1	Can not be used.																																					
6	TEST15	①	Fix to "0".																																					
		1	Can not be used.																																					
7	TEST16	①	Fix to "0".																																					
		1	Can not be used.																																					
8	TEST17	①	Fix to "0".																																					
		1	Can not be used.																																					
9	TEST30	①	Fix to "0".																																					
		1	Can not be used.																																					
A	DSPON	①	Display OFF																																					
		1	Display ON																																					
B	RAMERS	①	RAM not erased	When register RAMERS is set to "1", do not stop the display clock. There is no need to reset because there is no register for this bit.																																				
		1	RAM erased																																					
C	SPACE0	①	<table><tr><th>SPACE2</th><th>SPACE1</th><th>SPACE0</th><th>Number of Lines and Space<(S) represents space></th></tr><tr><td>0</td><td>0</td><td>0</td><td>12</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 (S) 10 (S) 1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 (S) 8 (S) 2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>3 (S) 6 (S) 3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>4 (S) 4 (S) 4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>5 (S) 2 (S) 5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>6 (S) 6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>6 (S)(S) 6</td></tr></table>	SPACE2	SPACE1	SPACE0	Number of Lines and Space<(S) represents space>	0	0	0	12	0	0	1	1 (S) 10 (S) 1	0	1	0	2 (S) 8 (S) 2	0	1	1	3 (S) 6 (S) 3	1	0	0	4 (S) 4 (S) 4	1	0	1	5 (S) 2 (S) 5	1	1	0	6 (S) 6	1	1	1	6 (S)(S) 6	Leave one line worth of space in the vertical direction. For example, 6 (S) 6 indicates two sets of 6 lines with a line of spaces between lines 6 and 7. A line is 18 X N horizontal scan lines. N is determined by the character size in the vertical direction
		SPACE2	SPACE1	SPACE0	Number of Lines and Space<(S) represents space>																																			
0	0	0	12																																					
0	0	1	1 (S) 10 (S) 1																																					
0	1	0	2 (S) 8 (S) 2																																					
0	1	1	3 (S) 6 (S) 3																																					
1	0	0	4 (S) 4 (S) 4																																					
1	0	1	5 (S) 2 (S) 5																																					
1	1	0	6 (S) 6																																					
1	1	1	6 (S)(S) 6																																					
1	(S) represents one line worth of space																																							
F	-	①	Fix to "0".																																					
		1	Can not be used.																																					
10	-	①	Fix to "0".																																					
		1	Can not be used.																																					
11	-	①	Fix to "0".																																					
		1	Can not be used.																																					
12	-	①	Fix to "0".																																					
		1	Can not be used.																																					
13	-	①	Fix to "0".																																					
		1	Can not be used.																																					
14	-	①	Fix to "0".																																					
		1	Can not be used.																																					
15	-	①	Fix to "0".																																					
		1	Can not be used.																																					
16	-	①	Fix to "0".																																					
		1	Can not be used.																																					
17	-	①	Fix to "0".																																					
		1	Can not be used.																																					

Note: The mark ① around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(9) Address 128₁₆

DA	Register	Contents		Remarks
		Status	Function	
0	TEST0	①	Fix to "0".	
		1	Can not be used.	
1	TEST1	①	Fix to "0".	
		1	Can not be used.	
2	TEST2	①	Fix to "0".	
		1	Can not be used.	
3	TEST3	①	Fix to "0".	
		1	Can not be used.	
4	TEST10	①	Fix to "0".	
		1	Can not be used.	
5	TEST26	①	Fix to "0".	
		1	Can not be used.	
6	TEST27	①	Fix to "0".	
		1	Can not be used.	
7	TEST28	①	Fix to "0".	
		1	Can not be used.	
8	TEST21	①	Fix to "0".	
		1	Can not be used.	
9	TEST22	①	Fix to "0".	
		1	Can not be used.	
A	TEST29	①	Fix to "0".	
		1	Can not be used.	
B	TEST20	①	Fix to "0".	
		1	Can not be used.	
C	—	①	Fix to "0".	
		1	Can not be used.	
D	—	①	Fix to "0".	
		1	Can not be used.	
E	—	①	Fix to "0".	
		1	Can not be used.	
F	—	①	Fix to "0".	
		1	Can not be used.	
10	—	①	Fix to "0".	
		1	Can not be used.	
11	—	①	Fix to "0".	
		1	Can not be used.	
12	—	①	Fix to "0".	
		1	Can not be used.	
13	—	①	Fix to "0".	
		1	Can not be used.	
14	—	①	Fix to "0".	
		1	Can not be used.	
15	—	①	Fix to "0".	
		1	Can not be used.	
16	—	①	Fix to "0".	
		1	Can not be used.	
17	—	①	Fix to "0".	
		1	Can not be used.	

Note: The mark ① around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

REGISTER SUPPLEMENTARY DESCRIPTION

(1) Setting external clock input and display frequency mode Setting external clock input and display frequency mode (by use of EXCK0, EXCK1 and DIV11 to DIV0 (120₁₆), as explained here following.

- (a) When (EXCK1, EXCK0) = (0, 0) External clock mode 1
 Fosc = 6.3 to 80 MHz (VDD = 4.75V to 5.25V)
 Fosc = 6.3 to 40 MHz (VDD = 3.00V to 3.60V)
 Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronous signal. And input from HOR pin a constant period continuous horizontal synchronous signal.
 Never stop inputting the clock while displaying.
 Do not have to set a display frequency because the clock just as it is entered from outside is used as the display clock.

- (b) When (EXCK1, EXCK0) = (0, 1) Internal clock mode
 Fosc = 20 to 120 MHz (VDD = 4.75V to 5.25V)
 Clock input from the TCK pin is unnecessary. The multiply clock of the internally generated horizontal synchronous signal is used as the display clock.
 The display frequency is set by setting the multiply value of the horizontal synchronous frequency (of the display frequency) in DIV11 to DIV0 (address 120₁₆). Also, set the display frequency range. (See the next page.)
 Display frequency is calculated using the below expression.

$$\text{Display frequency} = \text{Horizontal synchronous frequency} \times \text{Multiply value}$$

- (c) When (EXCK1, EXCK0) = (1, 0) Setting disabled
 (d) When (EXCK1, EXCK0) = (1, 1) External clock mode 2
 Fosc = 20 to 120 MHz (VDD = 4.75V to 5.25V)
 Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronous signal. And input from HOR pin a constant-period continuous horizontal synchronous signal.
 Never stop inputting the clock while displaying.
 An internal clock which is in sync with the external input clock is used as the display clock.
 Because the display frequency equals the external clock frequency, set N1 (division value) that satisfies the below expressions to DIV11 to DIV0 (address 120₁₆) for make the display frequency is equal to the external clock frequency.

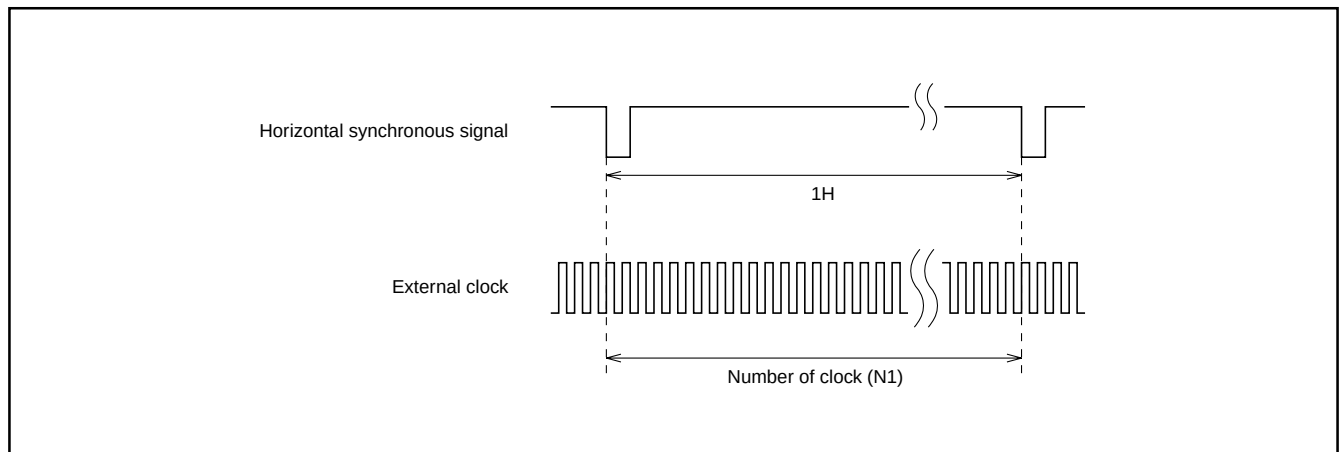


Fig. 3 Example of external clock input

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) To set display frequency range

Whenever setting display frequency (when EXCK1 = "0", EXCK0 = "1", or EXCK1 = "1", EXCK0 = "1"), always set the display frequency range in accordance with the display frequency. This range is set from DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1 (address 120₁₆). Frequency ranges are given here below.

RSEL1	RSEL0	DIVS2	DIVS1	DIVS0	Display frequency range MHz
1	1	0	0	0	112.0 to 120.0
1	0	0	0	0	104.0 to 112.0
0	1	0	0	0	93.0 to 104.0
0	0	0	0	0	80.0 to 93.0
1	1	0	0	1	75.0 to 80.0
1	0	0	0	1	69.5 to 75.0
0	1	0	0	1	62.0 to 69.5
0	0	0	0	1	55.0 to 62.0
1	1	0	1	0	—
1	0	0	1	0	52.0 to 55.0
0	1	0	1	0	46.5 to 52.0
0	0	0	1	0	40.0 to 46.5
1	1	0	1	1	37.5 to 40.0
1	0	0	1	1	35.0 to 37.5
0	1	0	1	1	31.0 to 35.0
0	0	0	1	1	27.5 to 31.0
1	1	1	0	0	—
1	0	1	0	0	26.0 to 27.5
0	1	1	0	0	23.5 to 26.0
0	0	1	0	0	20.0 to 23.5

(3) Notes on setting display frequency

To change external clock (display) frequency or horizontal synchronization frequency, always use the following procedures.

To set EXCK1 = "0", EXCK0 = "1"

- Turn the display OFF. ... DSPON (address 127₁₆) = "0"
- Set the display frequency. ... Set from DIV11 to DIV0, DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1 (address 120₁₆).
- Wait 20 ms while the horizontal synchronization signal is being input.
- Turn the display ON. ... DSPON (address 127₁₆) = "1"

To set EXCK1 = "1", EXCK0 = "1"

- Turn the display OFF. ... DSPON (address 127₁₆) = "0"
- Set the display frequency. ... Set from DIV11 to DIV0, DIVS0, DIVS1, DIVS2, RSEL0 and RSEL1 (address 120₁₆).
- Wait 20 ms while the horizontal synchronization signal and external clock are being input.
- Turn the display ON. ... DSPON (address 127₁₆) = "1"

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DISPLAY FORM 1

(1) blanking mode

Character size

: Blanking same as the character size.

Border size

: Blanking the background as a size from character.

Matrix-outline size

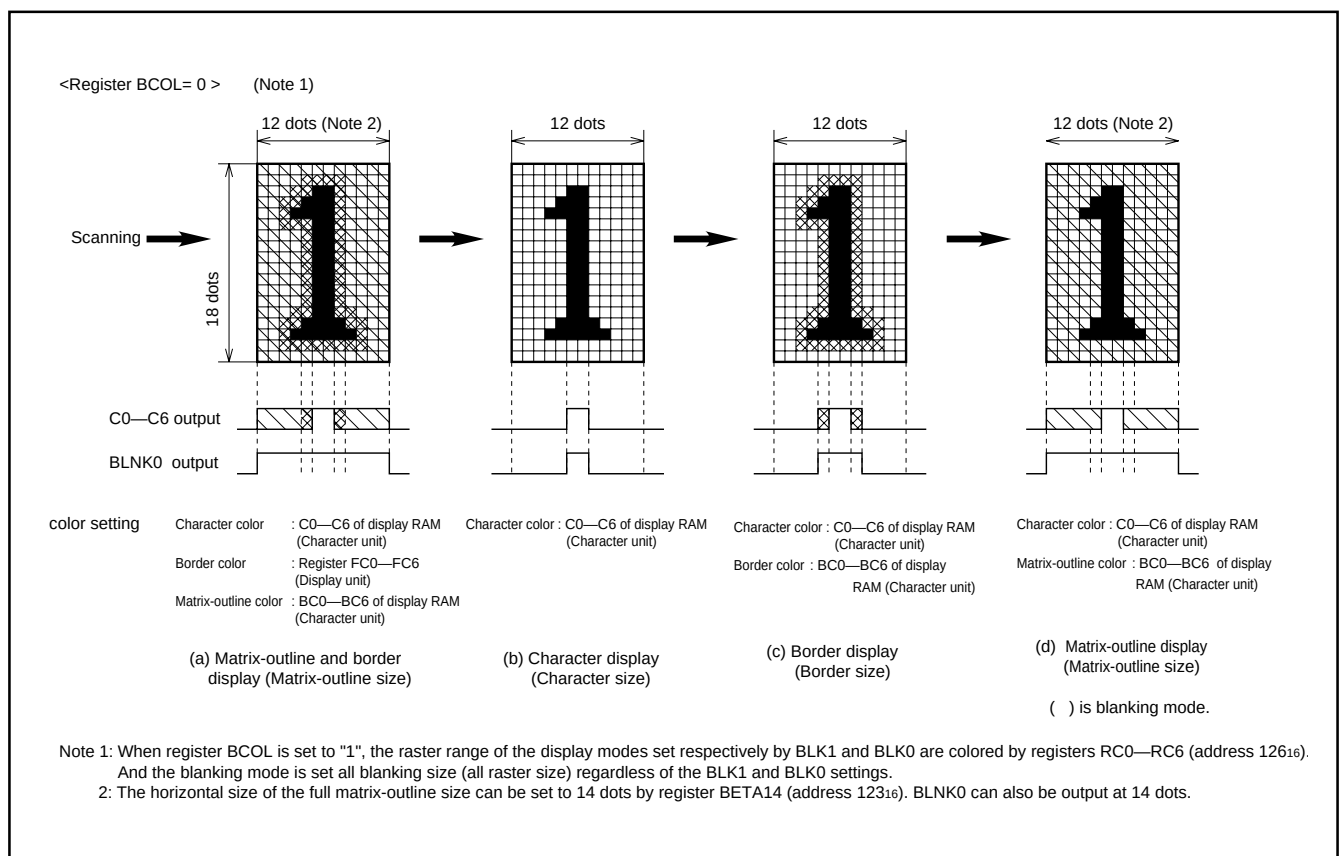
: Blanking the background 12 X 18 dot.

All blanking size

: When set register BCOL to "1", all raster area is blanking.

The display mode and blanking mode can be set line-by-line, as follows, from registers BCOL, BLK1, BLK0, DSP0 to DSP11 (address 123₁₆).

BCOL	BLK1	BLK0	Line of DSPn = "0"		Line of DSPn = "1"	
			Display mode	Blanking mode	Display mode	Blanking mode
0	0	0	Matrix-outline border display	Matrix-outline size	Matrix-outline display	Matrix-outline size
	0	1	Character display	Character size	Border display	Border size
	1	0	Border display	Border size	Matrix-outline display	Matrix-outlinesize
	1	1	Matrix-outline display	Matrix-outline size	Character display	Character size
1	0	0	Matrix-outline border display	All blanking size	Matrix-outline display	All blanking size
	0	1	Character display		Border display	
	1	0	Border display		Matrix-outline display	
	1	1	Matrix-outline display		Character display	

**Fig. 4 Display form**

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) Shadow display

When border display mode, if set SYAD (address 12316) = "0"
to "1", it change to shadow display mode.

Border and shadow display are shown below.

Set shadow display color by BR, BG and BB of display RAM or
by register FR, FG and FB.

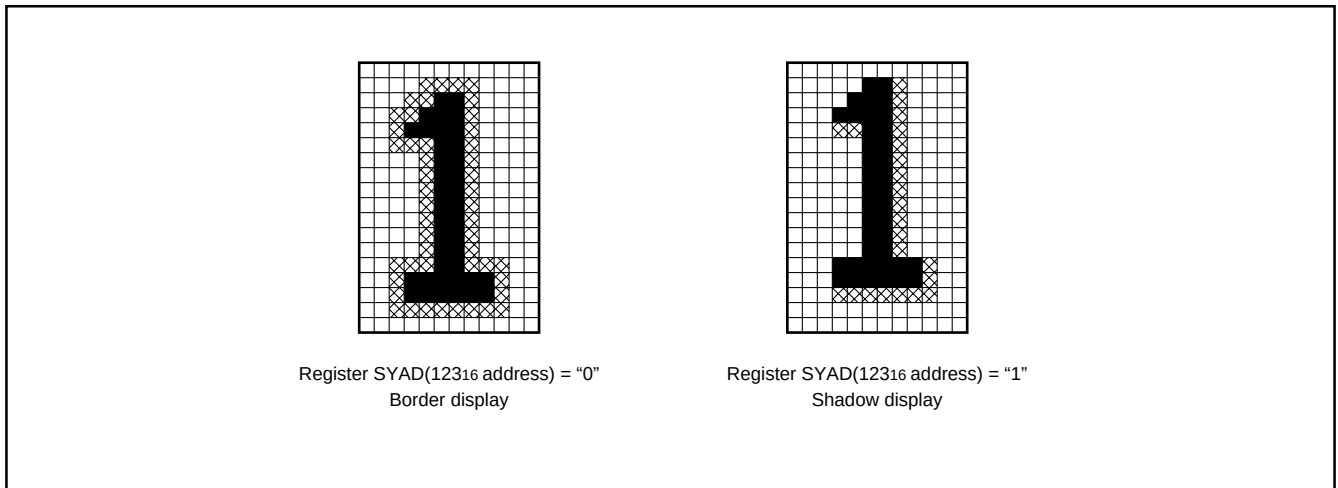


Fig.5 Shadow display

CHARACTER FONT

Images are composed on a 12 X 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

Character code FF16 is fixed as a blank without background. Therefore, cannot register a character font in this code.

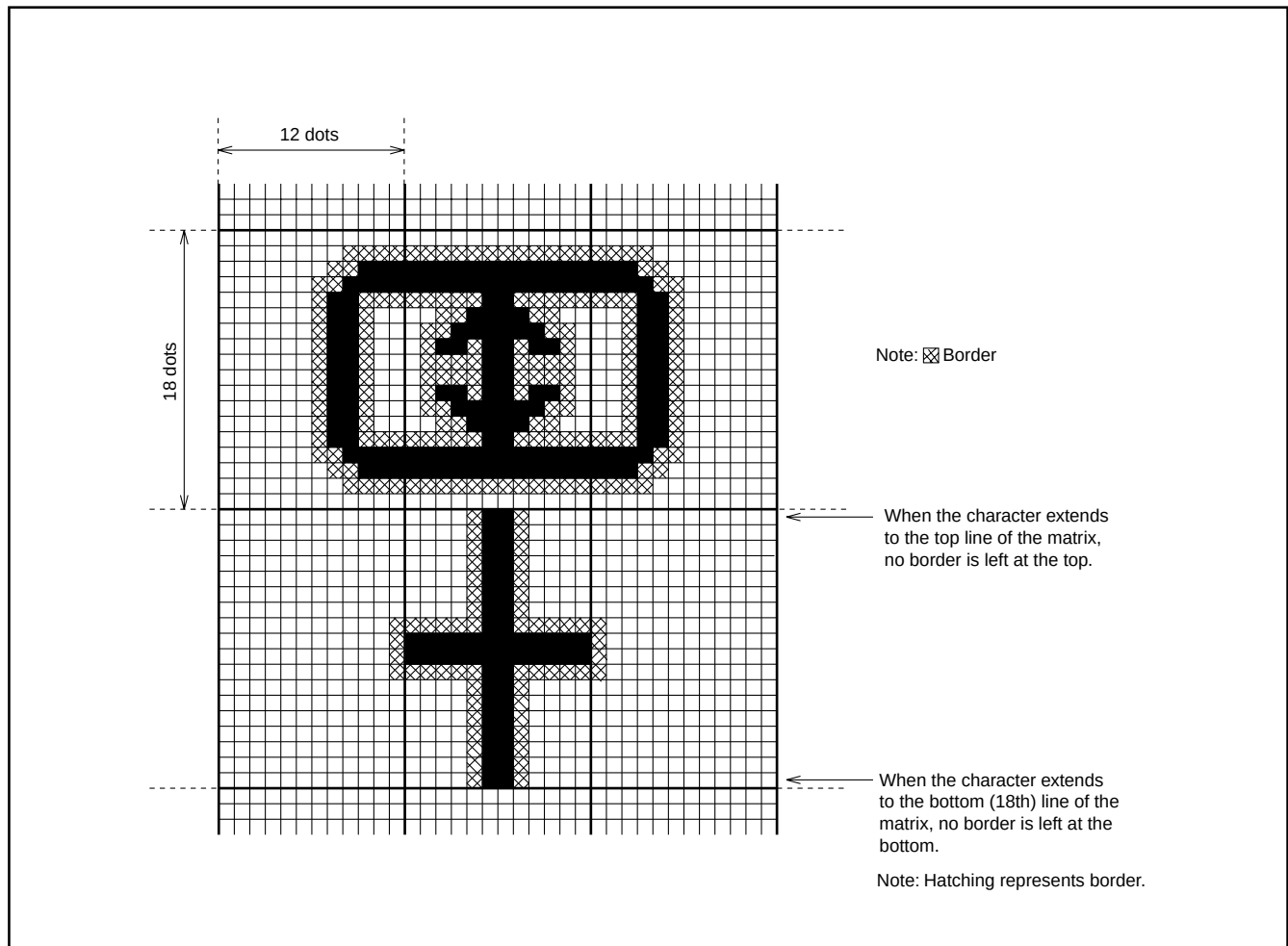


Fig.6 Example of border display

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the 24-bit serial input function or the I²C-BUS serial input function. Example of data setting is shown in Figure 7 (at EXCK0 = "1", EXCK1 = "0" setting).

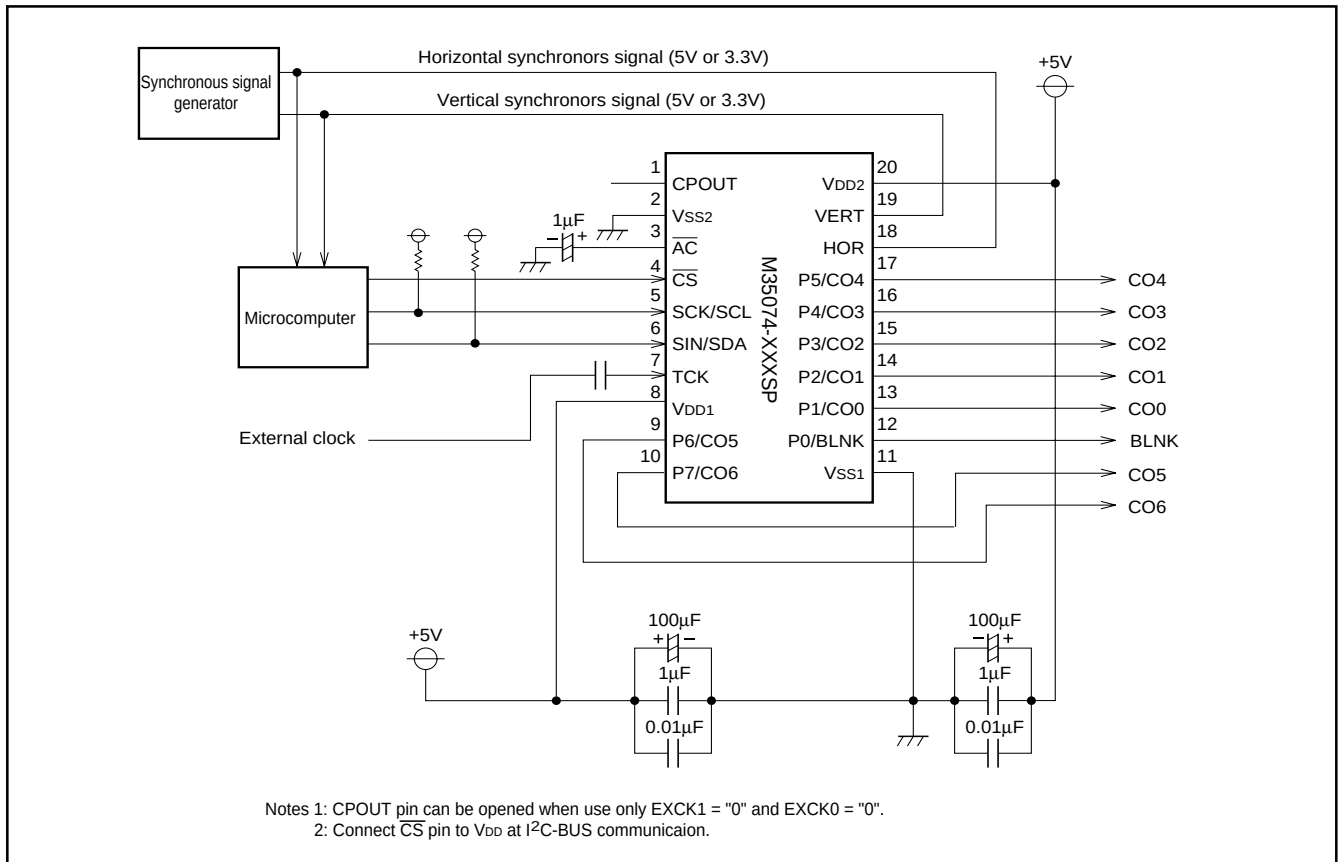
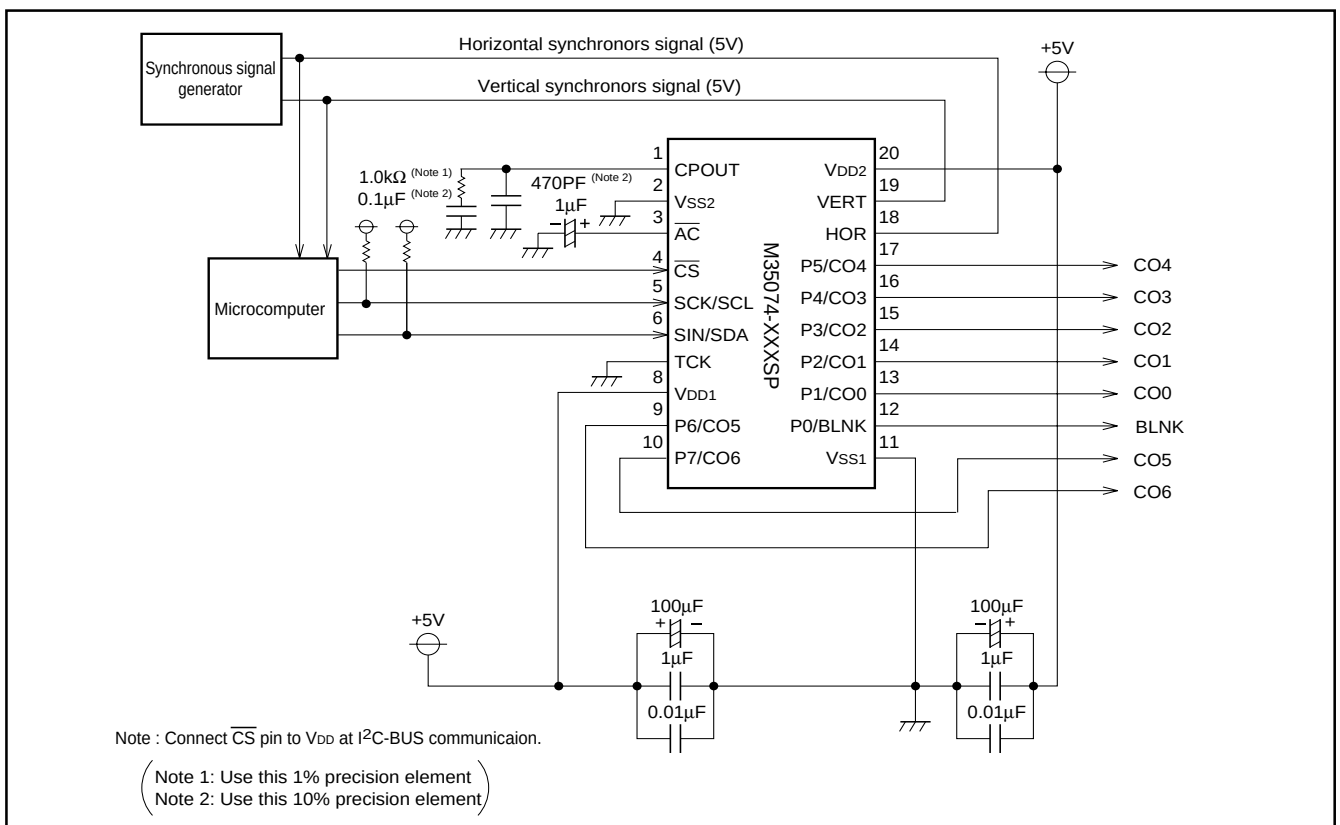
Example of the M35074-XXXSP Data input setting (at EXCK0 = "1", EXCK1 = "0")

Address/data	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Remarks								
	200 m sec hold																																
Address 120 ₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	Address setting								
data 120 ₁₆	0	0	0	0	0	0	1	RSEL1	RSEL0	0	DM52	DM51	DM50	DM11	DM10	DM8	DM7	DM6	DM5	DM4	DM3	DM2	DM1	DM0	Frequency value setting								
data 121 ₁₆	0	0	0	0	0	0	0	0	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0	PTC7	PTC6	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0	Output set								
data 122 ₁₆	0	VP10	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	HP11	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display location setting								
data 123 ₁₆	0	0	0	SVAD	BEAT14	0	0	0	0	0	1	BCOL	0	0	0	0	0	0	0	0	0	0	0	0	Display form setting								
data 124 ₁₆	0	0	0	0	0	0	0	0	LN17	LN16	LN15	LN14	LN13	LN12	LN11	LN10	LN9	LN8	LN7	LN6	LN5	LN4	LN3	LN2	Character size setting								
data 125 ₁₆	0	0	0	HSZ21	HSZ20	HSZ21	HSZ20	0	0	VSZ21H0	VSZ21H0	VSZ21L1	VSZ21L1	VSZ21L1	VSZ21L1	VSZ21L1	VSZ21L1	VSZ21L1	VSZ21H1	VSZ21H0	VSZ21L1	VSZ21L0	VSZ21L1	VSZ20	Character size setting								
data 126 ₁₆	0	0	0	0	0	0	0	0	0	FC6	FC5	FC4	FC3	FC2	FC1	FC0	0	RC6	RC5	RC4	RC3	RC2	RC1	RC0	Color character size setting								
data 127 ₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	POLH	POLV	0	0	Display OFF								
	200 m sec hold																								Be stable/Waiting time								
Address 000 ₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Address setting								
data 000 ₁₆	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	C6	C5	C4	C3	C2	C1	C0	C8	C7	C6	C5	C4	C3	C2	C1	C0	Character setting								
	Background coloring																Character color									Character code							
data 11F ₁₆	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	C6	C5	C4	C3	C2	C1	C0	C8	C7	C6	C5	C4	C3	C2	C1	C0									
Address 127 ₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	1	1	Address setting								
data 127 ₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	POLH	POLV	0	0	Display ON								

- Notes 1: Input a horizontal synchronous signal into the HOR pin and a vertical synchronous signal into the VERT pin.
 2: Matrix-outline display in this data.
 3: Secure the waiting time of 200ms after releasing $\overline{AC}$, and set data from setting the display frequency (setting of the register).
 4: Set data to Display RAM at internal clock (display clock) is stabilized.

Fig. 7 Example of data setting

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

**Fig.8 Example of the M35074-XXXSP peripheral circuit (External clock mode 1. At EXCK1 = "0", EXCK0 = "0")****Fig.9 Example of the M35074-XXXSP peripheral circuit (Internal clock mode. At EXCK1 = "0", EXCK0 = "1")**

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

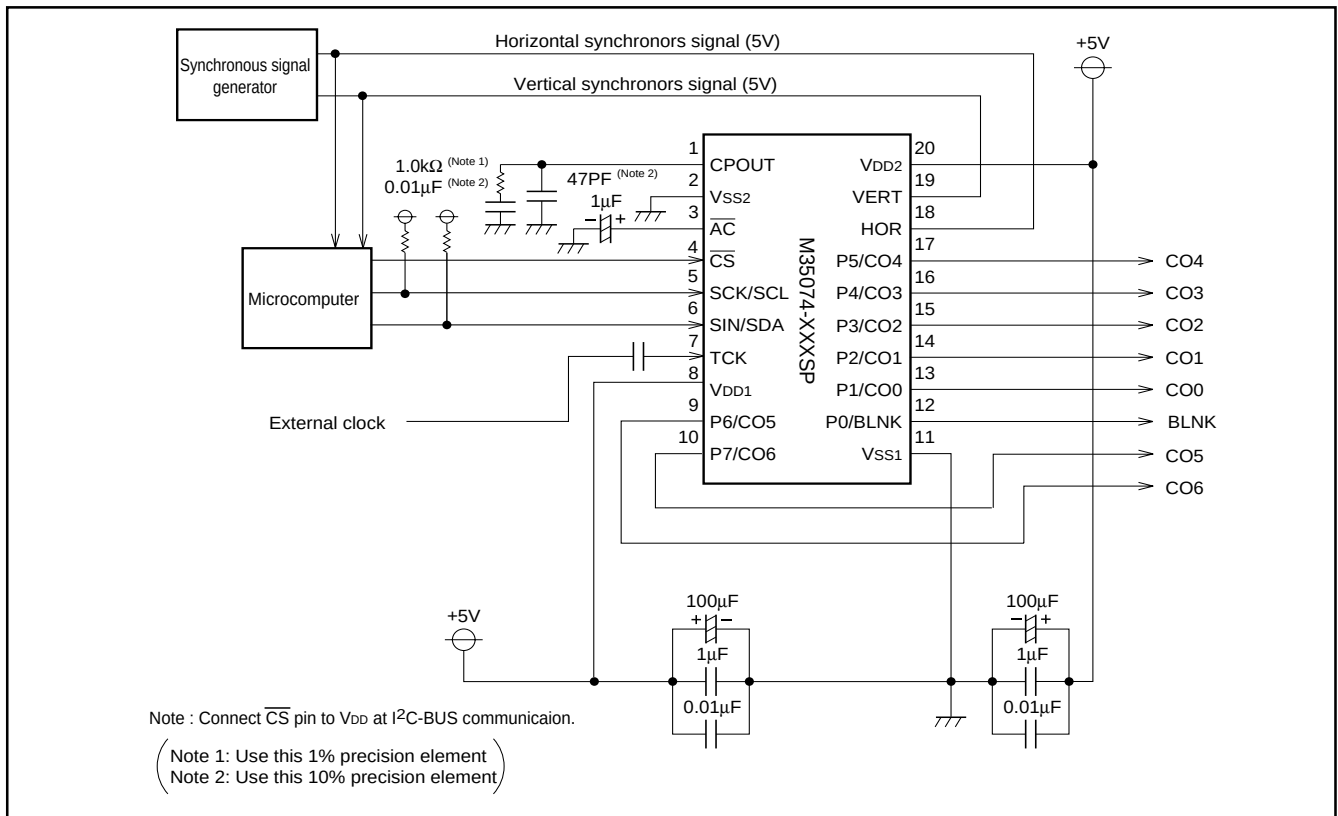
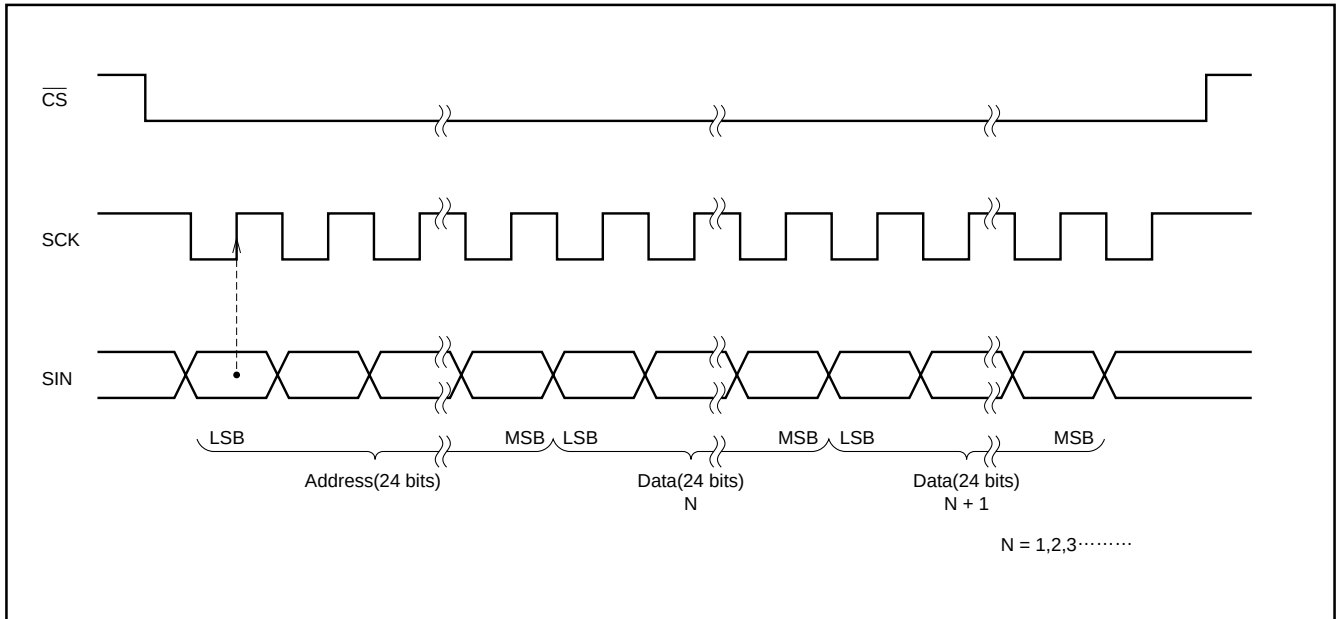


Fig.10 Example of the M35074-XXXSP peripheral circuit (External clock mode2. At EXCK1 = "1", EXCK0 = "1")

DATA INPUT 1**(1) SERIAL DATA INPUT TIMING**

- (a) Serial data should be input with the LSB first.
- (b) The address consists of 24 bits.
- (c) The data consists of 24 bits.
- (d) The 24 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 24 bits. Therefore, it is not necessary to input the address from the second data.

**Fig.11 Serial input timing**

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) TIMING REQUIREMENTS

Data input

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
$t_w(\text{SCK})$	SCK width	200	—	—	ns	See Figure 12
$t_{su}(\overline{\text{CS}})$	$\overline{\text{CS}}$ setup time	200	—	—	ns	
$t_h(\overline{\text{CS}})$	$\overline{\text{CS}}$ hold time	2	—	—	μs	
$t_{su}(\text{SIN})$	SIN setup time	200	—	—	ns	
$t_h(\text{SIN})$	SIN hold time	200	—	—	ns	
t_{word}	1 word writing time	14	—	—	μs	

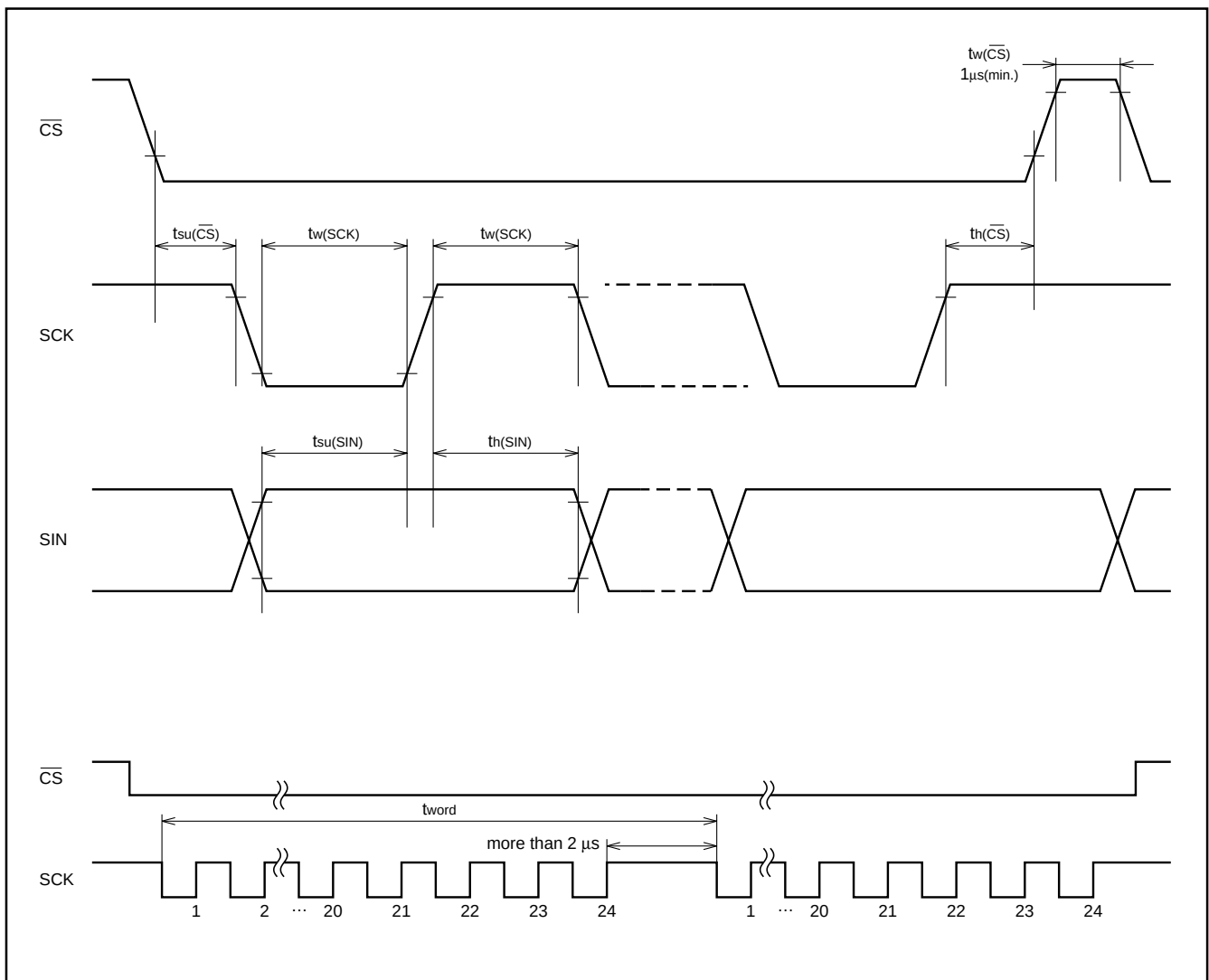


Fig. 12 Serial input timing requirements

DATA INPUT 2

(1) I²C-Bus communication function (At only VDD = 5V)

This IC has a built-in data transmission interface which utilizes 2 unidirectional buses. In communications, this IC functions as a slave reception device.

The IC is synchronized with the serial clock (SCL) sent from the master device and receives the data (SDA).

Communications are controlled from the start/stop states.

Also, always in put the control byte after attaining the start state.

The below chart shows the start/stop state and control byte configuration.

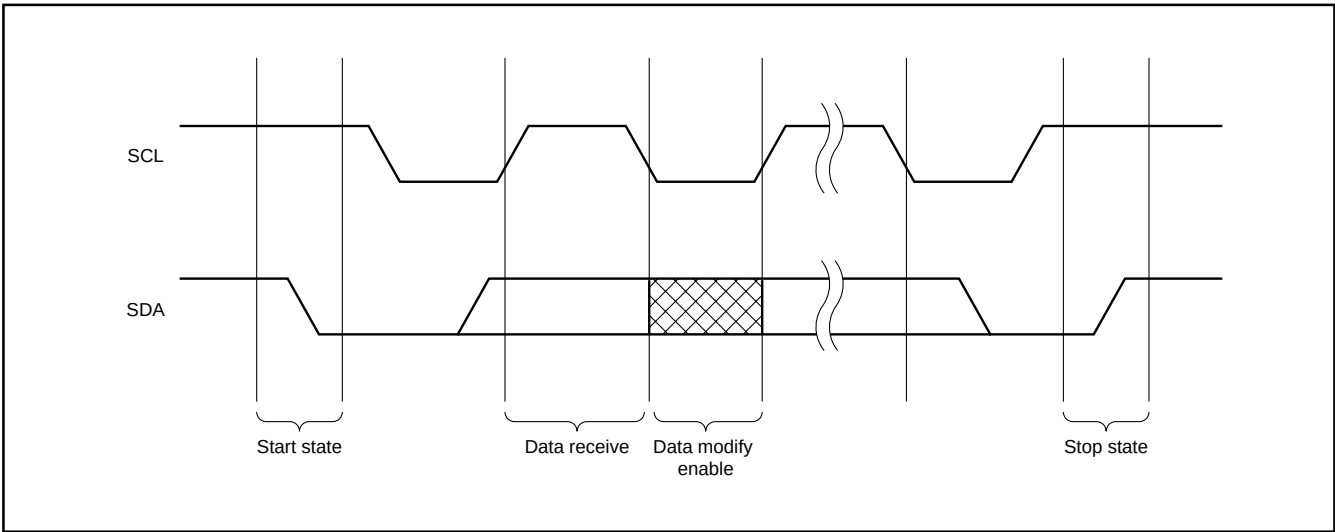


Fig.13 Start state / Stop state

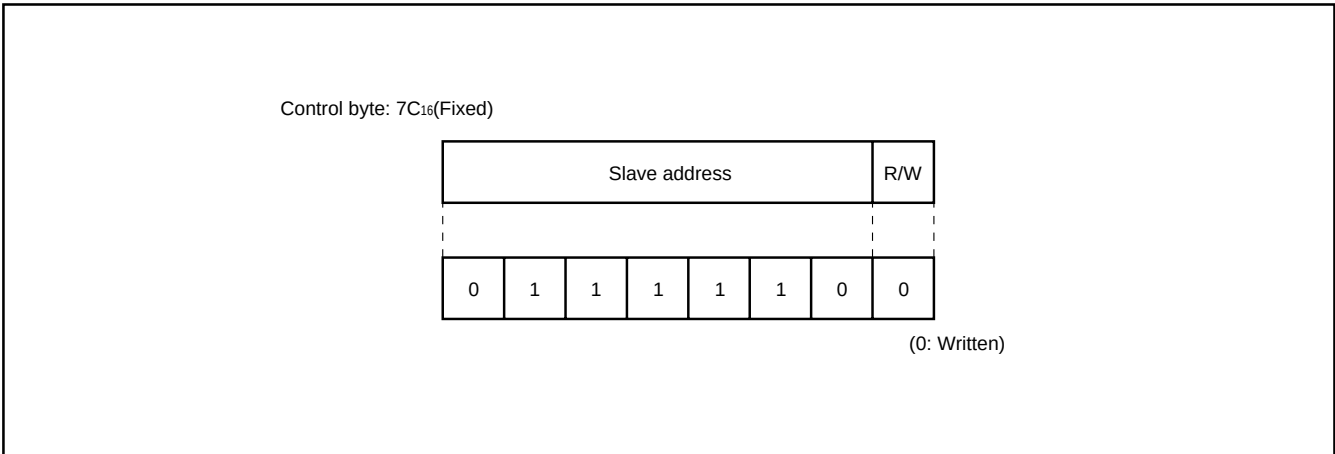


Fig.14 Control byte configuration

(2) Data input (Sequence)

- Addresses are consists of 16 bits.
- Data is consists of 24 bits.
- Addresses and data are communicated in 8-bit units. Input the lower 8 bits before the upper 8 bits. Make input from the MSB side.
- After the start state has been attained and the control byte (7CH) received, the next 16 bits (2 bytes) are for inputting the address. Addresses are increased in increments for every 24 bits (3 bytes) of data input thereafter. As a result, it is not necessary to input the address from the second data.

Note: During external synchronous , do not stop the external clock input from the TCK pin while inputting data.

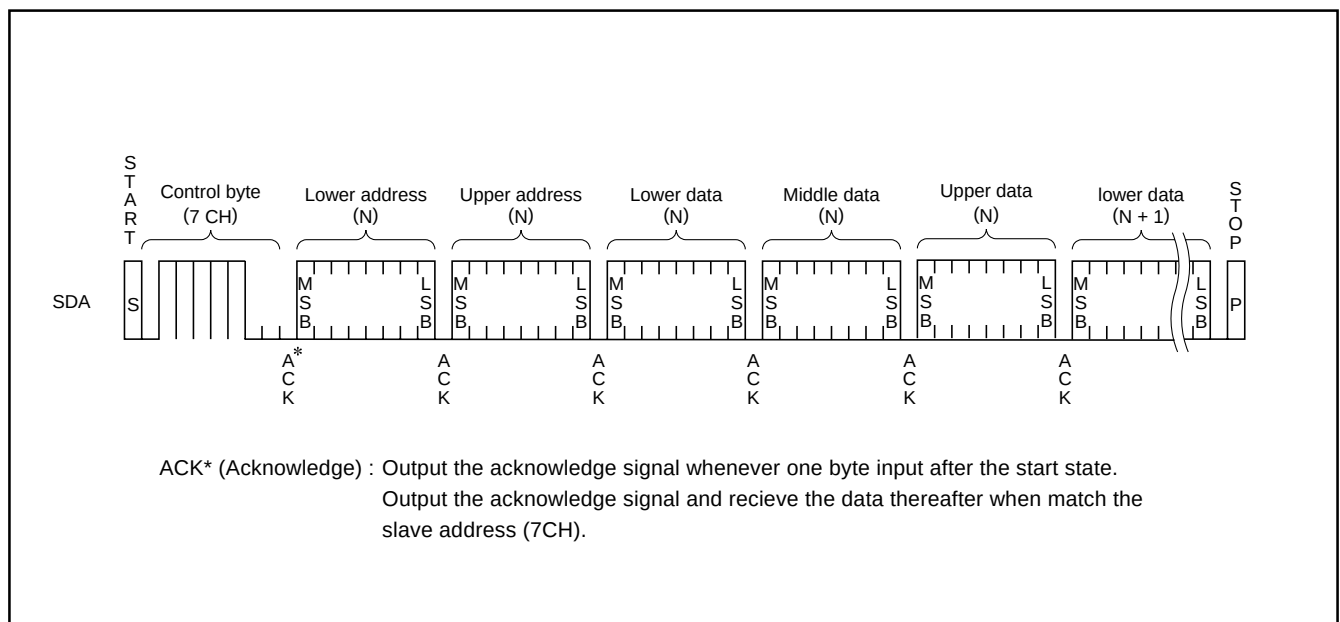


Fig.15 Data input sequence

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(3) TIMING REQUIREMENTS

Data input

Symbol	Parameter	Limits				Unit	Remarks
		Typ. mode		High-speed mode			
		Min.	Max.	Min.	Max.		
fCLK	Clock frequency	0	100	0	400	KHz	
tHIGH	HIGH period of Clock	4000	–	600	–	ns	
tLOW	LOW period of Clock	4700	–	1300	–	ns	
tR	SDA & SCL rise time	–	1000	20+(Note) 0.1CB	300	ns	
tF	SDA & SCL fall time	–	300	20+(Note) 0.1CB	300	ns	
tHD : STA	Hold time at START status	4000	–	600	–	ns	
tsu : STA	Set up time at START status	4700	–	600	–	ns	Only at START state repeating generation
tHD : DAT	Data input hold time	0	–	0	–	ns	
tsu : DAT	Data input setup time	250	–	100	–	ns	
tsu : STO	Set up time at STOP state	4000	–	600	–	ns	
tBUF	Bus release time	4700	–	1300	–	ns	Time must be re- leased bus before next transmission
tSP	Input filter / spike suppress (SDA & SCL pin)	N/A	N/A	0	50	ns	

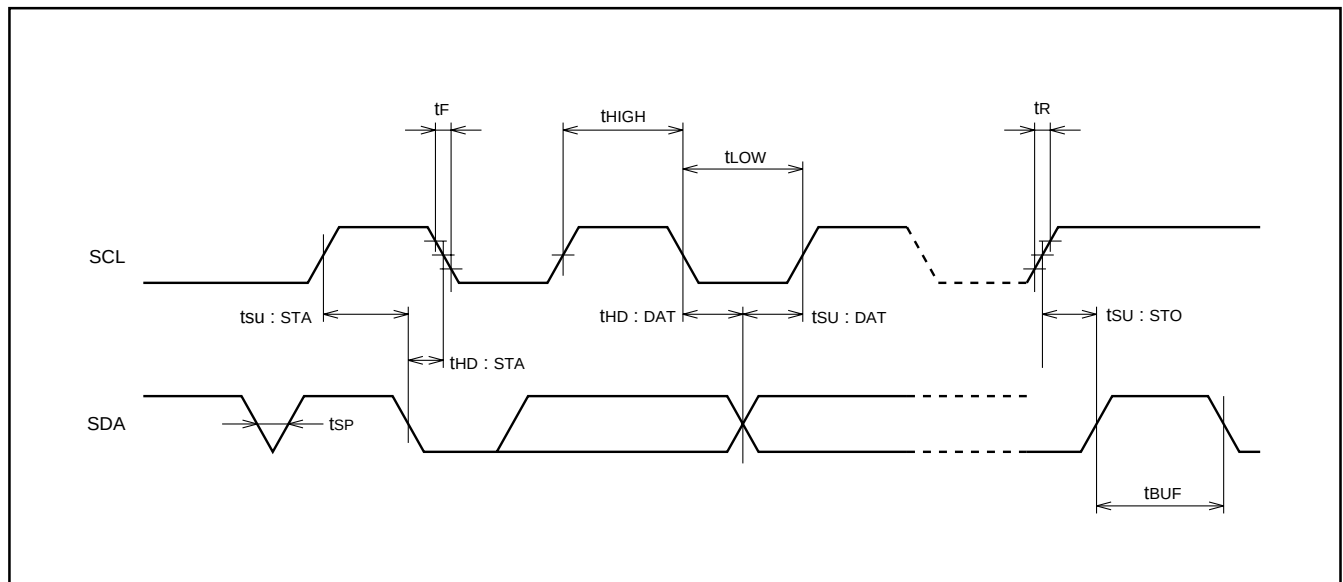
Note: C_B = total capacitance of 1 bus line.


Fig.16 Data input timing

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

ABSOLUTE MAXIMUM RATINGS ($V_{DD} = 5.00V$, $T_a = -20$ to $+85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS} .	-0.3 to $+6.0$	V
V_I	Input voltage		$V_{SS} - 0.3 \leq V_I \leq V_{DD} + 0.3$	V
V_O	Output voltage		$V_{SS} \leq V_O \leq V_{DD}$	V
P_d	Power dissipation	$T_a = +25^{\circ}C$	+300	mW
T_{opr}	Operating temperature		-20 to $+85$	$^{\circ}C$
T_{stg}	Storage temperature		-40 to $+125$	$^{\circ}C$

RECOMMENDED OPERATING CONDITIONS ($V_{DD} = 5.00V$, $T_a = -20$ to $+85^{\circ}C$, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V _{DD}	Supply voltage	5V	4.75	5.00	5.25	V	
		3.3V	3.00	3.30	3.60	V	
V _{IH}	"H" level input voltage	$\overline{AC}$, $\overline{CS}$, HOR, VERT	0.8 × V _{DD}	V _{DD}	V _{DD}	V	
		SCK/SCL, SIN/SDA	0.7 × V _{DD}	V _{DD}	V _{DD}	V	
V _{IL}	"L" level input voltage	$\overline{AC}$, $\overline{CS}$, HOR, VERT	0	0	0.2 × V _{DD}	V	
		SCK/SCL, SIN/SDA	0	0	0.3 × V _{DD}	V	
F _{osc}	Oscillating frequency for display	External clock mode 1	V _{DD} =4.75 to 5.25V	6.3	—	80.0	MHz
			V _{DD} =3.00 to 3.60V	6.3	—	40.0	MHz
		External clock mode 2	V _{DD} =4.75 to 5.25V	20.0	—	120.0	MHz
			Internal clock mode	V _{DD} =4.75 to 5.25V	20.0	—	120.0
H.sync	Horizontal synchronous signal input frequency	V _{DD} =4.75 to 5.25V	15.0	—	130.0	kHz	
		V _{DD} =3.00 to 3.60V	15.0	—	60.0	kHz	

ELECTRICAL CHARACTERISTICS 1 $V_{DD} = 5V$ ($V_{DD} = 5.00V$, $T_a = 25^{\circ}C$, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage		$T_a = -20$ to $+85^{\circ}C$	4.75	5.0	5.25	V
I_{DD}	Supply current		$V_{DD} = 5.00V$	—	40	60	mA
V_{OH}	"H" level output voltage	P0 to P7 (Note1)	$V_{DD} = 4.75V$, $I_{OH} = -0.4mA$	3.5	—	—	V
		CPOUT	$V_{DD} = 4.75V$, $I_{OH} = -0.05mA$				
V_{OL}	"L" level output voltage	P0 to P7 (Note2)	$V_{DD} = 4.75V$, $I_{OL} = 0.4mA$	—	—	0.4	V
		CPOUT	$V_{DD} = 4.75V$, $I_{OL} = 0.05mA$				
		SIN/SDA	$V_{DD} = 4.75V$, $I_{OL} = 3.0mA$				
R_I	Pull-up resistance $\overline{AC}$, $\overline{CS}$		$V_{DD} = 5.00V$	10	30	100	$k\Omega$
V_{TCK}	External clock input width		$4.75V \leq V_{DD} \leq 5.25V$	$0.6 \times V_{DD}$	—	$0.9 \times V_{DD}$	V

Notes 1: The current from the IC must not exceed -0.4 mA/port at any of the port pins (P0 to P7).

2: The current flowing into the IC must not exceed 0.4 mA/port at any of port pins (P0 to P7).

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

ELECTRICAL CHARACTERISTICS 2 V_{DD} = 3.3V (V_{DD} = 3.30V, T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{DD}	Supply voltage	T _a = -20 to +85°C	3.00	3.30	3.60	V
I _{DD}	Supply current	V _{DD} = 3.30V	—	20	30	mA
V _{OH}	"H" level output voltage P0 to P7 (Note1)	V _{DD} = 3.00V, I _{OH} = -0.1mA	2.60	—	—	V
V _{OL}	"L" level output voltage P0 to P7 (Note2)	V _{DD} = 3.00V, I _{OL} = 0.1mA	—	—	0.4	V
R _I	Pull-up resistance $\overline{AC}$, $\overline{CS}$	V _{DD} = 3.30V	30	—	150	kΩ
V _{TCK}	External clock input width	3.00V ≤ V _{DD} ≤ 3.60V	0.9 X V _{DD}	—	V _{DD}	V

Notes 1: The current from the IC must not exceed - 0.1 mA/port at any of the port pins (P0 to P7).

2: The current flowing into the IC must not exceed 0.1 mA/port at any of port pins (P0 to P7).

NOTE FOR SUPPLYING POWER

(1) Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35074-XXXSP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin in hysteresis input with the pull-up resistor.

The timing about power supplying of $\overline{AC}$ pin is shown in Figure 15.

After supplying the power (V_{DD} and V_{SS}) to M35074-XXXSP and the supply voltage becomes more than $0.8 \times V_{DD}$, it needs to keep V_{IL} time; t_w of the $\overline{AC}$ pin for more than 1ms.

Start inputting from microcomputer after $\overline{AC}$ pin supply voltage becomes more than $0.8 \times V_{DD}$ and keeping 200ms wait time.

(2) Timing of power supplying to V_{DD1} and V_{DD2} .

Supply power to V_{DD1} and V_{DD2} at the same time.

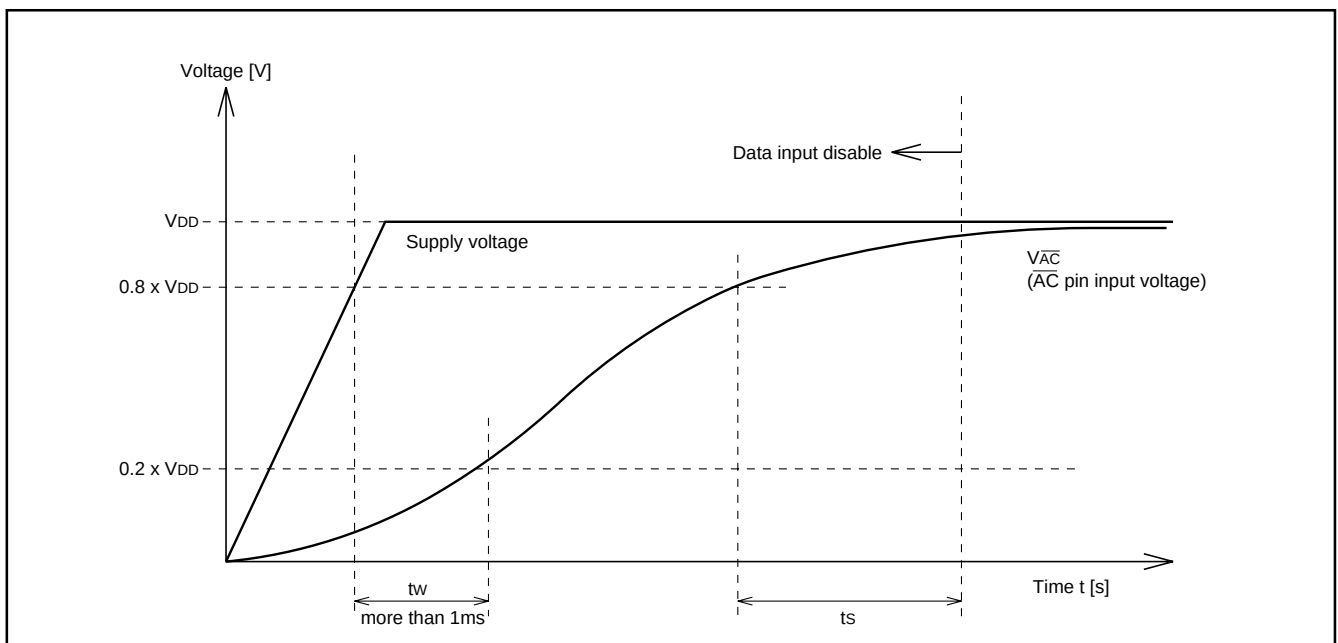


Fig.17 Timing of power supplying to $\overline{AC}$ pin

PRECAUTION FOR USE

Notes on noise and latch-up

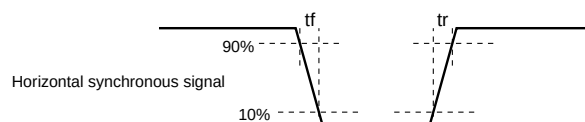
In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{DD1} pin and V_{SS1} pin, and the V_{DD2} pin and V_{SS2} pin using a heavy wire.

Note for waveform timing of the horizontal signals to the HOR pin

Set horizontal synchronous signal edge* waveform timing to under 5ns and input to HOR pin.

Set only the side which set by $B/\overline{F}$ register waveform timing under 5ns and input to HOR pin.

*: Set front porch edge or back porch edge by $B/\overline{F}$ register (address 127₁₆).



DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

- (1) M35074-XXXSP mask ROM order confirmation form
- (2) 20P4B mark specification form
- (3) ROM data : EPROMs or floppy disks

*In the case of EPROMs, three sets of EPROMs are required per pattern.

*In the case of floppy disks, 3.5-inch 2HD disk (1BM format) is required per pattern.

STANDARD ROM TYPE : M35074-002SP

M35074-002SP is a standard ROM type of M35074-XXXSP.
The character patterns are fixed to the contents of Figure 18 to 25.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

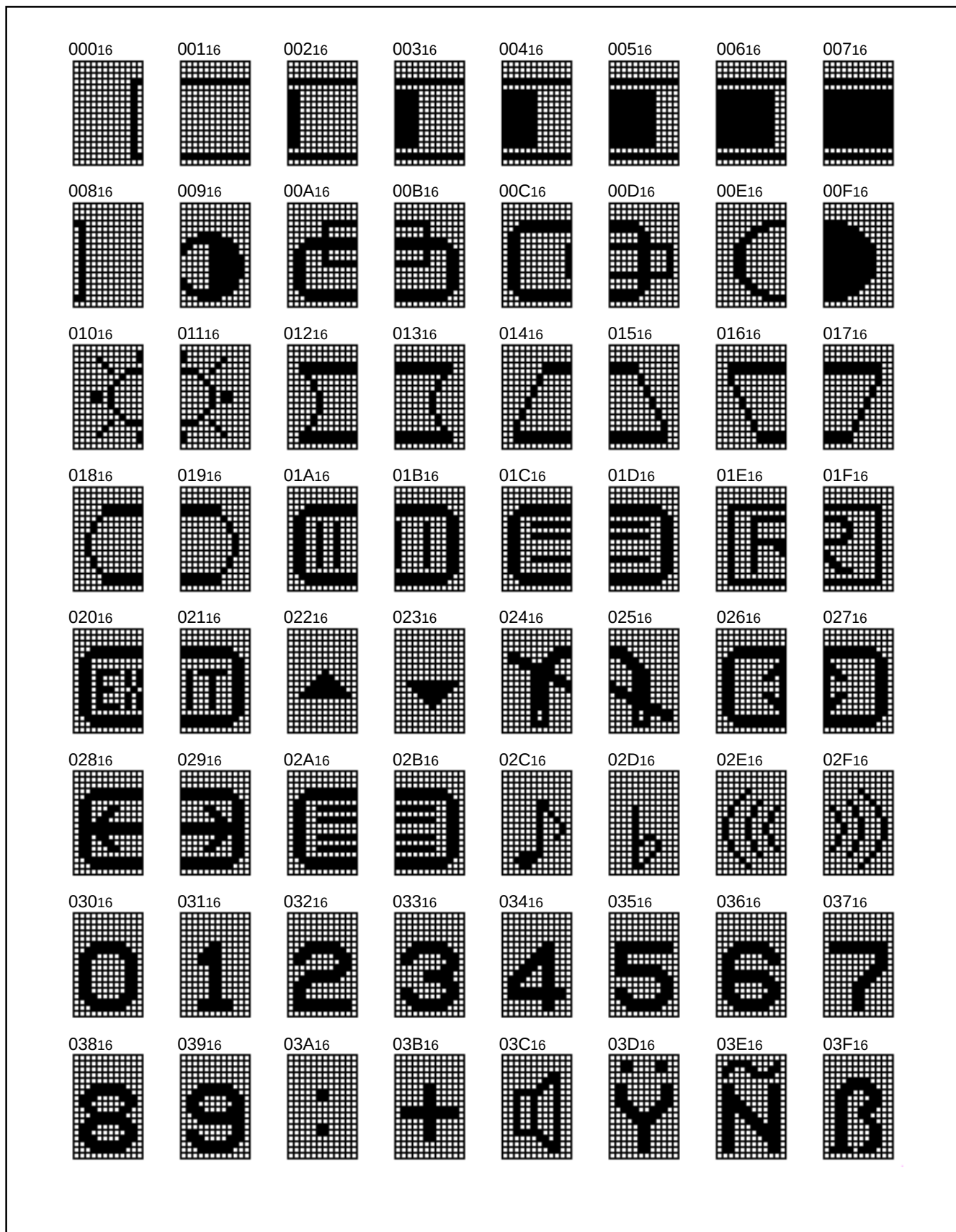


Fig.18 M35074-002SP character patterns (1)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

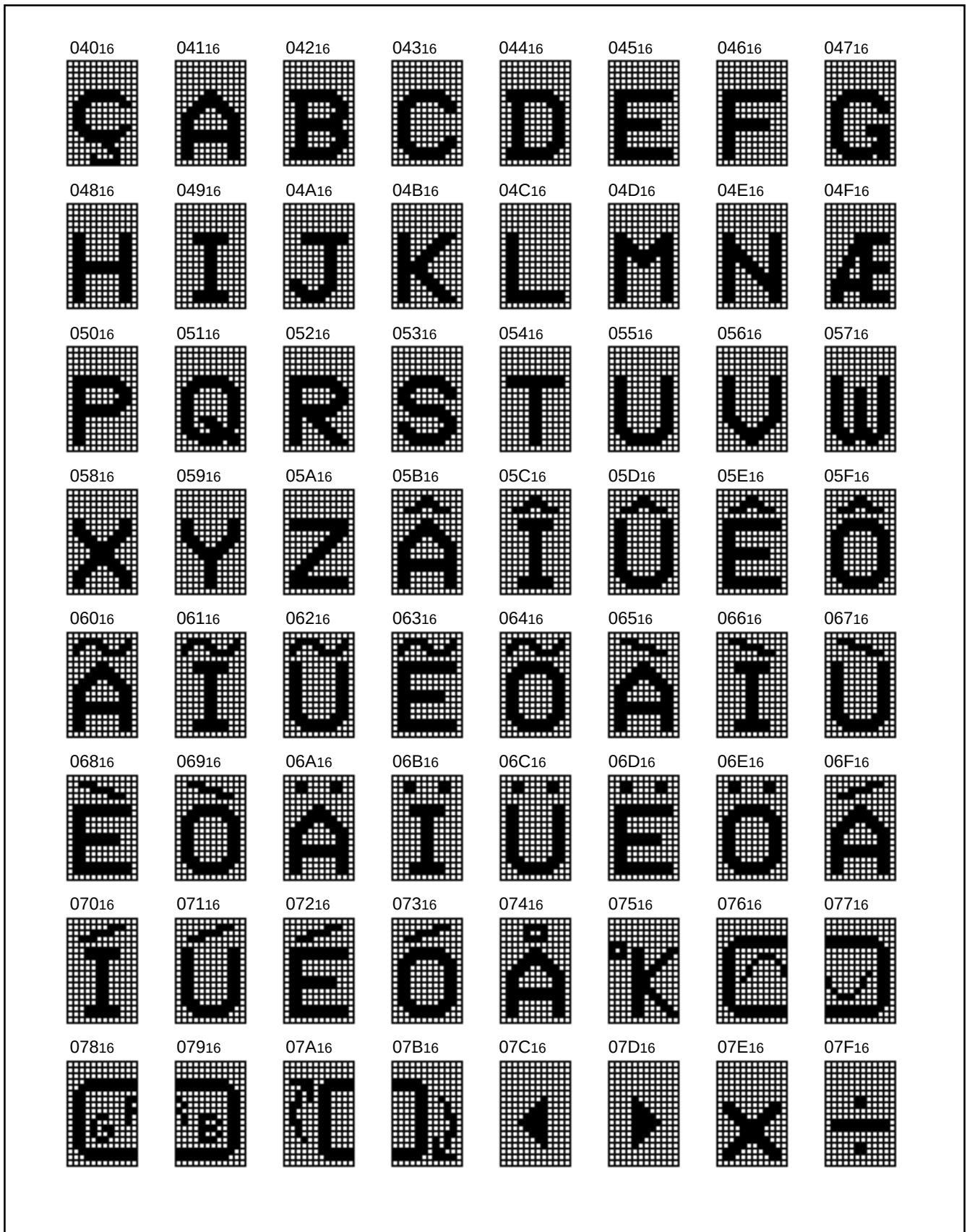


Fig.19 M35074-002SP character patterns (2)

08016	08116	08216	08316	08416	08516	08616	08716
/	a	b	c	d	e	f	g
08816	08916	08A16	08B16	08C16	08D16	08E16	08F16
h	i	j	k	l	m	n	o
09016	09116	09216	09316	09416	09516	09616	09716
p	q	r	s	t	u	v	w
09816	09916	09A16	09B16	09C16	09D16	09E16	09F16
x	y	z	â	î	û	ê	ô
0A016	0A116	0A216	0A316	0A416	0A516	0A616	0A716
ă	ı	ı	ı	ı	ă	ï	ù
0A816	0A916	0AA16	0AB16	0AC16	0AD16	0AE16	0AF16
ě	õ	à	ì	ù	è	ö	á
0B016	0B116	0B216	0B316	0B416	0B516	0B616	0B716
ĩ	ú	ë	õ	å	%	ñ	€
0B816	0B916	0BA16	0BB16	0BC16	0BD16	0BE16	0BF16
©	93	00	65	50	®	©	®

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Fig.21 M35074-002SP character patterns (4)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS



Fig.22 M35074-002SP character patterns (5)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS



Fig.23 M35074-002SP character patterns (6)

180 ₁₆ 	181 ₁₆ 	182 ₁₆ 	183 ₁₆ 	184 ₁₆ 	185 ₁₆ 	186 ₁₆ 	187 ₁₆
188 ₁₆ 	189 ₁₆ 	18A ₁₆ 	18B ₁₆ 	18C ₁₆ 	18D ₁₆ 	18E ₁₆ 	18F ₁₆
190 ₁₆ 	191 ₁₆ 	192 ₁₆ 	193 ₁₆ 	194 ₁₆ 	195 ₁₆ 	196 ₁₆ 	197 ₁₆
198 ₁₆ 	199 ₁₆ 	19A ₁₆ 	19B ₁₆ 	19C ₁₆ 	19D ₁₆ 	19E ₁₆ 	19F ₁₆
1A0 ₁₆ 	1A1 ₁₆ 	1A2 ₁₆ 	1A3 ₁₆ 	1A4 ₁₆ 	1A5 ₁₆ 	1A6 ₁₆ 	1A7 ₁₆
1A8 ₁₆ 	1A9 ₁₆ 	1AA ₁₆ 	1AB ₁₆ 	1AC ₁₆ 	1AD ₁₆ 	1AE ₁₆ 	1AF ₁₆
1B0 ₁₆ 	1B1 ₁₆ 	1B2 ₁₆ 	1B3 ₁₆ 	1B4 ₁₆ 	1B5 ₁₆ 	1B6 ₁₆ 	1B7 ₁₆
1B8 ₁₆ 	1B9 ₁₆ 	1BA ₁₆ 	1BB ₁₆ 	1BC ₁₆ 	1BD ₁₆ 	1BE ₁₆ 	1BF ₁₆

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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

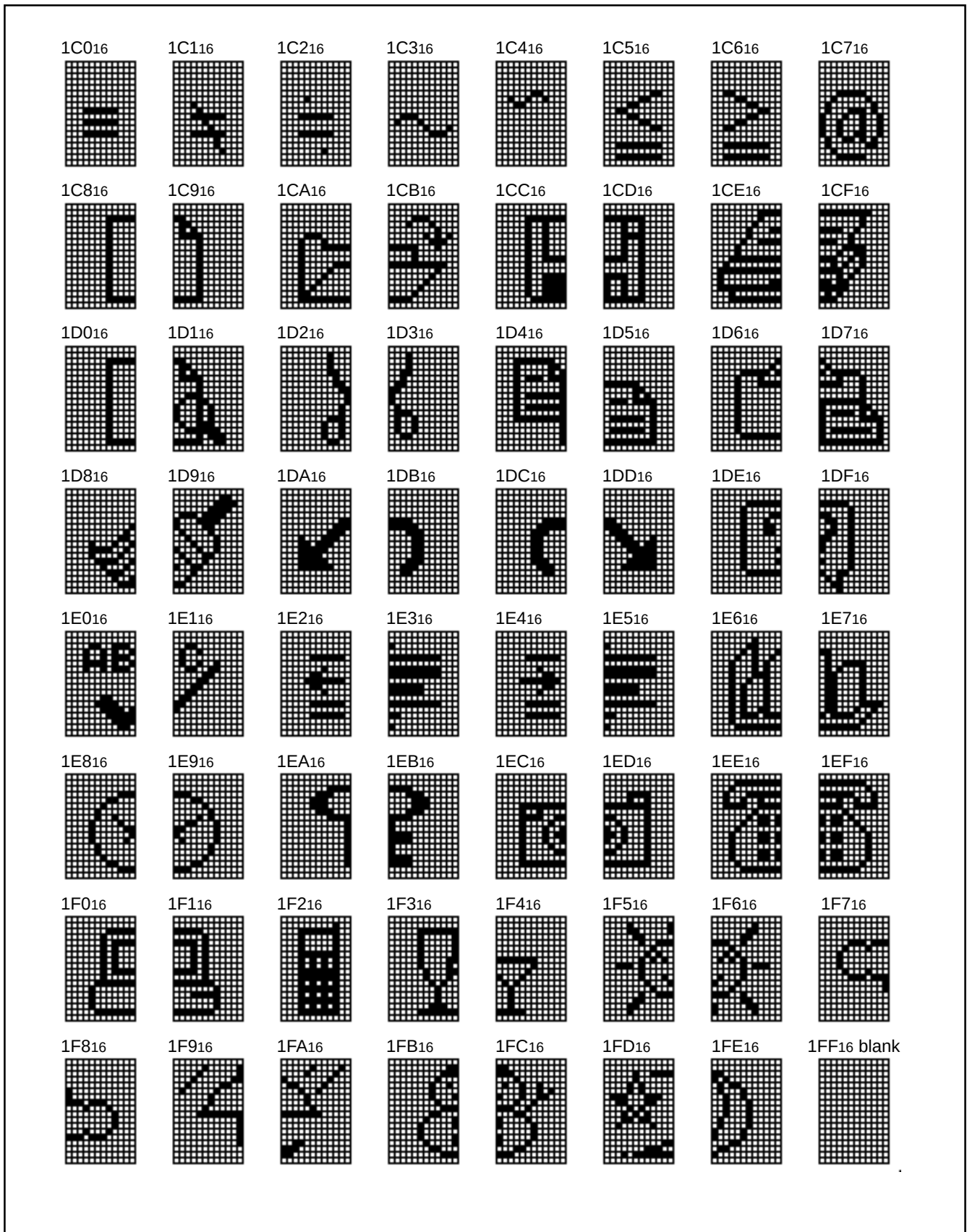
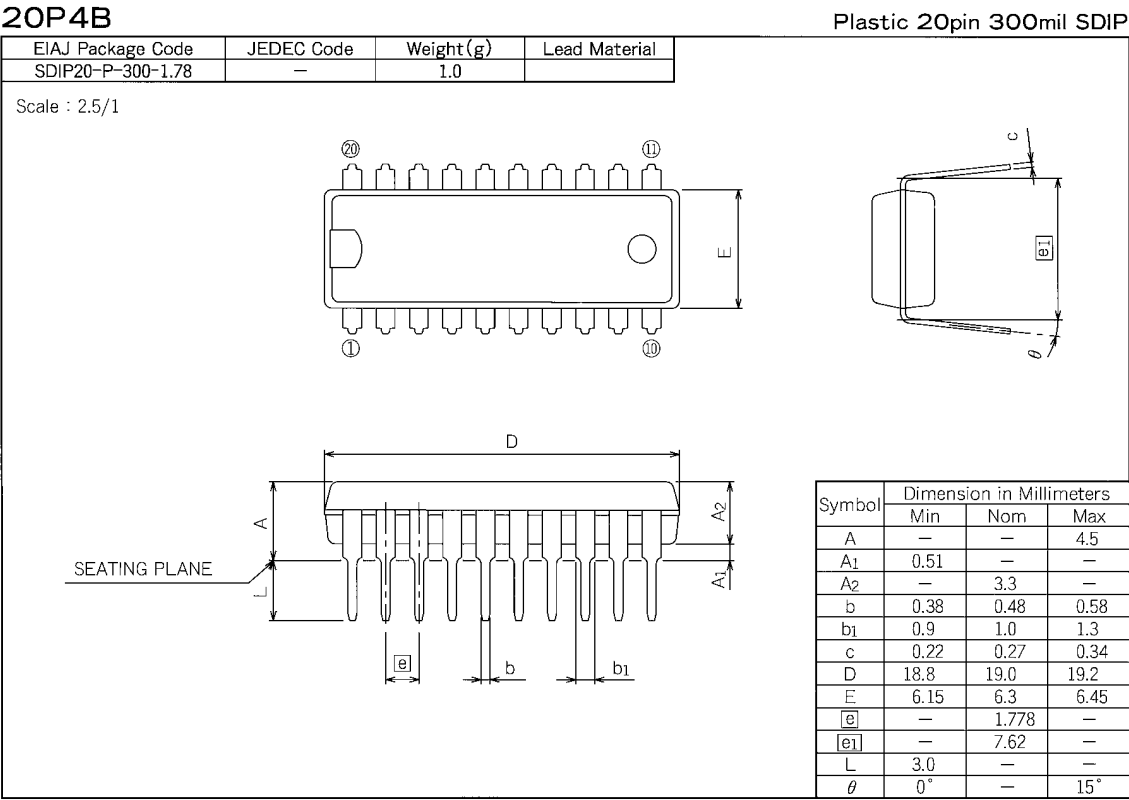


Fig.25 M35074-002SP character patterns (8)

PACKAGE OUTLINE



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REVISION DESCRIPTION LIST

M35074-XXXSP Data Sheet

Rev. No.	Revision Description	Rev. date																																																																						
1.0	First Edition	0111																																																																						
1.1	2nd Edition p10 <u>BEFORE</u> <table><tr><td>BLK0</td><td>BLK1</td><td>DSPn="0"</td><td>DSPn="1"</td></tr><tr><td>0</td><td>0</td><td>Matrix-outline border</td><td>Matrix-outline</td></tr><tr><td>0</td><td>1</td><td>Character</td><td>Border</td></tr><tr><td>1</td><td>0</td><td>Border</td><td>Matrix-outline</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline</td><td>Charcter</td></tr></table> (At register BCOL="0") <u>AFTER</u> <table><tr><td>BLK1</td><td>BLK0</td><td>DSPn="0"</td><td>DSPn="1"</td></tr><tr><td>0</td><td>0</td><td>Matrix-outline border</td><td>Matrix-outline</td></tr><tr><td>0</td><td>1</td><td>Character</td><td>Border</td></tr><tr><td>1</td><td>0</td><td>Border</td><td>Matrix-outline</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline</td><td>Charcter</td></tr></table> (At register BCOL="0") <u>BEFORE</u> <table><tr><td>BLK0</td><td>BLK1</td><td>Blanking mode</td></tr><tr><td>0</td><td>0</td><td>Matrix-outline size</td></tr><tr><td>0</td><td>1</td><td>Character size</td></tr><tr><td>1</td><td>0</td><td>Border size</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline size</td></tr></table> <u>AFTER</u> <table><tr><td>BLK1</td><td>BLK0</td><td>Blanking mode</td></tr><tr><td>0</td><td>0</td><td>Matrix-outline size</td></tr><tr><td>0</td><td>1</td><td>Character size</td></tr><tr><td>1</td><td>0</td><td>Border size</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline size</td></tr></table>	BLK0	BLK1	DSPn="0"	DSPn="1"	0	0	Matrix-outline border	Matrix-outline	0	1	Character	Border	1	0	Border	Matrix-outline	1	1	Matrix-outline	Charcter	BLK1	BLK0	DSPn="0"	DSPn="1"	0	0	Matrix-outline border	Matrix-outline	0	1	Character	Border	1	0	Border	Matrix-outline	1	1	Matrix-outline	Charcter	BLK0	BLK1	Blanking mode	0	0	Matrix-outline size	0	1	Character size	1	0	Border size	1	1	Matrix-outline size	BLK1	BLK0	Blanking mode	0	0	Matrix-outline size	0	1	Character size	1	0	Border size	1	1	Matrix-outline size	0202
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1.2	3rd Edition p1 FEATURES Data input By 16-bit → By 24-bit p2 PIN DESCRIPTION $\overline{CS}$, SCK/SCL, SIN/SDA Function <At 16-bit....> → <At 24-bit....> p14 (8) Address 127 ₁₆ B Remarks “Refer to REGISTER.....” → Deletion p21 DATA INPUT EXAMPLE “the 24-bit serial input function or” → Insertion p24 DATA INPUT 1 (d) “16 bits” → “24 bits”, Fig.11 (16 bits) → (24 bits) SERIAL DATA INPUT TIMING (d) “16 bits” → “24 bits” p25 Table Data input tword Limits “10” → “14”, Fig.12 SCK “12,13,14,15,16” → “20,21,22,23,24” p27 (2) Data input (Sequence) (d) “16 bits” → “24 bits”	0204																																																																						