

Product Summary

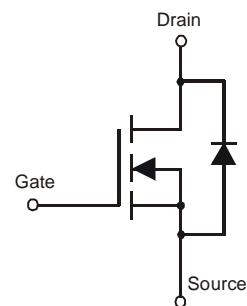
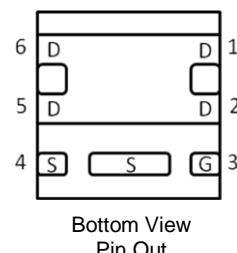
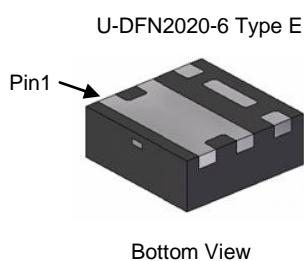
$V_{(BR)DSS}$	$R_{DS(on)}$ max	Package	I_D max $T_A = +25^\circ C$
20V	11.6m Ω @ $V_{GS} = 4.5V$	U-DFN2020-6 Type E	10.5A
	15m Ω @ $V_{GS} = 2.5V$		9.4A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- General Purpose Interfacing Switch
- Power Management Functions



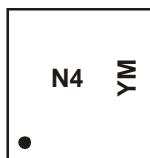
Ordering Information (Note 4)

Part Number	Marking	Reel size (inches)	Quantity per reel
DMN2015UFDE-7	N4	7	3,000
DMN2015UFDE-13	N4	13	10,000

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



N4 = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: Y = 2011)
 M = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017					
Code	Y	Z	A	B	C	D	E					
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	20	V
Gate-Source Voltage			V_{GSS}	± 12	V
Continuous Drain Current (Note 6) $V_{GS} = 4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	10.5 8.5	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	12.5 10.0	A
Continuous Drain Current (Note 6) $V_{GS} = 2.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	9.4 7.5	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	11.2 8.8	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	80	A
Maximum Body Diode Continuous Current			I_S	2.5	A

Thermal Characteristics

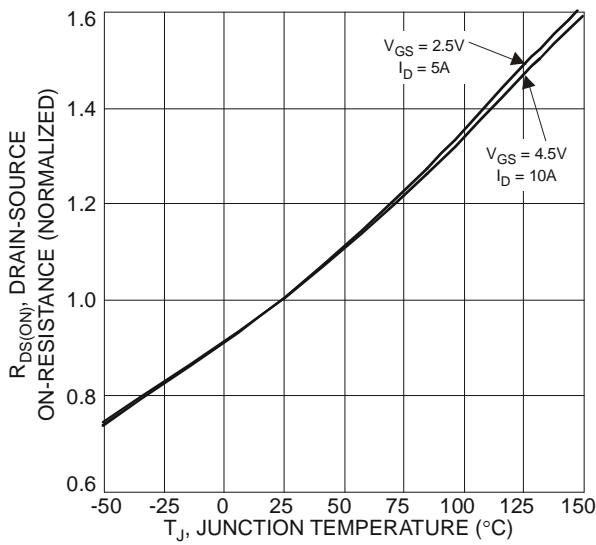
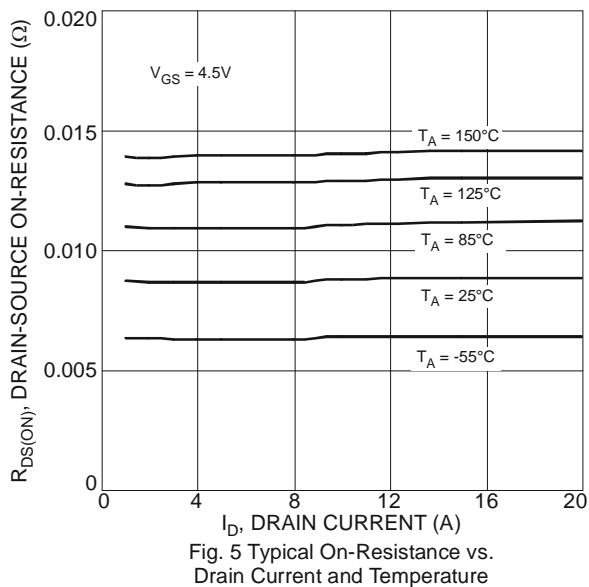
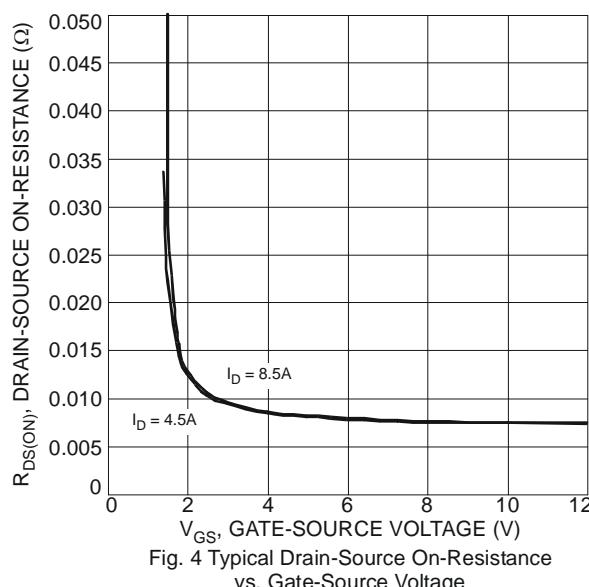
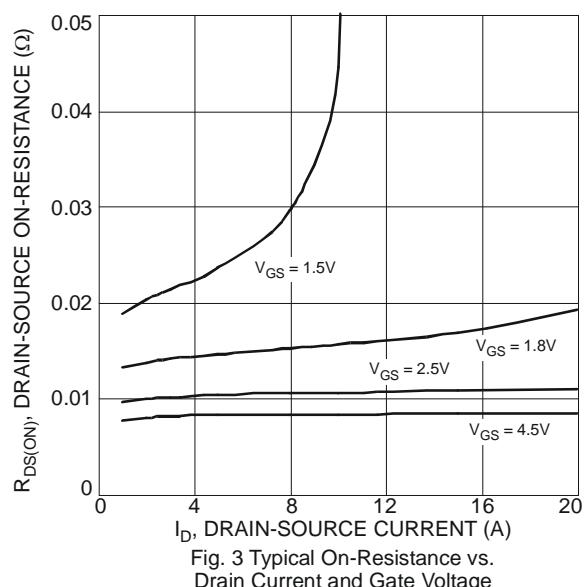
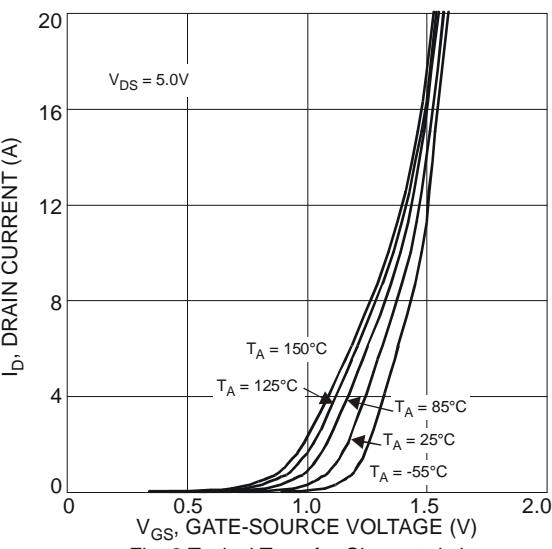
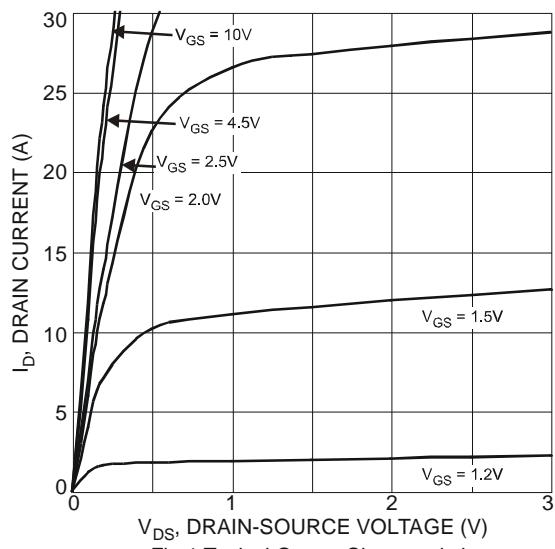
Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	0.66	W
	$T_A = +70^\circ\text{C}$		0.42	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	189	°C/W
	$t < 10\text{s}$		132	
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	2.03	W
	$T_A = +70^\circ\text{C}$		1.31	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	61	°C/W
	$t < 10\text{s}$		43	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	9.3	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	1	μA	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	0.5	—	1.1	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	—	9.3	11.6	$\text{m}\Omega$	$V_{GS} = 4.5\text{V}, I_D = 8.5\text{A}$
			11.4	15		$V_{GS} = 2.5\text{V}, I_D = 8.5\text{A}$
			17	30		$V_{GS} = 1.8\text{V}, I_D = 5\text{A}$
			24	50		$V_{GS} = 1.5\text{V}, I_D = 3\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	—	11.3	—	S	$V_{DS} = 10\text{V}, I_D = 8.5\text{A}$
Diode Forward Voltage	V_{SD}	—	—	1.2	V	$V_{GS} = 0\text{V}, I_S = 8.5\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	1779	—	pF	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	175	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	154	—	pF	
Gate Resistance	R_g	—	0.94	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	19.7	—	nC	$V_{DS} = 10\text{V}, I_D = 8.5\text{A}$
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	45.6	—	nC	
Gate-Source Charge	Q_{gs}	—	2.9	—	nC	
Gate-Drain Charge	Q_{gd}	—	3.8	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	7.4	—	ns	$V_{DS} = 10\text{V}, I_D = 8.5\text{A}$ $V_{GS} = 4.5\text{V}, R_G = 1.8\Omega$
Turn-On Rise Time	t_r	—	16.8	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	43.6	—	ns	
Turn-Off Fall Time	t_f	—	10.9	—	ns	
Reverse Recovery Time	T_{rr}	—	8.6	—	ns	$I_F = 8.5\text{A}, di/dt = 210\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}	—	3.7	—	nC	

Notes:

- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
- Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
- Short duration pulse test used to minimize self-heating effect.
- Guaranteed by design. Not subject to production testing.



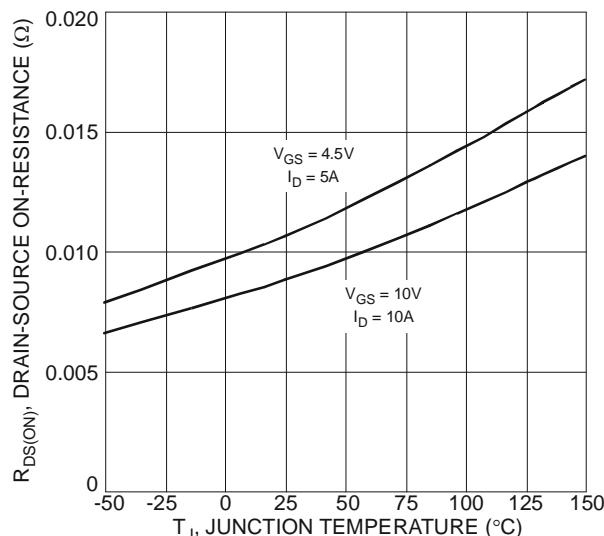


Fig. 7 On-Resistance Variation with Temperature

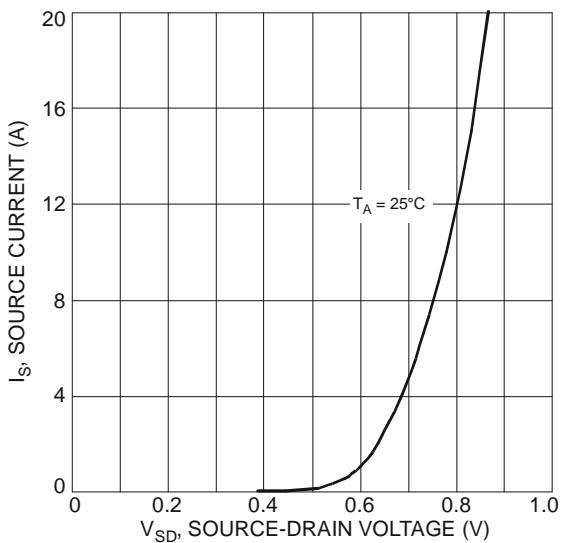


Fig. 9 Diode Forward Voltage vs. Current

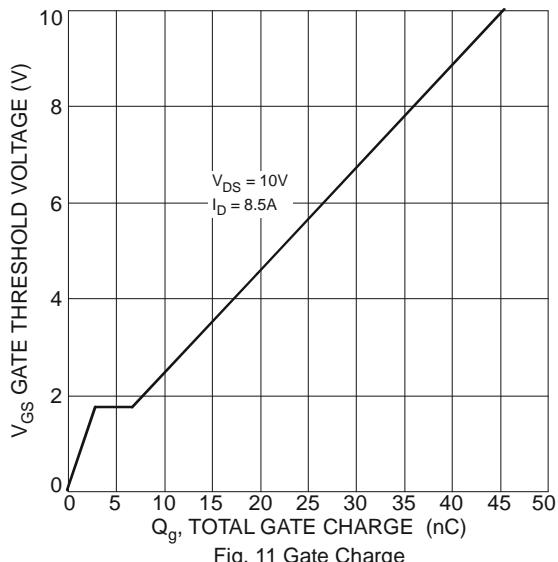


Fig. 11 Gate Charge

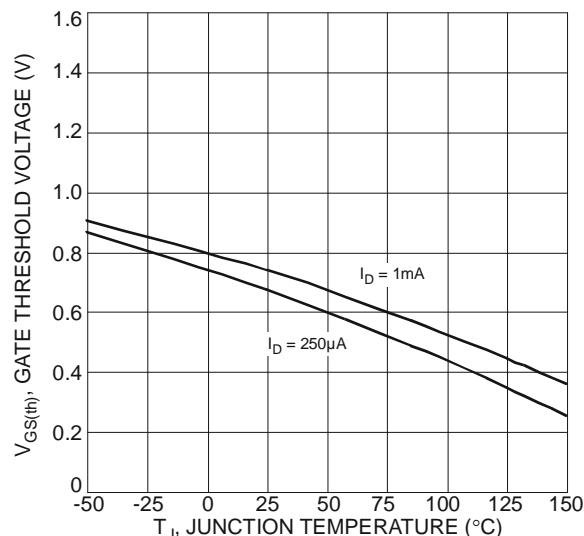


Fig. 8 Gate Threshold Variation vs. Ambient Temperature

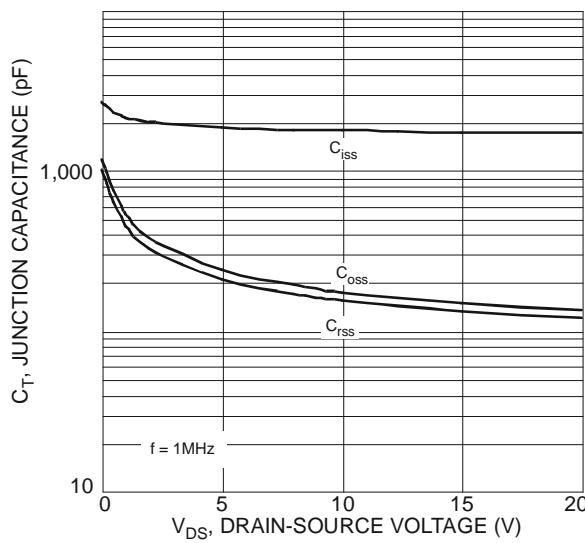


Fig. 10 Typical Junction Capacitance

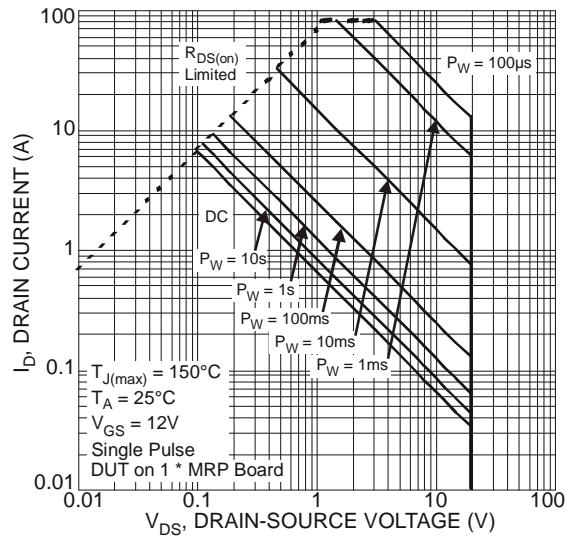
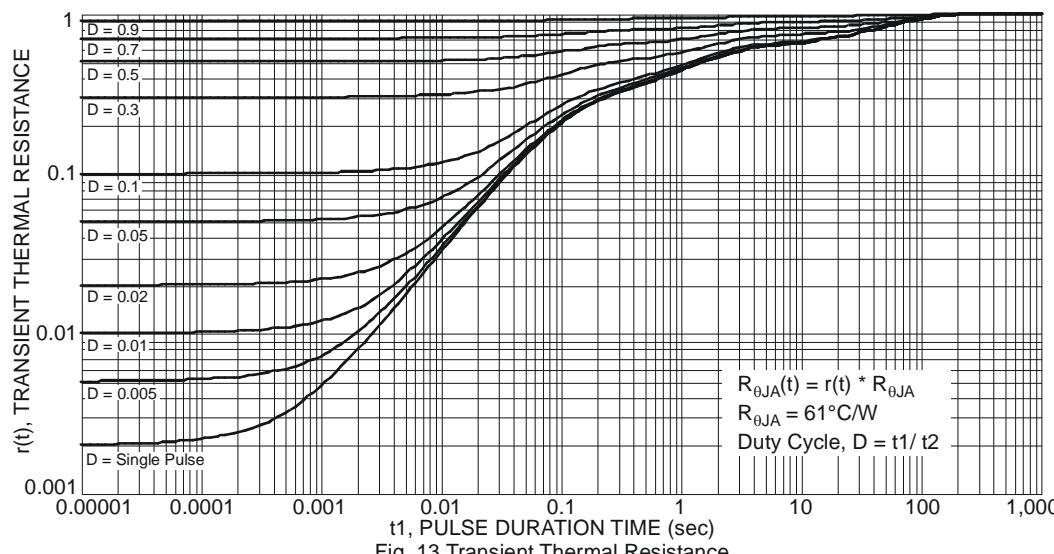
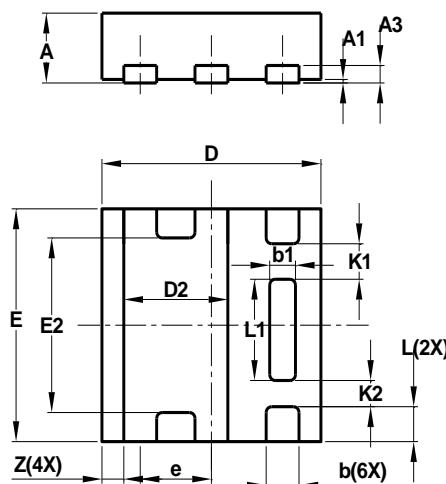


Fig. 12 SOA, Safe Operation Area



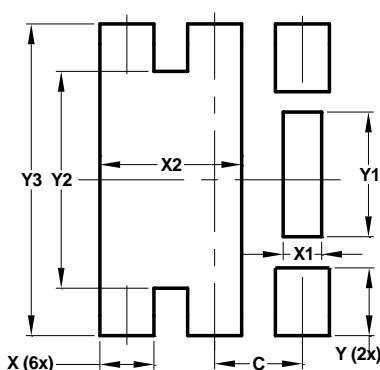
Package Outline Dimensions



U-DFN2020-6 Type E			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.03
A3	—	—	0.15
b	0.25	0.35	0.30
b1	0.185	0.285	0.235
D	1.95	2.05	2.00
D2	0.85	1.05	0.95
E	1.95	2.05	2.00
E2	1.40	1.60	1.50
e	—	—	0.65
L	0.25	0.35	0.30
L1	0.82	0.92	0.87
K1	—	—	0.305
K2	—	—	0.225
Z	—	—	0.20

All Dimensions in mm

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	0.285
X2	1.050
Y	0.500
Y1	0.920
Y2	1.600
Y3	2.300

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