

TLE202x High-Speed, Low-Power, Bipolar Precision Operational Amplifiers

1 Features

- Supply current: 300 μ A, max
- High unity-gain bandwidth: 2MHz
- High slew rate: 0.65V/ μ s
- Specified for both 5V single-supply and $\pm$ 15V operation
- Phase-reversal protection
- High open-loop gain: 6.5V/ μ V (136dB)
- Low offset voltage: 100 μ V, max
- Low input bias current: 50nA, max
- Low noise voltage: 19nV/ $\sqrt{\text{Hz}}$

2 Applications

- [Flow transmitter](#)
- [Lab and field instrumentation](#)
- [Analog input module](#)
- [Pressure transmitter](#)

3 Description

The TLE2021, TLE2022, and TLE2024 (TLE202x) devices are precision, high-speed, low-power operational amplifiers using a new Texas Instruments state-of-the art bipolar process. These devices combine the best features of the OP21, with a highly improved slew rate and unity-gain bandwidth.

The complementary bipolar process uses isolated vertical pnp transistors that yield dramatic improvement in unity-gain bandwidth and slew rate over similar devices.

The addition of a bias circuit in conjunction with this process results in extremely stable parameters with both time and temperature. Therefore, a precision

device remains a precision device even with changes in temperature and over years of use.

This combination of excellent dc performance with a common-mode input voltage range that includes the negative rail makes these devices an excellent choice for low-level signal conditioning applications in either single-supply or split-supply configurations. In addition, these devices offer phase-reversal protection circuitry that eliminates an unexpected change in output states when one of the inputs is less than the negative supply rail.

A variety of available options includes small-outline and chip-carrier versions for high-density systems applications.

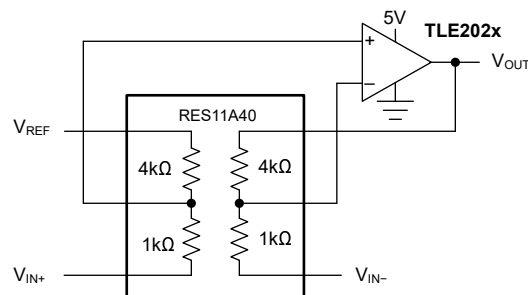
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to +85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to +125°C.

Device Information

PART NUMBER ⁽¹⁾	CHANNEL COUNT	PACKAGE ⁽²⁾
TLE2021	Single	D (SOIC, 8)
		P (PDIP, 8)
TLE2022	Dual	D (SOIC, 8)
		P (PDIP, 8)
TLE2024	Quad	DW (SOIC, 16)
		N (PDIP, 14)

(1) See [Section 4](#).

(2) For more information, see [Section 10](#).



Difference Amplifier Circuit With the RES11A



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4 Device Comparison Tables

Table 4-1. TLE2021 Available Options

TEMPERATURE RANGE	INPUT OFFSET VOLTAGE	PART NUMBER	PACKAGES
0°C to 70°C	500µV 200µV	TLE2021C TLE2021AC	D (SOIC, 8) P (PDIP, 8)
–40°C to 85°C	500µV 200µV	TLE2021I TLE2021AI	D (SOIC, 8) P (PDIP, 8)
–55°C to 125°C	500µV	TLE2021M	D (SOIC, 8)

Table 4-2. TLE2022 Available Options

TEMPERATURE RANGE	INPUT OFFSET VOLTAGE	PART NUMBER	PACKAGES
0°C to 70°C	500µV 300µV	TLE2022C TLE2022AC	D (SOIC, 8) P (PDIP, 8)
–40°C to 85°C	500µV 300µV	TLE2022I TLE2022AI	D (SOIC, 8) P (PDIP, 8)
–55°C to 125°C	500µV 300µV	TLE2022M TLE2022AM	D (SOIC, 8)

Table 4-3. TLE2024 Available Options

TEMPERATURE RANGE	INPUT OFFSET VOLTAGE	PART NUMBER	PACKAGES
0°C to 70°C	1000µV 750µV	TLE2024C TLE2024AC	DW (SOIC, 16) N (PDIP, 14)
–40°C to 85°C	1000µV 750µV	TLE2024I TLE2024AI	DW (SOIC, 16) N (PDIP, 14)
–55°C to 125°C	500µV	TLE2024BM	DW (SOIC, 16)

5 Pin Configuration and Functions

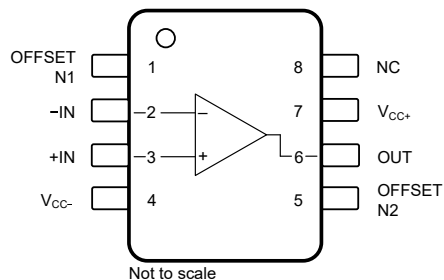


Figure 5-1. TLE2021: D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP (Top View)

Table 5-1. Pin Functions: TLE2021

PIN		TYPE	DESCRIPTION
NAME	NO. D (SOIC), P (PDIP)		
-IN	2	Input	Inverting input
+IN	3	Input	Noninverting input
NC	8	—	No connection
OFFSET N1	1	—	External input offset voltage adjustment
OFFSET N2	2	—	External input offset voltage adjustment
OUT	6	Output	Output
V _{CC-}	4	Power	Negative (lowest) power supply
V _{CC+}	7	Power	Positive (highest) power supply

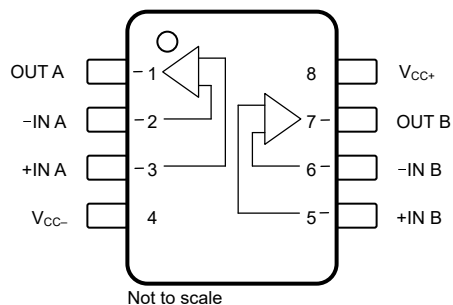


Figure 5-2. TLE2022: D Package, 8-Pin SOIC and P Package, 8-Pin PDIP (Top View)

Table 5-2. Pin Functions: TLE2022

PIN		TYPE	DESCRIPTION
NAME	NO. D (SOIC), P (PDIP)		
-IN A	2	Input	Inverting input channel A
-IN B	6	Input	Inverting input channel B
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
NC	—	—	No connection
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
V _{CC-}	4	Power	Negative supply
V _{CC+}	8	Power	Positive supply

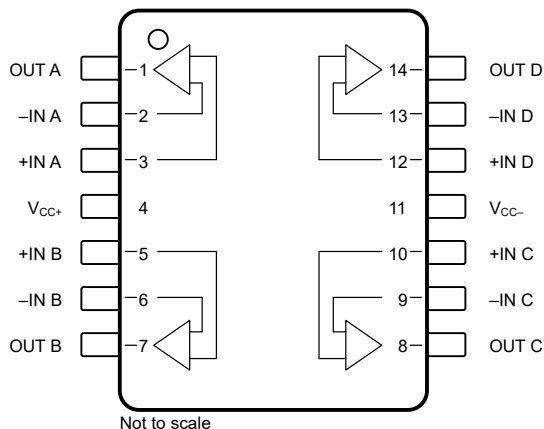


Figure 5-3. TLE2024: N Package, 14-Pin PDIP (Top View)

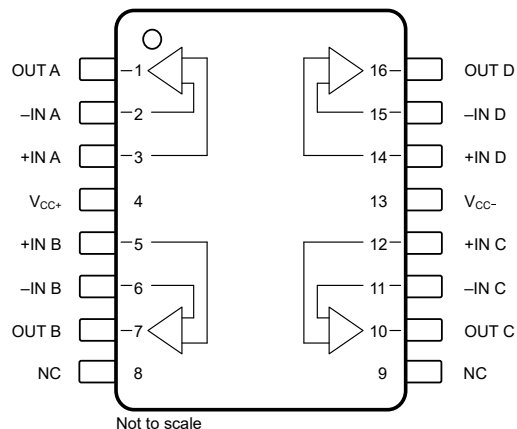


Figure 5-4. TLE2024: DW Package, 16-Pin (Top View)

Table 5-3. Pin Functions: TLE2024

NAME	PIN NO.		TYPE	DESCRIPTION
	N (PDIP), J (CDIP)	DW (SOIC)		
-IN A	2	2	Input	Inverting input channel A
-IN B	6	6	Input	Inverting input channel B
-IN C	9	11	Input	Inverting input channel C
-IN D	13	15	Input	Inverting input channel D
+IN A	3	3	Input	Noninverting input channel A
+IN B	5	5	Input	Noninverting input channel B
+IN C	10	12	Input	Noninverting input channel C
+IN D	12	14	Input	Noninverting input channel D
NC	—	8, 9	—	No connection
OUT A	1	1	Output	Output channel A
OUT B	7	7	Output	Output channel B
OUT C	8	10	Output	Output channel C
OUT D	14	16	Output	Output channel D
V _{CC-}	11	13	Power	Negative supply
V _{CC+}	4	4	Power	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC+}	Supply voltage (positive)			20	V
V _{CC-}	Supply voltage (negative)			-20	V
V _{ID}	Differential input voltage ⁽²⁾			±0.6	V
V _I	Input voltage (any input)			±V _{CC}	V
I _I	Input current (each input)			±1	mA
I _O	Output current (each output)	TLE2021		±20	mA
		TLE2022		±30	
		TLE2024		±40	
	Total current into V _{CC+}			80	mA
	Total current out of V _{CC-}			80	mA
	Duration of short-circuit current at (or below) 25°C ⁽⁴⁾			Unlimited	
	Lead temperature 1.6mm (1/16in) from case, D and P package (10s)			260	°C
T _A	Operating free-air temperature	C suffix	0	70	°C
		I suffix	-40	85	
		M suffix	-55	150	
T _{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Differential voltages are at IN+ with respect to IN-. Excessive current flows if a differential input voltage in excess of approximately ±600mV is applied between the inputs unless some limiting resistance is used.
- (3) Do not short the output to V_{CC+}. Limit temperature, supply voltages or both to not exceed maximum dissipation ratings.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage, V _{CC} = (V _{CC+}) – (V _{CC-})		3		15.5	V
V _{IC}	Common mode input voltage	V _{CC} = 5V, C suffix	0		3.5	V
		V _{CC} = 5V, I and M suffix	0		3.2	
		V _{CC±} = ±15V, C suffix	-15		13.5	
		V _{CC±} = ±15V, I and M suffix	-15		13.2	
T _A	Operating free-air temperature	C suffix	0		70	°C
		I suffix	-40		85	
		M suffix	-55		125	

6.3 Thermal Information for TLE2021

THERMAL METRIC ⁽¹⁾		TLE2021		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	129.1	84.5	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	68.8	62.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	76.8	46.8	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	15.7	29.8	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	75.8	46.2	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.4 Thermal Information for TLE2022

THERMAL METRIC ⁽¹⁾		TLE2022		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	122.4	76.2	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	61.5	55.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	70.0	39.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	11.2	21.7	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	69.1	38.9	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information for TLE2024

THERMAL METRIC ⁽¹⁾		TLE2024		UNIT
		DW (SOIC)	N (PDIP)	
		16 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	62.7	53.9	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	28.0	30.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	31.6	25.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	4.3	9.0	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	31.0	24.7	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics for TLE2021, $V_{CC} = \pm 15V$

at $T_A = 25^\circ C$, $V_{CC} = \pm 15V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V _{IO}	Input offset voltage	TLE2021C R _S = 50Ω		±120	±500	μV	
			T _A = 0°C to 70°C	±750			
		TLE2021AC R _S = 50Ω		±80	±200		
			T _A = 0°C to 70°C	±500			
		TLE2021I R _S = 50Ω		±120	±500		
			T _A = −40°C to +85°C	±850			
		TLE2021AI R _S = 50Ω		±80	±200		
			T _A = −40°C to +85°C	±500			
TLE2021M R _S = 50Ω		±120	±500				
	T _A = −55°C to +125°C	±1000					
dV _{IO} /dT	Input offset voltage drift	TLE2021C, TLE2021AC R _S = 50Ω, T _A = 0°C to 70°C		±2		μV/°C	
		TLE2021I, TLE2021AI R _S = 50Ω, T _A = −40°C to +85°C		±2			
		TLE2022M R _S = 50Ω, T _A = −55°C to +125°C		±2			
I _{IB}	Input bias current	TLE2021C, TLE2021AC R _S = 50Ω		25	70	nA	
			T _A = 0°C to 70°C	90			
		TLE2021I, TLE2021AI R _S = 50Ω		25	70		
			T _A = −40C to +85°C	90			
		TLE2021M R _S = 50Ω		25	70		
T _A = −55°C to +125°C	90						
I _{IO}	Input offset current	TLE2021C, TLE2021AC R _S = 50Ω		0.2	6	nA	
			T _A = 0°C to 70°C	10			
		TLE2021I, TLE2021AI R _S = 50Ω		0.2	6		
			T _A = −40°C to +85°C	10			
		TLE2021M R _S = 50Ω		0.2	6		
T _A = −55°C to +125°C	10						
PSRR	Power-supply rejection ratio	TLE2021IC, TLE2021AC V _{CC±} = ±2.5 to ±15V		105	120	dB	
			T _A = 0°C to 70°C	100			
		TLE2021I, TLE2021AI V _{CC±} = ±2.5 to ±15V		105	120		
			T _A = −40°C to +85°C	100			
		TLE2021M V _{CC±} = ±2.5 to ±15V		105	120		
T _A = −55°C to +125°C	100						
A _V	Large signal voltage gain	TLE2021C, TLE2021AC R _L = 10kΩ, −10V ≤ V _O ≤ 10V		1	6.5	V/μV	
			T _A = 0°C to 70°C	1			
		TLE2021I, TLE2021AI R _L = 10kΩ, −10V ≤ V _O ≤ 10V		1	6.5		
			T _A = −40°C to +85°C	0.75			
		TLE2021M R _L = 10kΩ, −10V ≤ V _O ≤ 10V		1	6.5		
T _A = −55°C to +125°C	0.5						

6.6 Electrical Characteristics for TLE2021, $V_{CC} = \pm 15V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = \pm 15V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	TLE2021C, TLE2021AC To positive rail, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	13.5	14		V
				13.5			
		TLE2021C, TLE2021AC To negative rail, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	-15	-15.3		
				-15			
		TLE2021I, TLE2021AI To positive rail, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	13.5	14		
				13.2			
		TLE2021I, TLE2021AI To negative rail, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	-15	-15.3		
				-15			
CMRR	Common-mode rejection ratio	TLE2021M To positive rail, $R_S = 50\Omega$	$T_A = -55^\circ C$ to $+125^\circ C$	13.5	14		dB
				13.2			
		TLE2021M To negative rail, $R_S = 50\Omega$	$T_A = -55^\circ C$ to $+125^\circ C$	-15	-15.3		
				-15			
		TLE2021C, TLE2021AC $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	100	115		
				96			
		TLE2021I, TLE2021AI $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	100	115		
				96			
V_O	Voltage output swing	TLE2021C, TLE2021AC $R_L = 10k\Omega$	Positive	14	14.3		V
			Positive, $T_A = 0^\circ C$ to $70^\circ C$	13.9			
			Negative		-14.1	-13.7	
			Negative, $T_A = 0^\circ C$ to $70^\circ C$			-13.7	
		TLE2021I, TLE2021AI $R_L = 10k\Omega$	Positive	14	14.3		
			Positive, $T_A = -40^\circ C$ to $+85^\circ C$	13.9			
			Negative		-14.1	-13.7	
			Negative, $T_A = -40^\circ C$ to $+85^\circ C$			-13.6	
		TLE2021M $R_L = 10k\Omega$	Positive	14	14.3		
			Positive, $T_A = -55^\circ C$ to $+125^\circ C$	13.8			
			Negative		-14.1	-13.7	
			Negative, $T_A = -55^\circ C$ to $+125^\circ C$			-13.6	
I_{CC}	Supply current	No load TLE2021IC, TLE2021AC	$T_A = 0^\circ C$ to $70^\circ C$		240	350	μA
						350	
		No load TLE2021I, TLE2021AI	$T_A = -40^\circ C$ to $+85^\circ C$		240	350	
						350	
		No load TLE2021M			200	300	
			$T_A = -55^\circ C$ to $+125^\circ C$			300	

6.6 Electrical Characteristics for TLE2021, $V_{CC} = \pm 15V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = \pm 15V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC SPECS							
SR	Slew rate	V _O = ±10V, G = 1		0.65			V/μs
e _N	Input voltage noise density	f = 10Hz	TLE2021xC, TLE2021xI	19	50	nV/√Hz	
			TLE2021M	19			
		f = 1kHz	TLE2021xC, TLE2021xI	15	30		
			TLE2021M	15			
	Input voltage noise	f = 0.1Hz to 1Hz		0.16		μV _{PP}	
		f = 0.1Hz to 10Hz		0.47			
	Input current noise			0.09		pA/√Hz	
GBW	Gain bandwidth	G = 1		2			MHz
Θ _M	Phase margin			46°			

6.7 Electrical Characteristics for TLE2021, $V_{CC} = 5V$

at $T_A = 25^\circ C$, $V_{CC} = 5V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V _{IO}	Input offset voltage	TLE2021C R _S = 50Ω		±120	±600	μV	
			T _A = 0°C to 70°C	±850			
		TLE2021AC R _S = 50Ω		±100	±300		
			T _A = 0°C to 70°C	±600			
		TLE2021I R _S = 50Ω		±120	±600		
			T _A = −40°C to +85°C	±950			
		TLE2021AI R _S = 50Ω		±100	±300		
			T _A = −40°C to +85°C	±600			
TLE2021M R _S = 50Ω		±120	±600				
	T _A = −55°C to +125°C	±1100					
dV _{IO} /dT	Input offset voltage drift	TLE2021C, TLE2021AC T _A = 0°C to 70°C		±2		μV/°C	
		TLE2021I, TLE2021AI T _A = −40°C to +85°C		±2			
		TLE2021M T _A = −55°C to +125°C		±2			
I _{IB}	Input bias current	TLE2021C, TLE2021AC R _S = 50Ω		25	70	nA	
			T _A = 0°C to 70°C	90			
		TLE2021I, TLE2021AI R _S = 50Ω		25	70		
			T _A = −40°C to +85°C	90			
		TLE2021M R _S = 50Ω		25	70		
T _A = −55°C to +125°C	90						
I _{IO}	Input offset current	TLE2021C, TLE2021AC R _S = 50Ω		0.2	6	nA	
			T _A = 0°C to 70°C	10			
		TLE2021I, TLE2021AI R _S = 50Ω		0.2	6		
			T _A = −40°C to +85°C	10			
		TLE2021M R _S = 50Ω		0.2	6		
T _A = −55°C to +125°C	10						
PSRR	Power-supply rejection ratio	TLE2021C, TLE2021AC V _{CC} = 5V to 30V		105	120	dB	
			T _A = 0°C to 70°C	100			
		TLE2021I, TLE2021AI V _{CC} = 5V to 30V		105	120		
			T _A = −40°C to +85°C	100			
		TLE2021M V _{CC} = 5V to 30V		105	120		
T _A = −55°C to +125°C	100						
A _V	Large signal voltage gain	TLE2021C, TLE2021AC R _L = 10kΩ, 1.4V ≤ V _O ≤ 4V		0.3	1.5	V/μV	
			T _A = 0°C to 70°C	0.3			
		TLE2021I, TLE2021AI R _L = 10kΩ, 1.4V ≤ V _O ≤ 4V		0.3	1.5		
			T _A = −40°C to +85°C	0.25			
		TLE2021M R _L = 10kΩ, 1.4V ≤ V _O ≤ 4V		0.3	1.5		
T _A = −55°C to +125°C	0.1						

6.7 Electrical Characteristics for TLE2021, $V_{CC} = 5V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = 5V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	TLE2021C, TLE2021AC To positive rail, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	3.5	4		V
				3.5			
		TLE2021C, TLE2021AC To negative rail, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	0	–0.3		
				0			
		TLE2021I, TLE2021AI To positive rail, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	3.5	4		
				3.2			
		TLE2021I, TLE2021AI To negative rail, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	0	–0.3		
				0			
$CMRR$	Common-mode rejection ratio	TLE2021C, TLE2021AC $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	85	110		dB
				80			
		TLE2021I, TLE2021AI $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	85	110		
				80			
		TLE2021M $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = -55^\circ C$ to $+125^\circ C$	85	110		
				80			
V_O	Voltage output swing	TLE2021C, TLE2021AC $R_L = 10k\Omega$	Positive	4	4.3		V
			Positive, $T_A = 0^\circ C$ to $70^\circ C$	3.9			
			Negative		0.7	0.8	
			Negative, $T_A = 0^\circ C$ to $70^\circ C$			0.85	
		TLE2021I, TLE2021AI $R_L = 10k\Omega$	Positive	4	4.3		
			Positive, $T_A = -40^\circ C$ to $+85^\circ C$	3.9			
			Negative		0.7	0.8	
			Negative, $T_A = -40^\circ C$ to $+85^\circ C$			0.9	
		TLE2021M $R_L = 10k\Omega$	Positive	4	4.3		
			Positive, $T_A = -55^\circ C$ to $+125^\circ C$	3.8			
			Negative		0.7	0.8	
			Negative, $T_A = -55^\circ C$ to $+125^\circ C$			0.95	
I_{CC}	Supply current	No load TLE2021C, TLE2021AC	$T_A = 0^\circ C$ to $70^\circ C$		200	300	μA
						300	
		No load TLE2021I, TLE2021AI	$T_A = -40^\circ C$ to $+85^\circ C$		200	300	
						300	
		No load TLE2021M	$T_A = -55^\circ C$ to $+125^\circ C$		170	230	
						230	

6.7 Electrical Characteristics for TLE2021, $V_{CC} = 5V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = 5V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC SPECS							
SR	Slew rate	V _O = 1V to 3V, G = 1		0.5			V/μs
e _N	Input voltage noise density	f = 10Hz	TLE2021xC, TLE2021xI	21	50	nV/√Hz	
			TLE2021xM	21			
		f = 1kHz	TLE2021xC, TLE2021xI	17	30		
			TLE2021xM	17			
	Input voltage noise	f = 0.1Hz to 1Hz		0.16		μV	
		f = 0.1Hz to 10Hz		0.47			
	Input current noise			0.09		pA/√Hz	
GBW	Gain bandwidth	G = 1		1.2		MHz	
Θ _M	Phase margin			42°			

6.8 Electrical Characteristics for TLE2022, $V_{CC} = \pm 15V$

at $T_A = 25^\circ C$, $V_{CC} = \pm 15V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V _{IO}	Input offset voltage	TLE2022C R _S = 50Ω		±150	±500	μV	
			T _A = 0°C to 70°C	±700			
		TLE2022AC R _S = 50Ω		±120	±300		
			T _A = 0°C to 70°C	±450			
		TLE2022I R _S = 50Ω		±150	±500		
			T _A = −40°C to +85°C	±700			
		TLE2022AI R _S = 50Ω		±120	±300		
			T _A = −40°C to +85°C	±450			
TLE2022M R _S = 50Ω		±150	±500				
	T _A = −55°C to +125°C	±700					
TLE2022AM R _S = 50Ω		±120	±300				
	T _A = −55°C to +125°C	±450					
dV _{IO} /dT	Input offset voltage drift	TLE2022C, TLE2022AC R _S = 50Ω, T _A = 0°C to 70°C		±2		μV/°C	
		TLE2022I, TLE2022AI R _S = 50Ω, T _A = −40°C to +85°C		±2			
		TLE2022M, TLE2022AM R _S = 50Ω, T _A = −55°C to +125°C		±2			
I _{IB}	Input bias current	TLE2022C R _S = 50Ω		35	70	nA	
			T _A = 0°C to 70°C	90			
		TLE2022AC R _S = 50Ω		33	70		
			T _A = 0°C to 70°C	90			
		TLE2022I R _S = 50Ω		35	70		
			T _A = −40C to +85°C	90			
		TLE2022AI R _S = 50Ω		33	70		
			T _A = −40°C to +85°C	90			
TLE2022M R _S = 50Ω		35	70				
	T _A = −55°C to +125°C	90					
TLE2022AM R _S = 50Ω		33	70				
	T _A = −55°C to +125°C	90					
I _{IO}	Input offset current	TLE2022C R _S = 50Ω		0.5	6	nA	
			T _A = 0°C to 70°C	10			
		TLE2022AC R _S = 50Ω		0.4	6		
			T _A = 0°C to 70°C	10			
		TLE2022I R _S = 50Ω		0.5	6		
			T _A = −40°C to +85°C	10			
		TLE2022AI R _S = 50Ω		0.4	6		
			T _A = −40°C to +85°C	10			
TLE2022M R _S = 50Ω		0.5	6				
	T _A = −55°C to +125°C	10					
TLE2022AM R _S = 50Ω		0.4	6				
	T _A = −55°C to +125°C	10					

6.8 Electrical Characteristics for TLE2022, $V_{CC} = \pm 15V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = \pm 15V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power supply rejection ratio	TLE2022C $V_{CC\pm} = \pm 2.5V$ to $\pm 15V$		100	115	dB
		$T_A = 0^\circ C$ to $70^\circ C$	95			
		TLE2022AC $V_{CC\pm} = \pm 2.5V$ to $\pm 15V$		103	118	
		$T_A = 0^\circ C$ to $70^\circ C$	98			
		TLE2022I $V_{CC\pm} = \pm 2.5V$ to $\pm 15V$		100	115	
		$T_A = -40^\circ C$ to $+85^\circ C$	95			
		TLE2022AI $V_{CC\pm} = \pm 2.5V$ to $\pm 15V$		103	118	
A_v	Large signal voltage gain	$T_A = -40^\circ C$ to $+85^\circ C$	98			V/ μV
		TLE2022M $V_{CC\pm} = \pm 2.5V$ to $\pm 15V$		100	115	
		$T_A = -55^\circ C$ to $+125^\circ C$	95			
		TLE2022AM $V_{CC\pm} = \pm 2.5V$ to $\pm 15V$		103	118	
		$T_A = -55^\circ C$ to $+125^\circ C$	98			
		TLE2022IC, $R_L = 10k\Omega$, $V_O = \pm 10V$		0.8	4	
		$T_A = 0^\circ C$ to $70^\circ C$	0.8			
V_{IC}	Common-mode voltage	TLE2022AC $R_L = 10k\Omega$, $V_O = \pm 10V$		1	7	V
		$T_A = 0^\circ C$ to $70^\circ C$	1			
		TLE2022I $R_L = 10k\Omega$, $V_O = \pm 10V$		0.8	4	
		$T_A = -40^\circ C$ to $+85^\circ C$	0.8			
		TLE2022AI, $R_L = 10k\Omega$, $V_O = \pm 10V$		1	7	
		$T_A = -40^\circ C$ to $+85^\circ C$	1			
		TLE2022M $R_L = 10k\Omega$, $V_O = \pm 10V$		0.8	4	
		$T_A = -55^\circ C$ to $+125^\circ C$	0.8			
		TLE2022AM $R_L = 10k\Omega$, $V_O = \pm 10V$		1	7	
		$T_A = -55^\circ C$ to $+125^\circ C$	1			
		To positive rail, $R_S = 50\Omega$ TLE2022C, TLE2022AC		13.5	14	V
		$T_A = 0^\circ C$ to $70^\circ C$	13.2			
		To negative rail, $R_S = 50\Omega$ TLE2022C, TLE2022AC		-15	-15.3	
		$T_A = 0^\circ C$ to $70^\circ C$	-15			
		To positive rail, $R_S = 50\Omega$ TLE2022C, TLE2022AC		13.5	14	
		$T_A = -40^\circ C$ to $+85^\circ C$	13.2			
		To negative rail, $R_S = 50\Omega$ TLE2022C, TLE2022AC		-15	-15.3	
		$T_A = -40^\circ C$ to $+85^\circ C$	-15			
		To positive rail, $R_S = 50\Omega$ TLE2022C, TLE2022AC		13.5	14	
		$T_A = -55^\circ C$ to $+125^\circ C$	13.2			
		To negative rail, $R_S = 50\Omega$ TLE2022M, TLE2022AM		-15	-15.3	V
		$T_A = -55^\circ C$ to $+125^\circ C$	-15			

6.8 Electrical Characteristics for TLE2022, $V_{CC} = \pm 15V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = \pm 15V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	TLE2022C $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	95	106		dB
				91			
		TLE2022AC $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	97	109		
				93			
		TLE2022BC $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	100	112		
				96			
		TLE2022I $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	95	106		
				91			
		TLE2022AI $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	97	109		
				93			
		TLE2022BI $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	100	112		
				96			
V_O	Voltage output swing	TLE2022C, TLE2022AC $R_L = 10k\Omega$	Positive	14	14.3		V
			Positive $T_A = 0^\circ C$ to $70^\circ C$	13.9			
			Negative		-14.1	-13.7	
			Negative $T_A = 0^\circ C$ to $70^\circ C$			-13.7	
		TLE2022I, TLE2022AI $R_L = 10k\Omega$	Positive	14	14.3		
			Positive $T_A = -40^\circ C$ to $+85^\circ C$	13.9			
			Negative		-14.1	-13.7	
			Negative $T_A = -40^\circ C$ to $+85^\circ C$			-13.7	
		TLE2022M, TLE2022AM $R_L = 10k\Omega$	Positive	14	14.3		
			Positive $T_A = -55^\circ C$ to $+125^\circ C$	13.9			
			Negative		-14.1	-13.7	
			Negative $T_A = -55^\circ C$ to $+125^\circ C$			-13.6	
I_{CC}	Supply current	TLE2022C, TLE2022AC No load			550	700	μA
			$T_A = 0^\circ C$ to $70^\circ C$			700	
		TLE2022I, TLE2022AI No load			550	700	
			$T_A = -40^\circ C$ to $+85^\circ C$			700	
		TLE2022M, TLE2022AM No load			550	700	
			$T_A = -55^\circ C$ to $+125^\circ C$			700	

6.8 Electrical Characteristics for TLE2022, $V_{CC} = \pm 15V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = \pm 15V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC SPECS							
SR	Slew rate	V _O = ±10V, G = 1		0.65		V/μs	
e _N	Input voltage noise density	f = 10Hz	TLE2022xC, TLE2022xI	19		nV/√Hz	
			TLE2022xM	19			
		f = 1kHz	TLE2022xC, TLE2022xI	15			
			TLE2022xM	15			
	Input voltage noise	f = 0.1Hz to 1Hz		0.16		μV	
		f = 0.1Hz to 10Hz		0.47			
	Input current noise density			0.1		pA/√Hz	
GBW	Gain bandwidth	G = 1		2.8		MHz	
Θ _M	Phase margin			52°			

6.9 Electrical Characteristics for TLE2022, $V_{CC} = 5V$

at $T_A = 25^\circ C$, $V_{CC} = 5V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V _{IO}	Input offset voltage	TLE2022C R _S = 50Ω				±600	μV
			T _A = 0°C to 70°C			±800	
		TLE2022AC R _S = 50Ω				±400	
			T _A = 0°C to 70°C			±550	
		TLE2022I R _S = 50Ω				±600	
			T _A = −40°C to +85°C			±800	
		TLE2022AI R _S = 50Ω				±400	
			T _A = −40°C to +85°C			±550	
	TLE2022M R _S = 50Ω				±600		
		T _A = −55°C to +125°C			±800		
	TLE2022AM R _S = 50Ω				±400		
		T _A = −55°C to +125°C			±550		
dV _{IO} /dT	Input offset voltage drift	TLE2022C, TLE2022AC T _A = 0°C to 70°C				±2	μV/°C
		TLE2022I, TLE2022AI T _A = −40°C to +85°C				±2	
		TLE2022M, TLE2022AM T _A = −55°C to +125°C				±2	
I _{IB}	Input bias current	TLE2022C R _S = 50Ω			35	70	nA
			T _A = 0°C to 70°C			90	
		TLE2022AC R _S = 50Ω			33	70	
			T _A = 0°C to 70°C			90	
		TLE2022I R _S = 50Ω			35	70	
			T _A = −40C to +85°C			90	
		TLE2022AI R _S = 50Ω			33	70	
			T _A = −40°C to +85°C			90	
	TLE2022M R _S = 50Ω			35	70		
		T _A = −55°C to +125°C			90		
	TLE2022AM R _S = 50Ω			33	70		
		T _A = −55°C to +125°C			90		
I _{IO}	Input offset current	TLE2022C R _S = 50Ω			0.5	6	nA
			T _A = 0°C to 70°C			10	
		TLE2022AC R _S = 50Ω			0.4	6	
			T _A = 0°C to 70°C			10	
		TLE2022I R _S = 50Ω			0.5	6	
			T _A = −40°C to +85°C			10	
		TLE2022AI R _S = 50Ω			0.4	6	
			T _A = −40°C to +85°C			10	
	TLE2022M R _S = 50Ω			0.5	6		
		T _A = −55°C to +125°C			10		
	TLE2022AM R _S = 50Ω			0.4	6		
		T _A = −55°C to +125°C			10		

6.9 Electrical Characteristics for TLE2022, $V_{CC} = 5V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = 5V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power-supply rejection ratio	TLE2022C $V_{CC} = 5V$ to $30V$	100	115		dB
		$T_A = 0^\circ C$ to $70^\circ C$	95			
		TLE2022AC $V_{CC} = 5V$ to $30V$	103	118		
		$T_A = 0^\circ C$ to $70^\circ C$	98			
		TLE2022I $V_{CC} = 5V$ to $30V$	100	115		
		$T_A = -40^\circ C$ to $+85^\circ C$	95			
		TLE2022AI $V_{CC} = 5V$ to $30V$	103	118		
A_V	Large signal voltage gain	$T_A = -40^\circ C$ to $+85^\circ C$	98			V/ μV
		TLE2022M $V_{CC} = 5V$ to $30V$	100	115		
		$T_A = -55^\circ C$ to $+125^\circ C$	95			
		TLE2022AM $V_{CC} = 5V$ to $30V$	103	118		
		$T_A = -55^\circ C$ to $+125^\circ C$	98			
		TLE2022C, $R_L = 10k\Omega$ $1.4V \leq V_O \leq 4V$	0.3	1.5		
		$T_A = 0^\circ C$ to $70^\circ C$	0.3			
V_{ICR}	Common-mode input voltage range	TLE2022AC, $R_L = 10k\Omega$ $1.4V \leq V_O \leq 4V$	0.4	1.5		V
		$T_A = 0^\circ C$ to $70^\circ C$	0.4			
		TLE2022I, $R_L = 10k\Omega$ $1.4V \leq V_O \leq 4V$	0.3	1.5		
		$T_A = -40^\circ C$ to $+85^\circ C$	0.2			
		TLE2022AI, $R_L = 10k\Omega$ $1.4V \leq V_O \leq 4V$	0.4	1.5		
		$T_A = -40^\circ C$ to $+85^\circ C$	0.2			
		TLE2022M, $R_L = 10k\Omega$ $1.4V \leq V_O \leq 4V$	0.3	1.5		
$CMRR$	Common-mode rejection ratio	$T_A = -55^\circ C$ to $+125^\circ C$	0.1			
		TLE2022AM, $R_L = 10k\Omega$ $1.4V \leq V_O \leq 4V$	0.4	1.5		
		$T_A = -55^\circ C$ to $+125^\circ C$	0.1			
		TLE2022C, TLE2022AC To positive rail, $R_S = 50\Omega$	3.5	4		V
		$T_A = 0^\circ C$ to $70^\circ C$	3.5			
		TLE2022C, TLE2022AC To negative rail, $R_S = 50\Omega$	0	-0.3		
		$T_A = 0^\circ C$ to $70^\circ C$	0			
		TLE2022I, TLE2022AI To positive rail, $R_S = 50\Omega$	3.5	4		
$CMRR$	Common-mode rejection ratio	$T_A = -40^\circ C$ to $+85^\circ C$	3.2			
		TLE2022I, TLE2022AI To negative rail, $R_S = 50\Omega$	0	-0.3		
		$T_A = -40^\circ C$ to $+85^\circ C$	0			
		TLE2022M, TLE2022AM To positive rail, $R_S = 50\Omega$	3.5	4		dB
		$T_A = -55^\circ C$ to $+125^\circ C$	3.2			
		TLE2022M, TLE2022AM To positive rail, $R_S = 50\Omega$	0	-0.3		
		$T_A = -55^\circ C$ to $+125^\circ C$	0			
$CMRR$	Common-mode rejection ratio	TLE2021C $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	85	100		dB
		$T_A = 0^\circ C$ to $70^\circ C$	80			
		TLE2021AC $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	87	102		
		$T_A = 0^\circ C$ to $70^\circ C$	82			
		TLE2022I $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	85	100		
		$T_A = -40^\circ C$ to $+85^\circ C$	80			
		TLE202AI $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	87	102		
$CMRR$	Common-mode rejection ratio	$T_A = -40^\circ C$ to $+85^\circ C$	82			
		TLE2022M $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	85	100		dB
		$T_A = -55^\circ C$ to $+125^\circ C$	80			
		TLE2022AM $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	87	102		
		$T_A = -55^\circ C$ to $+125^\circ C$	82			
		TLE2021C $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	85	100		
		$T_A = 0^\circ C$ to $70^\circ C$	80			

6.9 Electrical Characteristics for TLE2022, $V_{CC} = 5V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = 5V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _O	Voltage output swing	TLE2022C, TLE2022AC R _L = 10kΩ	Positive	4	4.3		V
			Positive, T _A = 0°C to 70°C	3.9			
			Negative		0.7	0.8	
			Negative, T _A = 0°C to 70°C			0.85	
		TLE2022I, TLE2022AI R _L = 10kΩ	Positive	4	4.3		
			Positive, T _A = −40°C to +85°C	3.9			
			Negative		0.7	0.8	
			Negative, T _A = −40°C to +85°C			0.9	
		TLE2022M, TLE2022AM R _L = 10kΩ	Positive	4	4.3		
			Positive, T _A = −55°C to +125°C	3.8			
			Negative		0.7	0.8	
			Negative, T _A = −55°C to +125°C			0.95	
I _{CC}	Supply current	TLE2022C, TLE2022AC		450	600	μA	
			T _A = 0°C to 70°C		600		
		TLE2022I, TLE2022AI		450	600		
			T _A = −40°C to +85°C		600		
		TLE2022M, TLE2022AM		450	600		
			T _A = −55°C to +125°C		600		
AC SPECS							
SR	Slew rate	V _O = ±10V, G = 1		0.65			V/μs
e _N	Input voltage noise density	f = 10Hz	TLE2022xC, TLE2022xI	21		nV/√Hz	
			TLE2022xM	21			
		f = 1kHz	TLE2022xC, TLE2022xI	17			
			TLE2022xM	17			
	Input voltage noise	f = 0.1Hz to 1Hz		0.16		μV	
		f = 0.1Hz to 10Hz		0.47			
	Input current noise density			0.1		pA/√Hz	
GBW	Gain bandwidth	G = 1		1.7		MHz	
Θ _M	Phase margin			47°			

6.10 Electrical Characteristics for TLE2024, $V_{CC} = \pm 15V$

at $T_A = 25^\circ C$, $V_{CC} = \pm 15V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V _{IO}	Input offset voltage	TLE2024C R _S = 50Ω		±1000		μV	
			T _A = 0°C to 70°C	±1200			
		TLE2024AC R _S = 50Ω		±750			
			T _A = 0°C to 70°C	±950			
		TLE2024I R _S = 50Ω		±1000			
			T _A = −40°C to +85°C	±1200			
		TLE2024AAI R _S = 50Ω		±750			
			T _A = −40°C to +85°C	±950			
dV _{IO} /dT	Input offset voltage drift	TLE2024C,TLE2024AC R _S = 50Ω, T _A = 0°C to 70°C		±2		μV/°C	
		TLE2024I,TLE2024AI R _S = 50Ω, T _A = −40C to +85°C		±2			
		TLE2024BM R _S = 50Ω, T _A = −55°C to +125°C		±2			
I _{IB}	Input bias current	TLE2024C R _S = 50Ω		50	70	nA	
			T _A = 0°C to 70°C		90		
		TLE2024AC R _S = 50Ω		45	70		
			T _A = 0°C to 70°C		90		
		TLE2024I R _S = 50Ω		50	70		
			T _A = −40C to +85°C		90		
		TLE2024AI R _S = 50Ω		45	70		
			T _A = −40°C to +85°C		90		
I _{IO}	Input offset current	TLE2024C R _S = 50Ω		0.6	6	nA	
			T _A = 0°C to 70°C		10		
		TLE2024AC R _S = 50Ω		0.5	6		
			T _A = 0°C to 70°C		10		
		TLE2024I R _S = 50Ω		0.6	6		
			T _A = −40°C to +85°C		10		
PSRR	Power-supply rejection ratio	TLE2024C V _{CC±} = ±2.5V to ±15V		98	112	dB	
			T _A = 0°C to 70°C		93		
		TLE2024AC V _{CC±} = ±2.5V to ±15V		100	115		
			T _A = 0°C to 70°C		95		
		TLE2024I V _{CC±} = ±2.5V to ±15V		98	112		
			T _A = −40°C to +85°C		93		
		TLE2024AI V _{CC±} = ±2.5V to ±15V		100	115		
			T _A = −40°C to +85°C		95		
		TLE2024BM V _{CC±} = ±2.5V to ±15V		103	108		
			T _A = −55°C to +125°C		98		

6.10 Electrical Characteristics for TLE2024, $V_{CC} = \pm 15V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = \pm 15V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_V	Large signal voltage gain	TLE2024C $R_L = 10k\Omega$, $V_O = \pm 10V$	$T_A = 0^\circ C$ to $70^\circ C$	0.4	2		V/ μV
				0.4			
		TLE2024AC $R_L = 10k\Omega$, $V_O = \pm 10V$	$T_A = 0^\circ C$ to $70^\circ C$	0.8	4		
				0.8			
		TLE2024I $R_L = 10k\Omega$, $V_O = \pm 10V$	$T_A = -40^\circ C$ to $+85^\circ C$	0.4	2		
				0.4			
		TLE2024AI $R_L = 10k\Omega$, $V_O = \pm 10V$	$T_A = -40^\circ C$ to $+85^\circ C$	0.8	4		
				0.8			
V_{ICR}	Common-mode input voltage range	TLE2024C, TLE2024AC To positive rail, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	13.5	14		V
				13.5			
		TLE2024C, TLE2024AC To negative rail, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	-15	-15.3		
				-15			
		TLE2024I, TLE2024AI To positive rail, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	13.5	14		
				13.2			
		TLE2024I, TLE2024AI To negative rail, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	-15	-15.3		
				-15			
CMRR	Common-mode rejection ratio	TLE2024C $V_{IC} = V_{ICRmin}$	$T_A = 0^\circ C$ to $70^\circ C$	92	102		dB
				88			
		TLE2024AC $V_{IC} = V_{ICRmin}$	$T_A = 0^\circ C$ to $70^\circ C$	94	105		
				90			
		TLE2024I $V_{IC} = V_{ICRmin}$	$T_A = -40^\circ C$ to $+85^\circ C$	92	102		
				88			
		TLE2024AI $V_{IC} = V_{ICRmin}$	$T_A = -40^\circ C$ to $+85^\circ C$	94	105		
				90			
		TLE2024BM $V_{IC} = V_{ICRmin}$	$T_A = -40^\circ C$ to $+85^\circ C$	97	108		
			$T_A = -55^\circ C$ to $+125^\circ C$	93			

6.10 Electrical Characteristics for TLE2024, $V_{CC} = \pm 15V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = \pm 15V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _O	Voltage output swing	TLE2024C R _L = 10kΩ	Positive	13.8	14.1		V
			Positive, T _A = 0°C to 70°C	13.7			
			Negative	−13.7	−14.1		
			Negative, T _A = 0°C to 70°C	−13.6			
		TLE2024AC R _L = 10kΩ	Positive	13.9	14.2		
			Positive, T _A = 0°C to 70°C	13.8			
			Negative	−13.7	−14.1		
			Negative, T _A = 0°C to 70°C	−13.6			
		TLE2024I R _L = 10kΩ	Positive	13.8	14.1		
			Positive, T _A = −40°C to +85°C	13.7			
			Negative	−13.7	−14.1		
			Negative, T _A = −40°C to +85°C	−13.6			
		TLE2024AI R _L = 10kΩ	Positive	13.9	14.2		
			Positive, T _A = −40°C to +85°C	13.7			
			Negative	−13.7	−14.1		
			Negative, T _A = −40°C to +85°C	−13.6			
		TLE2024BM R _L = 10kΩ	Positive	14	14.3		
			Positive, T _A = −55°C to +125°C	13.8			
			Negative	−13.7	−14.1		
			Negative, T _A = −55°C to +125°C	−13.6			
I _{CC}	Supply current	TLE2024C, TLE2024AC			1050	1400	μA
			T _A = 0°C to 70°C			1400	
		TLE2024I, TLE2024AI			1050	1400	
			T _A = −40°C to +85°C			1400	
		TLE2024BM			1050	1400	
			T _A = −55°C to +125°C			1400	
AC SPECS							
SR	Slew rate	V _O = ±10V, G = 1			0.7		V/μs
e _N	Input voltage noise density	f = 10Hz	TLE2024xC, TLE2024xI		19	50	nV/√Hz
			TLE2024BM		19		
		f = 1kHz	TLE2024xC, TLE2024I		15	30	
			TLE2024BM		15		
	Input voltage noise	f = 0.1Hz to 1Hz			0.16		μV
f = 0.1Hz to 10Hz			0.47				
	Input current noise density				0.1		pA/√Hz
GBW	Gain bandwidth	G = 1			2.8		MHz
Θ _M	Phase margin				52°		

6.11 Electrical Characteristics for TLE2024, $V_{CC} = 5V$

at $T_A = 25^\circ C$, $V_{CC} = 5V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V _{IO}	Input offset voltage	TLE2024C R _S = 50Ω				±1100	μV
			T _A = 0°C to 70°C			±1300	
		TLE2024AC R _S = 50Ω				±850	
			T _A = 0°C to 70°C			±1050	
		TLE2024I R _S = 50Ω				1100	
			T _A = −40°C to +85°C			±1300	
		TLE2024AI R _S = 50Ω				±850	
T _A = −40°C to +85°C				±1050			
TLE2024BM R _S = 50Ω				±600			
	T _A = −55°C to +125°C			±800			
dV _{IO} /dT	Input offset voltage drift	TLE2024C, TLE2024AC R _S = 50Ω, T _A = 0°C to 70°C				±2	μV/°C
		TLE2024I, TLE2024AI R _S = 50Ω, T _A = −40°C to +85°C				±2	
		TLE2024BM R _S = 50Ω, T _A = −55°C to +125°C				±2	
I _{IB}	Input bias current	TLE2024C R _S = 50Ω			45	70	nA
			T _A = 0°C to 70°C			90	
		TLE2024AC R _S = 50Ω			40	70	
			T _A = 0°C to 70°C			90	
		TLE2024I R _S = 50Ω			45	70	
			T _A = −40°C to +85°C			90	
		TLE2024AI R _S = 50Ω			40	70	
T _A = −40°C to +85°C				90			
TLE2024BM R _S = 50Ω			35	70			
	T _A = −55°C to +125°C			90			
I _{IO}	Input offset current	TLE2024C R _S = 50Ω			0.6	6	nA
			T _A = 0°C to 70°C			10	
		TLE2024AC R _S = 50Ω			0.5	6	
			T _A = 0°C to 70°C			10	
		TLE2024I R _S = 50Ω			0.6	6	
			T _A = −40°C to +85°C			10	
		TLE2024AI R _S = 50Ω			0.5	6	
T _A = −40°C to +85°C				10			
TLE2024BM R _S = 50Ω			0.4	6			
	T _A = −55°C to +125°C			10			
PSRR	Power-supply rejection ratio	TLE2024IC V _{CC} = 5V to 30V		98	112	dB	
			T _A = 0°C to 70°C	93			
		TLE2024AC V _{CC} = 5V to 30V		100	115		
			T _A = 0°C to 70°C	95			
		TLE2024I V _{CC} = 5V to 30V		98	112		
			T _A = −40°C to +85°C	93			
		TLE2024AI V _{CC} = 5V to 30V		100	115		
T _A = −40°C to +85°C	95						
TLE2024BM V _{CC} = 5V to 30V		103	117				
	T _A = −55°C to +125°C	98					

6.11 Electrical Characteristics for TLE2024, $V_{CC} = 5V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = 5V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_V	Large signal voltage gain	TLE2024C $R_L = 10k\Omega$, $1.4V \leq V_O \leq 4V$	$T_A = 0^\circ C$ to $70^\circ C$	0.2	1.5		V/ μV
				0.1			
		TLE2024C $R_L = 10k\Omega$, $1.4V \leq V_O \leq 4V$	$T_A = 0^\circ C$ to $70^\circ C$	0.3	1.5		
				0.1			
		TLE2024I $R_L = 10k\Omega$, $1.4V \leq V_O \leq 4V$	$T_A = -40^\circ C$ to $+85^\circ C$	0.2	1.5		
				0.1			
		TLE2024AI, $R_L = 10k\Omega$, $1.4V \leq V_O \leq 4V$	$T_A = -40^\circ C$ to $+85^\circ C$	0.3	1.5		
				0.1			
V_{ICR}	Common-mode input voltage range	TLE2024C, TLE2024AC To positive rail, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	3.5	4		V
				3.5			
		TLE2024C, TLE2024AC To negative rail, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	0	-0.3		
				0			
		TLE2024I, TLE2024AI To positive rail, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	3.5	4		
				3.2			
		TLE2024I, TLE2024AI To negative rail, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	0	-0.3		
				0			
CMRR	Common-mode rejection ratio	TLE2024C $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	80	90		dB
				80			
		TLE2024AC $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = 0^\circ C$ to $70^\circ C$	82	92		
				82			
		TLE2024I $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	80	90		
				80			
		TLE2024AI $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	82	92		
				82			
		TLE2024BM $V_{IC} = V_{ICRmin}$, $R_S = 50\Omega$	$T_A = -40^\circ C$ to $+85^\circ C$	85	95		
			$T_A = -55^\circ C$ to $+125^\circ C$	85			

6.11 Electrical Characteristics for TLE2024, $V_{CC} = 5V$ (continued)

at $T_A = 25^\circ C$, $V_{CC} = 5V$, and $V_{IC} = V_{OUT} = V_{CC} / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _O	Voltage output swing	TLE2024C R _L = 10kΩ	Positive	3.9	4.2		V
			Positive, T _A = 0°C to 70°C	3.7			
			Negative		0.7	0.8	
			Negative, T _A = 0°C to 70°C			0.95	
		TLE2024AC R _L = 10kΩ	Positive	3.9	4.2		
			Positive, T _A = 0°C to 70°C	3.7			
			Negative		0.7	0.8	
			Negative, T _A = 0°C to 70°C			0.95	
		TLE2024I R _L = 10kΩ	Positive	3.9	4.2		
			Positive, T _A = −40°C to +85°C	3.7			
			Negative		0.7	0.8	
			Negative, T _A = −40°C to +85°C			0.95	
		TLE2024AI R _L = 10kΩ	Positive	3.9	4.2		
			Positive, T _A = −40°C to +85°C	3.7			
			Negative		0.7	0.8	
			Negative, T _A = −40°C to +85°C			0.95	
		TLE2024BM R _L = 10kΩ	Positive	3.8	4.3		
			Positive, T _A = −55°C to +125°C	3.8			
			Negative		0.7	0.8	
			Negative, T _A = −55°C to +125°C			0.95	
I _{CC}	Supply current	TLE2024C, TLE2024AC		800	1200	μA	
			T _A = 0°C to 70°C				1200
		TLE2024I, TLE2024AI		800	1200		
			T _A = −40°C to +85°C				1200
		TLE2024BM		800	1200		
			T _A = −55°C to +125°C				1200
AC SPECS							
SR	Slew rate	V _O = ±10V, G = 1		0.5			V/μs
e _N	Input voltage noise density	f = 10Hz	TLE2024xC, TLE2024xI	21		nV/√Hz	
			TLE2024BM	21			
		f = 1kHz	TLE2024xC, TLE2024xI	17			
			TLE2024BM	17			
	Input voltage noise	f = 0.1Hz to 1Hz		0.16		μV	
		f = 0.1Hz to 10Hz		0.47			
	Input current noise density			0.1		pA/√Hz	
GBW	Gain bandwidth	G = 1		1.7		MHz	
Θ _M	Phase margin			47°			

6.12 Typical Characteristics

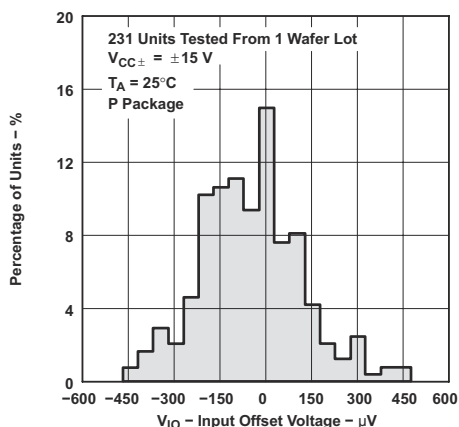


Figure 6-1. Distribution of TLE2021 Input Offset Voltage

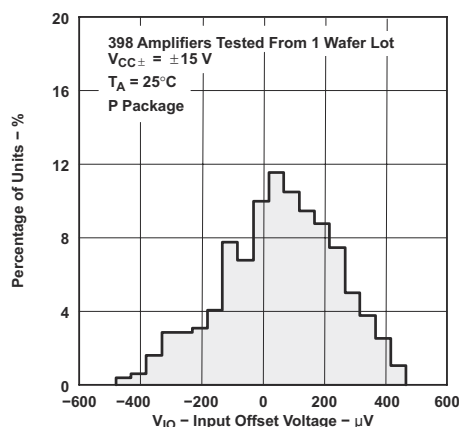


Figure 6-2. Distribution of TLE2022 Input Offset Voltage

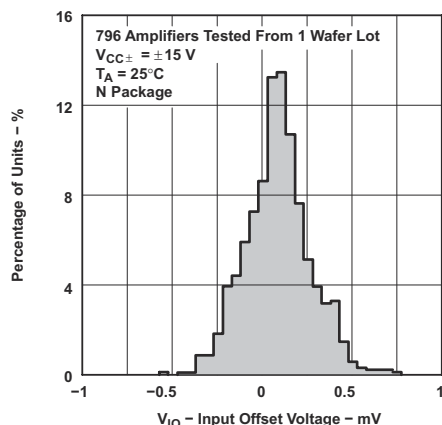


Figure 6-3. Distribution of TLE2024 Input Offset Voltage

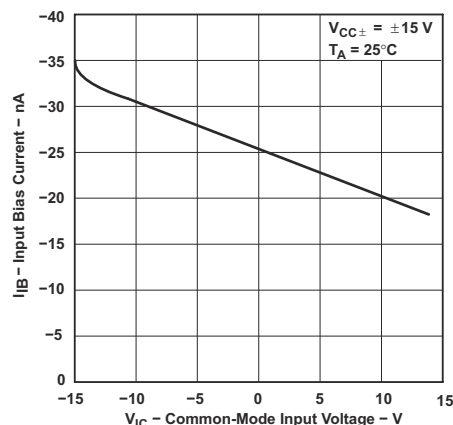


Figure 6-4. TLE2021 Input Bias Current vs Common-Mode Input Voltage

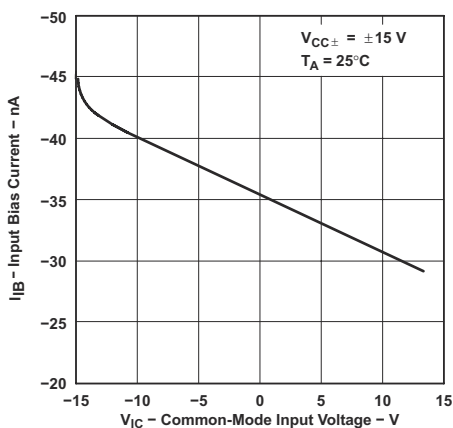


Figure 6-5. TLE2022 Input Bias Current vs Common-Mode Input Voltage

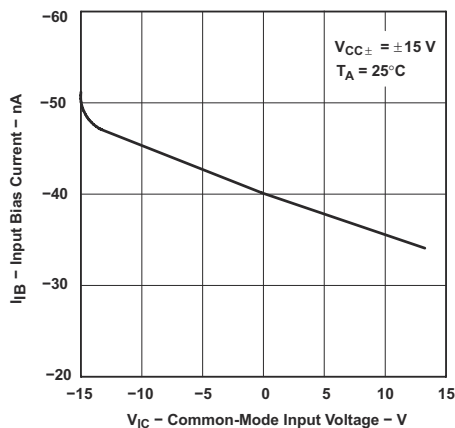
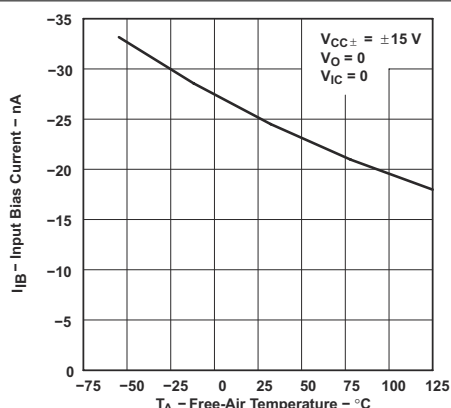


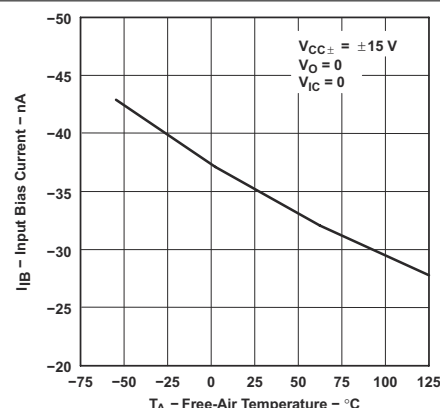
Figure 6-6. TLE2024 Input Bias Current vs Common-Mode Input Voltage

6.12 Typical Characteristics (continued)



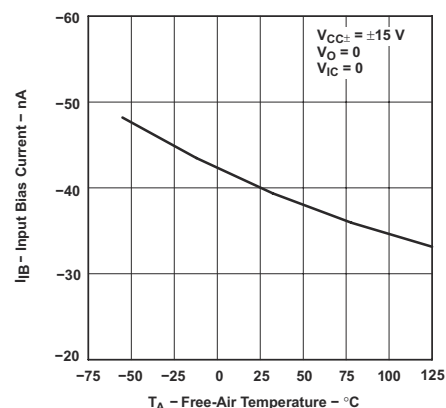
Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 6-7. TLE2021 Input Bias Current vs Free-Air Temperature



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 6-8. TLE2022 Input Bias Current vs Free-Air Temperature



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 6-9. TLE2024 Input Bias Current vs Free-Air Temperature

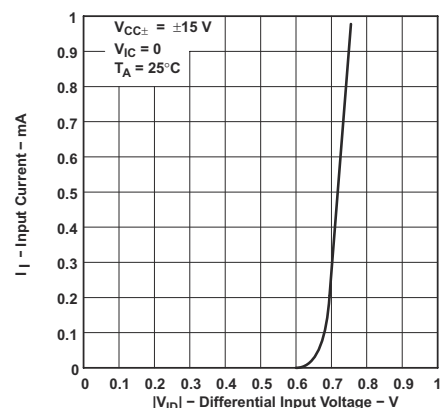


Figure 6-10. Input Current vs Differential Input Voltage

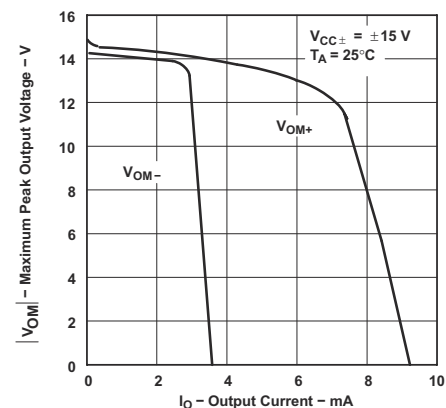


Figure 6-11. TLE2021 Maximum Peak Output Voltage vs Output Current

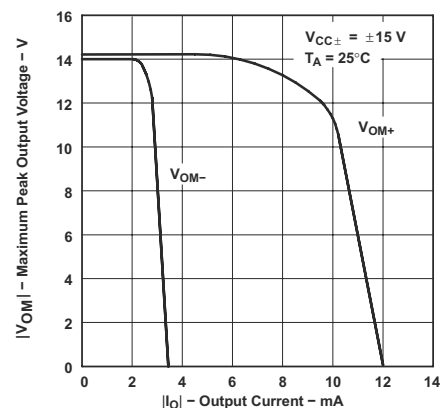


Figure 6-12. TLE2022 Maximum Peak Output Voltage vs Output Current

6.12 Typical Characteristics (continued)

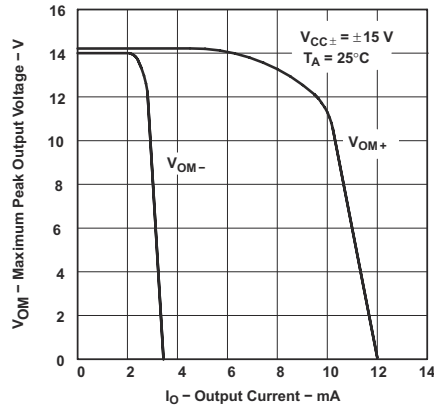
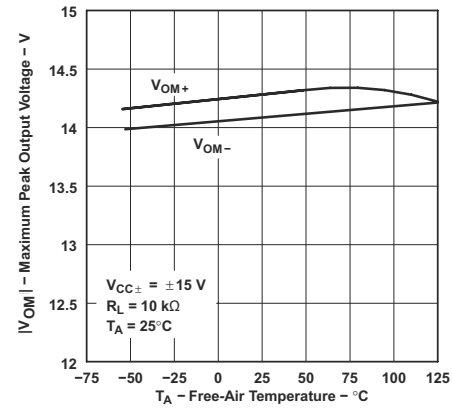


Figure 6-13. TLE2024 Maximum Peak Output Voltage vs Output Current



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 6-14. Maximum Peak Output Voltage vs Free-Air Temperature

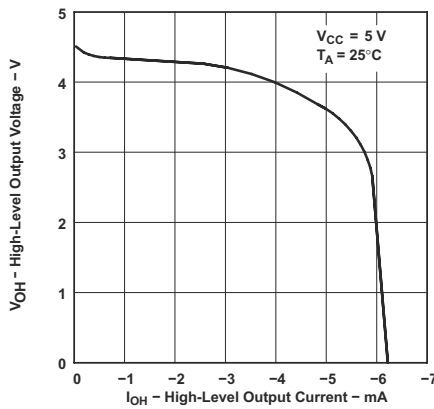


Figure 6-15. TLE2021 High-Level Output Voltage vs High-Level Output Current

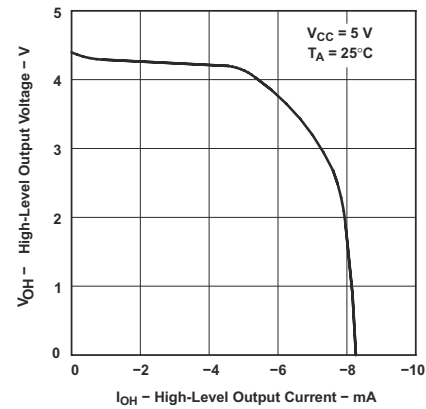
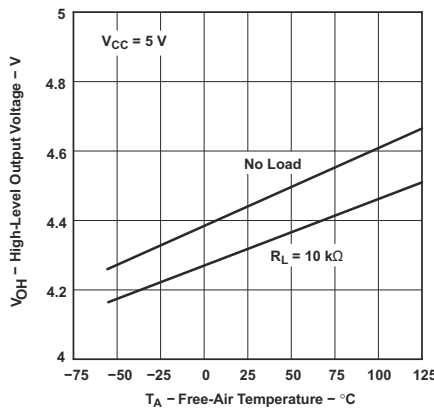


Figure 6-16. TLE2022 and TLE2024 High-Level Output Voltage vs High-Level Output Current



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 6-17. High-Level Output Voltage vs Free-Air Temperature

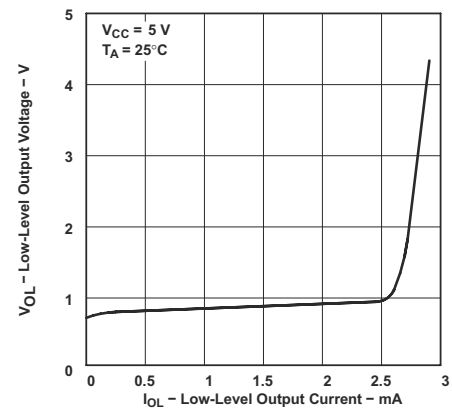
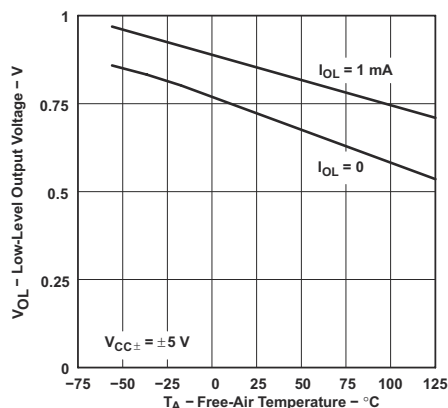


Figure 6-18. Low-Level Output Voltage vs Low-Level Output Current

6.12 Typical Characteristics (continued)



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 6-19. Low-Level Output Voltage vs Free-Air Temperature

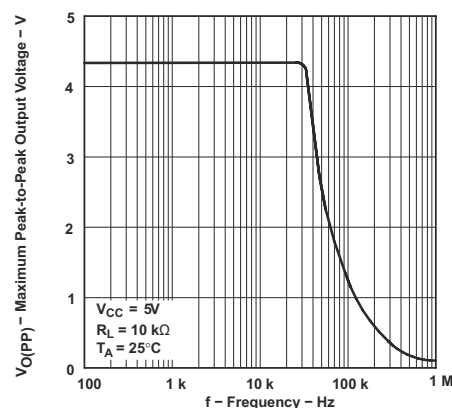


Figure 6-20. Maximum Peak-to-Peak Output Voltage Vs Frequency

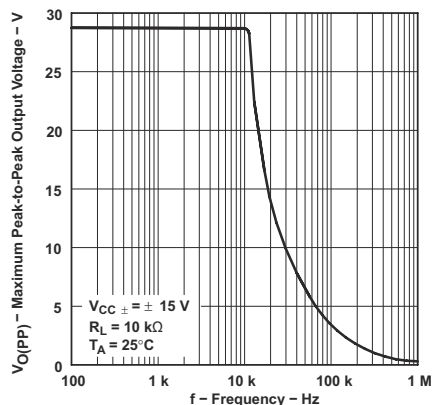


Figure 6-21. Maximum Peak-to-Peak Output Voltage vs Frequency

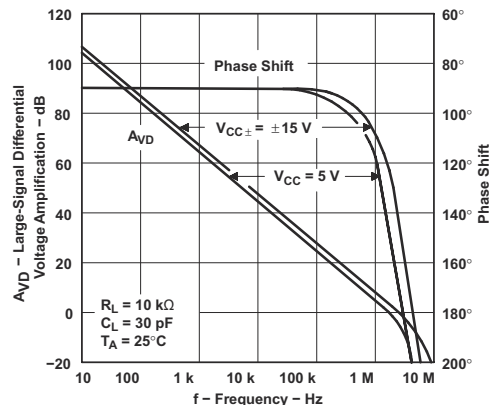


Figure 6-22. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

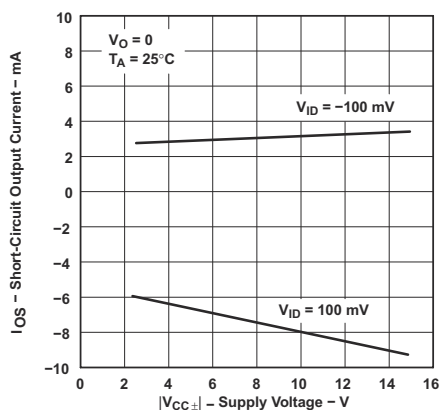


Figure 6-23. TLE2021 Short-Circuit Output Current vs Supply Voltage

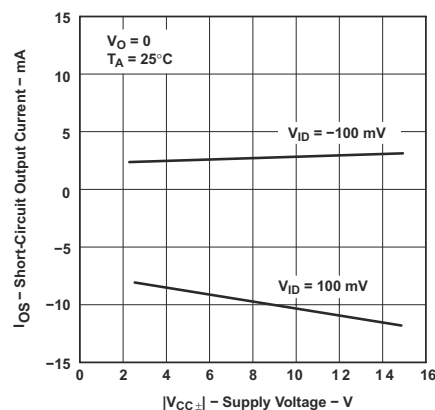


Figure 6-24. TLE2022 and TLE2024 Short-Circuit Output Current vs Supply Voltage

6.12 Typical Characteristics (continued)

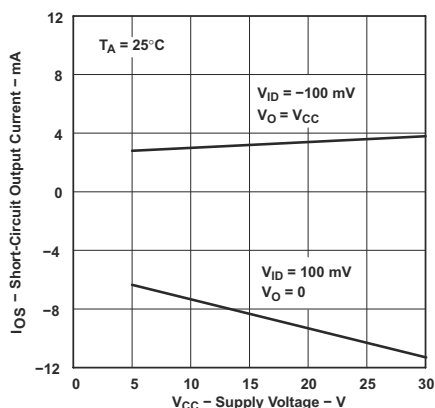
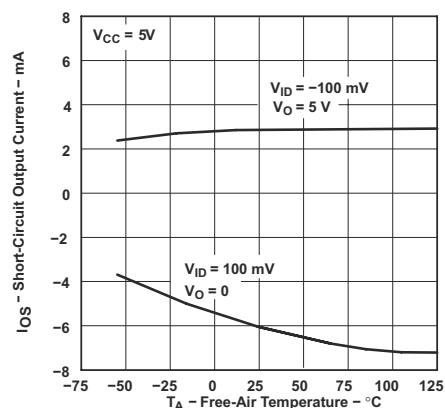


Figure 6-25. TLE2021 Short-Circuit Output Current vs Supply Voltage



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 6-26. TLE2021 Short-Circuit Output Current vs Free-Air Temperature

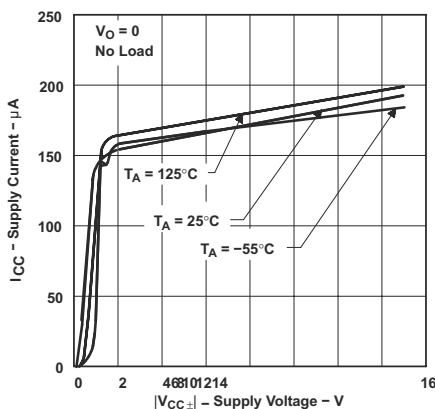


Figure 6-27. TLE2021 Supply Current vs Supply Voltage

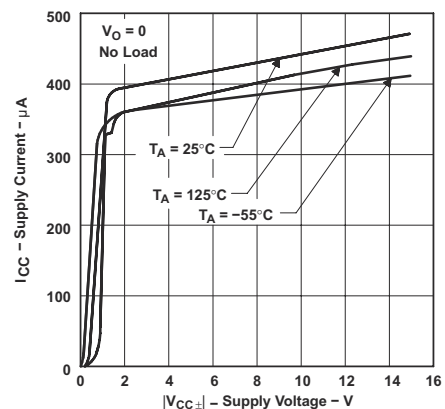


Figure 6-28. TLE2022 Supply Current vs Supply Voltage

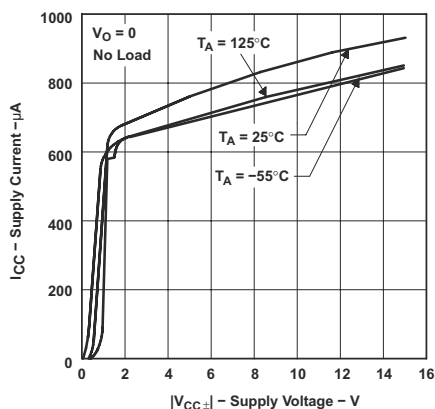
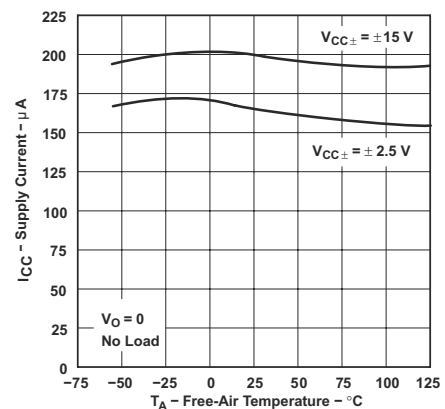


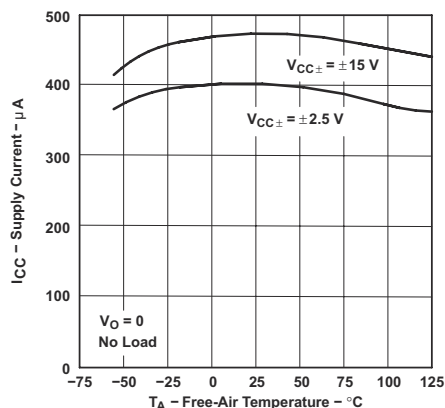
Figure 6-29. TLE2024 Supply Current vs Supply Voltage



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

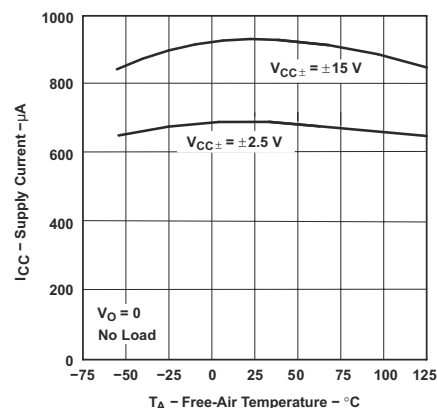
Figure 6-30. TLE2021 Supply Current vs Free-Air Temperature

6.12 Typical Characteristics (continued)



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 6-31. TLE2022 Supply Current vs Free-Air Temperature



Data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Figure 6-32. TLE2024 Supply Current vs Free-Air Temperature

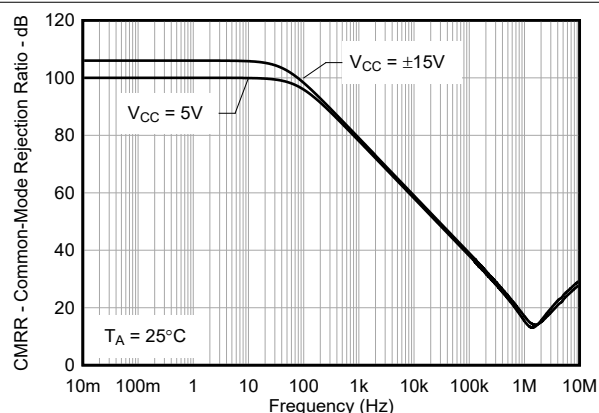


Figure 6-33. TLE202x Common-Mode Rejection Ratio vs Frequency

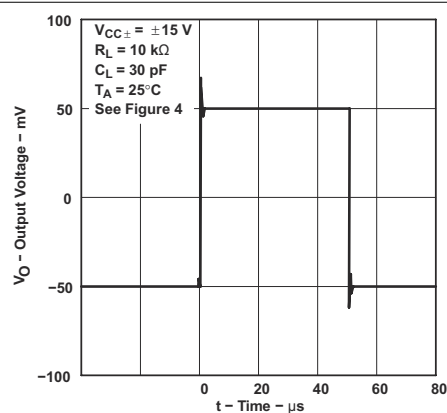


Figure 6-34. Voltage-Follower Small-Signal Pulse Response

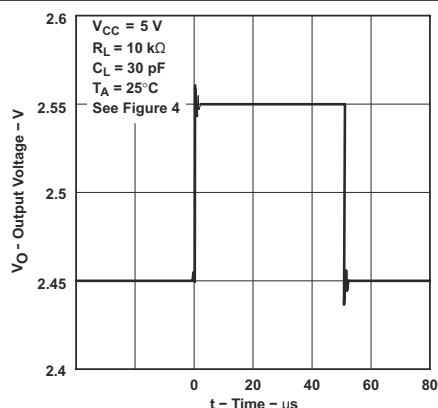


Figure 6-35. Voltage-Follower Small-Signal Pulse Response

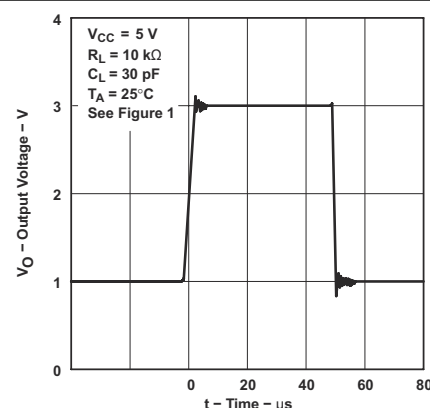


Figure 6-36. TLE2021 Voltage-Follower Large-Signal Pulse Response

6.12 Typical Characteristics (continued)

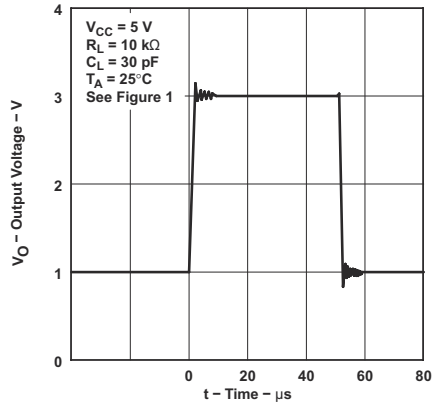


Figure 6-37. TLE2022 Voltage-Follower Large-Signal Pulse Response

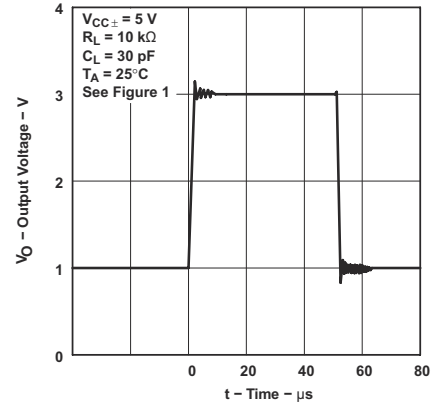


Figure 6-38. TLE2024 Voltage-Follower Large-Scale Pulse Response

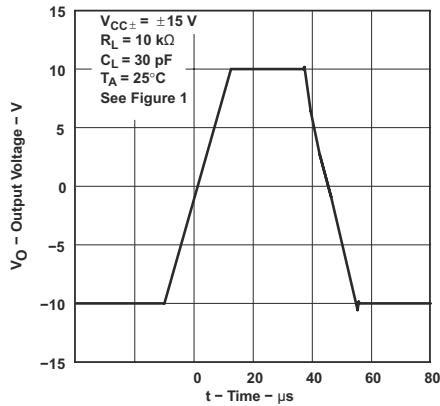


Figure 6-39. TLE2021 Voltage-Follower Large-Signal Pulse Response

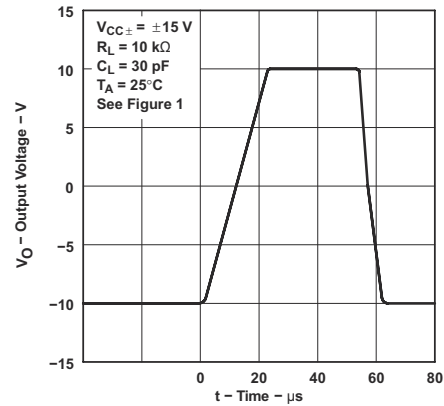


Figure 6-40. TLE2022 Voltage-Follower Large-Signal Pulse Response

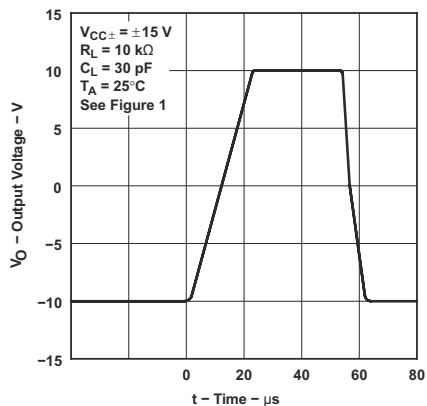


Figure 6-41. TLE2024 Voltage-Follower Large-Signal Pulse Response

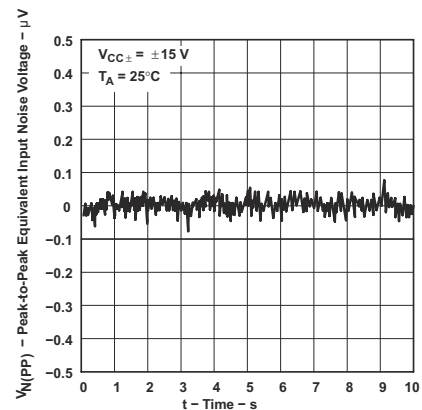
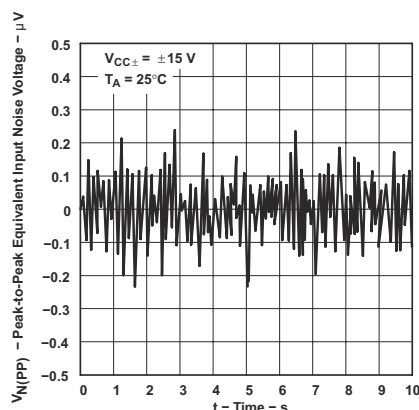


Figure 6-42. Peak-to-Peak Equivalent Input Noise Voltage 0.1Hz to 1Hz

6.12 Typical Characteristics (continued)



**Figure 6-43. Peak-to-Peak Equivalent Input Noise Voltage
0.1Hz to 10Hz**

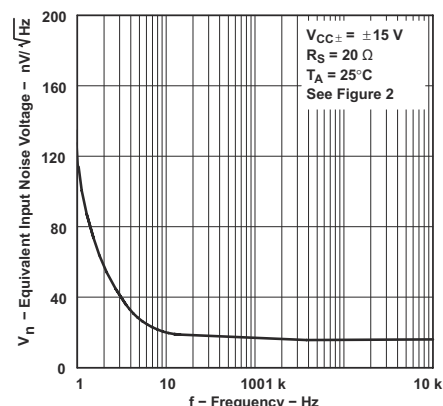


Figure 6-44. Equivalent Input Noise Voltage vs Frequency

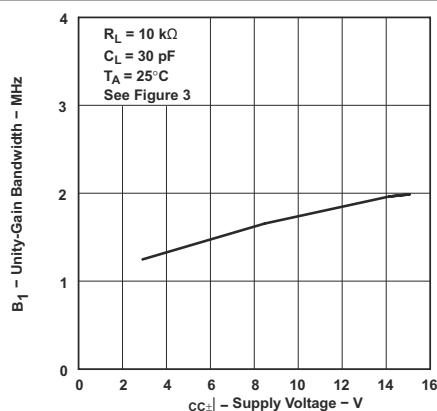
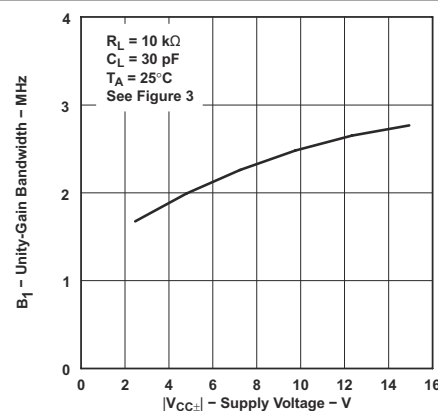


Figure 6-45. TLE2021 Unity-Gain Bandwidth vs Supply Voltage



**Figure 6-46. TLE2022 and TLE2024 Unity-Gain Bandwidth vs
Supply Voltage**

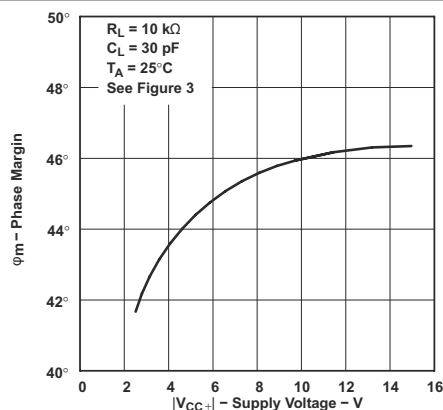
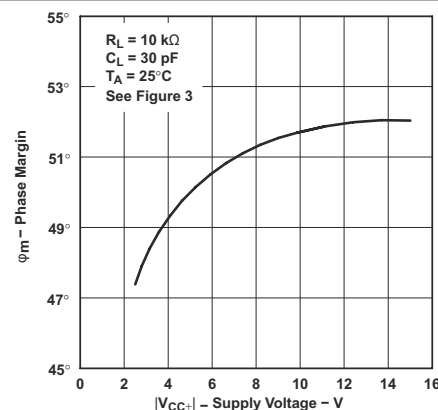


Figure 6-47. TLE2021 Phase Margin vs Supply Voltage



**Figure 6-48. TLE2022 and TLE2024 Phase Margin vs Supply
Voltage**

6.12 Typical Characteristics (continued)

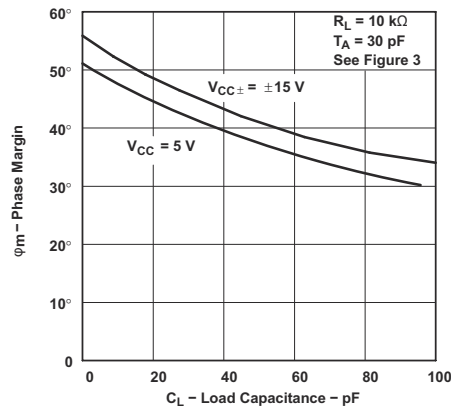


Figure 6-49. TLE2021 Phase Margin vs Load Capacitance

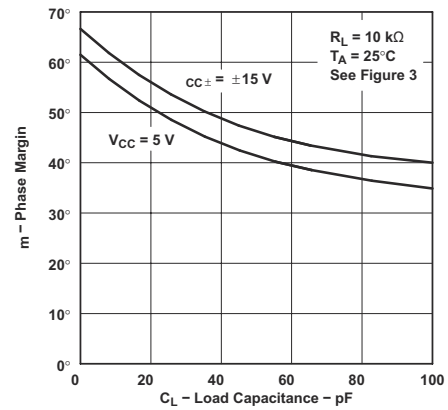


Figure 6-50. TLE2022 and TLE2024 Phase Margin vs Load Capacitance

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Voltage-Follower Applications

The TLE202x circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition sometimes occurs when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. Use a feedback resistor to limit the current to a maximum of 1mA to prevent degradation of the device. This feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10kΩ, this pole degrades the amplifier phase margin. Figure 7-1 shows that to alleviate this problem, add a capacitor (20pF to 50pF) in parallel with the feedback resistor.

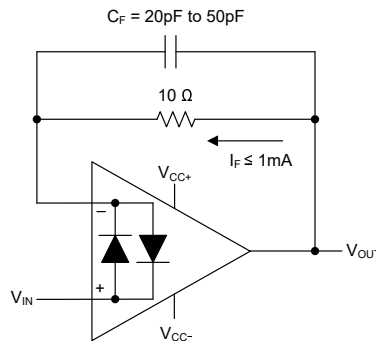


Figure 7-1. Voltage Follower

7.1.2 Input Offset Voltage Null

The TLE202x series offers external null pins that further reduce the input offset voltage. Figure 7-2 shows how to connect the circuit if this feature is desired. Adjust the external resistance value to achieve desired performance. When external null is not needed, leave the null pins disconnected. Only use this adjustment to null the offset of the operational amplifier. Do not use this adjustment to compensate for offsets created elsewhere in a system because of the possible introduction of additional temperature drift.

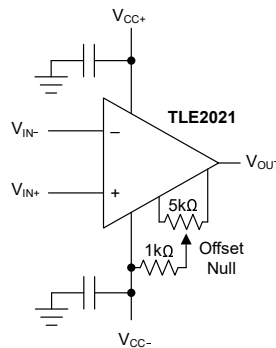


Figure 7-2. Input Offset Voltage Null Circuit

Internal resistances vary; unexpected results are sometimes produced when using fixed resistors to null the offset of the amplifier.

7.2 Layout

7.2.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

1. Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V_{CC+} to ground is applicable for single-supply applications. Noise propagates into analog circuitry through the power pins of the circuit as a whole, as well as through the individual op amp. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
2. Physically separate digital and analog grounds, paying special attention to the ground-current flow. Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
3. To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
4. Place the external components as close to the device as possible. Figure 7-4 shows how to keep R_F and R_G close to the inverting input to minimize parasitic capacitance.
5. Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
6. Consider a driven, low-impedance guard ring around the critical traces. Use a guard ring to significantly reduce leakage currents from nearby traces that are at different potentials.
7. Clean the PCB following board assembly for best performance.
8. Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.2.2 Layout Example

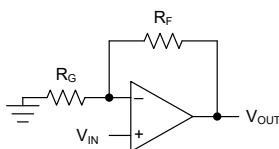


Figure 7-3. Schematic Representation

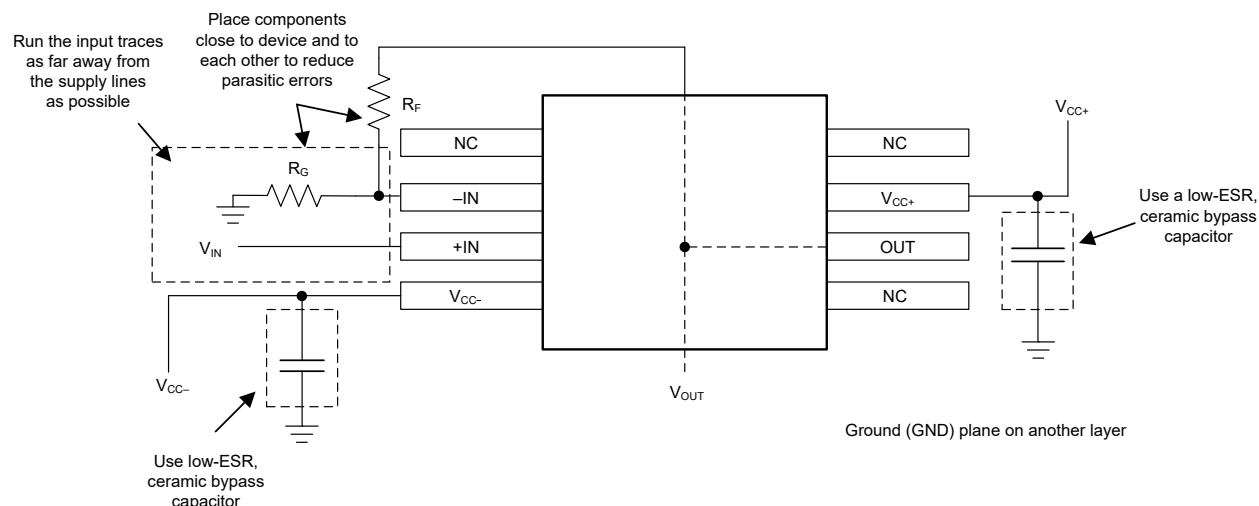


Figure 7-4. Operational Amplifier Board Layout for Noninverting Configuration

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.1.1 Device Nomenclature

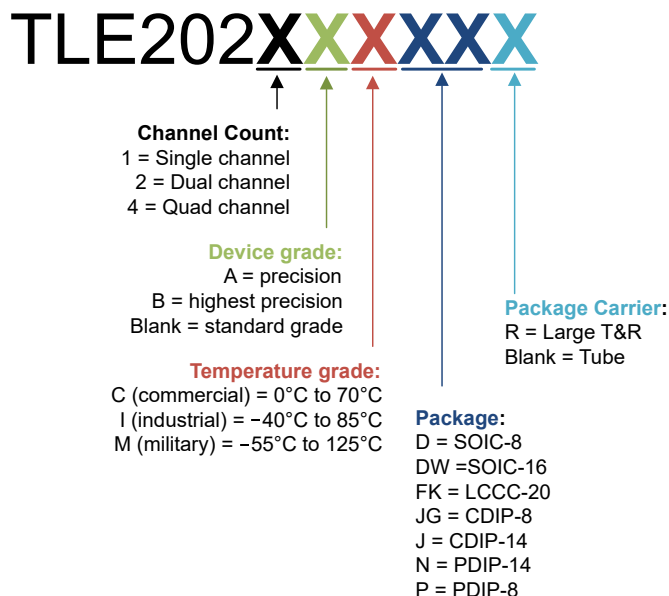


Figure 8-1. Demystifying the TLE202x Orderable Part Numbers

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision SLOS191D (November 2010) to Revision * (July 2025)	Page
• Deleted TLE2021Y, TLE2022Y, and TLE2024Y content from this document.....	1
• Deleted PW (TSSOP), FK (LCCC), JG (CDIP) and J (CDIP) packages and associated content throughout document.....	1
• Deleted all references to Excalibur process.....	1
• Moved TLE202x commercial devices from SLOS191D data sheet into new SLVSJD7 data sheet.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added <i>Applications, Pin Configuration and Functions, Specifications, Thermal Information, Application and Implementation, Layout, Device and Documentation Support, and Mechanical, Packaging, Orderable Information</i> , and <i>Revision History</i> sections, and associated subsections where applicable.....	1
• Updated <i>Features</i>	1
• Updated front page figure.....	1
• Updated available options tables.....	2
• Deleted <i>Equivalent Schematic (Each Amplifier)</i>	2
• Updated pin names and images in <i>Pin Configuration and Functions</i>	3
• Updated parameter names and symbols in all <i>Electrical Characteristics</i>	8
• Added $\pm$ to input offset voltage, input offset voltage drift, and input offset voltage long-term drift in all <i>Electrical Characteristics</i>	8
• Deleted input offset voltage long term drift in all <i>Electrical Characteristics</i>	8
• Moved voltage output swing (negative) values from MIN to MAX in all <i>Electrical Characteristics</i>	8
• Deleted supply-current change over operating temperature range in all <i>Electrical Characteristics</i>	8
• Deleted slew rate MIN in all $V_{CC\pm} = \pm 15V$ <i>Electrical Characteristics</i>	8
• Deleted slew rate over temperature in all $V_{CC\pm} = \pm 15V$ <i>Electrical Characteristics</i>	8
• Deleted <i>Parameter Measurement Information</i> section.....	27
• Deleted Figures 27 to 29, Figures 34 to 37, Figures 47 to 49, Figures 63 to 64, and Figures 69 to 70.....	27
• Updated Figures 44 to 46 (<i>Common-Mode Rejection Ratio vs Frequency</i>).....	27
• Deleted <i>Parameter Measurement Information</i>	36
• Updated Figure 7-1, <i>Voltage Follower</i>	36
• Deleted <i>Macromodel Information</i>	36
• Updated <i>Input Offset Voltage Nulling</i> description.....	36
• Updated Figure 7-2, <i>Input Offset Voltage Null Circuit</i>	36
• Added <i>Layout</i> and associated figures.....	37

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2021ACD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-	2021AC
TLE2021ACDR	Last Time Buy	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2021AC
TLE2021ACP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLE2021AC
TLE2021ACP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2021AC
TLE2021AID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	2021AI
TLE2021AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2021AI
TLE2021AIDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021AI
TLE2021AIP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLE2021AI
TLE2021AIP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2021AI
TLE2021CD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	2021C
TLE2021CDR	Last Time Buy	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2021C
TLE2021CP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLE2021CP
TLE2021CP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLE2021CP
TLE2021CPE4	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLE2021CP
TLE2021ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	2021I
TLE2021IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021I
TLE2021IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021I
TLE2021IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2021IP
TLE2021IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2021IP
TLE2021MD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2021M
TLE2021MD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2021M
TLE2021MDG4	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2021M
TLE2021MDG4.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2021M
TLE2022ACD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	2022AC
TLE2022ACDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2022AC
TLE2022ACDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022AC
TLE2022ACP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLE2022AC
TLE2022ACP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2022AC

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2022AID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	2022AI
TLE2022AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2022AI
TLE2022AIDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022AI
TLE2022AIP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLE2022AI
TLE2022AIP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2022AI
TLE2022AMD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-55 to 125	2022AM
TLE2022AMDG4	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2022AM
TLE2022AMDG4.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022AM
TLE2022AMDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022AM
TLE2022AMDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022AM
TLE2022AMDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2022AM
TLE2022AMDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022AM
TLE2022CD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-	2022C
TLE2022CDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2022C
TLE2022CDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2022C
TLE2022CP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLE2022CP
TLE2022CP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2022CP
TLE2022CPE4	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	See TLE2022CP	TLE2022CP
TLE2022ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	2022I
TLE2022IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022I
TLE2022IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022I
TLE2022IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLE2022IP
TLE2022IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2022IP
TLE2022IPE4	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	See TLE2022IP	TLE2022IP
TLE2022MD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-55 to 125	2022M
TLE2022MDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022M
TLE2022MDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022M
TLE2022MDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2022M
TLE2022MDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022M
TLE2024ACDW	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	-	TLE2024AC
TLE2024ACDWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLE2024AC

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2024ACDWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLE2024AC
TLE2024ACDWR.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLE2024ACN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLE2024ACN
TLE2024ACN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2024ACN
TLE2024AIDW	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLE2024AI
TLE2024AIDW.A	Active	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLE2024AI
TLE2024AIN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLE2024AIN
TLE2024AIN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLE2024AIN
TLE2024BMDW	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	-55 to 125	TLE2024BM
TLE2024BMDWG4	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	-55 to 125	TLE2024BM
TLE2024BMDWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	Call TI	Call TI	-55 to 125	TLE2024BM
TLE2024BMDWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	Call TI	Call TI	-55 to 125	TLE2024BM
TLE2024BMDWR.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	-	Call TI	Call TI	-55 to 125	
TLE2024CDW	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	-	TLE2024C
TLE2024CDWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLE2024C
TLE2024CDWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See TLE2024CDWR	TLE2024C
TLE2024CDWR.B	Active	Production	SOIC (DW) 16	2000 LARGE T&R	-	Call TI	Call TI	See TLE2024CDWR	
TLE2024CN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLE2024CN
TLE2024CN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	See TLE2024CN	TLE2024CN
TLE2024CNE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	See TLE2024CN	TLE2024CN
TLE2024IDW	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	-	TLE2024I
TLE2024IN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLE2024IN
TLE2024IN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	See TLE2024IN	TLE2024IN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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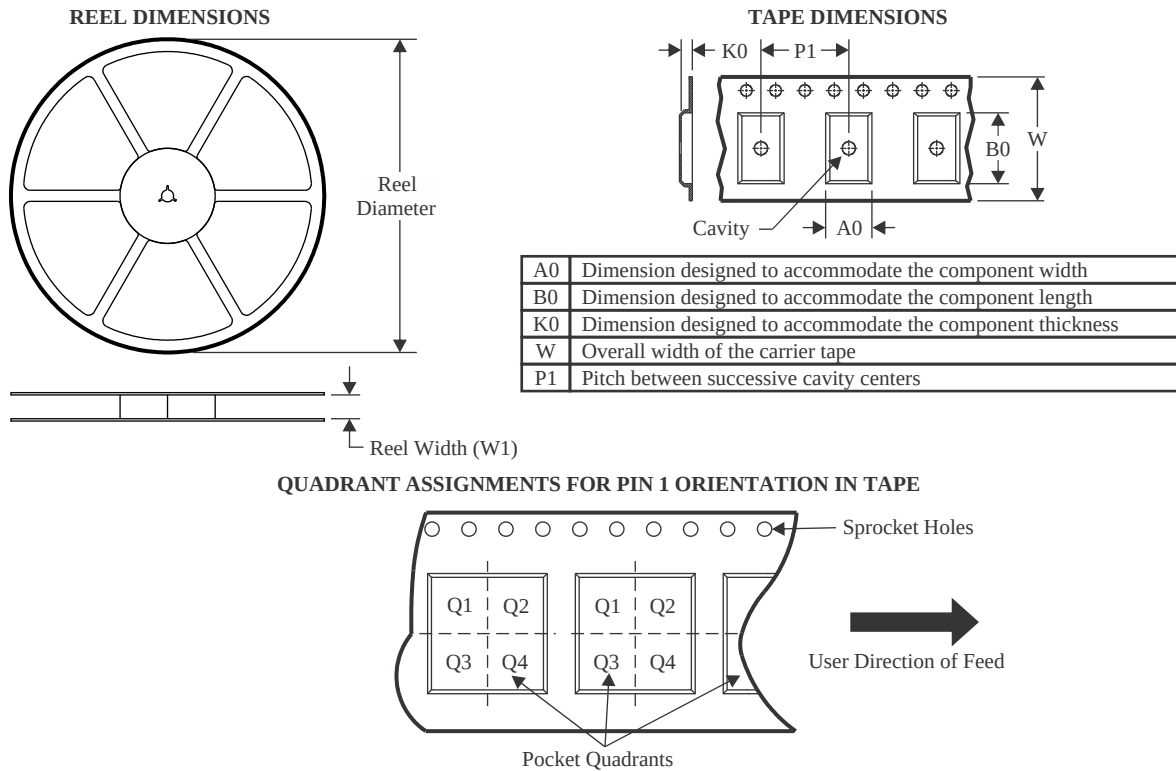
OTHER QUALIFIED VERSIONS OF TLE2021, TLE2021A, TLE2021M, TLE2022, TLE2022A, TLE2022AM, TLE2022M, TLE2024, TLE2024A, TLE2024B, TLE2024BM :

- Catalog : [TLE2021](#), [TLE2022A](#), [TLE2022](#), [TLE2024B](#)
- Automotive : [TLE2021-Q1](#), [TLE2021A-Q1](#), [TLE2021-Q1](#), [TLE2022-Q1](#), [TLE2022A-Q1](#), [TLE2022A-Q1](#), [TLE2022-Q1](#), [TLE2024-Q1](#)
- Enhanced Product : [TLE2021-EP](#), [TLE2021A-EP](#), [TLE2021-EP](#), [TLE2022-EP](#), [TLE2022A-EP](#), [TLE2022A-EP](#), [TLE2022-EP](#), [TLE2024-EP](#), [TLE2024A-EP](#)
- Military : [TLE2021M](#), [TLE2021AM](#), [TLE2022M](#), [TLE2022AM](#), [TLE2024M](#), [TLE2024AM](#), [TLE2024BM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

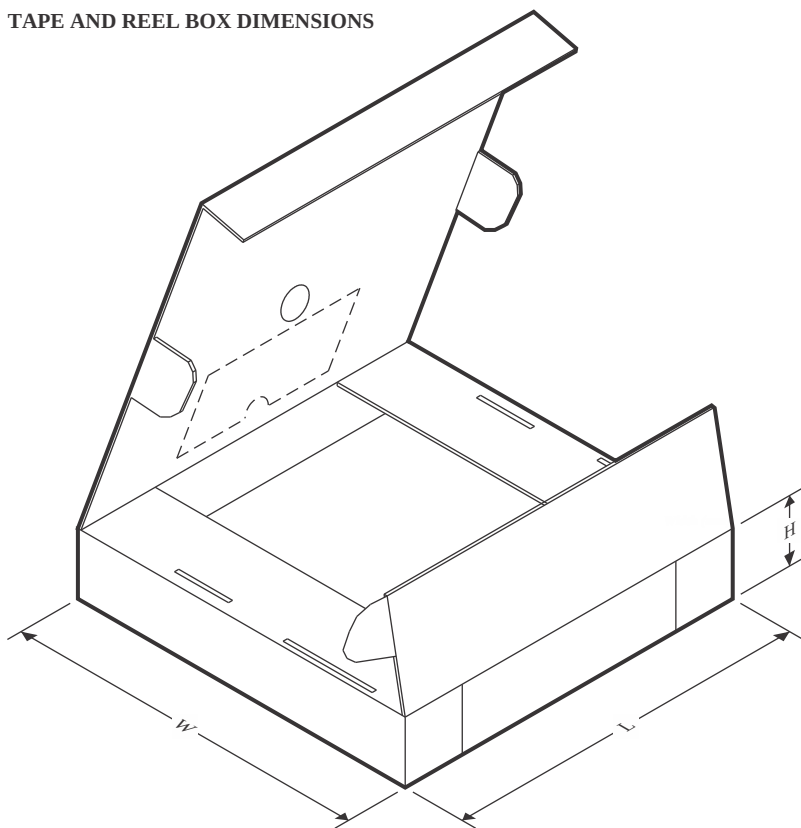
TAPE AND REEL INFORMATION



*All dimensions are nominal

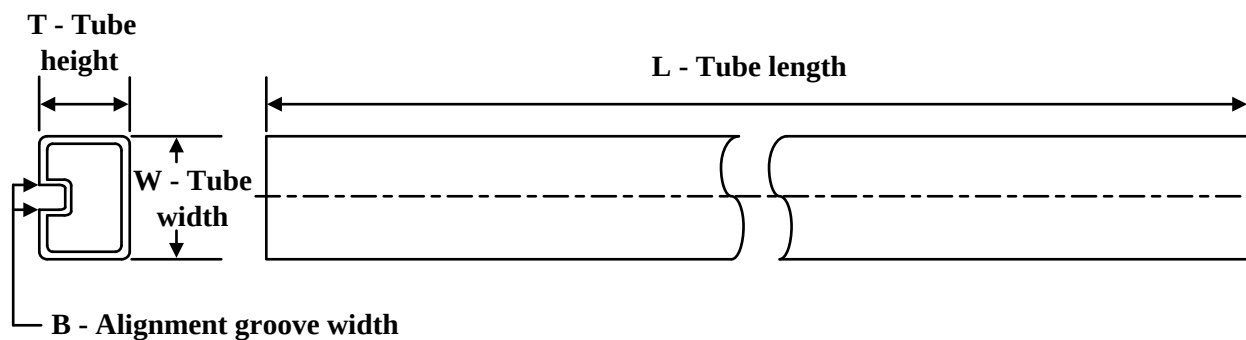
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2021ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2021AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2021CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2021IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022AMDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022AMDRG4	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2024CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2021ACDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2021AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2021CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2021IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2022ACDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2022AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2022AMDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2022AMDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLE2022CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2022IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2022MDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2024CDWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLE2021ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021CP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021IP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021MD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2021MD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLE2021MDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLE2021MDG4.A	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022AMDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022AMDG4.A	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022CP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022IP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022IPE4	P	PDIP	8	50	506	13.97	11230	4.32
TLE2024ACN	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024AIDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TLE2024AIDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLE2024AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024AIN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024CN	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024IN	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024IN.A	N	PDIP	14	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

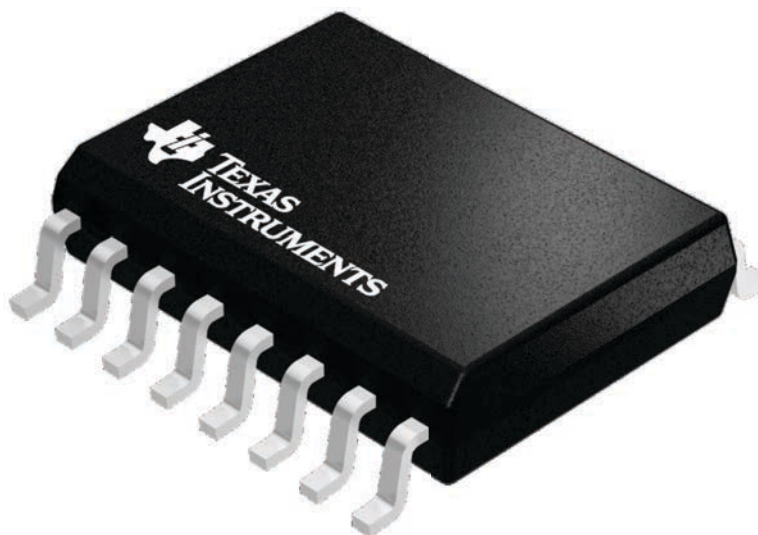
DW 16

SOIC - 2.65 mm max height

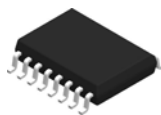
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

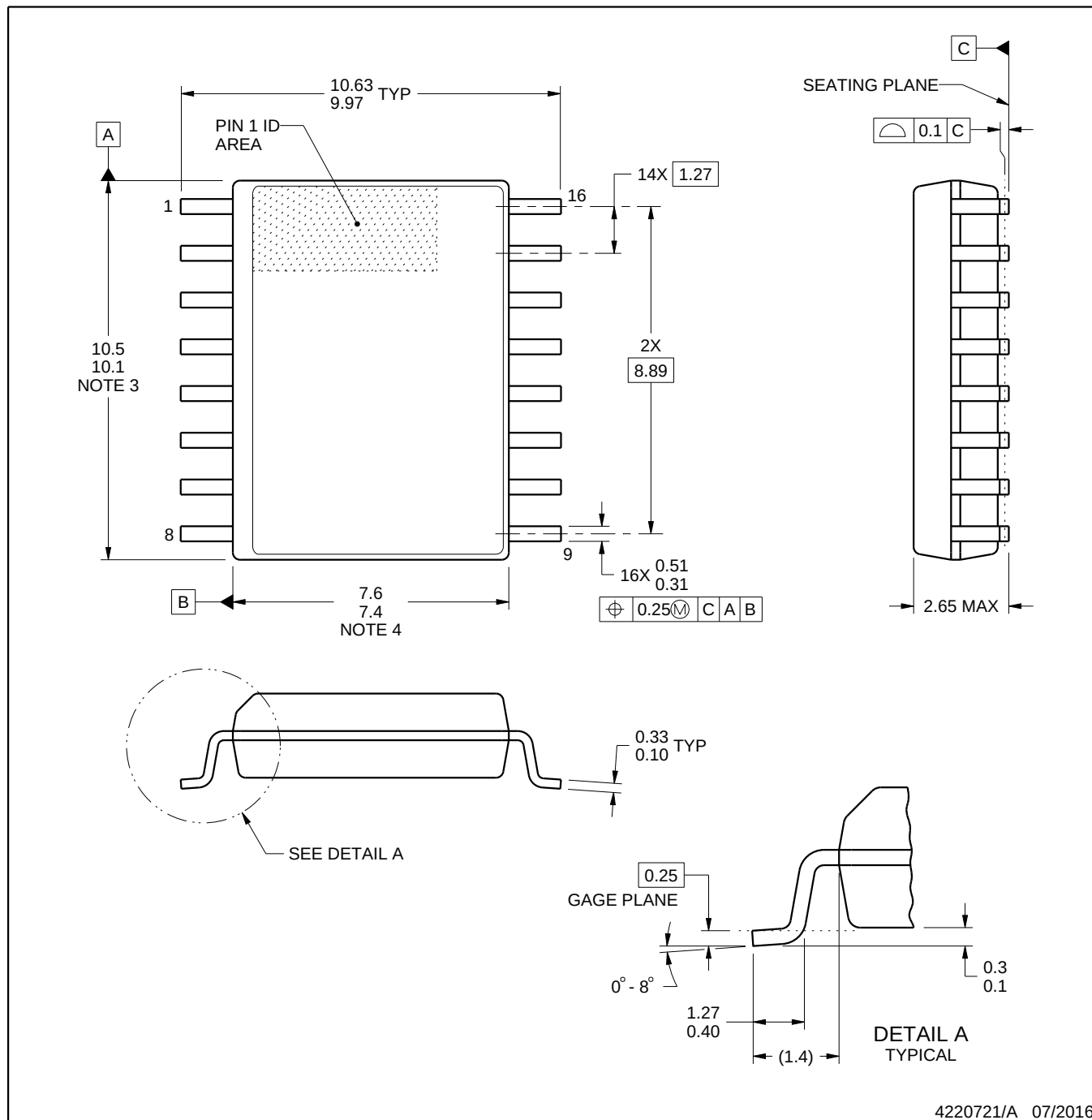


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

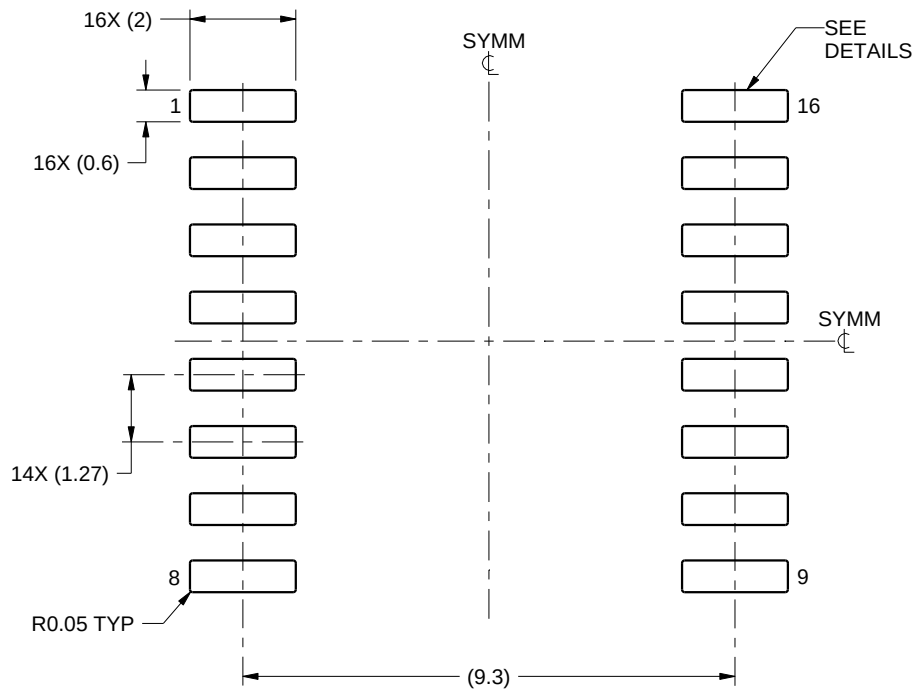
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

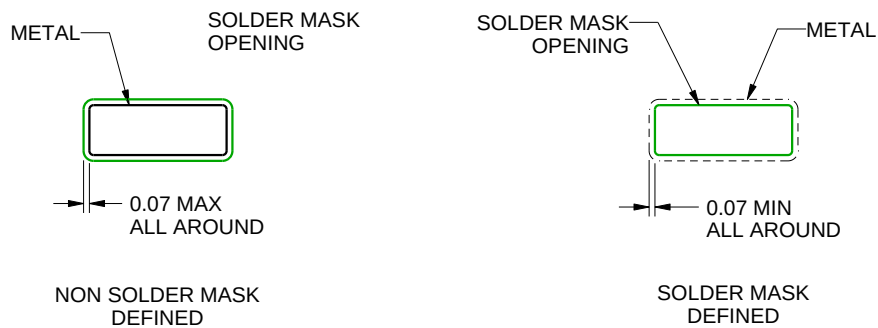
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

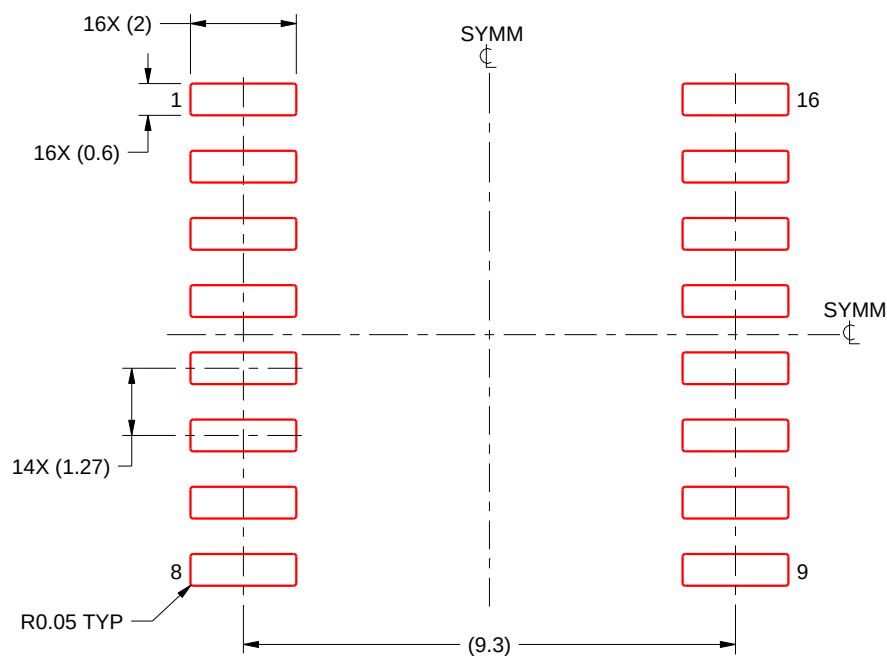
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC

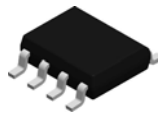


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

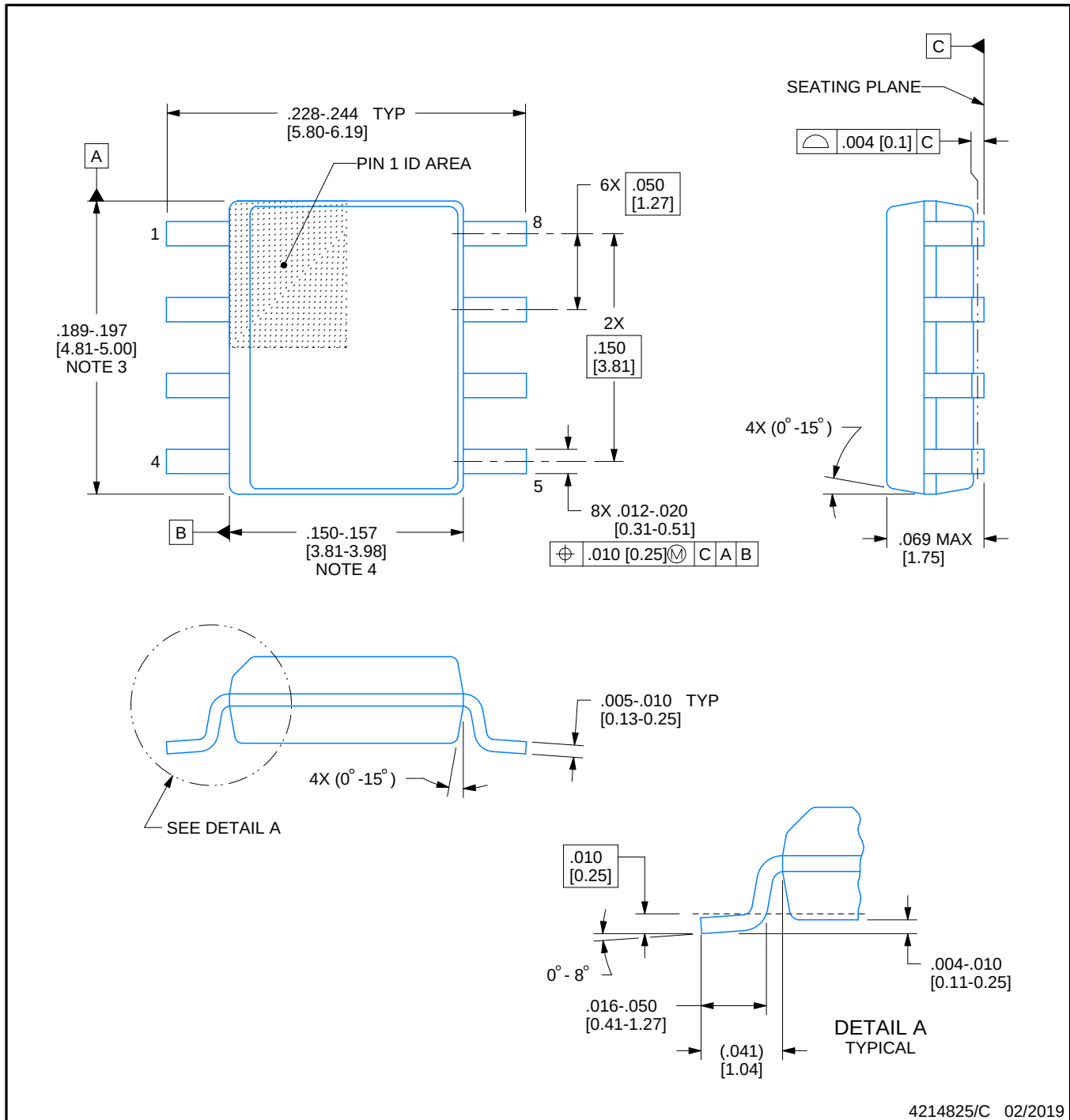


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

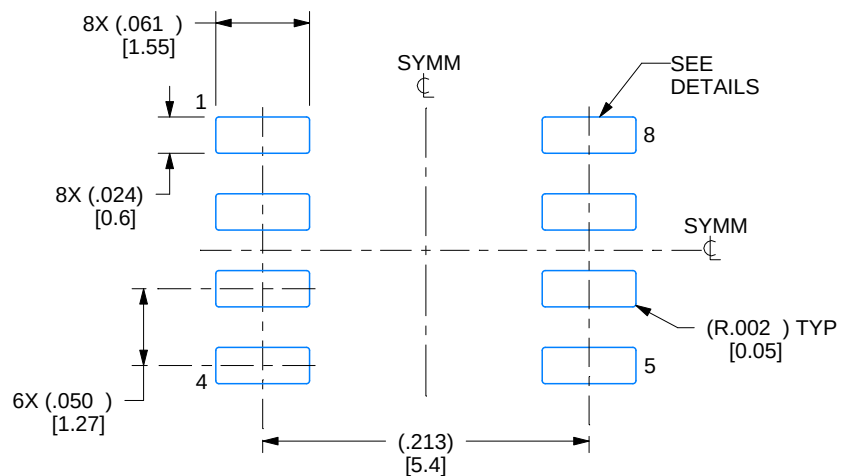
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

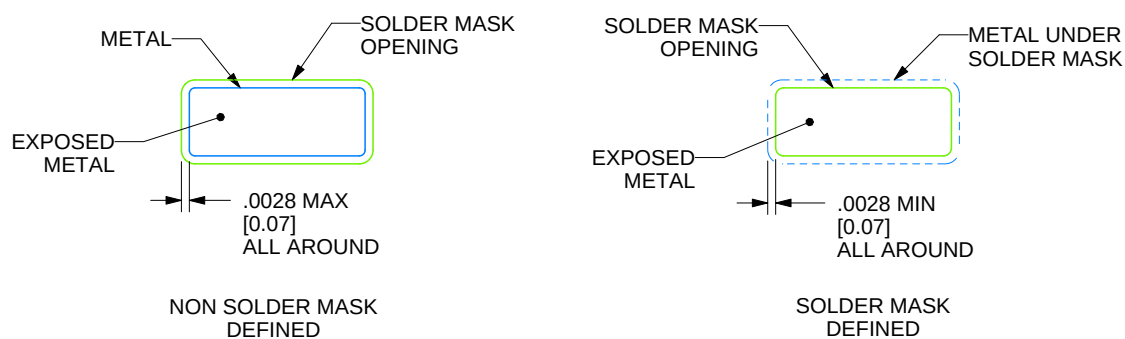
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

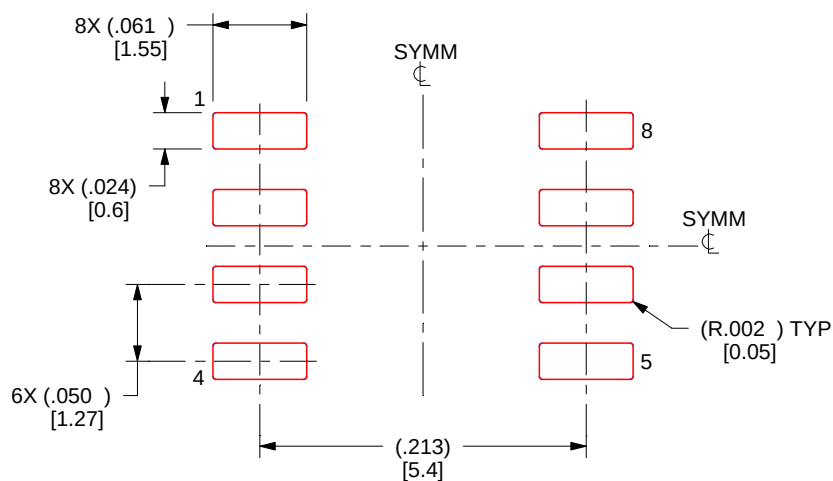
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

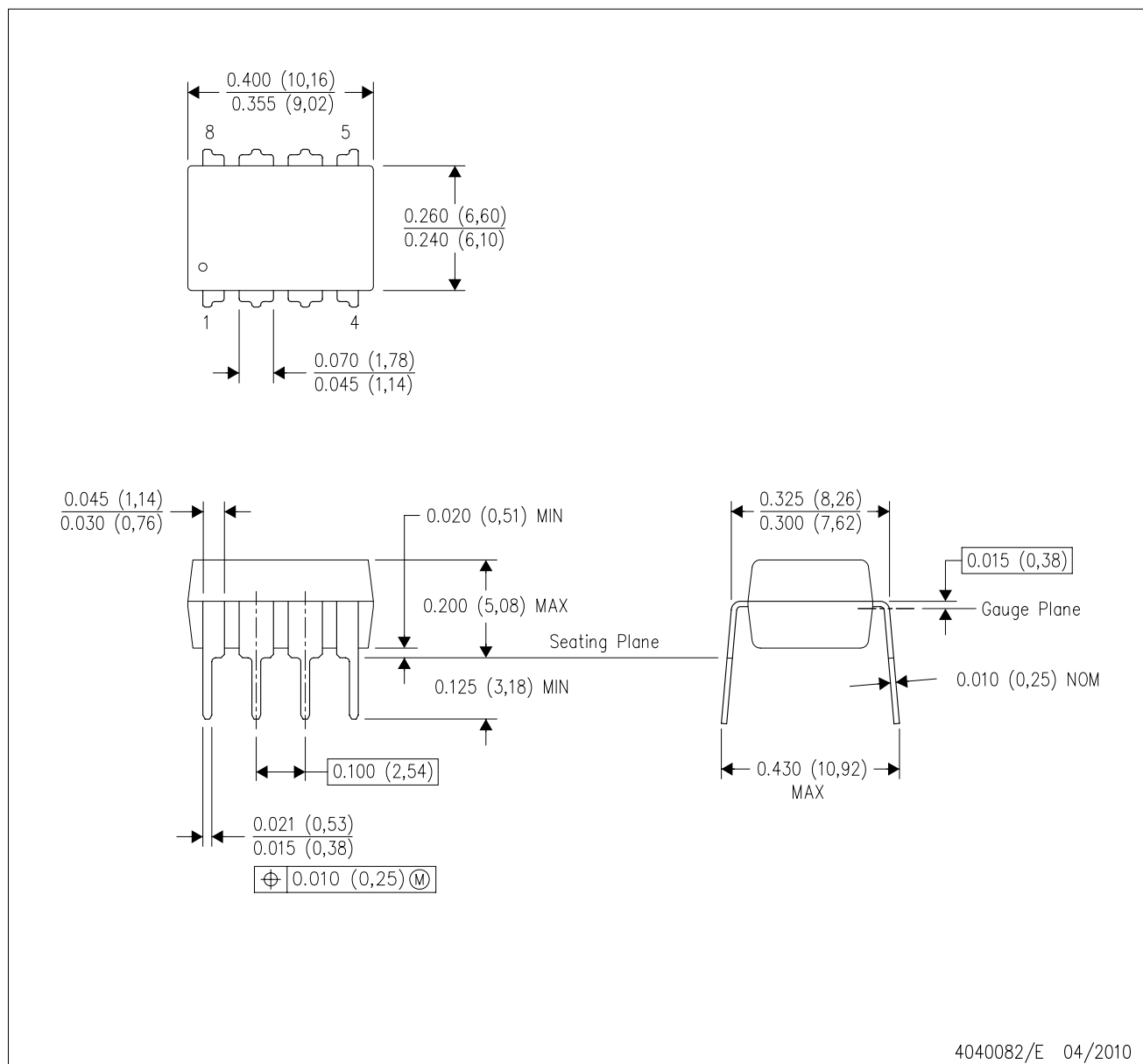
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

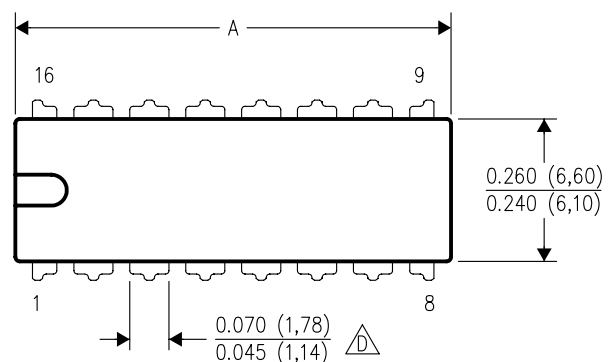


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

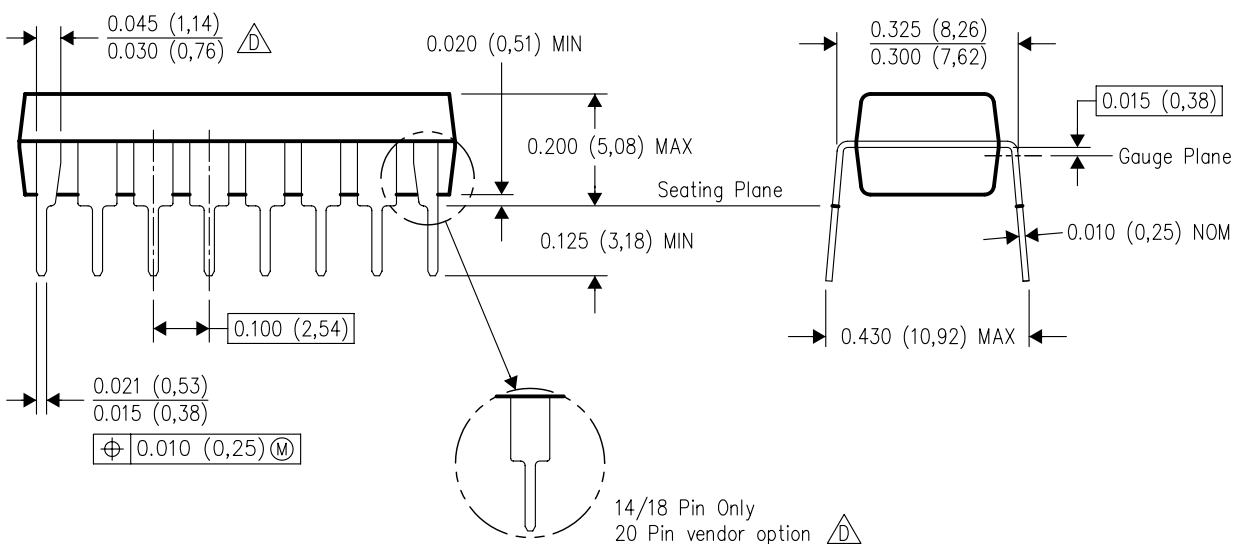
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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