

CY74FCT163245
CY74FCT163H245
CY74FCT163LD245
CY74FCT163LDH245

16-Bit Transceiver

Features

- Low power, pin-compatible replacement for LCX, LPT, LVC, LVCH & LVT families
- 5V tolerant inputs and outputs*
- 6 mA & 24 mA balanced drive outputs
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for reduced noise
- FCT-C speed at 4.1 ns
- Latch-up performance exceeds JEDEC standard no. 17
- Typical output skew < 250ps
- Industrial temperature range of -40°C to $+85^{\circ}\text{C}$
- TSSOP (19.6-mil pitch) or SSOP (25-mil pitch)
- Typical V_{olp} (ground bounce) performance exceeds Mil Std 883D
- $V_{\text{CC}} = 2.7\text{V}$ to 3.6V
- ESD (HBM) > 2000V

CY74FCT163H245

- Bus hold on data inputs
- Eliminates the need for external pull-up or pull-down resistors
- *Devices with bus hold are not recommended for translating rail-to-rail CMOS signals to 3.3V logic levels

CY74FCT163LD245

- Lite Drive™ option for low noise applications
- 6 mA balanced drive outputs
- FCT-A speed at 4.8 ns
- $V_{\text{CC}} = 3.0\text{V}$ to 3.6V
- ESD (HBM) > 1100V

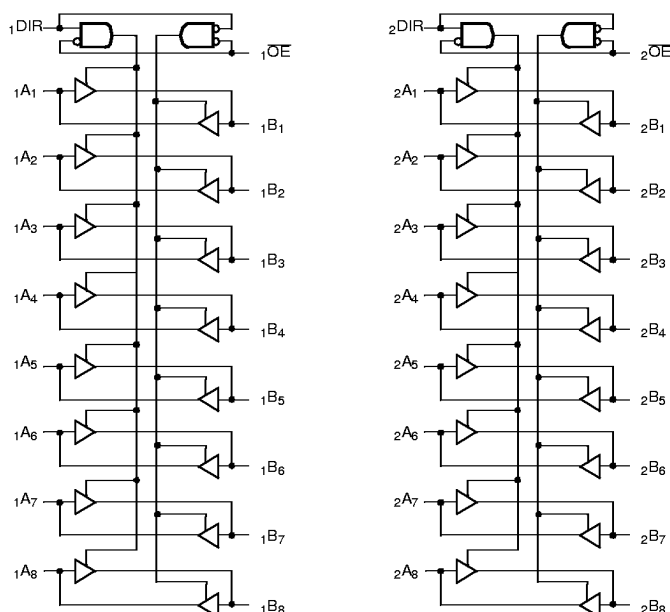
Functional Description

These 16-bit transceivers are designed for use in bidirectional synchronous communication between two buses, where high speed and low power are required. Direction of data flow is controlled by (DIR), the Output Enable (OE) transfers data when LOW and isolates the buses when HIGH. The outputs are 24-mA balanced output drivers with current limiting resistors to reduce the need for external terminating resistors and provide for minimal undershoot and reduced ground bounce.

The CY74FCT163H245 and the CY74FCT163LDH245 have "bus hold" on the data inputs, which retain the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

The CY74FCT163245 and the CY74FCT163LD245 are designed with inputs and outputs capable of being driven by 5.0V buses, allowing them to be used in mixed voltage systems as translators. The outputs are also designed with a power off disable feature enabling them to be used in applications requiring live insertion.

Logic Block Diagrams CY74FCT163245, CY74FCT163H245, CY74FCT163LD245, CY74FCT163LDH245



Pin Configuration

SSOP/TSSOP Top View

1 DIR	1	48	1 OE
1 B1	2	47	1 A1
1 B2	3	46	1 A2
GND	4	45	GND
1 B3	5	44	1 A3
1 B4	6	43	1 A4
VCC	7 163245	42	VCC
1 B5	8 163H245	41	1 A5
1 B6	9	40	1 A6
GND	10	39	GND
1 B7	11	38	1 A7
1 B8	12	37	1 A8
2 B1	13	36	2 A1
2 B2	14	35	2 A2
GND	15	34	GND
2 B3	16	33	2 A3
2 B4	17	32	2 A4
VCC	18	31	VCC
2 B5	19	30	2 A5
2 B6	20	29	2 A6
GND	21	28	GND
2 B7	22	27	2 A7
2 B8	23	26	2 A8
2 DIR	24	25	2 OE

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Pin Description

Name	Description
OE	Three-State Output Enable Inputs (Active LOW)
DIR	Direction Control
A	Inputs or Three-State Outputs ^[1]
B	Inputs or Three-State Outputs ^[1]

Function Table^[2]

Inputs		Outputs
OE	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to +125°C

Ambient Temperature with
Power Applied..... -55°C to +125°C

Supply Voltage Range 0.5V to 4.6V

DC Input Voltage -0.5V to +7.0V

DC Output Voltage..... -0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) -60 to +120 mA

Power Dissipation 1.0W

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	2.7V to 3.6V

Electrical Characteristics for Non Bus Hold Devices Over the Operating Range V_{CC}=2.7V to 3.6V

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{IH}	Input HIGH Voltage	All Inputs	2.0		5.5	V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[6]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =5.5			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	μA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =5.5V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =GND			±1	μA
I _{OS}	Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =GND	-60	-135	-240	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±100	μA
I _{CC}	Quiescent Power Supply Current	V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V, V _{CC} =Max.		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{IN} =V _{CC} -0.6V ^[8] , V _{CC} =Max.		2.0	30	μA

Note:

- On CY74FCT163H245 and CY74FCT163LDH245 these pins have bus hold.
- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- Typical values are at V_{CC}=3.3V, T_A = +25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Per TTL driven input; all other inputs at V_{CC} or GND.



Electrical Characteristics For Bus Hold Devices Over the Operating Range $V_{CC}=2.7V$ to $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V_{IH}	Input HIGH Voltage	All Inputs	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis ^[6]			100		mV
V_{IK}	Input Clamp Diode Voltage	$V_{CC}=\text{Min.}, I_{IN}=-18\text{ mA}$		-0.7	-1.2	V
I_{IH}	Input HIGH Current	$V_{CC}=\text{Max.}, V_I=V_{CC}$			± 100	μA
I_{IL}	Input LOW Current				± 100	μA
I_{BBH} I_{BBL}	Bus Hold Sustain Current on Bus Hold Input ^[9]	$V_{CC}=\text{Min.}$ $V_I=2.0V$	-50			μA
		$V_I=0.8V$	+50			μA
I_{BHHO} I_{BHLO}	Bus Hold Overdrive Current on Bus Hold Input ^[9]	$V_{CC}=\text{Max.}, V_I=1.5V$			± 500	μA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}, V_{OUT}=V_{CC}$			± 1	μA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}, V_{OUT}=\text{GND}$			± 1	μA
I_{OS}	Short Circuit Current ^[7]	$V_{CC}=\text{Max.}, V_{OUT}=\text{GND}$	-60	-135	-240	mA
I_{OFF}	Power-Off Disable	$V_{CC}=0V, V_{OUT}\leq 4.5V$			± 100	μA
I_{CC}	Quiescent Power Supply Current	$V_{IN}\leq 0.2V,$ $V_{IN}\geq V_{CC}-0.2V$ $V_{CC}=\text{Max.}$			+40	μA
ΔI_{CC}	Quiescent Power supply Current (TTL inputs HIGH)	$V_{IN}=V_{CC}-0.6V$ ^[8] $V_{CC}=\text{Max.}$			+350	μA

Electrical Characteristics For Balanced Drive Devices Over the Operating Range $V_{CC}=2.7V$ to $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
I_{ODL}	Output LOW Dynamic Current ^[7]	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	45		180	mA
I_{ODH}	Output HIGH Dynamic Current ^[7]	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	-45		-180	mA
V_{OH}	Output HIGH Voltage	$V_{CC}=\text{Min.}, I_{OH}=-0.1\text{ mA}$ $V_{CC}=\text{Min.}, I_{OH}=-8\text{ mA}$ $V_{CC}=3.0V, I_{OH}=-24\text{ mA}$	$V_{CC}-0.2$ 2.4 ^[10] 2.0			V
V_{OL}	Output LOW Voltage	$V_{CC}=\text{Min.}, I_{OL}=0.1\text{ mA}$ $V_{CC}=\text{Min.}, I_{OL}=24\text{ mA}$		0.3	0.55	V

Electrical Characteristics For Lite Drive Devices Over the Operating Range $V_{CC}=3.0V$ to $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
I_{ODL}	Output LOW Dynamic Current ^[7]	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	15.0		45	mA
I_{ODH}	Output HIGH Dynamic Current ^[7]	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	-15.0		-45	mA
V_{OH}	Output HIGH Voltage	$V_{CC}=3.0V, I_{OH}=-6\text{ mA}$	2.4	3.0		V
V_{OL}	Output LOW Voltage	$V_{CC}=3.0V, I_{OL}=6\text{ mA}$			0.55	V

Notes:

9. Pins with bus hold are described in Pin Description.
10. $V_{OH}=V_{CC}-0.6V$ at rated current.



Capacitance^[6](T_A = +25 °C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CCD}	Dynamic Power Supply Current ^[11]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE=GND	50	75	μA/MHz
I _C	Total Power Supply Current ^[12]	V _{CC} =Max., f ₁ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, OE=GND	0.5	0.8	mA
		V _{IN} =V _{CC} or V _{IN} =GND	0.5	0.8	mA
		V _{IN} =V _{CC} -0.6V or V _{IN} =GND	0.5	0.8	mA
		V _{CC} =Max., f ₁ =2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, OE=GND	2.0	3.0 ^[13]	mA
		V _{IN} =V _{CC} or V _{IN} =GND	2.0	3.0 ^[13]	mA
		V _{IN} =V _{CC} -0.6V or V _{IN} =GND	2.0	3.3 ^[13]	mA

Switching Characteristics Over the Operating Range V_{CC}=3.0V to 3.6V^[14,15]

Parameter	Description	CY74FCT163245A CY74FCT163H245A		CY74FCT163245C CY74FCT163H245C		Unit	Fig. No. ^[16]
		Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	1.5	4.8	1.5	4.1	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	6.2	1.5	5.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.6	1.5	5.2	ns	1, 7, 8
t _{SK(O)}	Output Skew ^[17]		0.5		0.5	ns	—

Notes:

11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH
N_T = Number of TTL inputs at D_H
N₁ = Number of inputs changing at f₁
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. For V_{CC}=2.7, propagation delay, output enable and output disable times should be degraded by 20%.
16. See "Parameter Measurement Information" in the General Information section.
17. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.



Switching Characteristics Over the Operating Range $V_{CC}=3.0V$ to $3.6V$ ^[14,15]

Parameter	Description	CY74FCT163LD245 CY74FCT163LDH245 ^[18]		CY74FCT163LD245A CY74FCT163LDH245A ^[18]		Unit	Fig. No. ^[16]
		Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5	7.0	1.5	4.8	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	9.5	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	7.5	1.5	5.6	ns	1, 7, 8
$t_{SK(O)}$	Output Skew ^[17]		0.5		0.5	ns	—

Note:

18. For Lite Drive devices the load capacitance is 30 pF. For other devices the load capacitance is 50 pF.

Ordering Information CY74FCT163245

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT163245CPAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163245CPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT163245APAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163245APVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT163H245

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT163H245CPAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163H245CPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT163H245APAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163H245APVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT163LD245

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.8	CY74FCT163LD245APAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163LD245APVC	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT163LD245PAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163LD245PVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT163LDH245

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.8	CY74FCT163LDH245APAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163LDH245APVC	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT163LDH245PAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163LDH245PVC	O48	48-Lead (300-Mil) SSOP	

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