

Complementary 20 V (D-S) Low-Threshold MOSFET

PRODUCT SUMMARY

	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.280 at $V_{GS} = 4.5$ V	1.28
		0.360 at $V_{GS} = 2.5$ V	1.13
		0.450 at $V_{GS} = 1.8$ V	1
P-Channel	- 20	0.490 at $V_{GS} = - 4.5$ V	- 1
		0.750 at $V_{GS} = - 2.5$ V	- 0.81
		1.10 at $V_{GS} = - 1.8$ V	- 0.67

FEATURES

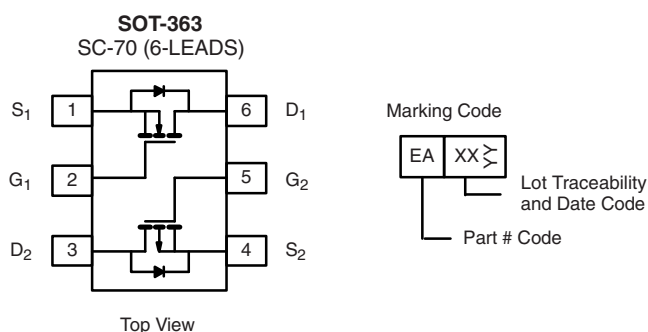
- TrenchFET® Power MOSFETS: 1.8 V Rated
- ESD Protected: 2000 V
- Thermally Enhanced SC-70 Package
- Material categorization:
For definitions of compliance please see
www.vishay.com/doc?99912



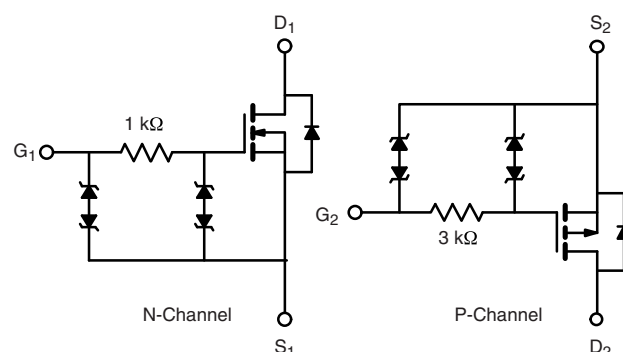
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Load Switching
- PA Switch
- Level Switch



Ordering Information: Si1563EDH-T1-E3 (Lead (Pb)-free)
Si1563EDH-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	N-Channel		P-Channel		Unit
		5 s	Steady State	5 s	Steady State	
Drain-Source Voltage	V_{DS}	20		- 20		V
Gate-Source Voltage	V_{GS}	± 12		± 12		V
Continuous Drain Current ($T_J = 150$ °C)	I_D	1.28	1.13	- 1	- 0.88	A
		0.92	0.81	- 0.72	- 0.63	
Pulsed Drain Current	I_{DM}	4		- 3		A
Continuous Source Current (Diode Conduction) ^a	I_S	0.61	0.48	- 0.61	- 0.48	A
Maximum Power Dissipation ^a	P_D	0.74	0.57	0.30	0.57	W
		0.38	0.30	0.16	0.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150				°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 5$ s	R_{thJA}	130	170	°C/W
	Steady State		170	220	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	80	100	°C/W

Notes:

a. Surface mounted on 1" x 1" FR4 board.

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 100 μA	N-Ch	0.45	1	V	
		V _{DS} = V _{GS} , I _D = - 100 μA	P-Ch	- 0.45	- 1		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 4.5 V	N-Ch		± 1	μA	
			P-Ch		± 1		
		V _{DS} = 0 V, V _{GS} = ± 12 V	N-Ch		± 10	mA	
			P-Ch		± 10		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V	N-Ch		1	μA	
		V _{DS} = - 16 V, V _{GS} = 0 V	P-Ch		- 1		
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 85 °C	N-Ch		5		
		V _{DS} = - 16 V, V _{GS} = 0 V, T _J = 85 °C	P-Ch		- 5		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	2		A	
		V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	P-Ch	- 2			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 1.13 A	N-Ch		0.220	0.280	Ω
		V _{GS} = - 4.5 V, I _D = - 0.88 A	P-Ch		0.400	0.490	
		V _{GS} = 2.5 V, I _D = 0.99 A	N-Ch		0.281	0.360	
		V _{GS} = - 2.5 V, I _D = - 0.71 A	P-Ch		0.610	0.750	
		V _{GS} = 1.8 V, I _D = 0.20 A	N-Ch		0.344	0.450	
		V _{GS} = - 1.8 V, I _D = - 0.20 A	P-Ch		0.850	1.10	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 1.13 A	N-Ch		2.6		S
		V _{DS} = - 10 V, I _D = - 0.88 A	P-Ch		1.5		
Diode Forward Voltage ^a	V _{SD}	I _S = 0.48 V, V _{GS} = 0 V	N-Ch		0.8	1.2	V
		I _S = - 0.48 V, V _{GS} = 0 V	P-Ch		- 0.8	- 1.2	
Dynamic ^b							
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 1.13 A P-Channel V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 0.88 A	N-Ch		0.65	1	nC
Gate-Source Charge	Q _{gs}		P-Ch		1.2	1.8	
			N-Ch		0.2		
Gate-Drain Charge	Q _{gd}		P-Ch		0.3		
		N-Ch		0.23			
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 20 Ω I _D ≅ 0.5 A, V _{GEN} = 4.5 V, R _g = 6 Ω P-Channel V _{DD} = - 10 V, R _L = 20 Ω I _D ≅ - 0.5 A, V _{GEN} = - 4.5 V, R _g = 6 Ω	P-Ch		0.3		ns
			N-Ch		45	70	
P-Ch			150	230			
N-Ch			85	130			
P-Ch			480	720			
Turn-Off Delay Time	t _{d(off)}		N-Ch		350	530	
			P-Ch		840	1200	
Fall Time	t _f		N-Ch		210	320	
		P-Ch		850	1200		

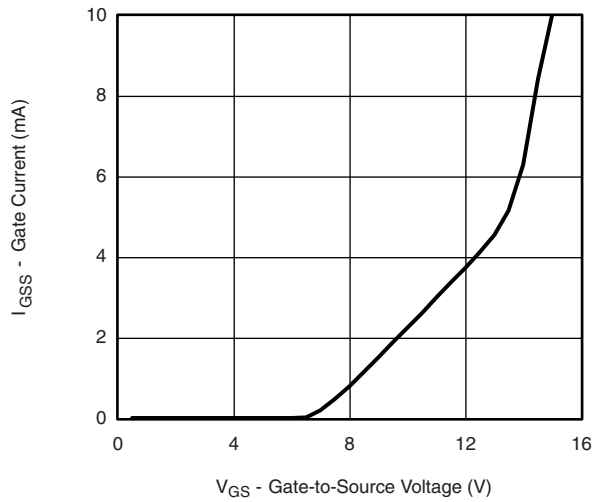
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

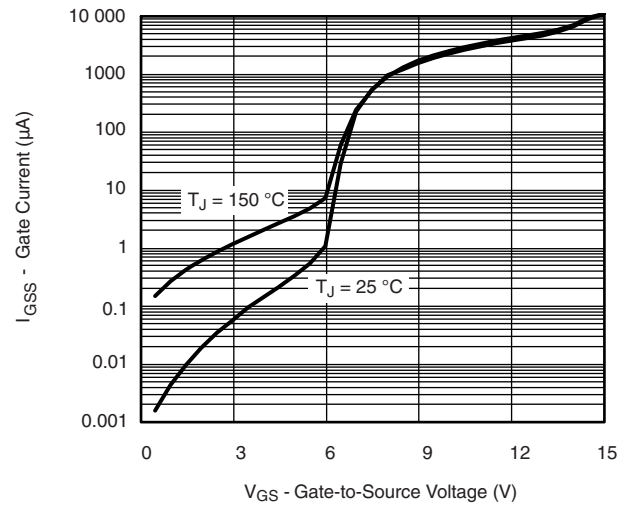
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

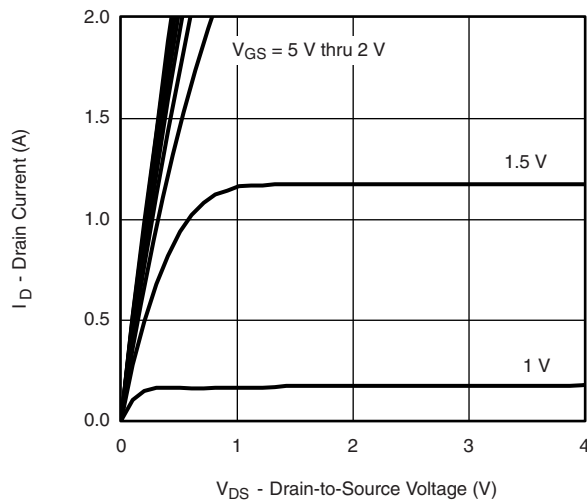
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



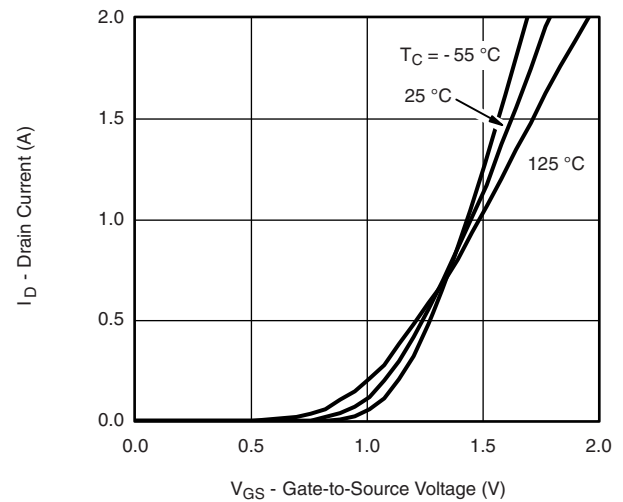
Gate-Current vs. Gate-Source Voltage



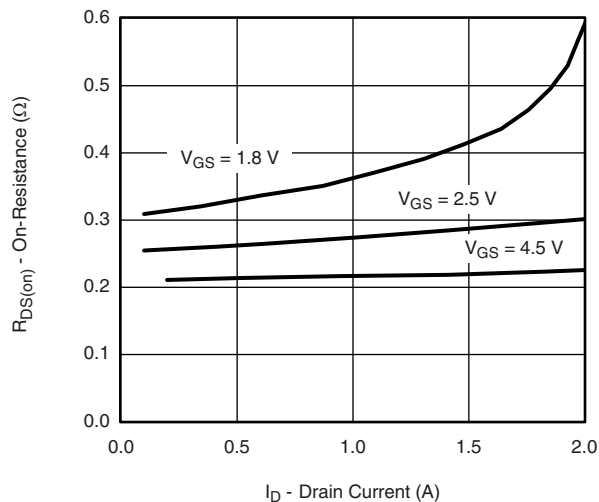
Gate-Current vs. Gate-Source Voltage



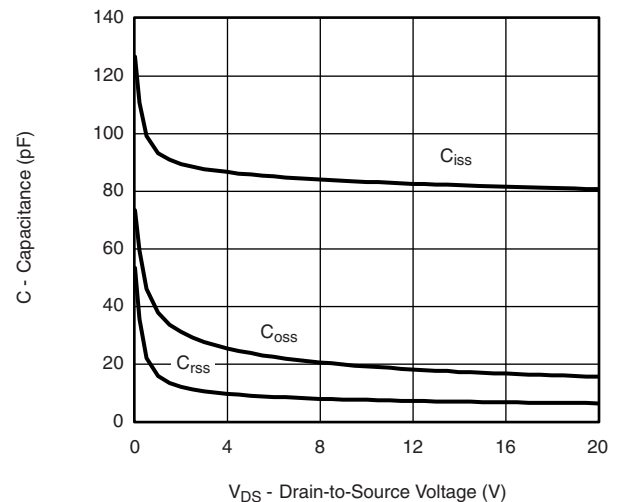
Output Characteristics



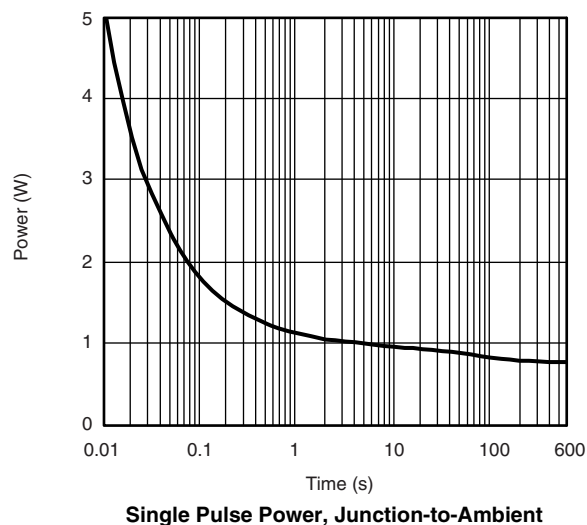
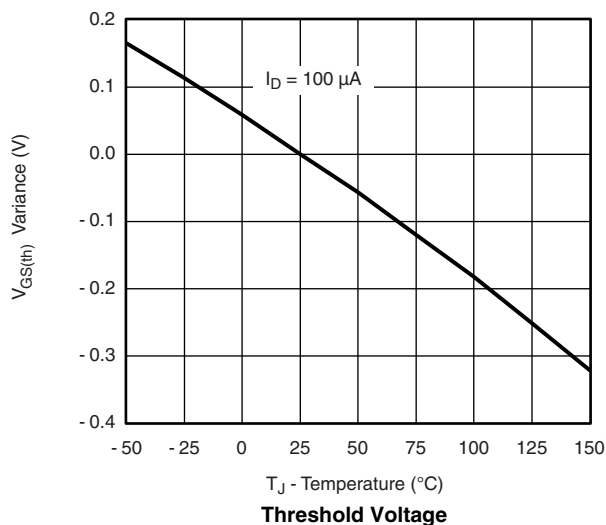
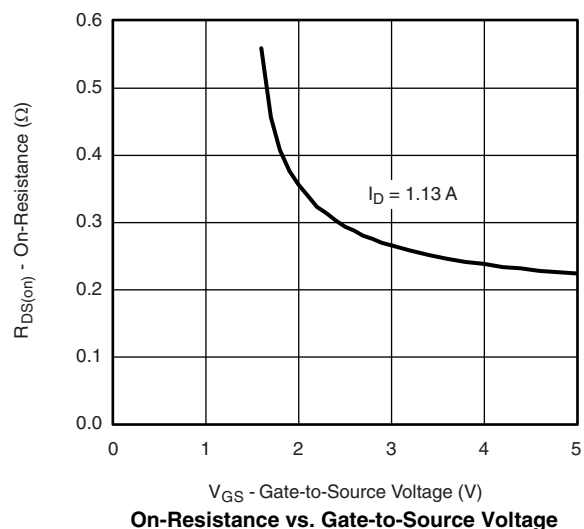
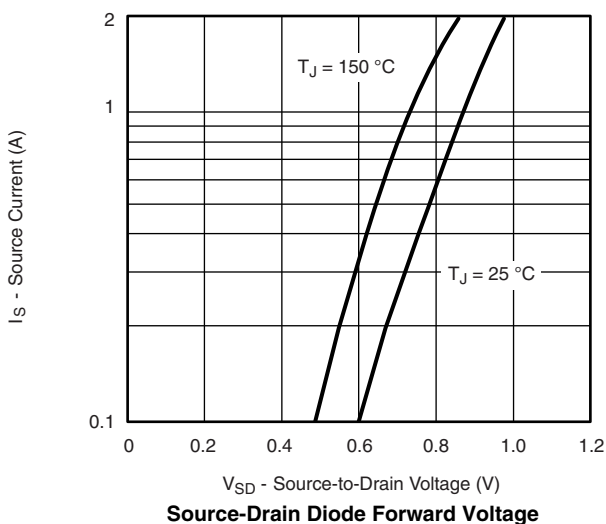
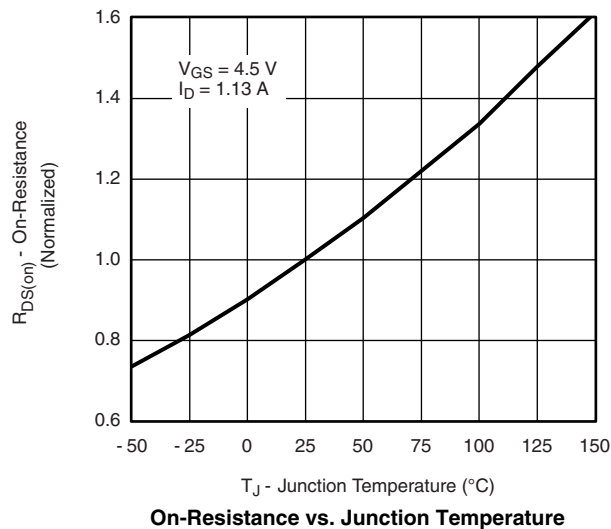
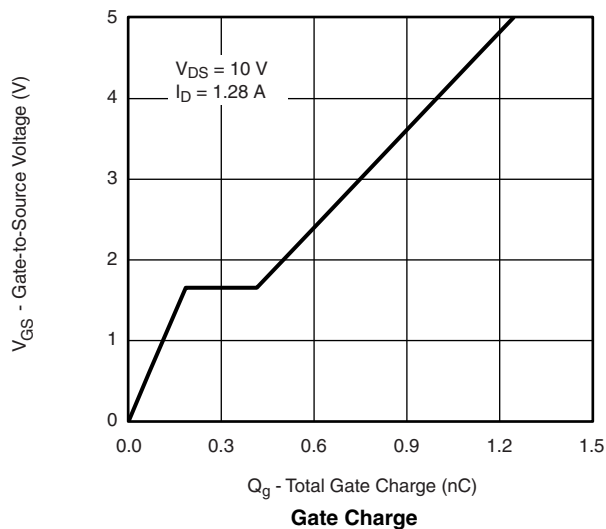
Transfer Characteristics



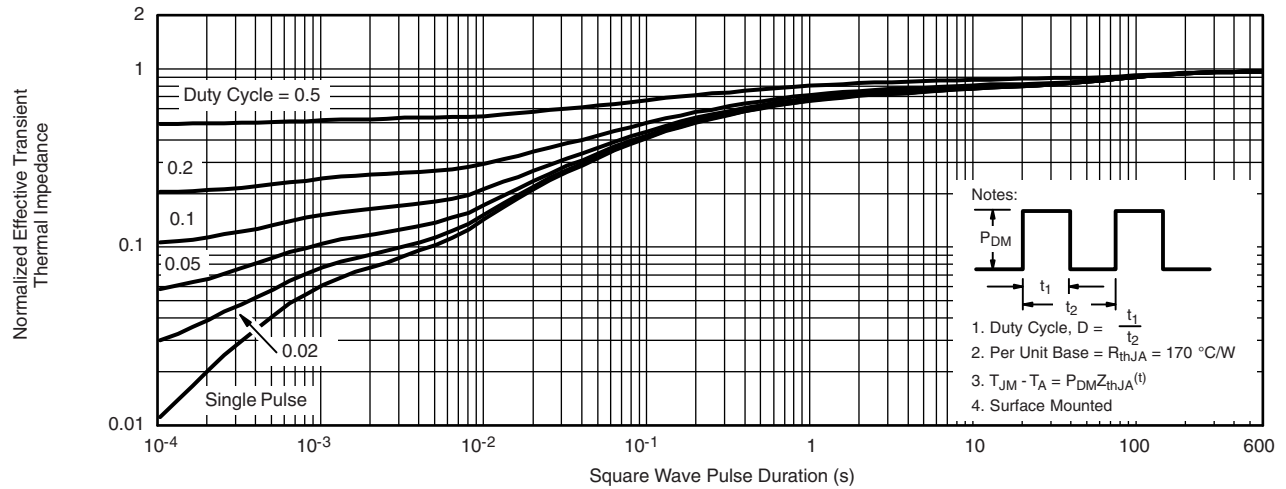
On-Resistance vs. Drain Current



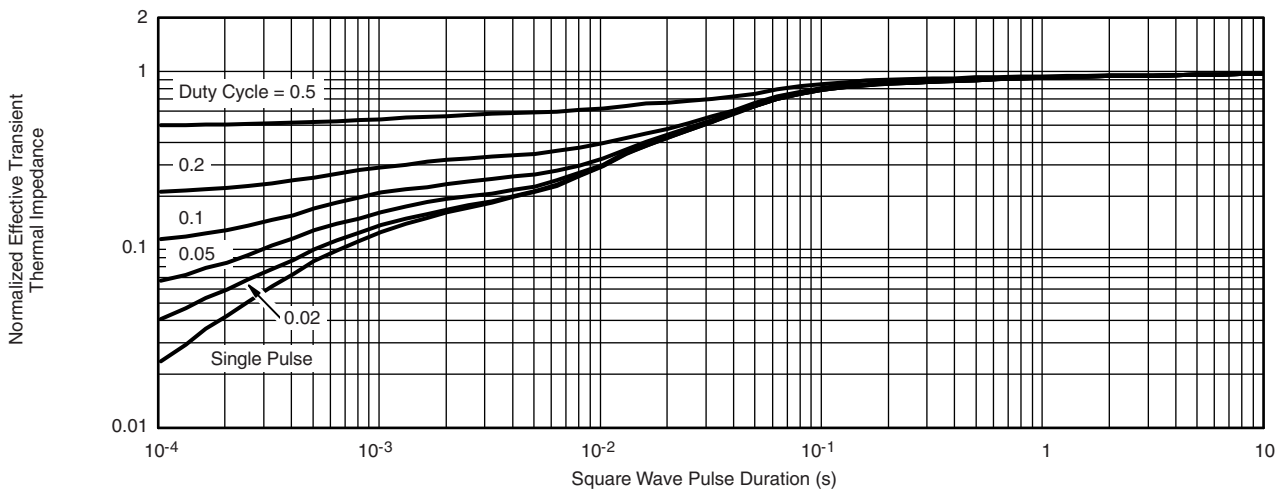
Capacitance

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

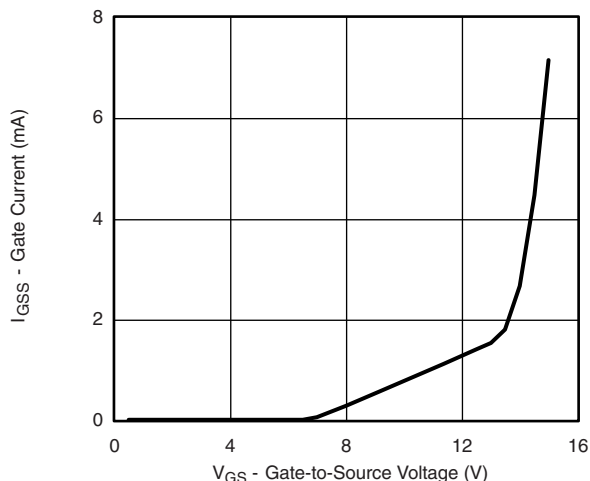
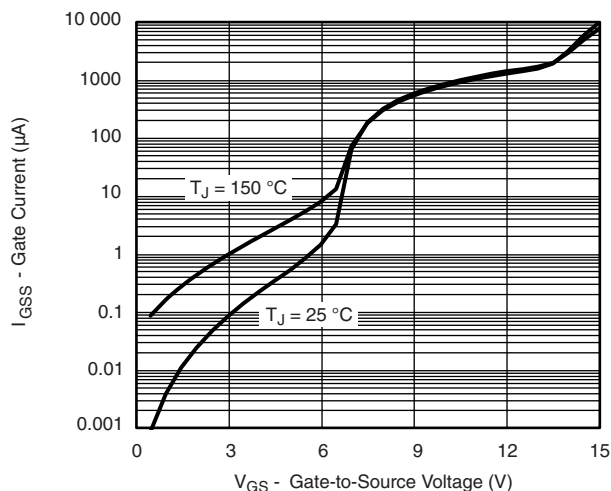
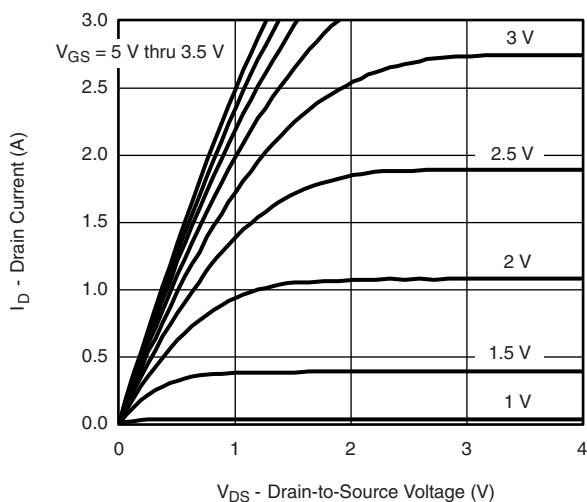
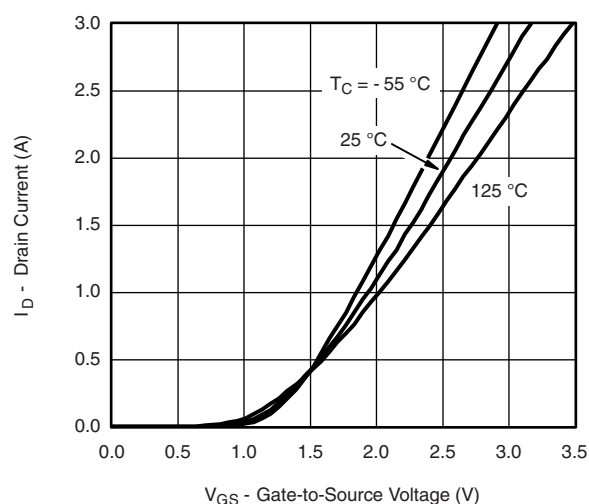
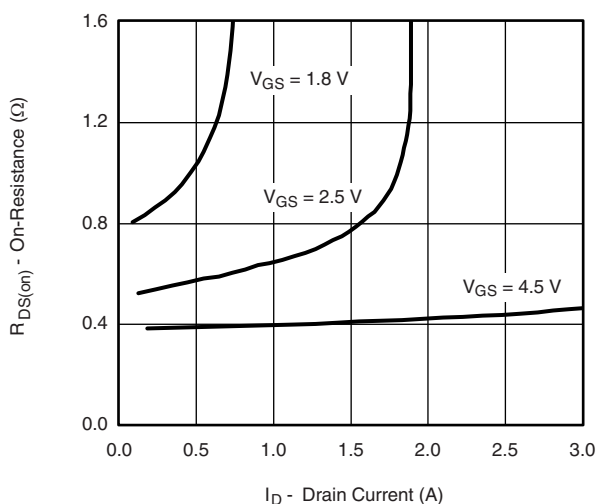
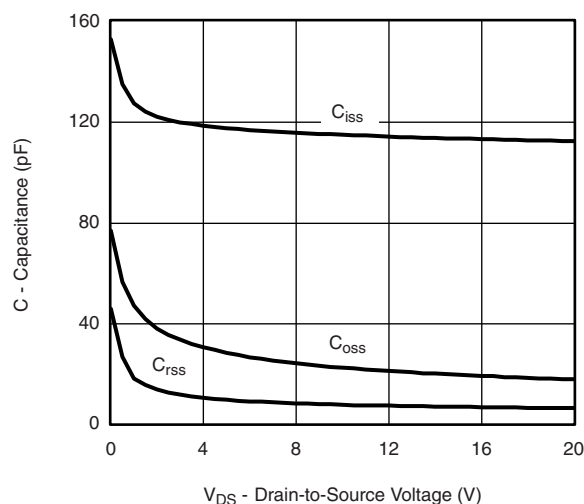
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



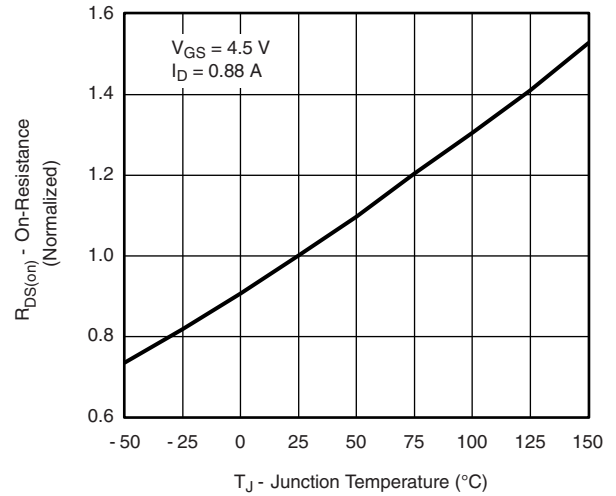
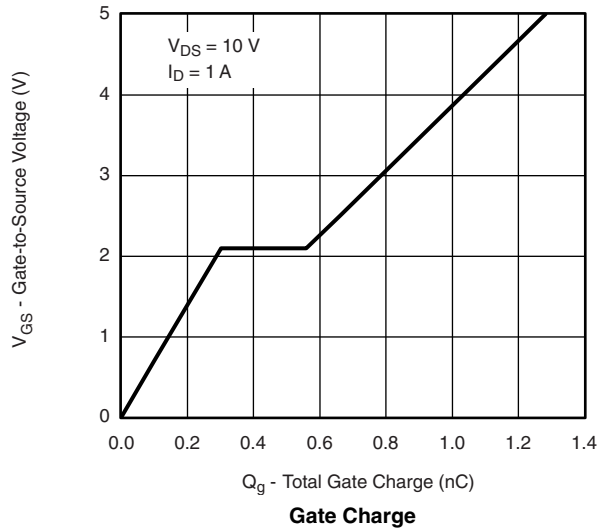
Normalized Thermal Transient Impedance, Junction-to-Ambient



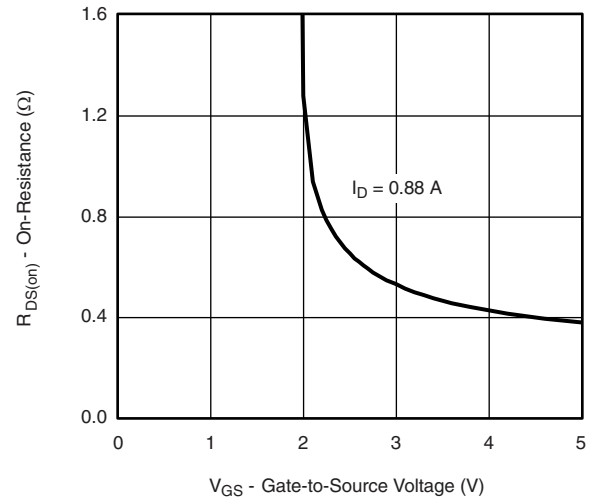
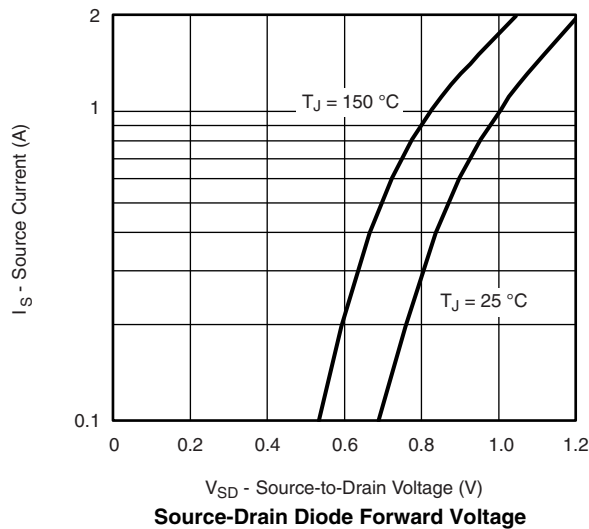
Normalized Thermal Transient Impedance, Junction-to-Foot

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Gate-Current vs. Gate-Source Voltage****Gate-Current vs. Gate-Source Voltage****Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance**

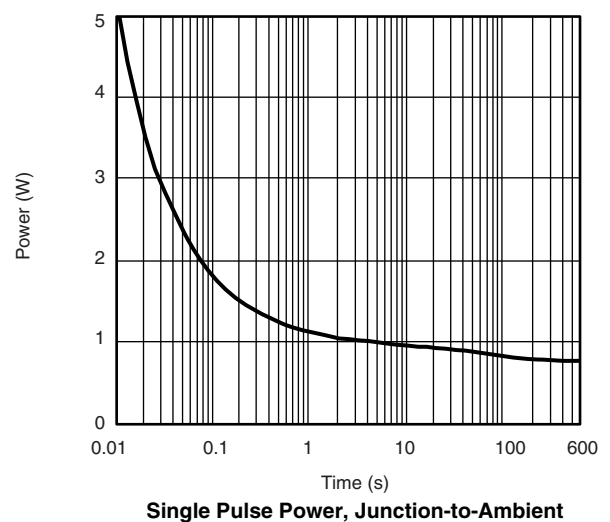
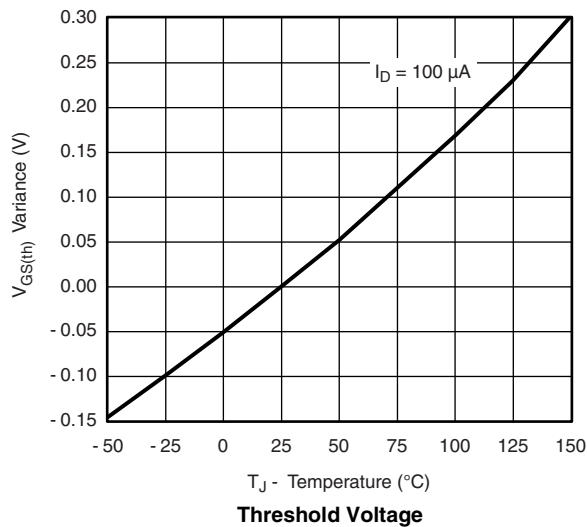
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



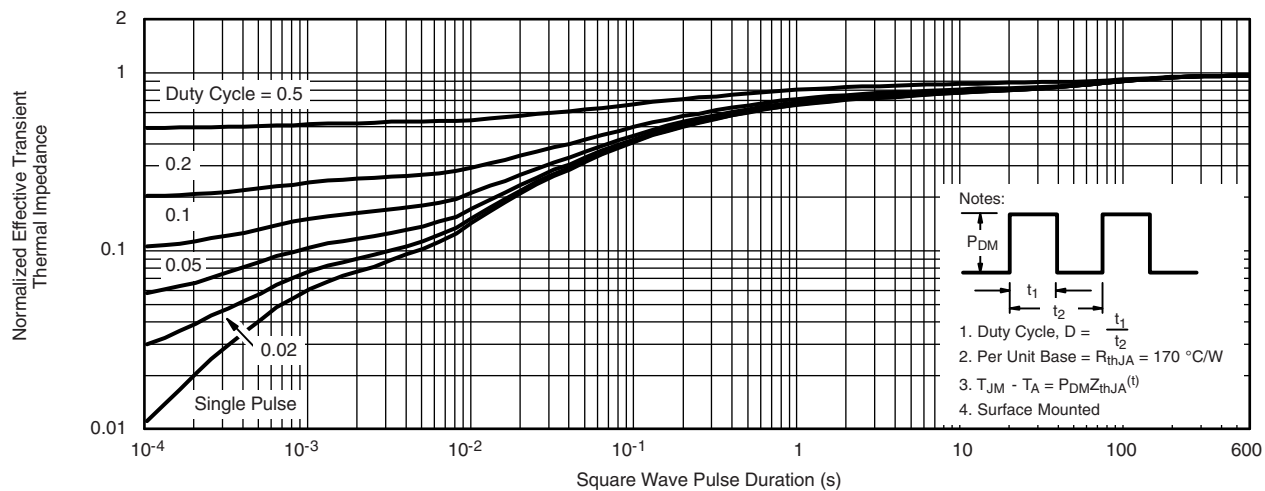
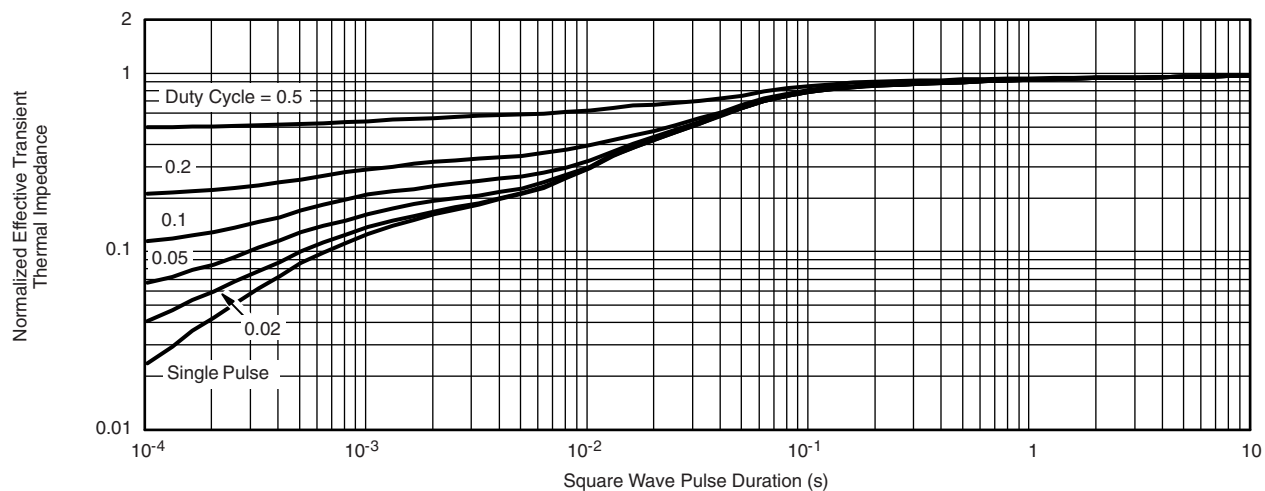
On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



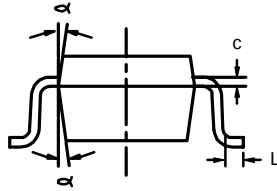
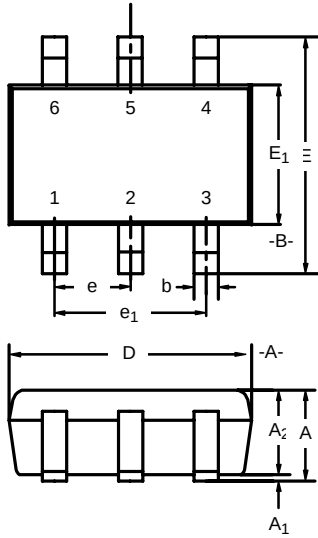
Single Pulse Power, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot**

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SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	–	1.10	0.035	–	0.043
A ₁	–	–	0.10	–	–	0.004
A ₂	0.80	–	1.00	0.031	–	0.039
b	0.15	–	0.30	0.006	–	0.012
c	0.10	–	0.25	0.004	–	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E ₁	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e ₁	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

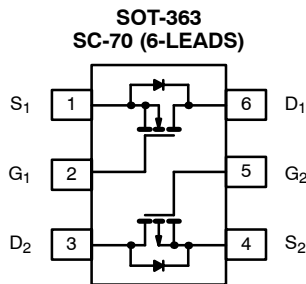
Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance

INTRODUCTION

The new dual 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the dual-channel version.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration. Both n-and p-channel devices are available in this package – the drawing example below illustrates the p-channel device.



Top View
FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (<http://www.vishay.com/doc?71154>)

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>) for the SC-70 6-pin basic pad layout and dimensions. This pad pattern is sufficient for the low-power applications for which this package is intended. Increasing the drain pad pattern (Figure 2) yields a reduction in thermal resistance and is a preferred footprint.

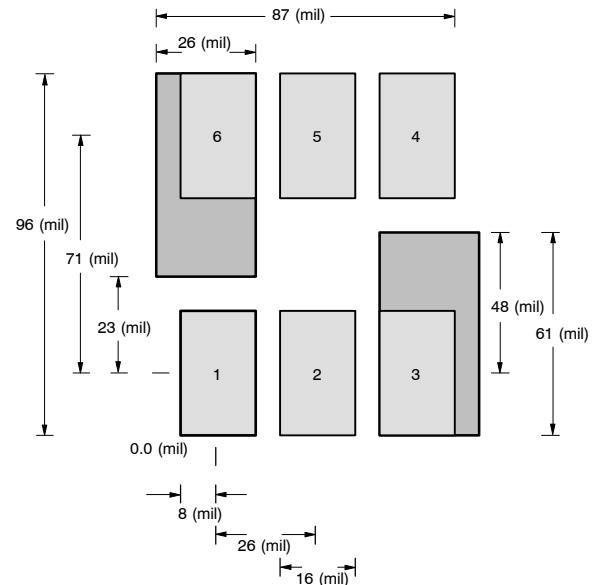


FIGURE 2. SC-70 (6 leads) Dual

EVALUATION BOARD FOR THE DUAL-CHANNEL SC70-6

The 6-pin SC-70 evaluation board (EVB) shown in Figure 3 measures 0.6 in. by 0.5 in. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows for examination from the outer pins to the 6-pin DIP connections, permitting test sockets to be used in evaluation testing.

The thermal performance of the dual 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was then repeated using the 1-inch² PCB with dual-side copper coating.

A helpful way of displaying the thermal performance of the 6-pin SC-70 dual copper leadframe is to compare it to the traditional Alloy 42 version.

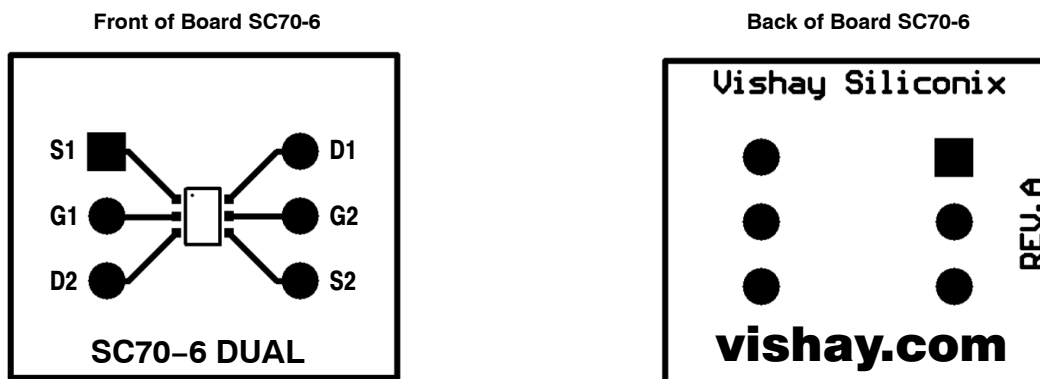


FIGURE 3.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package is measured as junction-to-foot thermal resistance, in which the “foot” is the drain lead of the device as it connects with the body. The junction-to-foot thermal resistance for this device is typically 80°C/W, with a maximum thermal resistance of approximately 100°C/W. This data compares favorably with another compact, dual-channel package – the dual TSOP-6 – which features a typical thermal resistance of 75°C/W and a maximum of 90°C/W.

Power Dissipation

The typical $R_{\theta JA}$ for the dual-channel 6-pin SC-70 with a copper leadframe is 224°C/W steady-state, compared to 413°C/W for the Alloy 42 version. All figures are based on the 1-inch² FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at varying ambient temperatures.

Alloy 42 Leadframe

ALLOY 42 LEADFRAME	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$
$P_D = \frac{150^{\circ}\text{C} - 25^{\circ}\text{C}}{413^{\circ}\text{C/W}}$	$P_D = \frac{150^{\circ}\text{C} - 60^{\circ}\text{C}}{413^{\circ}\text{C/W}}$
$P_D = 303 \text{ mW}$	$P_D = 218 \text{ mW}$

COOPER LEADFRAME

Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$
$P_D = \frac{150^{\circ}\text{C} - 25^{\circ}\text{C}}{224^{\circ}\text{C/W}}$	$P_D = \frac{150^{\circ}\text{C} - 60^{\circ}\text{C}}{224^{\circ}\text{C/W}}$
$P_D = 558 \text{ mW}$	$P_D = 402 \text{ mW}$

Although they are intended for low-power applications, devices in the 6-pin SC-70 dual-channel configuration will handle power dissipation in excess of 0.5 W.

TESTING

To further aid the comparison of copper and Alloy 42 leadframes, Figures 4 and 5 illustrate the dual-channel 6-pin SC-70 thermal performance on two different board sizes and pad patterns. The measured steady-state values of $R_{\theta JA}$ for the dual 6-pin SC-70 with varying leadframes are as follows:

LITTLE FOOT 6-PIN SC-70

	Alloy 42	Copper
1) Minimum recommended pad pattern on the EVB board (see Figure 3).	518°C/W	344°C/W
2) Industry standard 1-inch ² PCB with maximum copper both sides.	413°C/W	224°C/W

The results indicate that designers can reduce thermal resistance (θ_{JA}) by 34% simply by using the copper leadframe device as opposed to the Alloy 42 version. In this example, a 174°C/W reduction was achieved without an increase in board area. If an increase in board size is feasible, a further 120°C/W reduction can be obtained by utilizing a 1-inch² PCB area.

The Dual copper leadframe versions have the following suffix:

Dual: Si19xxEDH
 Compl.: Si15xxEDH

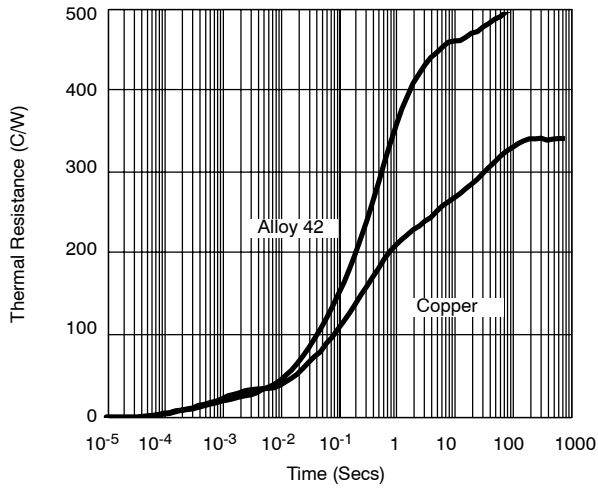


FIGURE 4. Dual SC70-6 Thermal Performance on EVB

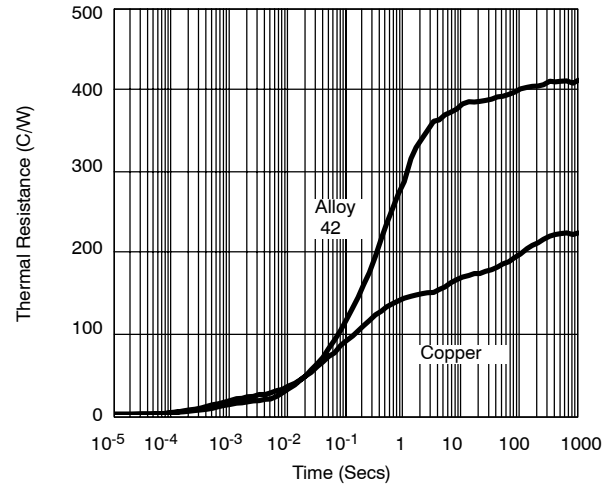
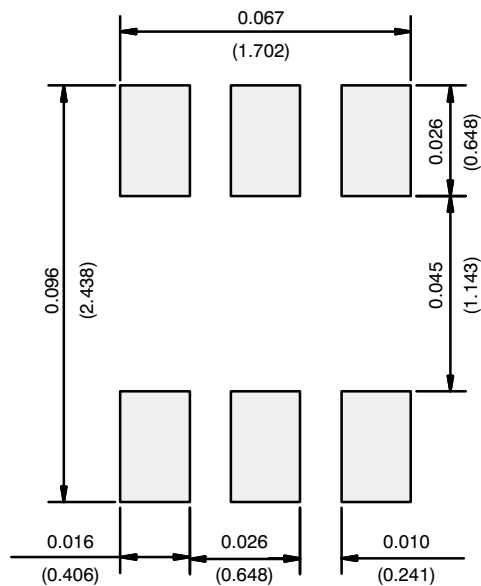


FIGURE 5. Dual SC70-6 Comparison on 1-inch² PCB

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.