

# Complete Embedded Flexibility

## Accelerating Storage System RAS & Performance

### EMBEDDED STORAGE SWITCH

The InSpeed<sup>®</sup> SOC 422 Embedded Storage Switch is the only storage switch that delivers an integrated 4Gb/s drop-in switched infrastructure for fastest time to market for storage system providers. Unlike in-house development efforts that use port bypass circuitry, InSpeed Embedded Storage Switches create Switched Bunches of Disks (SBOD<sup>®</sup>) that drastically improve the reliability, availability and serviceability (RAS) and performance while scaling of storage systems.



Available to OEMs only

With the introduction of the InSpeed SOC 422, the industry's first 4Gb/s Embedded Storage Switch, Emulex has once again advanced back-end switching to enable the next generation of storage systems using higher speeds and 2.5" Small Form Factor disk drives.

#### KEY BENEFITS:

- ⦿ Increase Availability and Reliability by 20%
- ⦿ Lower Service Costs by 10-15%
- ⦿ Reduce the Total Cost per MB of the Storage Offering by 20%
- ⦿ Increase Overall Storage System Performance up to 5x while Scaling

#### KEY FEATURES:

- ⦿ 4, 2 or 1Gb/s Non-Blocking Speeds Enable Next Generation Storage Systems
- ⦿ 22 Ports Support Emerging 2.5" Disk Drives in SBODs
- ⦿ Automatic Trunking Fully Multiplies Bandwidth with Failover Pathing
- ⦿ Integrated Fibre Channel Controller Delivers In-Band Communications—including SES
- ⦿ Fairness and Prioritization Ensures All Devices Have Guaranteed Equal Access
- ⦿ Advanced Diagnostics Continually Perform Tests and Automatically Take Corrective Actions
- ⦿ Compatible with Previous Generation InSpeed SOC and FibreSpy<sup>®</sup> Embedded Storage Switches

# Specifications

### STANDARDS

Fibre Channel Protocols:

FC-AL, FC-AL2, FC-PH, FC-PH2, FC-PI

Interoperability:

Connects to any FC-AL compliant device

Compatible with the InSpeed API

Compatible with InSpeed Embedded Storage Switches and previous generation InSpeed SOC's

### ARCHITECTURE

Fibre Channel Ports:

22

Interfaces:

Parallel bus microprocessor interface

I<sup>2</sup>C interface for access to internal

Registers:

LED interface

Testability interface

Scalability:

Up to 8 InSpeed SOC's

Trunking:

Automatic trunking fully multiplies throughput and bandwidth with failover pathing

Zoning:

Port- or ALPA-based overlapping and port-based non-overlapping

Stability:

Stealth Intelligent Change Manager automatically eliminates state and configuration change notification disruptions—zone and port-based management

Integration:

Integrated Fibre Channel Controller for in-band monitoring and control, including SES

Switch-on-a-chip (SOC) with integrated support chips

Embedded SERDES on each port

Selectable termination/swing

Equalization per port serial EEPROM

restores system configuration on power-up—configured in standalone

operation eliminates external microprocessor requirement

Reference clock:

106.25 MHz LVTTTL

### PERFORMANCE

Port Speed:

4.25, 2.125 or 1.0625Gb/s

bi-directional (800MBps per port, full duplex)

Latency:

Less than 1μSec with no contention, cut-through routing at 4Gb/s

Performance:

Full wire-speed switching

Aggregate Bandwidth:

176Gb/s

Switch Core:

23x23 non-blocking Crossbar switch core dynamically delivers multiple concurrent port-to-port connections

Retiming:

Architecture ensures jitter compliance and cleanest signals

Fairness & Prioritization:

Ensures all devices have guaranteed access to all other devices, or explicitly have prioritized access

### PHYSICAL ATTRIBUTES

Package:

35mm x 35mm footprint, 772-pin BGA

Power & Nominal Dissipation:

3.3V / 2.5V / 1.2V; 6W

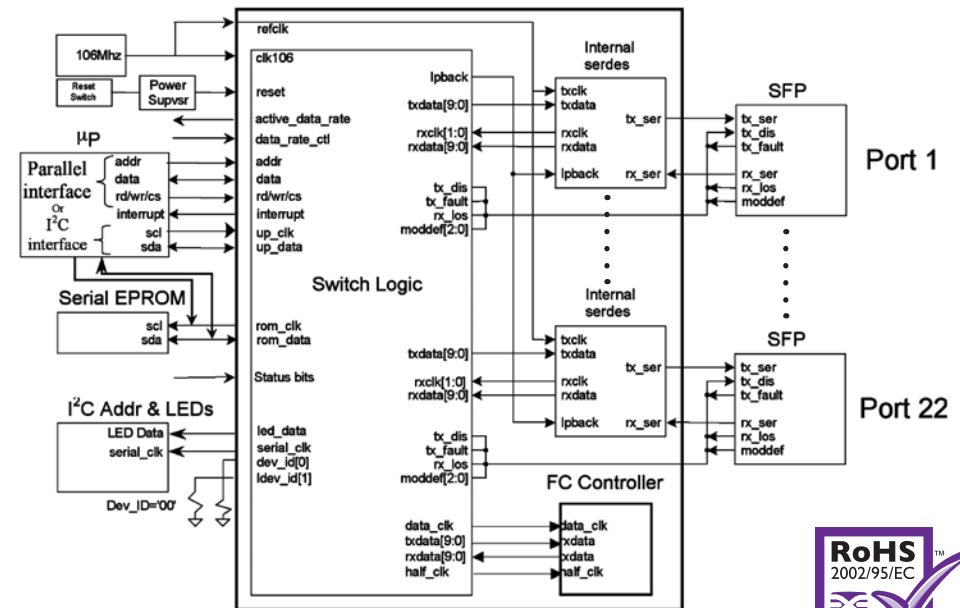
### DIAGNOSTICS

Continuous Diagnostic Operations:

power on self-test, port test before insertion, traffic & utilization monitoring, continuous link health monitoring, clock delta monitoring, pinpoint detection of drive problems, trend monitoring of device behavior, preventative action before failure, automatic bypass for rogue and unused ports

Diagnostic Troubleshooting Tools: CRC error monitoring & counting, ordered set detectors, counters on every port, ordered set capture, ordered set transmit, port snoop, internal and external loopback

<sup>1</sup> Patent pending



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