CMOS 4-Bit Microcontroller

TMP47C206M/P

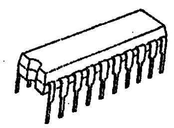
The TMP47C206 has Low Voltage Detector, Pulse output, Zero-cross detector based on the TLCS-470 series.

Part No.	ROM	RAM	Package	OTP
TMP47C206P	2048 × 8-bit	128 × 4-bit	P-DIP20-300-2.54A	TMP47P206VP
TMP47C206M			P-SOP20-300-1.27	TMP47P206VM –

Features

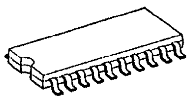
- 4-bit single chip microcomputer
- Instruction execution time: 1.0 μs (at 8 MHz)
- 90 basic instructions
  Instruction set is the same as TLCS-470 series
- Table look-up instructions
- Subroutine nesting: 15 levels max
- 5 interrupt sources (External: 2, Internal: 3)
  All sources have independent latches each,and selectable priority exists for external interrupts
- I/O port (15pins including 3 Tri-state I/O ports)
- Two 12-bit Timer/Counters
  Timer,event counter,and pulse width measurement mode
- Interval Timer
- Watchdog Timer
- Pulse output
  Buzzer drive/carrier for remote controller
- RESET Output
- Zero-cross detector interrupt (Wake-Up possible in HOLD mode)
- Low Voltage Detector
- High current outputs
  LED direct drive capability or TRIAC control:
  typ.20 mA × 5 bits (Port 4, R50)
- Hold function
  Battery/Capacitor back-up
- Real Time Emulator: BM47C206

P-DIP20-300-2.54A



TMP47C206P

P-SOP20-300-1.27



TMP47C206M

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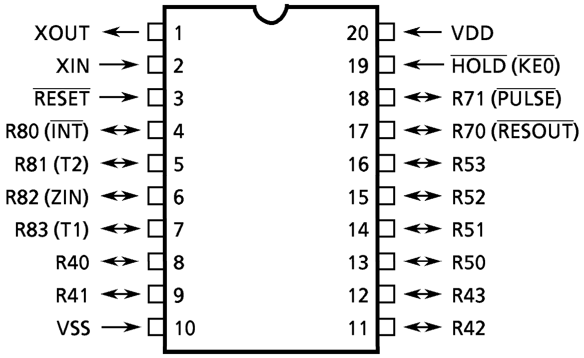
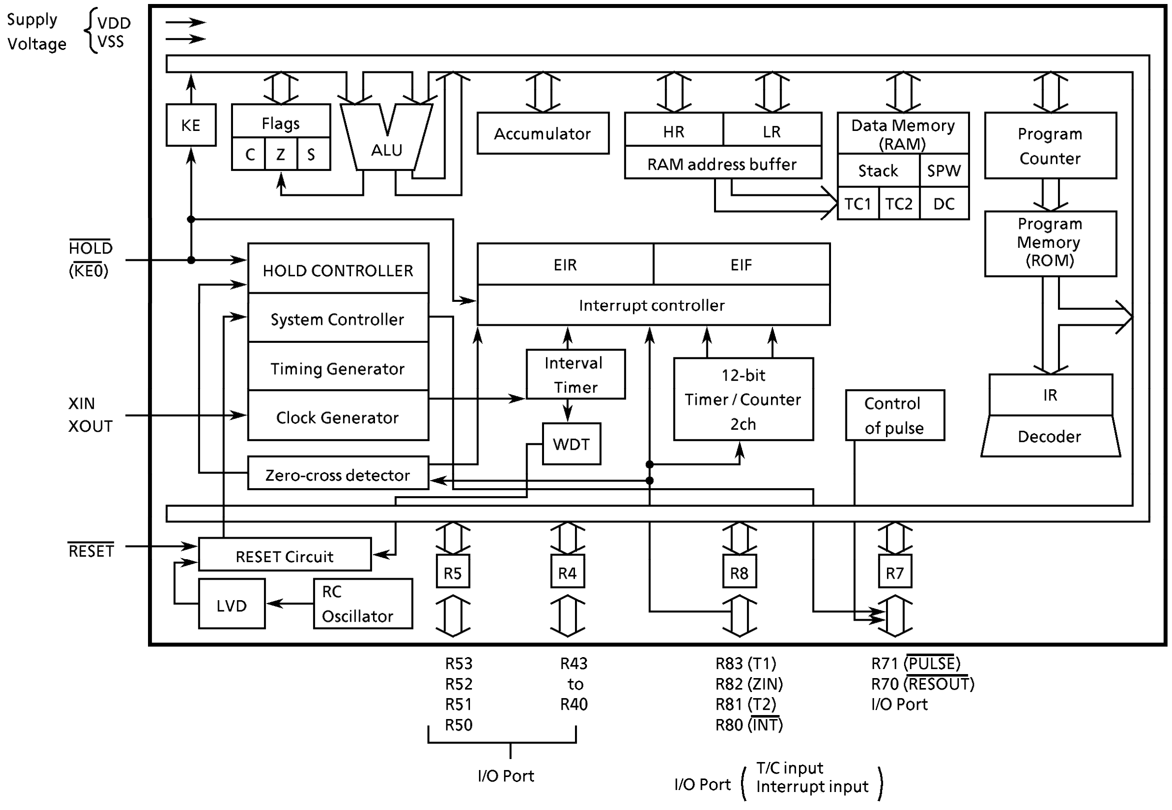
Pin Assignment

P-DIP20-300-2.54A / P-SOP20-300-1.27



Block Diagram



Pin Function

Pin Name	Input / Output	Functions	
R43 to R40	I/O (Output)	4-bit I/O port with latch (R7 port has only 2-bit). When used as input port,the latch must be set to "1". Every bit data is possible to be set,cleared and tested by the bit manipulation instruction of the L-register indirect addressing.	High Current Port
R53 to R51			Tri-State port
R50			High Current port
R71 ($\overline{\text{PULSE}}$)			Pulse output
R70 ($\overline{\text{RESOUT}}$)			Reset signal output
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer / counter external input pin, the latch must be set to "1".	Timer / Counter 1 external input
R82 (ZIN)			zero-cross interrupt input
R81 (T2)			Timer / Counter 2 external input
R80 ($\overline{\text{INT}}$)			External interrupt input
XIN	Input	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{\text{RESET}}$	Input	Reset signal input	
$\overline{\text{HOLD}}$ ($\overline{\text{KE0}}$)	Input (Input)	Hold request / release signal input	Sense input
VDD	Power Supply	+ 5 V	
VSS		0 V (GND)	

Operational Description

1. System Configuration

◆ Internal CPU Function

- 2.1 Program Counter (PC)
- 2.2 Program Memory (ROM)
- 2.3 H Register, L Register
- 2.4 Data Memory (RAM)
  - Stack
  - Stack Pointer Word (SPW)
  - Data Counter (DC)
- 2.5 ALU and Accumulator
- 2.6 Flags
- 2.7 System Controller
- 2.8 Interrupt Function
- 2.9 Reset Circuit
  - Reset Output
  - Low Voltage Detector

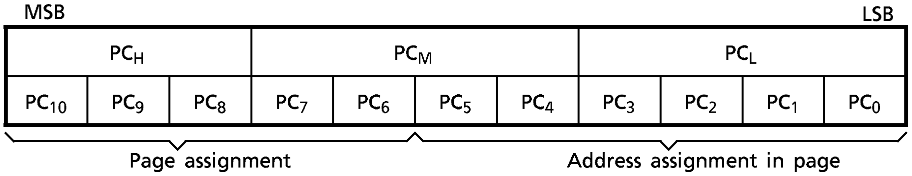
◆ Peripheral Hardware Function

- 3.1 I/O Ports
- 3.2 Interval Timer
- 3.3 Timer / Counters (TC1, TC2)
- 3.4 Watchdog Timer
- 3.5 Pulse Output
- 3.6 Zero-cross detector

2. Internal CPU Function

2.1 Program Counter (PC)

The program counter is a 11-bit binary counter which indicates the address of the program memory storing the next instruction to be executed. Normally, the PC is incremented by the number of bytes of the instruction every time it is fetched. When a branch instruction or a subroutine instruction has been executed or an interrupt has been accepted, the specified values listed in Table 2-1 are set to the PC. The PC is initialized to "0" during reset.



PC_H			PC_M				PC_L			
PC_{10}	PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0

Figure 2-1. Configuration of Program Counter

The PC can directly address a 2048-byte address space. However, with the short branch, the following points must be considered:

- Short branch instruction [BSS a]
  In [BSS a] instruction execution, when the branch condition is satisfied, the value specified in the instruction is set to the lower 6 bits of the PC. That is, [BSS a] becomes the in-page branch instruction. When [BSS a] is stored at the last address of the page, the upper 5 bits of the PC point the next page, so that branch is made to the next page.

Table 2-1. Status Change of Program Counter

Instruction or Operation		Condition		Program Counter (PC)										
				PC_{10}	PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
Execution of Instruction	BS a	SF = 1 (Branch condition is satisfied)		Immediate data specified by the instruction										
		SF = 0 (Branch condition is not satisfied)		+ 2										
	BSS a	SF = 1	Lower 6-bit address ≠ 111111	Hold					Immediate data specified by the instruction					
			Lower 6-bit address = 111111 (last address in page)	+ 1					Immediate data specified by the instruction					
		SF = 0		+ 1										
	CALL a			Immediate data specified by the instruction										
	CALLS a			0	0	0	The data generated by the immediate data specified by the instruction					1	1	0
	RET			The return address restored from stack										
	RETI			The return address restored from stack										
	Others			Incremented by the number of bytes in the instruction										
Interrupt acceptance				0	0	0	0	0	0	0	Interrupt vector			0
Reset				0	0	0	0	0	0	0	0	0	0	0

2.2 Program Memory (ROM)

Programs and fixed data are stored in the program memory. The instruction to be executed next is read from the address indicated by the contents of the PC.

The fixed data can be read by using the table look-up instructions.

- Table look-up instructions

  [LDL A, @DC], [LDH A, @DC +]

  The table look-up instructions read the lower and upper 4 bits of the fixed data stored at the address specified in the data counter (DC) to place them into the accumulator. [LDL A, @DC] instruction reads the lower 4 bits of fixed data, and [LDH A, @DC +] instruction reads the upper 4 bits.

  The DC is a 12-bit register, allowing it to address the entire program memory space.

  Example: When [LDL A, @DC] instruction is executed with the DC value being $7A0_H$ and the contents of program memory address $7A0_H$ being 58_H, "8" is stored in the accumulator; when [LDH A, @DC +] instruction is executed, "5" is stored in the accumulator and the DC value is incremented to $7A1_H$.

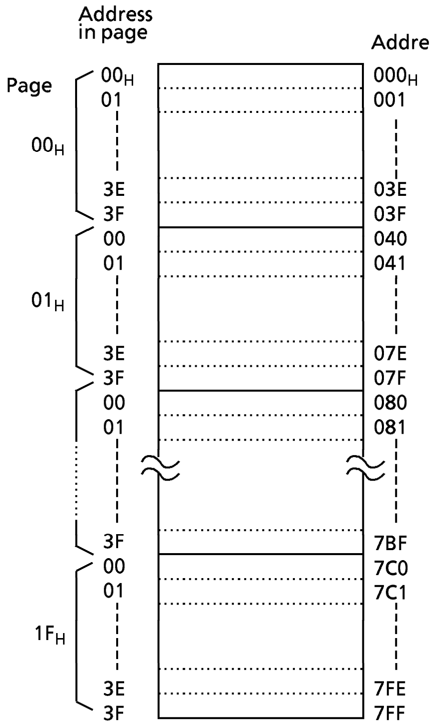


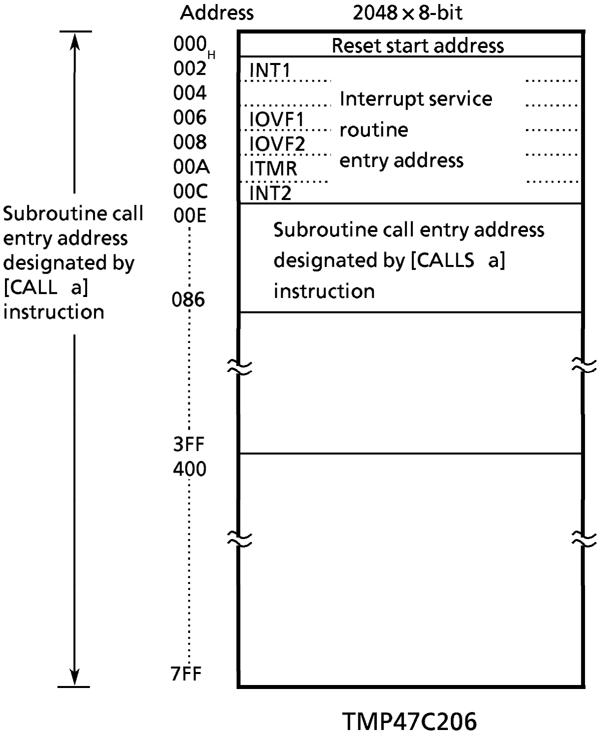
Figure 2-2. Configuration of Program Memory

2.2.1 Program Memory Capacity

The TMP47C206 has 2048 × 8 bits (addresses 000_H through $7FF_H$) of program memory (mask ROM).

2.2.2 Program Memory Map

Figure 2-3 shows the program memory map. Address 000_H to 086_H of the program memory are also used for special purposes.



Note: Address 004_H and 005_H can be used to store ordinary user's processing data.

Figure 2-3. Program Memory Map

2.3 H Register and L Register

The H register and the L register are 4-bit general registers. They are also used as a register pair (HL) for the data memory (RAM) addressing pointer. The RAM consists of pages, each page being 16 words long (1 word = 4 bits). The H register specifies a page and the L register specifies an address in the page.

The L register has the auto-post-increment/decrement capability, implementing the execution of composite instructions. For example, [ST A, @HL +] instruction automatically increments the contents of the L register after data transfer.

During the execution of [SET @L], [CLR @L], or [TEST @L] instructions, the L register is also used to specify the bits corresponding to I/O port pins R53-R40, R70, R71 (the indirect addressing of port bits by the L register).

Example: To write immediate values "5" and "F_H" to data memory addresses 10_H and 11_H.

```
LD    HL,#10H        ;  HL←10H
ST    #5,@HL+        ;  RAM [10H] ←5H,  LR←LR + 1
ST    #0FH,@HL+      ;  RAM [11H] ←FH,  LR←LR + 1
```

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	I_{OUT1}	Port R4, R50	30	V
	I_{OUT2}	Port R51 to R53, R8, R70, R71	3.2	
Output Current (Total)	$\Sigma\ I_{OUT1}$	Port R4, R50	100	mA
	$\Sigma\ I_{OUT2}$	Port R51 to 53, R8, R70, R71	28.8	
Power Dissipation [Topr = 85°C]	PD	SOP	150	mW
		DIP	250	
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins		Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		Normal mode	Crystar or ceramic	fc = 8 MHz	4.0 (2.7) (Note 2)	5.7	V
					fc = 4.2 MHz	4.0 (2.2) (Note 2)		
				RC	fc = 2.5 MHz	4.0 (2.2) (Note 2)		
			HOLD mode	–	–	4.0 (2.0) (Note 2)		
Input High Voltage	V_{IH1}	Except Hysteresis Input		In the normal operating area		V_{DD} × 0.7	V_{DD}	V
	V_{IH2}	Hysteresis Input				V_{DD} × 0.75		
	V_{IH3}			In the HOLD mode		V_{DD} × 0.9		
Input Low Voltage	V_{IL1}	Except Hysteresis Input		In the normal operating area		0	V_{DD} × 0.3	V
	V_{IL2}	Hysteresis Input					V_{DD} × 0.25	
	V_{IL3}			In the HOLD mode			V_{DD} × 0.1	
Clock Frequency	fc	XIN, XOUT		V_{DD} = 2.7 to 5.7 V		1	8	MHz
				V_{DD} = 2.2 to 5.7 V			4.2	
				V_{DD} = 2.2 to 5.7 V (RC)			2.5	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: LVD id initially enable and initial Min. V_{DD} is 4.0 V. After LVD is disabled above 4.0 V. Min. V_{DD} will be 2.7 or 2.2 to 2.0 V.

DC Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1} (Note 1)	$\overline{\text{RESET}}$, $\overline{\text{HOLD}}$	V_{DD} = 5.7 V, V_{IN} = 5.7 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain output ports					
Input Resistance	R_{IN}	$\overline{\text{RESET}}$		100	220	450	kΩ
Pull down Resistance	R_{PD}	R82		22	70	160	
Input Low Current	I_{IL}	Push-pull output ports	V_{DD} = 5.7 V, V_{IN} = 0.4 V	–	–	– 2	mA
Output Leakage Current	I_{LO}	Open drain output ports	V_{DD} = 5.7 V, V_{OUT} = 5.7 V	–	–	2	μA
Output High Voltage	V_{OH}	Push-pull output ports	V_{DD} = 4.5 V, I_{OH} = – 100 μA	4.8	–	–	V
			V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	–	–	
			V_{DD} = 2.2 V, I_{OH} = – 5 μA	2.0	–	–	
Output Low Voltage	V_{OL1}	Port R8, R7, R51 to R53	V_{DD} = 4.5 V, I_{OL} = 3.3 mA	–	–	1.0	V
			V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	
			V_{DD} = 2.2 V, I_{OL} = 20 μA	–	–	0.1	
	V_{OL2}	Port R4, R50	V_{DD} = 4.5 V, I_{OL} = 15 mA	–	–	1.0	
			V_{DD} = 4.5 V, I_{OL} = 7 mA	–	–	0.4	
			V_{DD} = 2.2 V, I_{OL} = 50 μA	–	–	0.1	
Output Low Current	I_{OL1}	Port R8, R7, R51 to R53	V_{DD} = 4.5 V, V_{OL} = 0.4 V	1.6	–	–	mA
	I_{OL2}	Port R4, R50	V_{DD} = 4.5 V, V_{OL} = 1.0 V	15	–	–	
			V_{DD} = 4.5 V, V_{OL} = 0.4 V	7	17	–	
Supply Current (in the Normal operating mode) (Note 2)	I_{DD}		V_{DD} = 5.7 V, fc = 8 MHz	–	3	6	mA
			V_{DD} = 5.7 V, fc = 4 MHz	–	2	4	
			V_{DD} = 3.0 V, fc = 4 MHz	–	1	2	
			V_{DD} = 3.0 V, fc = 1 MHz	–	0.6	1.2	
Supply Current (in the HOLD operating mode) (Note 2)	I_{DDH}	LVD always Enable	V_{DD} = 5.7 V	–	50	200	μA
		LVD On and Off	V_{DD} = 5.7 V	–	2.5	20	
Injection Current	I_{ZC}	R82		–	–	1	mA

<General Conditions>

Typ. values show those at T_{opr} = 25℃, V_{DD} = 5 V.

Note 1: Input Current I_{INT1}: The current through resistor is not included.

Note 2: Supply Current: V_{IN} = 5.5 V / 0.2 V (V_{DD} = 5.7 V) or 2.8 V / 0.2 V (V_{DD} = 3.0 V)

AC Characteristics

(V_{SS} = 0 V, Topr = –40 to 85°C)

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Instruction Cycle Time	tcy		V_{DD} = 2.7 to 5.7 V	1.0	–	8	μs
			V_{DD} = 2.2 to 5.7 V	1.9			
			RC Oscillation	3.2			
High level Clock pulse Width	t_{WCH}	For external clock operation	$V_{DD} \geqq 2.7$ V	60	–	–	ns
			$V_{DD} < 2.7$ V	120			
Low level Clock pulse Width	t_{WCL}		$V_{DD} \geqq 2.7$ V	60			
			$V_{DD} < 2.7$ V	120			
Delay Reset Output Signal	t_{rd}	fc = 1 MHz		–	–	16	μs

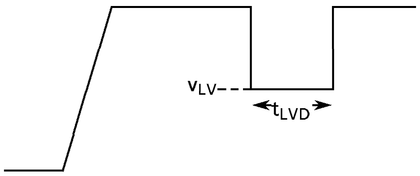
Low Voltage Detector Characteristics

(V_{SS} = 0 V, Topr = –40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
LVD internal time (Note 1)	t_{int}		8.5	–	128	ms
LVD Enable time (Note 1)	t_{en}		100	–	–	μs
LVD pulse width (Note 1, 2)	t_{LVD}		50	–	–	μs
Detection Voltage (Note 3)	V_{LV}	LVDDTY = 0 LVDD = 0	2.7	3.3	3.8	V
		LVDDTY = 1 LVDD = 0	2.2	2.7	3.3	
LVD Operating Voltage (Note 1)	V_{LVD}		2.0	–	–	V

Note 1: These parameters are characterized but not tested.

Note 2: Less than Min. t_{LVD}, CPU will not be reset.



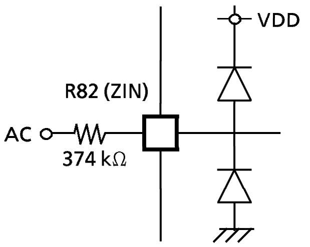
Note 3: Detection voltage has typ. 0.2 V hysteresis (Refer to Figure 2-24)

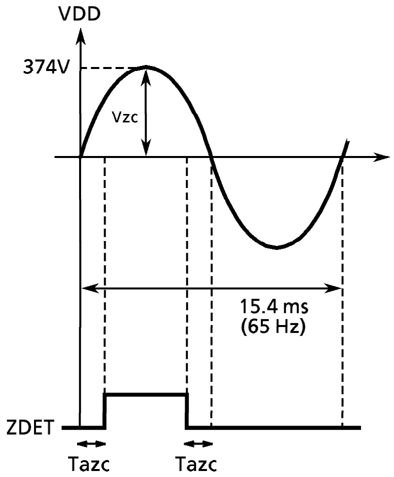
Zero-Cross Detection Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Zero-cross Accuracy	Tazc	fzc = 45 to 65 Hz	–	–	90	μs
Injection Current	Izc		–	–	1	mA
Pull-down resistance	R_{PD}		22	70	160	kΩ

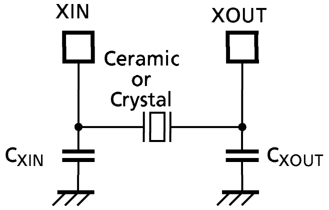
(*) Measurement conditions





Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 2.2 to 5.7 V, Topr = – 40 to 85°C)



(1) 8 MHz

Ceramic Resonator

CSA8.00MGU	(MURATA)	$C_{XIN} = C_{XOUT} = 30$ pF
KBR-8.0MS	(KYOCERA)	$C_{XIN} = C_{XOUT} = 30$ pF
EFOEC8004A4	(NATIONAL)	$C_{XIN} = C_{XOUT} = 30$ pF

(2) 6 MHz

Ceramic Resonator

CSA6.00MGU	(MURATA)	$C_{XIN} = C_{XOUT} = 30$ pF
KBR-6.0MS	(KYOCERA)	$C_{XIN} = C_{XOUT} = 30$ pF
EFOEC6004A4	(NATIONAL)	$C_{XIN} = C_{XOUT} = 30$ pF

(3) 4 MHz

Ceramic Resonator

CSA4.00MGU	(MURATA)	$C_{XIN} = C_{XOUT} = 30$ pF
KBR-4.0MS	(KYOCERA)	$C_{XIN} = C_{XOUT} = 30$ pF
EFOEC4004A4	(NATIONAL)	$C_{XIN} = C_{XOUT} = 30$ pF

Crystal Oscillator

204B-6F 4.0000	(TOYOCOM)	$C_{XIN} = C_{XOUT} = 20$ pF

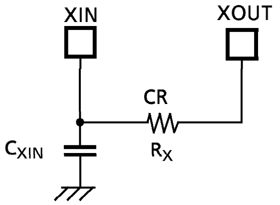
(4) 1 MHz

Ceramic Resonator

CSA1.00MGU	(MURATA)	$C_{XIN} = C_{XOUT} = 30$ pF
KBR-1.0MS	(KYOCERA)	$C_{XIN} = C_{XOUT} = 30$ pF
EFOEC1004A4	(NATIONAL)	$C_{XIN} = C_{XOUT} = 30$ pF

(5) RC Oscillation (V_{SS} = 0 V, V_{DD} = 5.0 V, Topr = 25°C)

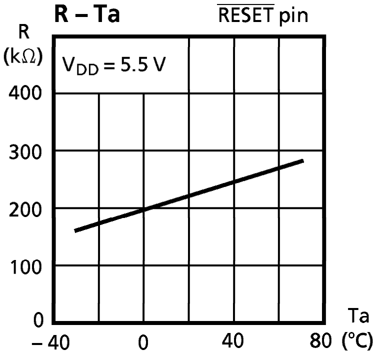
2 MHz (Typ.) C_{XIN} = 33 pF, R_X = 10 kΩ

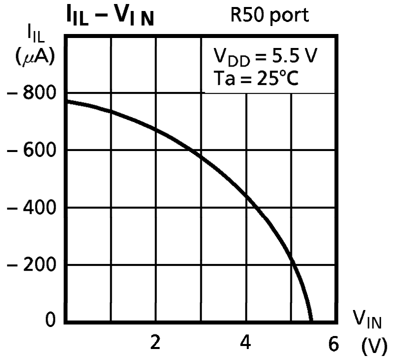


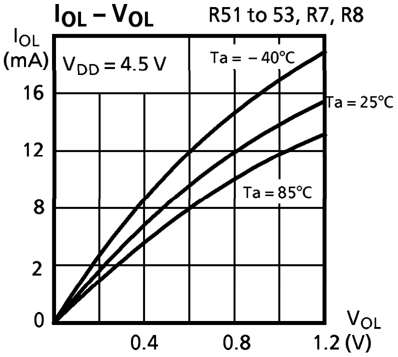
Typical Characteristics

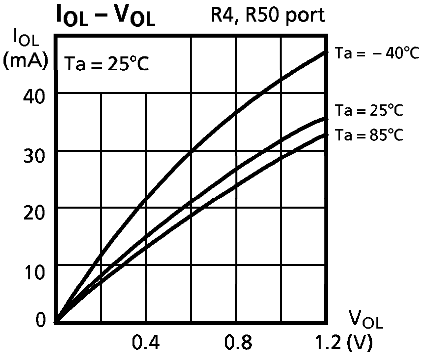
These graphs are for design guidance and not tested or guaranteed.

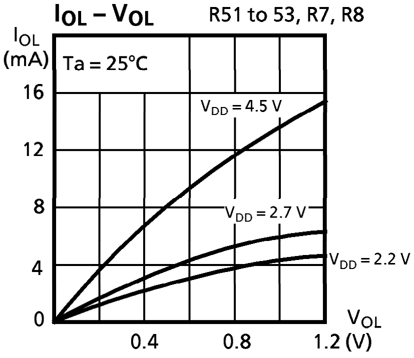
The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of distribution while “max” or “min” represents (mean + 3σ) and (mean – 3σ) respectively were σ is standard deviation.

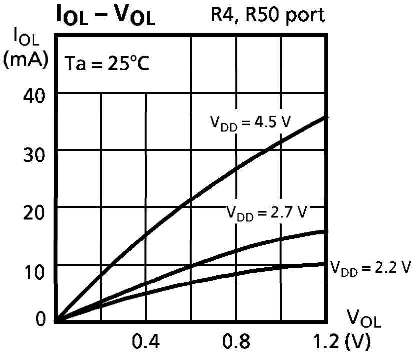




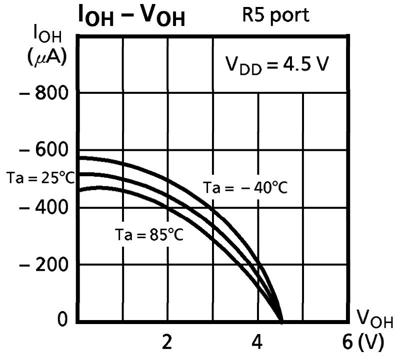




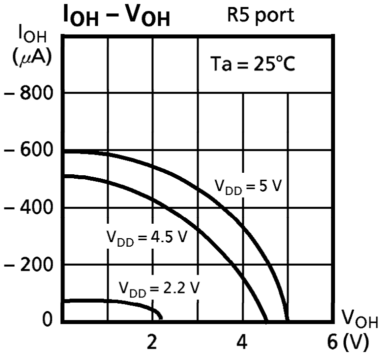




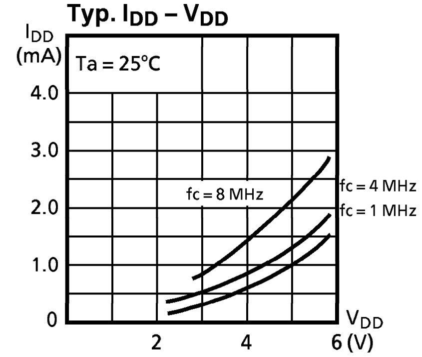
I_{OH} – V_{OH} R5 port



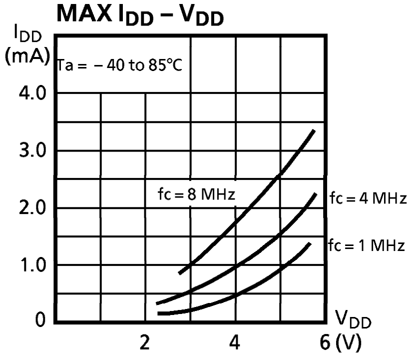
I_{OH} – V_{OH} R5 port



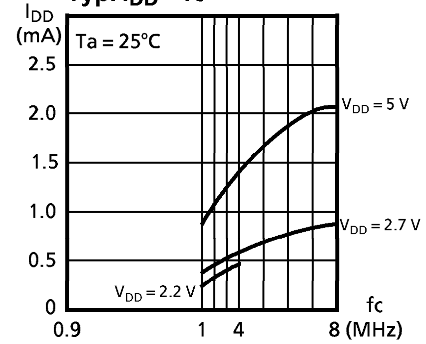
Typ. I_{DD} – V_{DD}



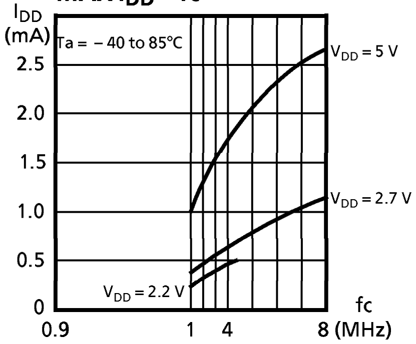
MAX I_{DD} – V_{DD}



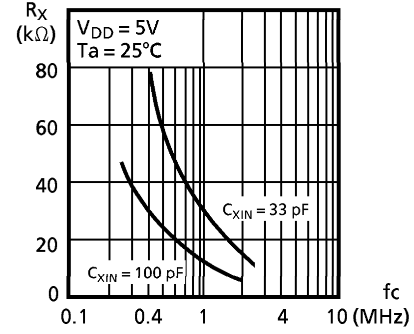
Typ. I_{DD} – fc



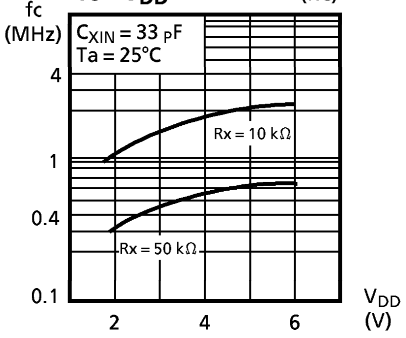
MAX I_{DD} – fc



fc – R_X (RC)



fc – V_{DD} (RC)



Operating area