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Renesas Technology Corp. Customer Support Dept. April 1, 2003



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Octal D-type Transparent Latches (with 3-state outputs)
Octal D-type Transparent Latches (with inverted 3-state outputs)



ADE-205-498 (Z) 1st. Edition Sep. 2000

#### **Description**

When the latch enable input is high, the Q outputs of HD74HC373 will follow the D inputs and the Q outputs of HD74HC533 will follow the inversion of the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

#### **Features**

• High Speed Operation:  $t_{pd}$  (D to Q) = 16 ns typ ( $C_L = 50 \text{ pF}$ )

High Output Current: Fanout of 15 LSTTL Loads

• Wide Operating Voltage:  $V_{CC} = 2 \text{ to } 6 \text{ V}$ 

• Low Input Current: 1 μA max

• Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max (Ta = 25°C)

#### **Function Table**

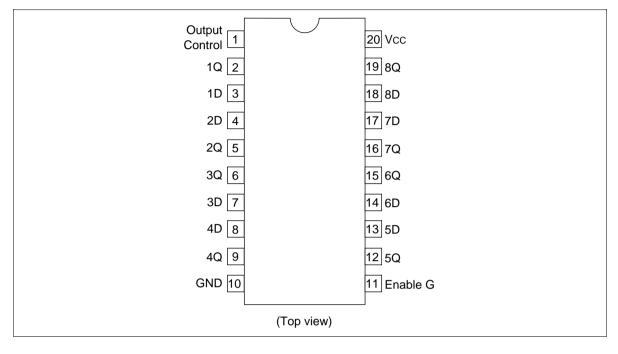
Output Control	Enable G	D	HD74HC373 Q	HD74HC533 Q
L	Н	Н	Н	L
L	Н	L	L	Н
L	L	Χ	No change	No change
Н	Х	Х	Z	Z

X: irrelevant

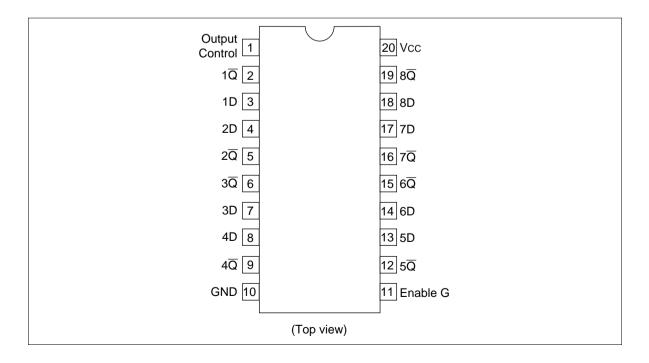
Z: Off (high-impedance) state of a 3-state output.

## **Pin Arrangement**

#### HD74HC373



#### **HD74HC533**



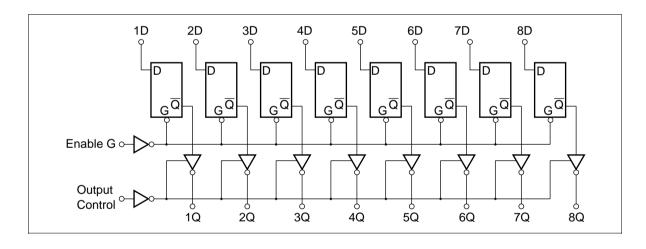
## RENESAS

## **Absolute Maximum Ratings**

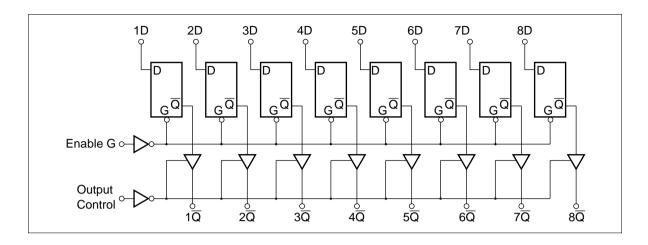
Item	Symbol	Rating	Unit	
Supply voltage range	V <sub>cc</sub>	-0.5 to +7.0	V	
Input voltage	$V_{IN}$	$-0.5$ to $V_{cc}$ + 0.5	V	
Output voltage	V <sub>OUT</sub>	$-0.5$ to $V_{cc}$ + 0.5	V	
DC current drain per pin	I <sub>OUT</sub>	±35	mA	
DC current drai per V <sub>CC</sub> GND	$I_{\rm CC},I_{\rm GND}$	±75	mA	_
DC input diode current	I <sub>IK</sub>	±20	mA	
DC output diode current	I <sub>ok</sub>	±20	mA	
Power Dissipation per package	P <sub>T</sub>	500	mW	
Storage temperature	Tstg	-65 to +150	°C	

## **Block Diagram**

## HD74HC373



## HD74HC533



## **DC** Characteristics

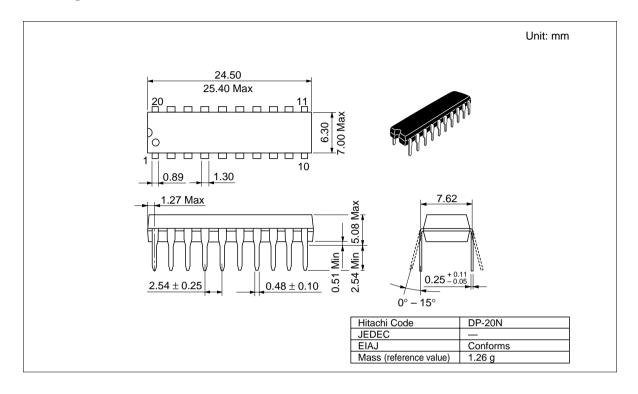
			Ta = 25°C		Ta = -40 to +85°C					
Item	Symbol	$V_{cc}$ (V)	Min	Тур	Max	Min	Max	Unit	Test Condition	ns
Input voltage	V <sub>IH</sub>	2.0	1.5	_	_	1.5	_	V		
		4.5	3.15	_	_	3.15	_			
		6.0	4.2	_	_	4.2	_			
	V <sub>IL</sub>	2.0	_	_	0.5	_	0.5	V		
		4.5	_	_	1.35	_	1.35			
		6.0	_	_	1.8	_	1.8	_		
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0	_	1.9	_	V	$Vin = V_{IH} \text{ or } V_{IL}$	I <sub>OH</sub> = -20 μA
		4.5	4.4	4.5	_	4.4	_			
		6.0	5.9	6.0	_	5.9	_	_		
		4.5	4.18	_	_	4.13	_	_		$I_{OH} = -6 \text{ mA}$
		6.0	5.68	_	_	5.63	_	_		$I_{OH} = -7.8 \text{ mA}$
	V <sub>OL</sub>	2.0	_	0.0	0.1	_	0.1	V	$Vin = V_{IH} \text{ or } V_{IL}$	I <sub>OL</sub> = 20 μA
		4.5	_	0.0	0.1	_	0.1	_		
		6.0	_	0.0	0.1	_	0.1	_		
		4.5	_	_	0.26	_	0.33	_		I <sub>OL</sub> = 6 mA
		6.0	_	_	0.26	_	0.33	_		$I_{OL} = 7.8 \text{ mA}$
Off-state output current	I <sub>oz</sub>	6.0	_	_	±0.5	_	±5.0	μΑ	$Vin = V_{IH} \text{ or } V_{IL},$ $Vout = V_{CC} \text{ or } C$	
Input current	lin	6.0	_	_	±0.1	_	±1.0	μΑ	Vin = V <sub>CC</sub> or GN	ND
Quiescent supply current	I <sub>cc</sub>	6.0	_	_	4.0	_	40	μΑ	Vin = V <sub>cc</sub> or GN	ND, lout = 0 μA

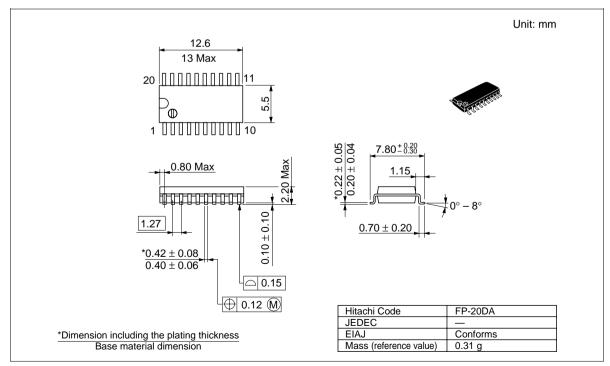
**AC Characteristics** ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

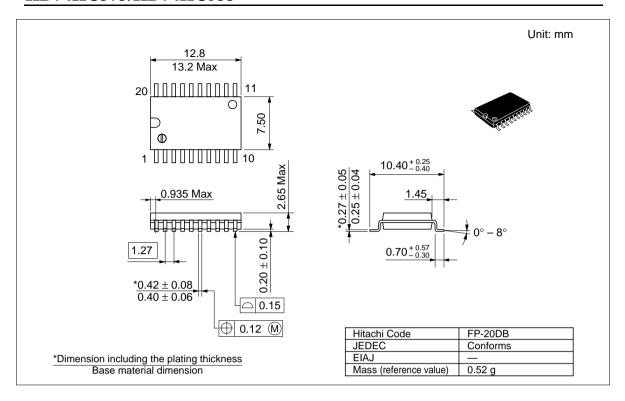
Ta = -40 to  $Ta = 25^{\circ}C$  +85°C

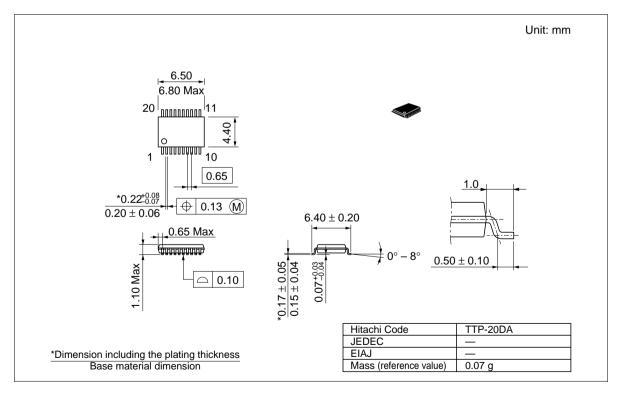
Item	Symbol	V <sub>cc</sub> (V)	Min	Тур	Max	Min	Max	- Unit	Test Conditions
Propagation delay	t <sub>PLH</sub>	2.0	_	_	150	_	190	ns	G to Q
time	t <sub>PHL</sub>	4.5	_	18	30	_	38	_	
		6.0	_	_	26	_	33	_	
	t <sub>PLH</sub>	2.0	_	_	125	_	155	ns	D to Q
	$t_{\tiny PHL}$	4.5	_	16	25	_	31	_	
		6.0	_	_	21	_	26	-	
Output enable	t <sub>zL</sub>	2.0	_	_	150	_	190	ns	
time		4.5	_	12	30	_	38	=	
		6.0	_	_	26	_	33	=	
	t <sub>zH</sub>	2.0	_	_	150	_	190	ns	
		4.5	_	15	30	_	38	=	
		6.0	_	_	26	_	33	-	
Output disable	t <sub>LZ</sub>	2.0	_	_	150	_	190	ns	
time		4.5	_	13	30	_	38	-	
		6.0	_	_	26	_	33	_	
	t <sub>HZ</sub>	2.0	_	_	150	_	190	ns	
		4.5	_	16	30	_	38	=	
		6.0	_	_	26	_	33	=	
Setup time	t <sub>su</sub>	2.0	100	_	_	125	_	ns	
		4.5	20	1	_	25	_	=	
		6.0	17	_	_	21	_	-	
Hold time	t <sub>h</sub>	2.0	50	_	_	65	_	ns	
		4.5	10	1	_	13	_	-	
		6.0	9	_	_	11	_	-	
Pulse width	t <sub>w</sub>	2.0	80	_	_	100	_	ns	
		4.5	16	6	_	20		=	
		6.0	14	_	_	17		_	
Output rise/fall	t <sub>TLH</sub>	2.0	_	_	60	_	75	ns	
time	$t_{\text{THL}}$	4.5	_	4	12	_	15	_	
		6.0	_	_	10	_	13	_	
Input capacitance	Cin	_	_	5	10	_	10	pF	

## **Package Dimensions**









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