

74LVC1G57-Q100

Low-power configurable multiple function gate

Rev. 1 — 15 April 2014

Product data sheet

1. General description

The 74LVC1G57-Q100 provides configurable multiple functions. Eight patterns of 3-bit input, determine the output state. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter and buffer. All inputs can be connected to V_{CC} or GND.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

All inputs (A, B and C) are Schmitt trigger inputs that can transform slowly changing input signals into sharply defined, jitter-free output signals.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8B/JESD36 (2.7 V to 3.6 V).
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- $\pm 24\text{ mA}$ output drive ($V_{CC} = 3.0\text{ V}$)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options



3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G57GW-Q100	−40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
74LVC1G57GV-Q100	−40 °C to +125 °C	SC-74	plastic surface-mounted package; 6 leads	SOT457

4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1G57GW-Q100	YC
74LVC1G57GV-Q100	V57

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

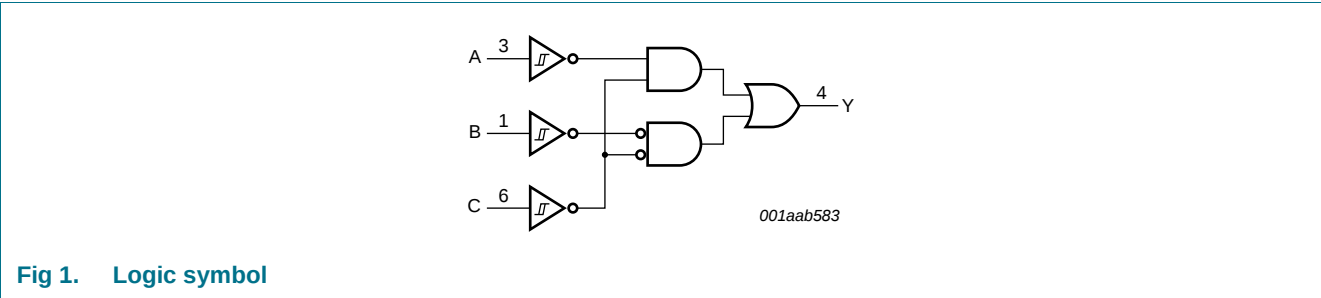


Fig 1. Logic symbol

6. Pinning information

6.1 Pinning

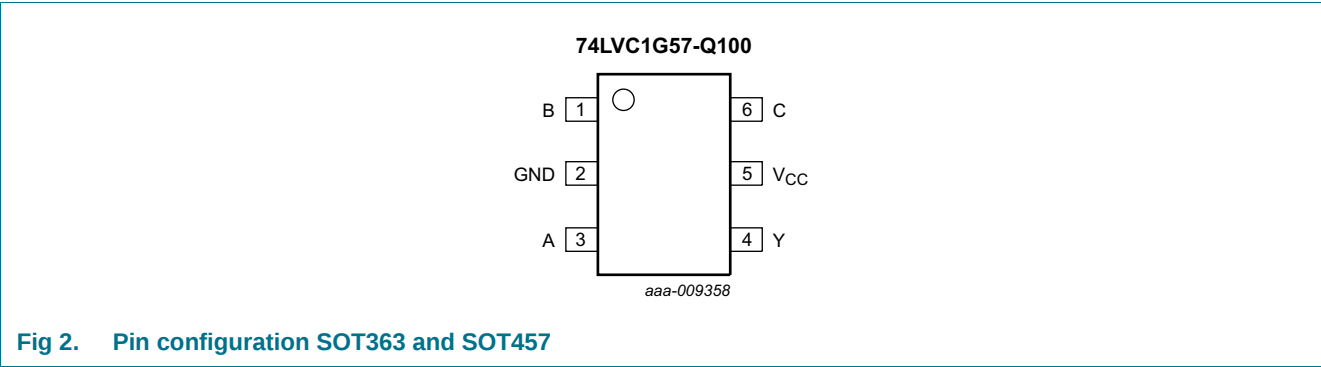


Fig 2. Pin configuration SOT363 and SOT457

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
GND	2	ground (0 V)
A	3	data input
Y	4	data output
V _{CC}	5	supply voltage
C	6	data input

7. Functional description

Table 4. Function table^[1]

Input			Output
C	B	A	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

[1] H = HIGH voltage level; L = LOW voltage level.

7.1 Logic configurations

Table 5. Function selection table

Logic function	Figure
2-input AND	see Figure 3
2-input AND with both inputs inverted	see Figure 6
2-input NAND with inverted input	see Figure 4 and Figure 5
2-input OR with inverted input	see Figure 4 and Figure 5
2-input NOR	see Figure 6
2-input NOR with both inputs inverted	see Figure 3
2-input XNOR	see Figure 7
Inverter	see Figure 8
Buffer	see Figure 9

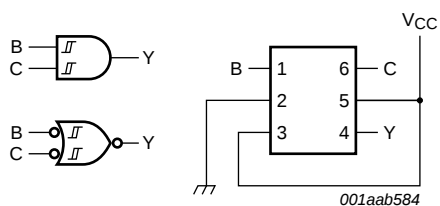


Fig 3. 2-input AND gate or 2-input NOR gate with both inputs inverted

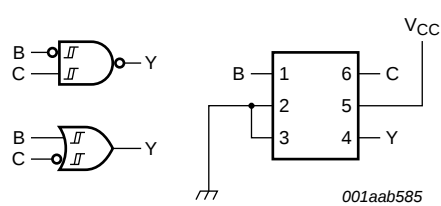


Fig 4. 2-input NAND gate with input B inverted or 2-input OR gate with inverted C input

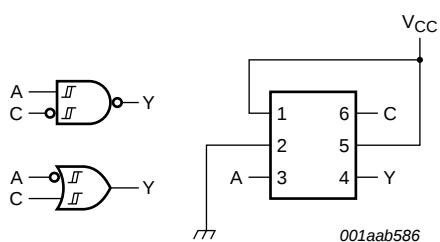


Fig 5. 2-input NAND gate with input C inverted or 2-input OR gate with inverted A input

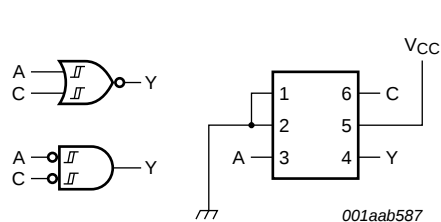


Fig 6. 2-input NOR gate or 2-input AND gate with both inputs inverted

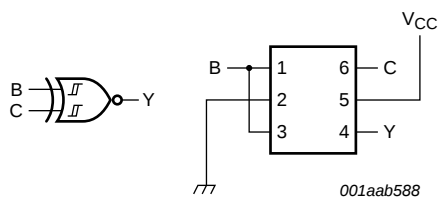


Fig 7. 2-input XNOR gate

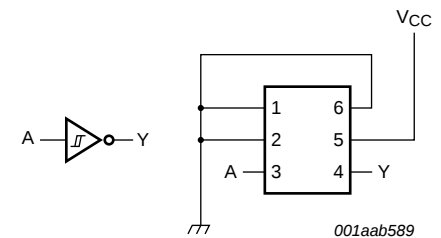


Fig 8. Inverter

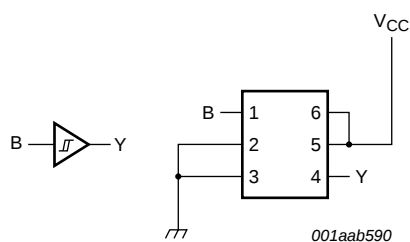


Fig 9. Buffer

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	Active mode [1][2]	-0.5	+6.5	V
		Power-down mode [1][2]	-0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [3]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For SC-88 and SC-74 packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		$V_{CC} = 0$ V; Power-down mode	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T–}						
		I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.7	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.3	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.55	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T–}						
		I _O = –100 µA; V _{CC} = 1.65 V to 5.5 V	V _{CC} – 0.1	-	-	V _{CC} – 0.1	-	V
		I _O = –4 mA; V _{CC} = 1.65 V	1.2	-	-	0.95	-	V
		I _O = –8 mA; V _{CC} = 2.3 V	1.9	-	-	1.7	-	V
		I _O = –12 mA; V _{CC} = 2.7 V	2.2	-	-	1.9	-	V
		I _O = –24 mA; V _{CC} = 3.0 V	2.3	-	-	2.0	-	V
		I _O = –32 mA; V _{CC} = 4.5 V	3.8	-	-	3.4	-	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±5	-	±100	µA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	±0.1	±10	-	±200	µA
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	0.1	10	-	200	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} – 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	5	500	-	5000	µA
C _I	input capacitance		-	2.5	-	-	-	pF

[1] Typical values are measured at maximum V_{CC} and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 11](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	A, B, C to Y; see Figure 10 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	6.0	14.4	1.0	18	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	3.5	8.3	0.5	10.4	ns
		V _{CC} = 2.7 V	0.5	4.2	8.5	0.5	10.6	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	3.8	6.3	0.5	7.9	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	3.0	5.1	0.5	6.4	ns
C _{PD}	power dissipation capacitance	V _{CC} = 3.3 V; V _I = GND to V _{CC} ^[3]	-	22	-	-	-	pF

[1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

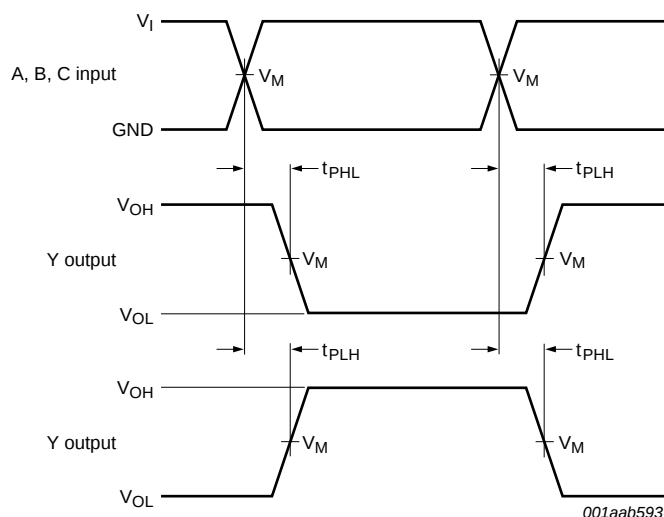
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of outputs.

12. Waveforms



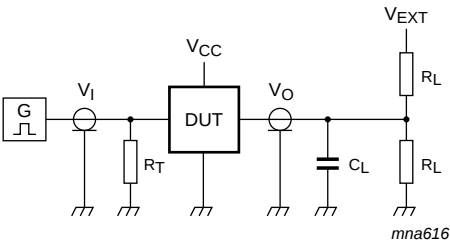
Measurement points are given in [Table 10](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. Input A, B and C to output Y propagation delay times

Table 10. Measurement points

Supply voltage	Input		Output
V _{CC}	V _M	V _I	V _M
1.65 V to 1.95 V	0.5V _{CC}	V _{CC}	0.5V _{CC}
2.3 V to 2.7 V	0.5V _{CC}	V _{CC}	0.5V _{CC}
2.7 V	1.5 V	2.7 V	1.5 V
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V
4.5 V to 5.5 V	0.5V _{CC}	V _{CC}	0.5V _{CC}



Measurement points are given in [Table 11](#).
Definitions test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

Fig 11. Test circuit for measuring switching times

Table 11. Measurement points

Supply voltage	Input		Load		V _{EXT}
V _{CC}	V _I	t _r = t _f	C _L	R _L	t _{PLH} , t _{PHL}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open

13. Transfer characteristics

Table 12. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V_{T+}	positive-going threshold voltage	see Figure 12 , Figure 13 , Figure 14 and Figure 15						
		$V_{CC} = 1.8 \text{ V}$	0.70	1.02	1.20	0.67	1.20	V
		$V_{CC} = 2.3 \text{ V}$	1.11	1.42	1.60	1.08	1.60	V
		$V_{CC} = 3.0 \text{ V}$	1.50	1.79	2.00	1.47	2.00	V
		$V_{CC} = 4.5 \text{ V}$	2.16	2.52	2.74	2.13	2.74	V
		$V_{CC} = 5.5 \text{ V}$	2.61	2.99	3.33	2.58	3.33	V
V_{T-}	negative-going threshold voltage	see Figure 12 , Figure 13 , Figure 14 and Figure 15						
		$V_{CC} = 1.8 \text{ V}$	0.30	0.53	0.72	0.30	0.75	V
		$V_{CC} = 2.3 \text{ V}$	0.58	0.77	1.00	0.58	1.03	V
		$V_{CC} = 3.0 \text{ V}$	0.80	1.04	1.30	0.80	1.33	V
		$V_{CC} = 4.5 \text{ V}$	1.21	1.55	1.90	1.21	1.93	V
		$V_{CC} = 5.5 \text{ V}$	1.45	1.86	2.29	1.45	2.32	V
V_H	hysteresis voltage	$(V_{T+} - V_{T-})$; see Figure 12 , Figure 13 , Figure 14 and Figure 15						
		$V_{CC} = 1.8 \text{ V}$	0.30	0.48	0.62	0.23	0.62	V
		$V_{CC} = 2.3 \text{ V}$	0.40	0.64	0.80	0.34	0.80	V
		$V_{CC} = 3.0 \text{ V}$	0.50	0.75	1.00	0.44	1.00	V
		$V_{CC} = 4.5 \text{ V}$	0.71	0.97	1.20	0.65	1.20	V
		$V_{CC} = 5.5 \text{ V}$	0.71	1.13	1.40	0.65	1.40	V

[1] Typical values are measured at $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

14. Waveforms transfer characteristics

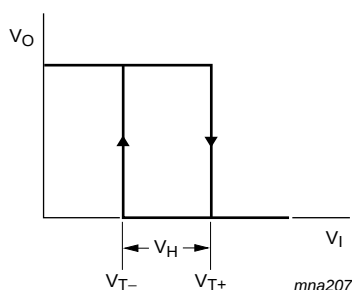
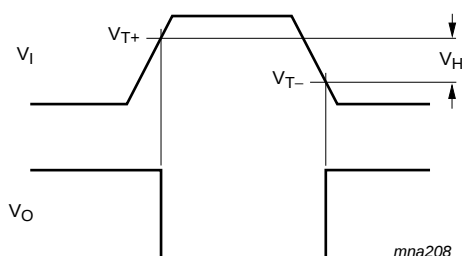


Fig 12. Transfer characteristic



V_{T+} and V_{T-} limits are at 70 % and 20 %.

Fig 13. Definition of V_{T+} , V_{T-} and V_H

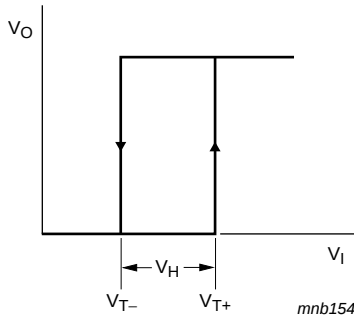
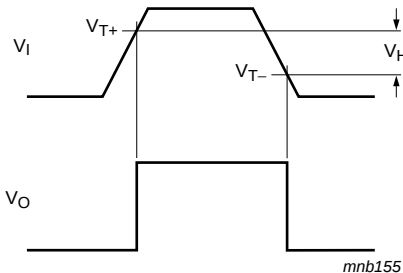


Fig 14. Transfer characteristic



V_{T+} and V_{T-} limits are at 70 % and 20 %.

Fig 15. Definition of V_{T+} , V_{T-} and V_H

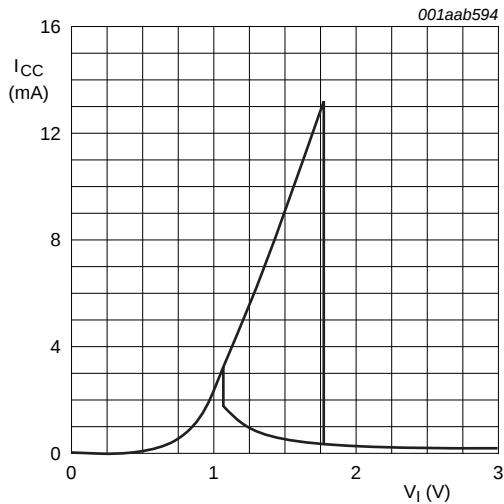


Fig 16. Typical 74LVC1G57-Q100 transfer characteristic; $V_{CC} = 3.0$ V

15. Package outline

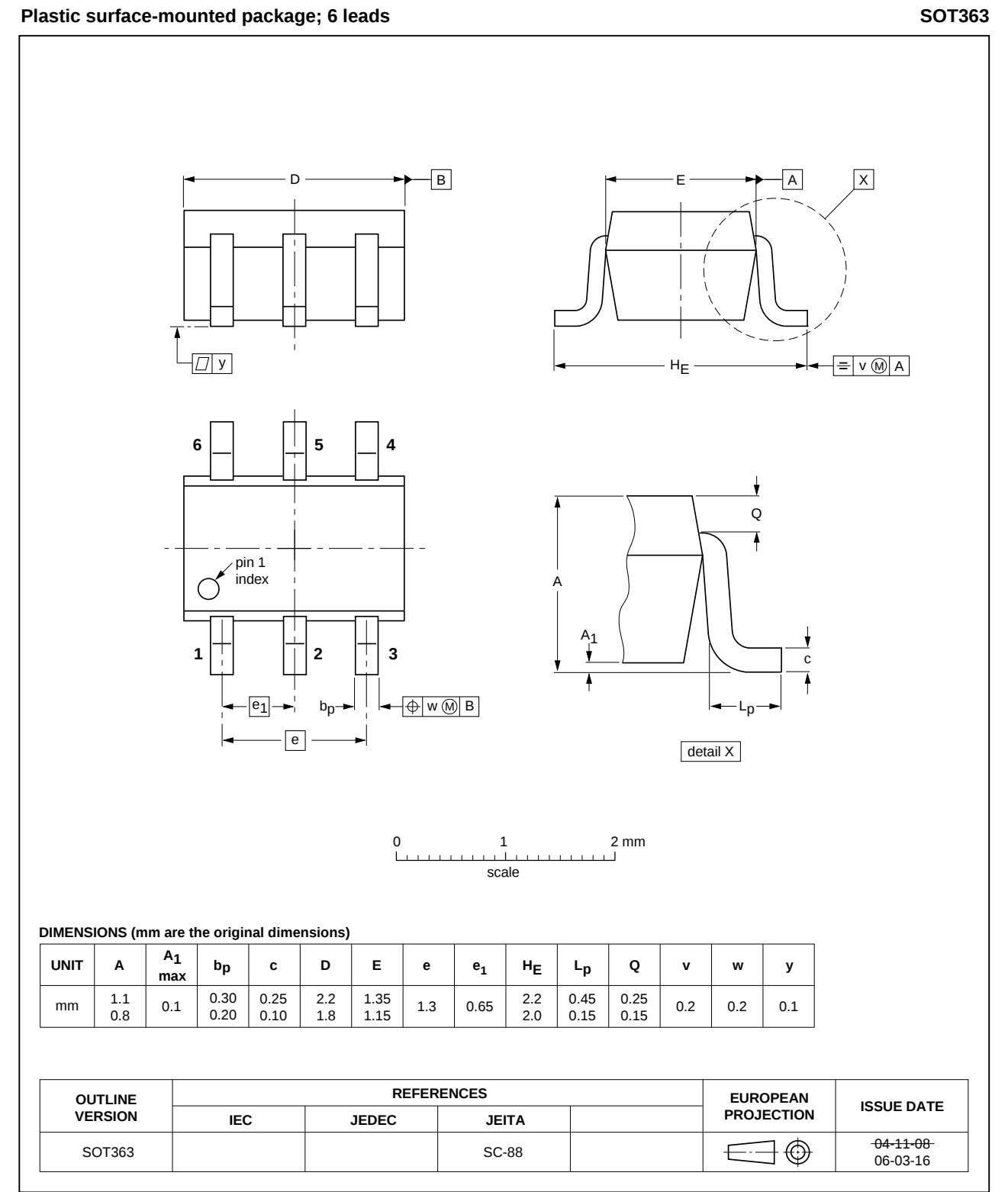


Fig 17. Package outline SOT363 (SC-88)

Plastic surface-mounted package (TSOP6); 6 leads

SOT457

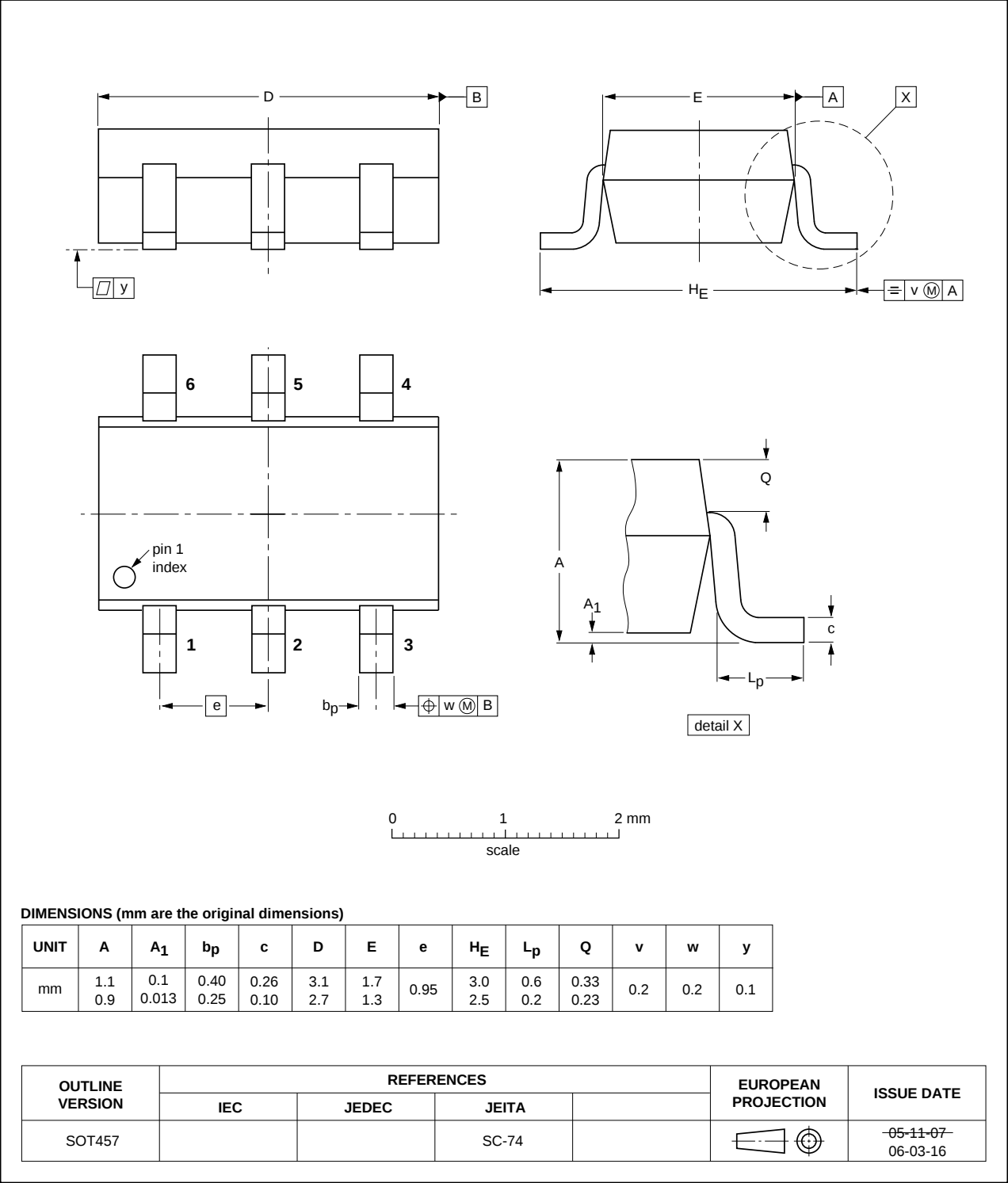


Fig 18. Package outline SOT457 (SC-74)

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
TTL	Transistor-Transistor Logic
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
DUT	Device Under Test

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G57_Q100 v.1	20140415	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

19. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

20. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Marking	2
5	Functional diagram	2
6	Pinning information	2
6.1	Pinning	2
6.2	Pin description	3
7	Functional description	3
7.1	Logic configurations	3
8	Limiting values	5
9	Recommended operating conditions	5
10	Static characteristics	6
11	Dynamic characteristics	7
12	Waveforms	7
13	Transfer characteristics	9
14	Waveforms transfer characteristics	9
15	Package outline	11
16	Abbreviations	13
17	Revision history	13
18	Legal information	14
18.1	Data sheet status	14
18.2	Definitions	14
18.3	Disclaimers	14
18.4	Trademarks	15
19	Contact information	15
20	Contents	16

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2014.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 15 April 2014

Document identifier: 74LVC1G57-Q100