19-4812; Rev 0; 7/09

MAXIM

SATA I/II Bidirectional Redriver with High ESD and Cable Detect

General Description

The MAX4951AE dual-channel buffer is designed to redrive serial-ATA (SATA) I and SATA II signals and can survive ESD events up to ±8kV Human Body Model (HBM). The MAX4951AE can be placed near an eSATA connector to overcome board losses and produce an eSATA-compliant signal level. This device is Serial ATA Revision 2.6 (gold standard)-compliant, while overcoming losses in the PCB and eSATA connector.

The MAX4951AE features low standby current for power-sensitive applications. This device features hardware SATA-drive cable detection, keeping the power low in standby mode.

The MAX4951AE preserves signal integrity at the receiver by reestablishing full output levels. It reduces the total system jitter (T_J) by squaring up the signal and providing excellent return loss match to the source. This device features channel-independent digital boost controls to drive SATA outputs over normal trace lengths and eSATA connector. SATA Out-Of-Band (OOB) signaling is supported using high-speed amplitude detection on the inputs, and squelch on the corresponding outputs. Inputs and outputs are all internally 50Ω terminated.

The MAX4951AE operates from a single +3.3V (typ) supply and is available in a small, 4mm x 4mm, TQFN package with flow-through traces for ease of layout. This device is specified over the 0°C to +70°C operating temperature range.

Applications

Laptop Computers

Docking Stations

Desktop Computers

Servers

Data Storage/Work Stations

Features

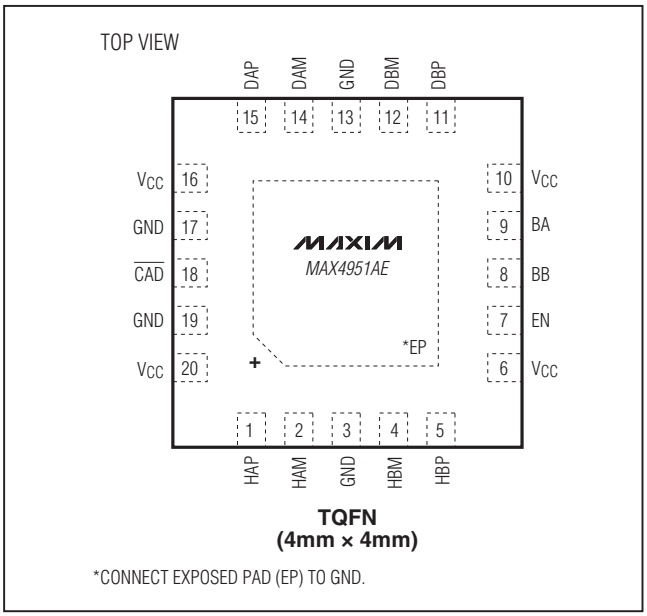
- **Single +3.3V (typ) Supply Operation**
- **Low-Power, 350µA (typ) eSATA Cable Detect**
- **Supports SATA 1.5Gbps and 3.0Gbps Data Rates**
- **Meets SATA I, SATA II Input/Output-Return Loss Mask**
- **Exceeds eSATA Standard Compliant Eye Mask for Jitter**
- **Meets or Exceeds eSATA Standard Compliant Eye Mask for Output Levels**
- **Supports SATA OOB Signaling**
- **Internal Input/Output 50Ω Termination Resistors**
- **Inline Signal Traces for Flow-Through Layout**
- **Pin Compatible with MAX4951**
- **Space-Saving, 4mm x 4mm, TQFN Package**
- **ESD Protection on All Pins: ±8kV (HBM)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4951AECTP+	0°C to +70°C	20 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



TQFN
(4mm × 4mm)

*CONNECT EXPOSED PAD (EP) TO GND.

SATA I/II Bidirectional Redriver with High ESD and Cable Detect

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND.)
V_{CC} ..... -0.3V to +4.0V
HAP, HAM, DBP, DBM, EN, $\overline{CAD}$, BA, BB (Note 1) ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Output Current (HBP, HBM, DAP, DAM) ..... ±30mA
Continuous Current at Inputs (HAP, HAM, DBP, DBM) ..... ±5mA
Continuous Current (EN, $\overline{CAD}$, BA, BB) ..... ±5mA

Continuous Power Dissipation (T_A = +70°C)
20-Pin TQFN (derate 25.6mW/°C above +70°C) 2051mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 2)
20-Pin TQFN ..... 6°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 2)
20-Pin TQFN ..... 39°C/W
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: All I/O pins are clamped by internal diodes.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C_L = 10nF, R_L = 50Ω, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Power-Supply Range	V_{CC}		3.0		3.6	V
Operating Supply Current	I_{CC}	BA = BB = V_{CC}		75	100	mA
		BA = BB = GND		70	90	
Power-Down Supply Current	I_{PWDN}	EN = GND or $\overline{CAD}$ = V_{CC}		0.35	2	mA
Differential Input Resistance	$Z_{RX-DIFF-DC}$		85	100	115	Ω
Differential Output Resistance	$Z_{TX-DIFF-DC}$		85	100	115	Ω
AC PERFORMANCE						
Differential Input Return Loss (Note 4)	$RL_{RX-DIFF}$	f = 150MHz to 300MHz			-18	dB
		f = 300MHz to 600MHz			-14	
		f = 600MHz to 1200MHz			-10	
		f = 1.2GHz to 2.4GHz			-8	
		f = 2.4GHz to 3.0GHz			-3	
Common-Mode Input Return Loss (Note 4)	RL_{RX-CM}	f = 150MHz to 300MHz			-5	dB
		f = 300MHz to 600MHz			-5	
		f = 600MHz to 1200MHz			-2	
		f = 1.2GHz to 2.4GHz			-2	
		f = 2.4GHz to 3.0GHz			-2	
Differential Output Return Loss (Note 4)	$RL_{TX-DIFF}$	f = 150MHz to 300MHz			-14	dB
		f = 300MHz to 600MHz			-8	
		f = 600MHz to 1200MHz			-6	
		f = 1.2GHz to 2.4GHz			-6	
		f = 2.4GHz to 3.0GHz			-3	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_L = 10nF, R_L = 50Ω, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Return Loss (Note 4)	RL_{TX-CM}	f = 150MHz to 300MHz				-8	dB
		f = 300MHz to 600MHz				-5	
		f = 600MHz to 1200MHz				-2	
		f = 1.2GHz to 2.4GHz				-2	
		f = 2.4GHz to 3.0GHz				-2	
Differential Input Signal Range	$V_{RX-DFF-PP}$	SATA 1.5Gbps/3.0Gbps		220		1600	mV_{P-P}
Differential Output Swing	$V_{TX-DFF-PP}$	f = 750MHz	BA = BB = GND	425	525	625	mV_{P-P}
			BA = BB = V_{CC}	525	625	725	
		f = 1.5GHz	BA = BB = GND	400	500	600	
			BA = BB = V_{CC}	500	600	700	
Propagation Delay	t_{PD}				240		ps
Output Rise/Fall Time	$t_{R/F}$	Figure 1, (Notes 4, 5)		67		136	ps
Deterministic Jitter	$T_{TX-DJ-DD}$	Up to 3.0Gbps (Notes 4, 6)				15	ps_{P-P}
Random Jitter	$T_{TX-RJ-DD}$	Up to 3.0Gbps (Notes 4, 6)				1.8	ps_{RMS}
OOB Detector Threshold	V_{TH-OOB}	SATA OOB pattern		50		200	mV_{P-P}
OOB Output Startup/Shutdown Time	t_{OOB}	(Note 7)			3	5	ns
CONTROL LOGIC (BA, BB, EN, $\overline{CAD}$)							
Input Logic High	V_{IH}			1.4			V
Input Logic Low	V_{IL}					0.6	V
Input Logic Hysteresis	V_{HYST}				0.1		V
Pullup/Pulldown Input Resistor	$R_{UP/DOWN}$				330		kΩ
ESD PROTECTION							
All Pins		Human Body Model			±8		kV

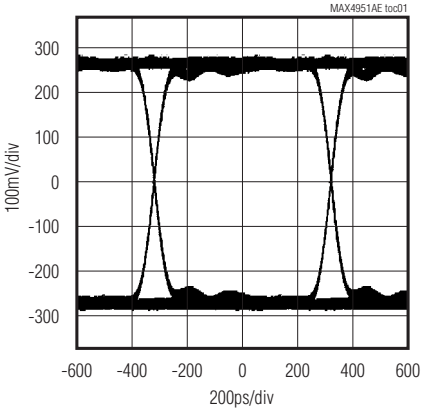
Note 3: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 4: Guaranteed by design.
Note 5: Rise and fall times are measured using 20% and 80% levels.
Note 6: DJ measured using K28.5 pattern; RJ measured using D10.2 pattern
Note 7: Total time for OOB detection circuit to enable/squelch the output.

SATA I/II Bidirectional Redriver with High ESD and Cable Detect

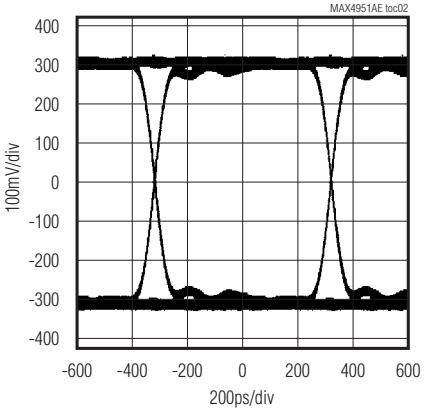
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, all eye diagrams measured using K28.5 pattern.)

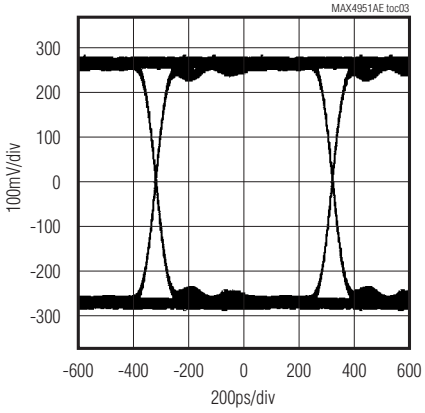
V_{IN} = 220mV$_{P-P}$, 1.5Gbps, B_ = 0



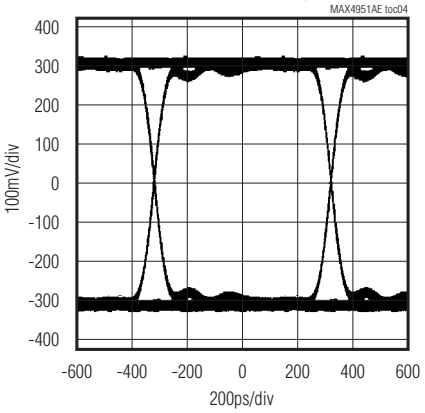
V_{IN} = 220mV$_{P-P}$, 1.5Gbps, B_ = 1



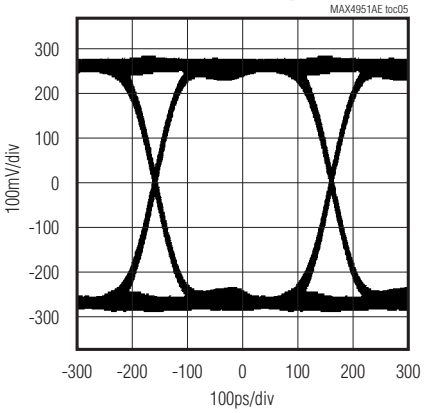
V_{IN} = 1600mV$_{P-P}$, 1.5Gbps, B_ = 0



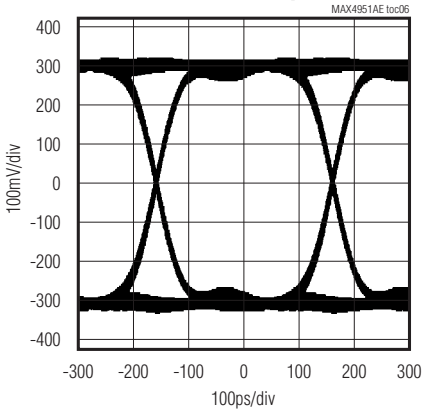
V_{IN} = 1600mV$_{P-P}$, 1.5Gbps, B_ = 1



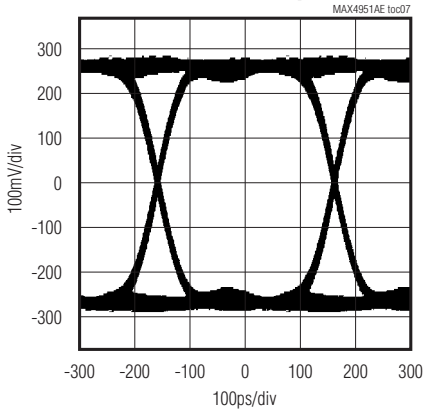
V_{IN} = 220mV$_{P-P}$, 3Gbps, B_ = 0



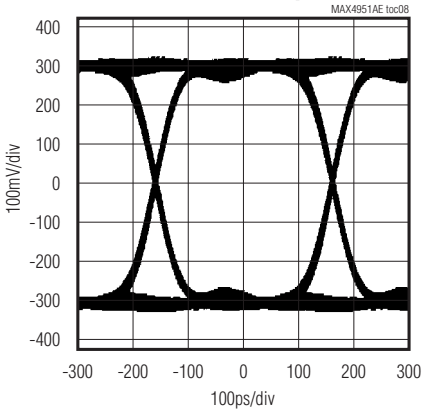
V_{IN} = 220mV$_{P-P}$, 3Gbps, B_ = 1



V_{IN} = 1600mV$_{P-P}$, 3Gbps, B_ = 0

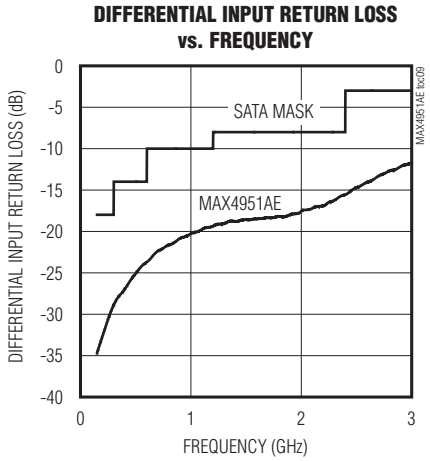


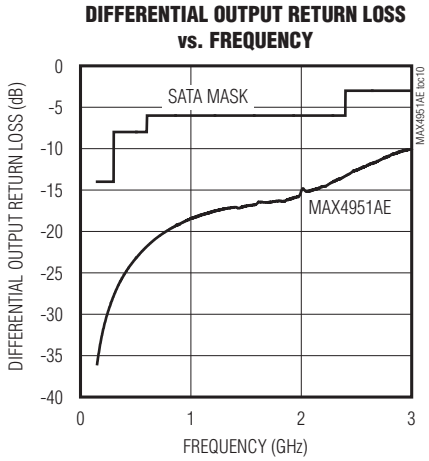
V_{IN} = 1600mV$_{P-P}$, 3Gbps, B_ = 1



Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, all eye diagrams measured using K28.5 pattern.)





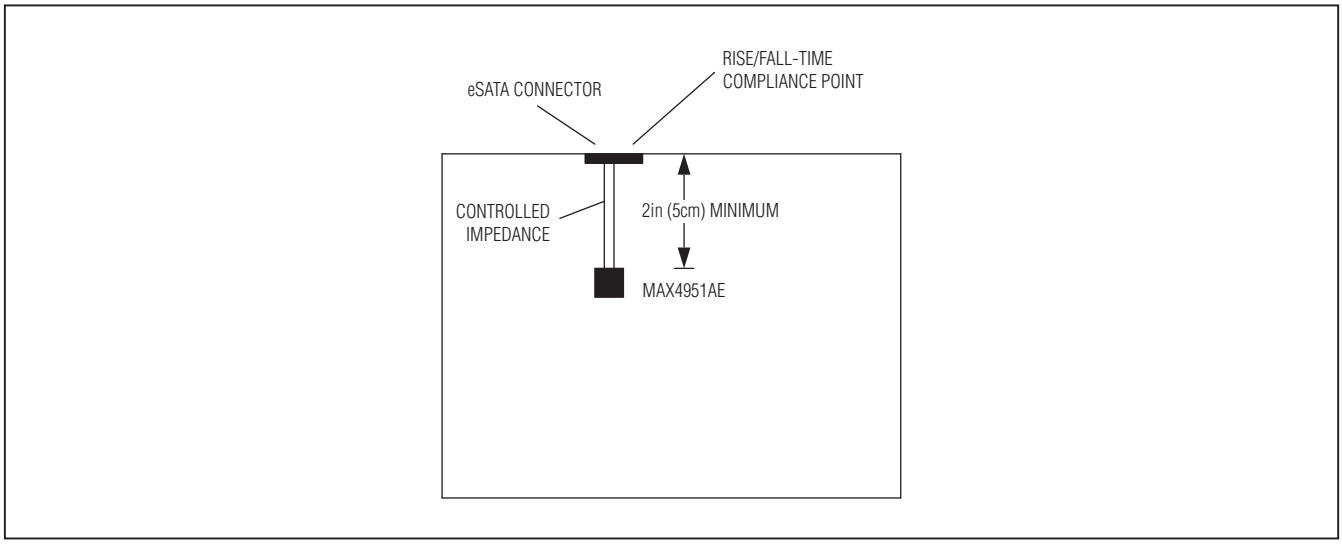


Figure 1. Circuit for Measuring $t_{R/F}$ for MAX4951AE (See SATA Specifications for Compliance Measurement)

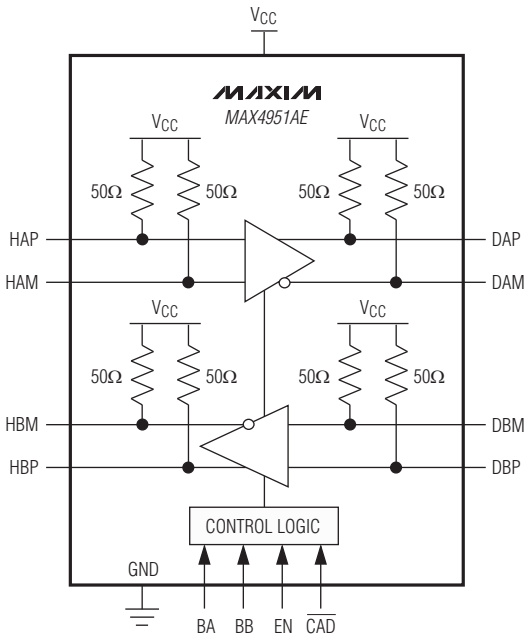
SATA I/II Bidirectional Redriver with High ESD and Cable Detect

Pin Description

PIN	NAME	FUNCTION
1	HAP	Noninverting Input from Host Channel A
2	HAM	Inverting Input from Host Channel A
3, 13, 17, 19	GND	Ground
4	HBM	Inverting Output to Host Channel B
5	HBP	Noninverting Output to Host Channel B
6, 10, 16, 20	V_{CC}	Positive Supply Voltage Input. Bypass V_{CC} to GND with 0.1µF and 0.001µF capacitors in parallel and as close as possible to the device.
7	EN	Active-High Enable Input. Drive EN low to put device in standby mode. Drive EN high for normal operation. EN is internally pulled down with a 330kΩ (typ) resistor.
8	BB	Channel-B Boost Enable Input. Drive BB high to enable channel-B output boost. Drive BB low for standard SATA output level. BB is internally pulled down with a 330kΩ (typ) resistor.
9	BA	Channel-A Boost Enable Input. Drive BA high to enable channel-A output boost. Drive BA low for standard SATA output level. BA is internally pulled down with a 330kΩ (typ) resistor.
11	DBP	Noninverting Input from Device Channel B
12	DBM	Inverting Input from Device Channel B
14	DAM	Inverting Output to Device Channel A
15	DAP	Noninverting Output to Device Channel A
18	$\overline{CAD}$	Active-Low Cable-Detect Input. Drive $\overline{CAD}$ high to put device in standby mode. Drive $\overline{CAD}$ low for normal operation. $\overline{CAD}$ is internally pulled up with a 330kΩ (typ) resistor.
—	EP	Exposed Pad. Internally connected to GND. EP must be electrically connected to a ground plane for proper thermal and electrical operation.

SATA I/II Bidirectional Redriver with High ESD and Cable Detect

Functional Diagram/Truth Table



EN	$\overline{CAD}$	STATUS
0	0	Low-Power Standby
0	1	Low-Power Standby
1	0	Active
1	1	Low-Power Standby

BB	BA	OUTPUT LEVELS
0	0	A and B are Standard Levels
0	1	A is Boosted and B is Standard
1	0	A is Standard and B is Boosted
1	1	A and B are Boosted

Note: BA, BB, and EN are internally pulled down to GND by 330kΩ resistors. $\overline{CAD}$ is internally pulled up to V_{CC} by a 330kΩ resistor.

SATA I/II Bidirectional Redriver with High ESD and Cable Detect

Detailed Description

The MAX4951AE consists of two identical buffers that take SATA input signals and return them to full output levels while withstanding ESD events up to ±8kV (HBM). This device functions for SATA I/SATA II applications

Input/Output Terminations

Inputs and outputs are internally 50Ω terminated to V_{CC} (see the *Functional Diagram/Truth Table*) and must be AC-coupled to the SATA controller IC and SATA device for proper operation.

OOB Logic

The MAX4951AE provides full OOB signal support through high-speed amplitude detection circuitry. SATA OOB differential input signals of 50mV_{P-P} or less are detected as off and not passed to the output. This prevents the system from responding to unwanted noise. SATA OOB differential input signals of 200mV_{P-P} or more are detected as on and passed to the output. This allows OOB signals to transmit through the MAX4951AE. The time for the amplitude detection circuit to detect an inactive SATA OOB input and squelch the associated output, or detect an active SATA OOB input and enable the output, is less than 5ns (max).

Enable Input

The MAX4951AE features an active-high enable input (EN). EN has an internal pulldown resistor of 330kΩ (typ). When EN is driven low or left unconnected, the MAX4951AE enters low-power standby mode and the buffers are disabled, reducing supply current to 350µA (typ). Drive EN high for normal operation.

Cable-Detect Input

The MAX4951AE features an active-low cable-detect input ($\overline{CAD}$). $\overline{CAD}$ has an internal pullup resistor of 330kΩ (typ). When $\overline{CAD}$ is driven high or left unconnected, the MAX4951AE enters low-power standby mode and the buffers are disabled, reducing supply current to 350µA (typ). This signal is normally driven low by inserting an eSATA cable into a properly wired socket (see Figure 4). If the cable-detect feature is not desired, simply ground this pin.

Output Boost Selection Inputs

The MAX4951AE has two digital control logic inputs, BA and BB. BA and BB have internal pulldown resistors of 330kΩ (typ). BA and BB control the boost level of their corresponding buffers (see the *Functional Diagram/Truth Table*). Drive BA or BB low or leave unconnected for standard SATA output levels. Drive BA or BB high to boost the output. The boosted output level compensates for attenuation from longer trace-length cables or to meet eSATA specifications.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX4951AE is protected against ESD up to ±8kV (Human Body Model) without damage. The ESD structures withstand ±8kV in all states: normal operation and powered down. After an ESD event, the MAX4951AE continues to function without latchup.

Human Body Model

The MAX4951AE is characterized for ±8kV ESD protection using the Human Body Model (MIL-STD-883, Method 3015). Figure 2 shows the Human Body Model and Figure 3 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

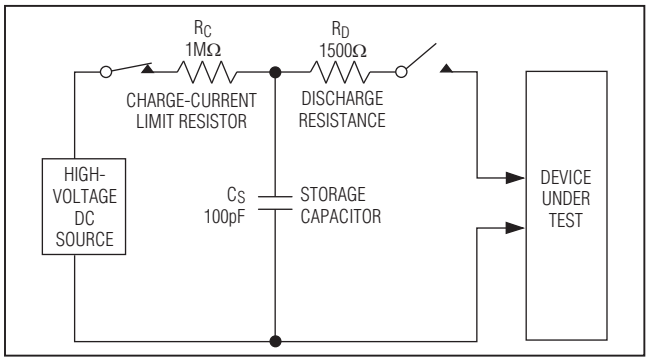


Figure 2. Human Body ESD Test Model

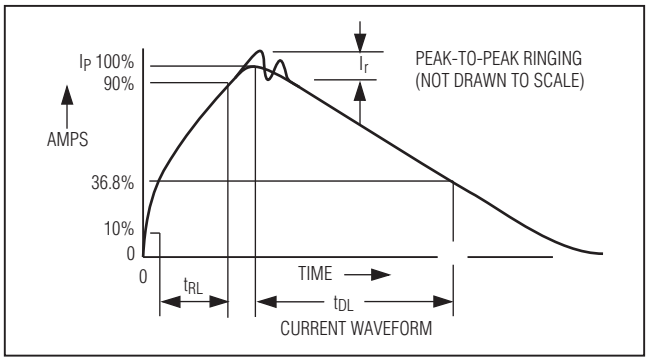


Figure 3. Human Body Current Waveform

Applications Information

Figure 4 shows a typical application circuit with the MAX4951AE used to drive an eSATA output. The diagram assumes that the MAX4951AE is close to the SATA host controller. In this application, BB is set low to drive standard SATA levels to the host, and BA is set high to overcome board/connector losses, matching eSATA levels at the connector. If the MAX4951AE is further from the controller, set BB high to compensate for the added attenuation. The MAX4951AE is backward-compatible with the MAX4951 (see Figure 5).

Exposed-Pad Package

The exposed-pad, 20-pin, TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the MAX4951AE must be soldered to GND for proper thermal and electrical performance. For more information on exposed-pad packages, refer to Maxim Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Layout

Use controlled-impedance transmission lines to interface with the MAX4951AE high-speed inputs and outputs. Place power-supply decoupling capacitors as close as possible to the V_{CC} pin.

Power Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply V_{CC} before applying signals, especially if the signal is not current limited.

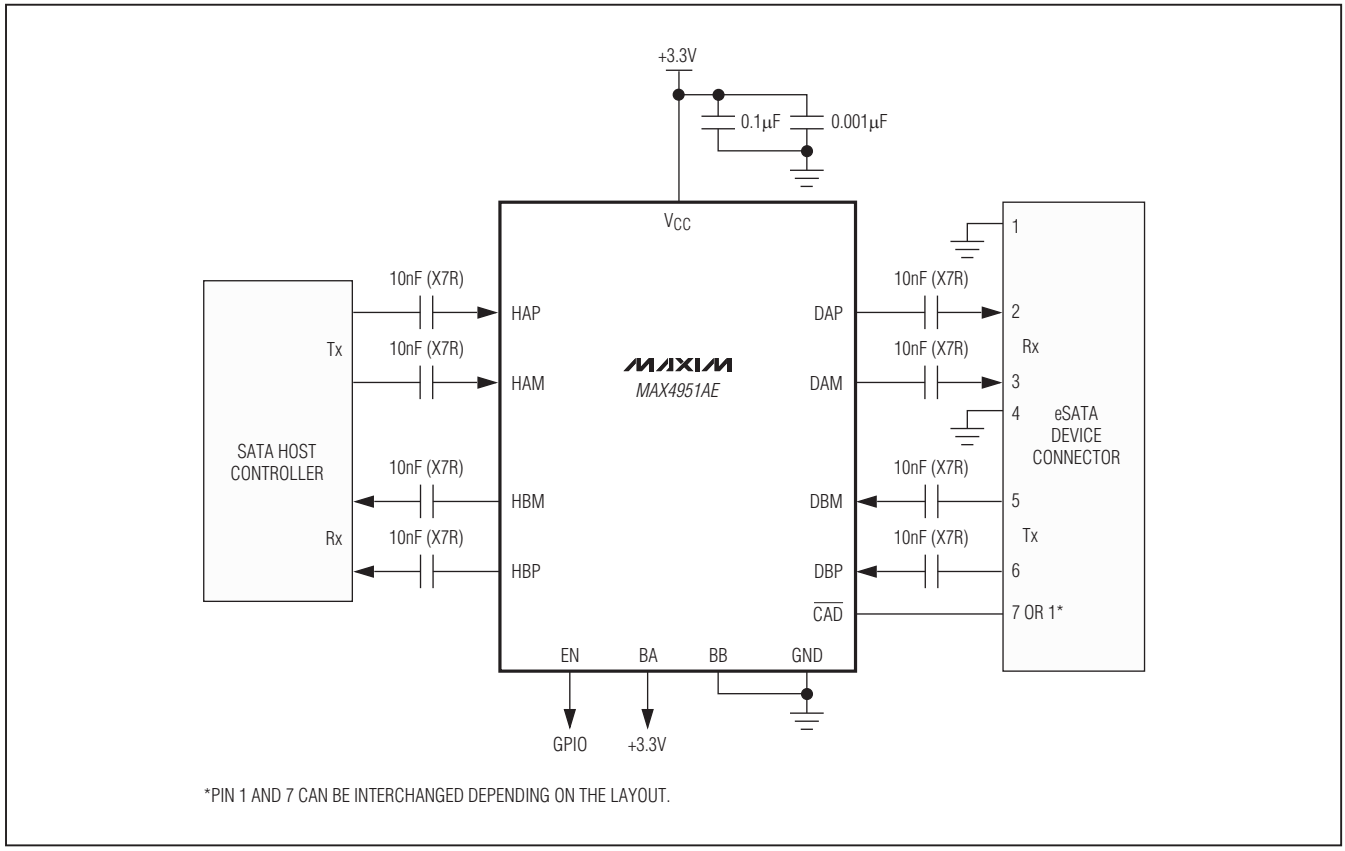


Figure 4. Typical Application Circuit

SATA I/II Bidirectional Redriver with High ESD and Cable Detect

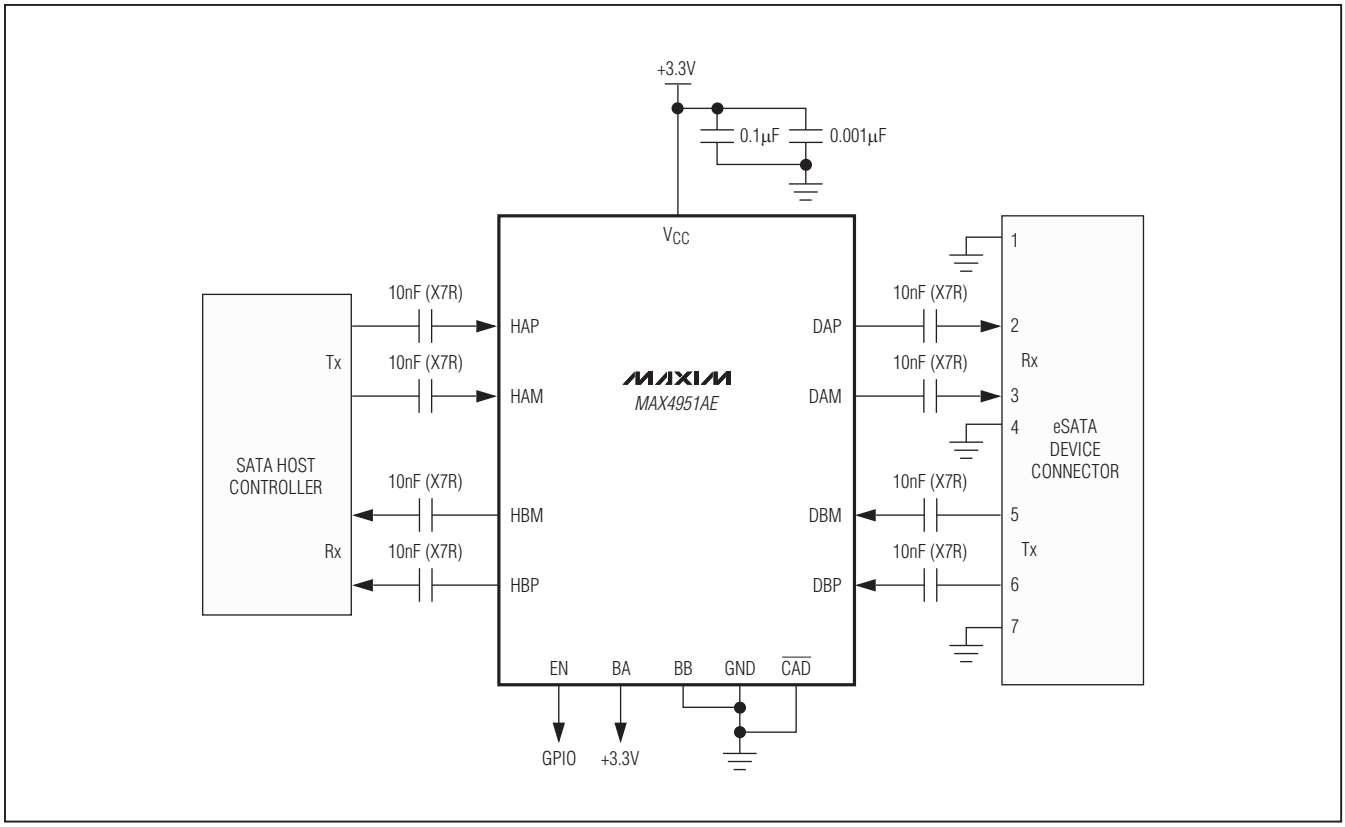


Figure 5. MAX4951 Backward-Compatible Mode

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 TQFN-EP	T2044+2	21-0139

Mouser Electronics

Authorized Distributor

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Maxim Integrated:
MAX4951AECTP+T