

CONFIGURABLE MULTIPLE-FUNCTION GATE

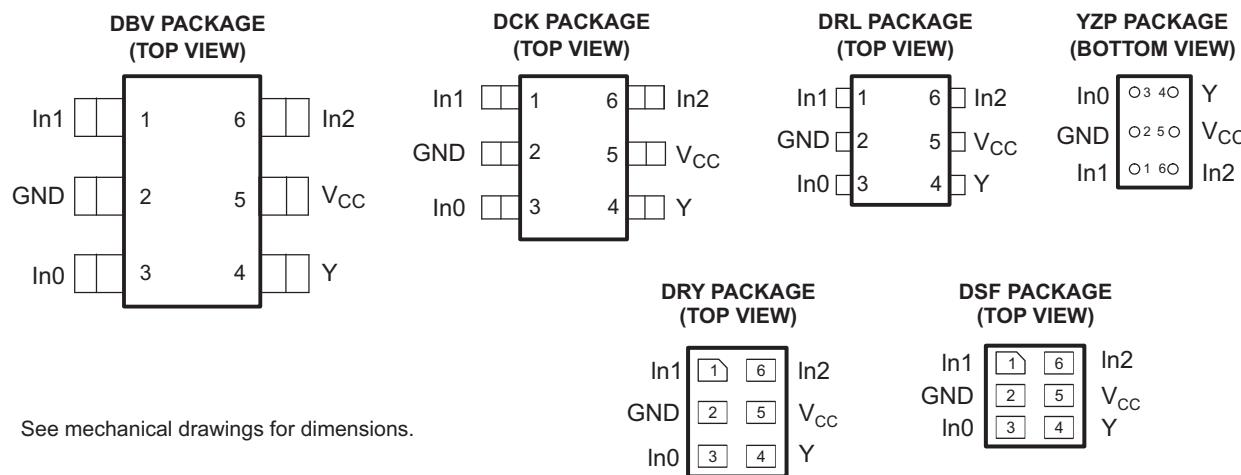
Check for Samples: [SN74LVC1G57](#)

FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.3 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{cc}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode

Operation

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION

This configurable multiple-function gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G57 features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter, and noninverter. All inputs can be connected to V_{CC} or GND.

This device functions as an independent gate, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

Table 1. FUNCTION TABLE

INPUTS			OUTPUT
In2	In1	In0	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

Figure 1. LOGIC DIAGRAM (POSITIVE LOGIC)

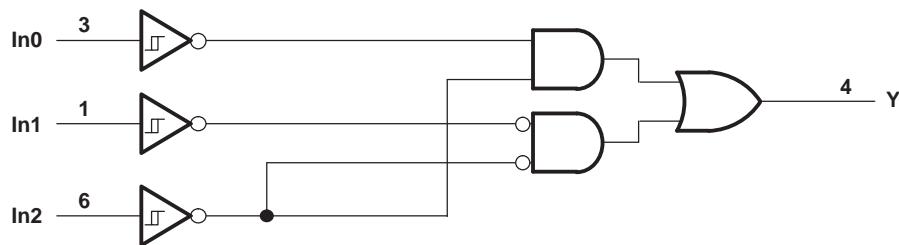


Table 2. FUNCTION SELECTION TABLE

LOGIC FUNCTION	FIGURE NO.
2-input AND	1
2-input AND with both inputs inverted	4
2-input NAND with inverted input	2, 3
2-input OR with inverted input	2, 3
2-input NOR	4
2-input NOR with both inputs inverted	1
2-input XNOR	5

LOGIC CONFIGURATIONS

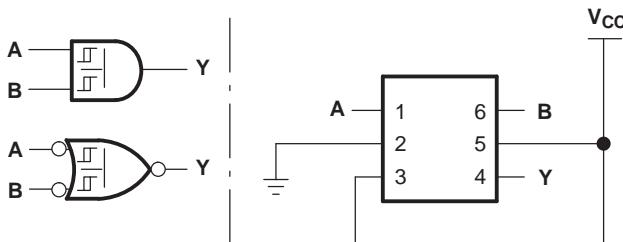


Figure 2. 2-Input AND Gate

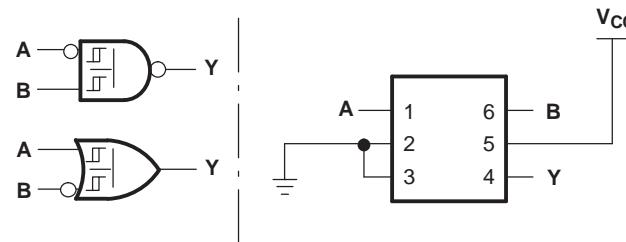


Figure 3. 2-Input NAND Gate With Inverted A Input

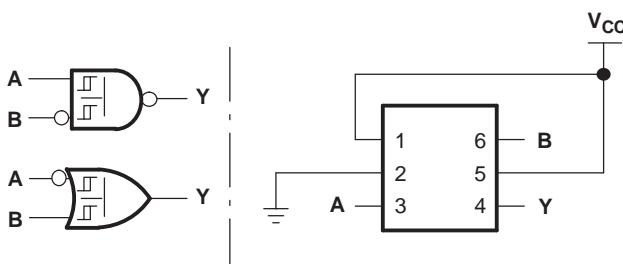


Figure 4. 2-Input NAND Gate With Inverted B Input

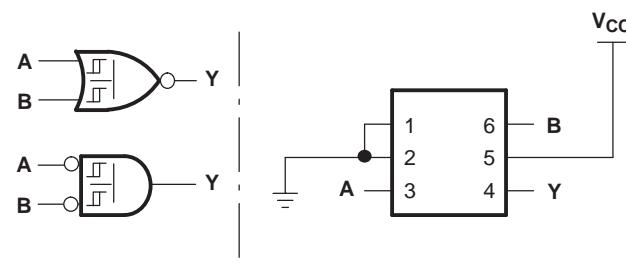


Figure 5. 2-Input NOR Gate

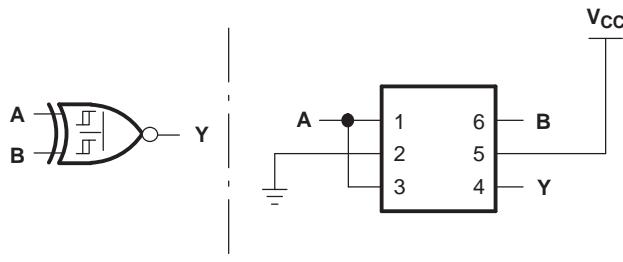


Figure 6. 2-Input XNOR Gate

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range ⁽²⁾	-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state ^{(2) (3)}	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 50	mA
	Continuous current through V_{CC} or GND		± 100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DBV package	165	°C/W
		DCK package	259	
		DRL package	142	
		YZP package	123	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	V
		Data retention only	1.5	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65$ V	-4	mA
		$V_{CC} = 2.3$ V	-8	
		$V_{CC} = 3$ V	-16	
		$V_{CC} = 4.5$ V	-24	
			-32	
I_{OL}	Low-level output current	$V_{CC} = 1.65$ V	4	mA
		$V_{CC} = 2.3$ V	8	
		$V_{CC} = 3$ V	16	
		$V_{CC} = 4.5$ V	24	
			32	
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{T+} Positive-going input threshold voltage		1.65 V	0.79	1.16		V
		2.3 V	1.11	1.56		
		3 V	1.5	1.87		
		4.5 V	2.16	2.74		
		5.5 V	2.61	3.33		
V _{T-} Negative-going input threshold voltage		1.65 V	0.35	0.62		V
		2.3 V	0.58	0.87		
		3 V	0.84	1.19		
		4.5 V	1.41	1.9		
		5.5 V	1.87	2.29		
ΔV _T Hysteresis (V _{T+} – V _{T-})		1.65 V	0.3	0.62		V
		2.3 V	0.4	0.8		
		3 V	0.53	0.87		
		4.5 V	0.71	1.04		
		5.5 V	0.71	1.11		
V _{OH}	I _{OH} = –100 µA	1.65 V to 5.5 V	V _{CC} – 0.1			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.9			
	I _{OH} = –16 mA	3 V	2.4			
	I _{OH} = –24 mA		2.3			
	I _{OH} = –32 mA	4.5 V	3.8			
V _{OL}	I _{OL} = 100 µA	1.65 V to 5.5 V		0.1		V
	I _{OL} = 4 mA	1.65 V		0.45		
	I _{OL} = 8 mA	2.3 V		0.3		
	I _{OL} = 16 mA	3 V		0.4		
	I _{OL} = 24 mA			0.55		
	I _{OL} = 32 mA	4.5 V		0.55		
I _I	V _I = 5.5 V or GND	0 to 5.5 V		±1	µA	
I _{off}	V _I or V _O = 5.5 V	0		±10	µA	
I _{CC}	V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V		10	µA	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V		500	µA	
C _i	V _I = V _{CC} or GND	3.3 V		3.5	pF	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7](#))

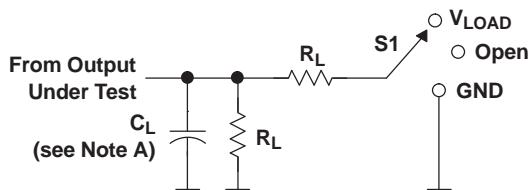
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	$V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$	UNIT				
			MIN	MAX	MIN	MAX					
t_{pd}	Any In	Y	3.2	14.4	2	8.3	1.5	6.3	1.1	5.1	ns

Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	$V_{CC} = 5\text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance $f = 10\text{ MHz}$	20	20	21	22	pF

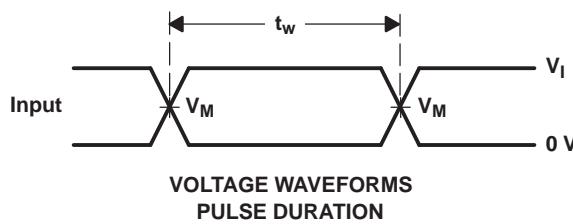
PARAMETER MEASUREMENT INFORMATION



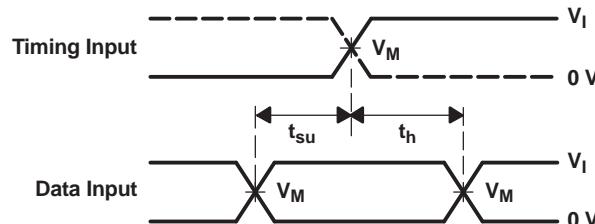
TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

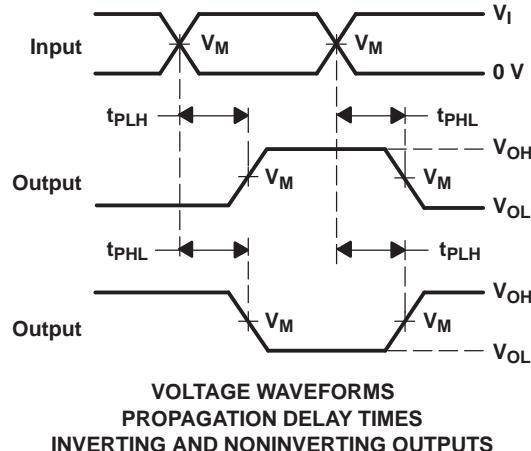
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5 \text{ V} \pm 0.5 \text{ V}$	V_{CC}	$\leq 2.5 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



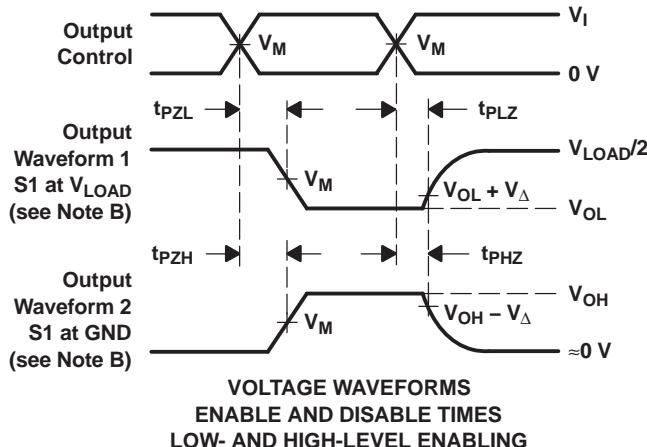
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PZH} are the same as t_{dis} .
 F. t_{PLZ} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 7. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision L (January 2007) to Revision M	Page
• Added DRY and DSF packages to datasheet.	1
• Added additional package options to the ORDERING INFORMATION table.	1

Changes from Revision M (October 2011) to Revision N	Page
• Removed ORDERING INFORMATION table, package updates now included in Package Ordering Addendum.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74LVC1G57DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CA72 ~ CA7O ~ CA7R)	Samples
SN74LVC1G57DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CA72 ~ CA7O ~ CA7R)	Samples
SN74LVC1G57DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CA72 ~ CA7O ~ CA7R)	Samples
SN74LVC1G57DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CL5 ~ CLF ~ CLK ~ CLR)	Samples
SN74LVC1G57DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CL5 ~ CLF ~ CLK ~ CLR)	Samples
SN74LVC1G57DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CL5 ~ CLF ~ CLK ~ CLR)	Samples
SN74LVC1G57DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CL7 ~ CLR)	Samples
SN74LVC1G57DRLRG4	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CL7 ~ CLR)	Samples
SN74LVC1G57DRY2	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL	Samples
SN74LVC1G57DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL	Samples
SN74LVC1G57DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL	Samples
SN74LVC1G57YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CL7 ~ CLN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

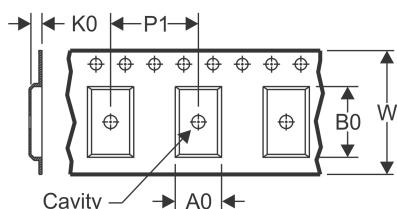
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

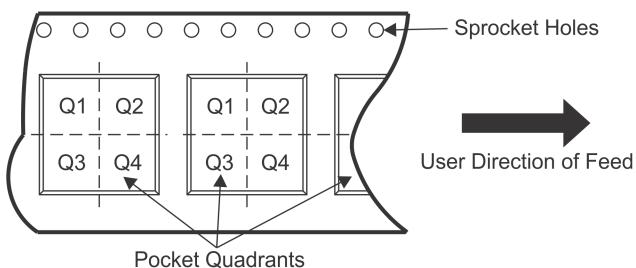
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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G57DRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1G57DRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G57DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G57DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G57DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G57YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

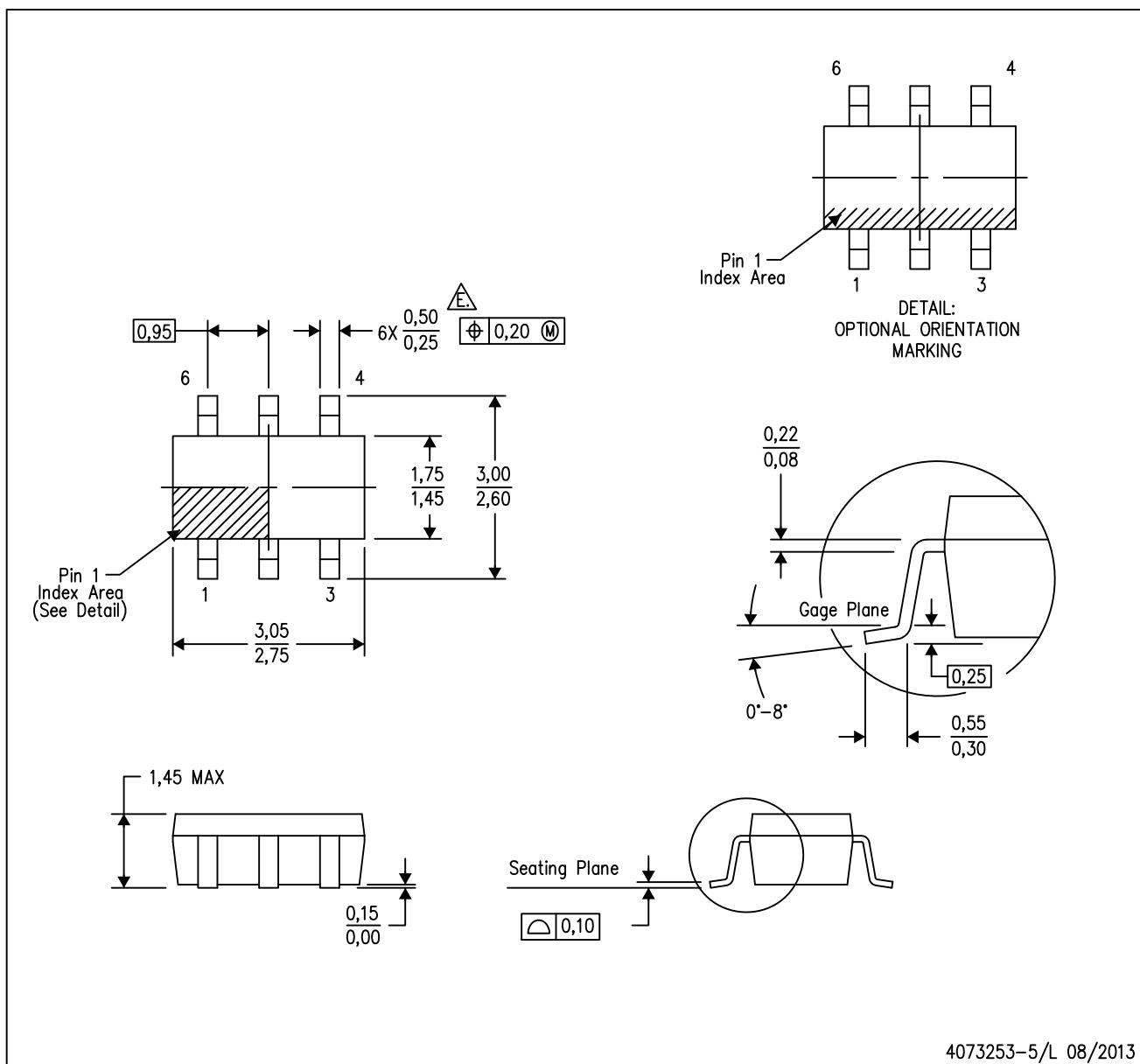

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G57DRLR	SOT	DRL	6	4000	180.0	180.0	30.0
SN74LVC1G57DRLR	SOT	DRL	6	4000	202.0	201.0	28.0
SN74LVC1G57DRY2	SON	DRY	6	5000	180.0	180.0	30.0
SN74LVC1G57DRYR	SON	DRY	6	5000	180.0	180.0	30.0
SN74LVC1G57DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74LVC1G57YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

MECHANICAL DATA

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-5/L 08/2013

NOTES:

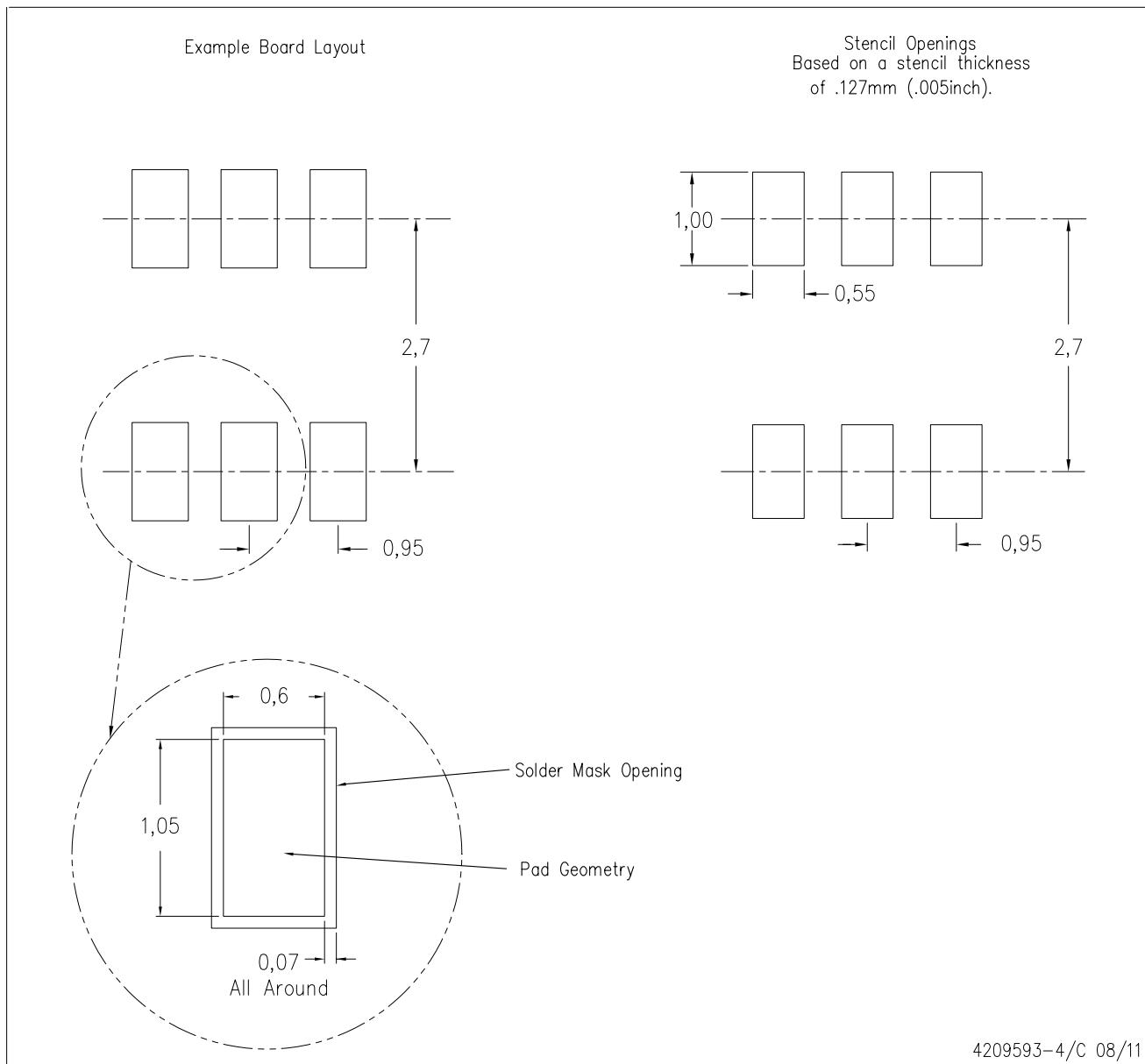
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.

△ Falls within JEDEC MO-178 Variation AB, except minimum lead width.

LAND PATTERN DATA

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE

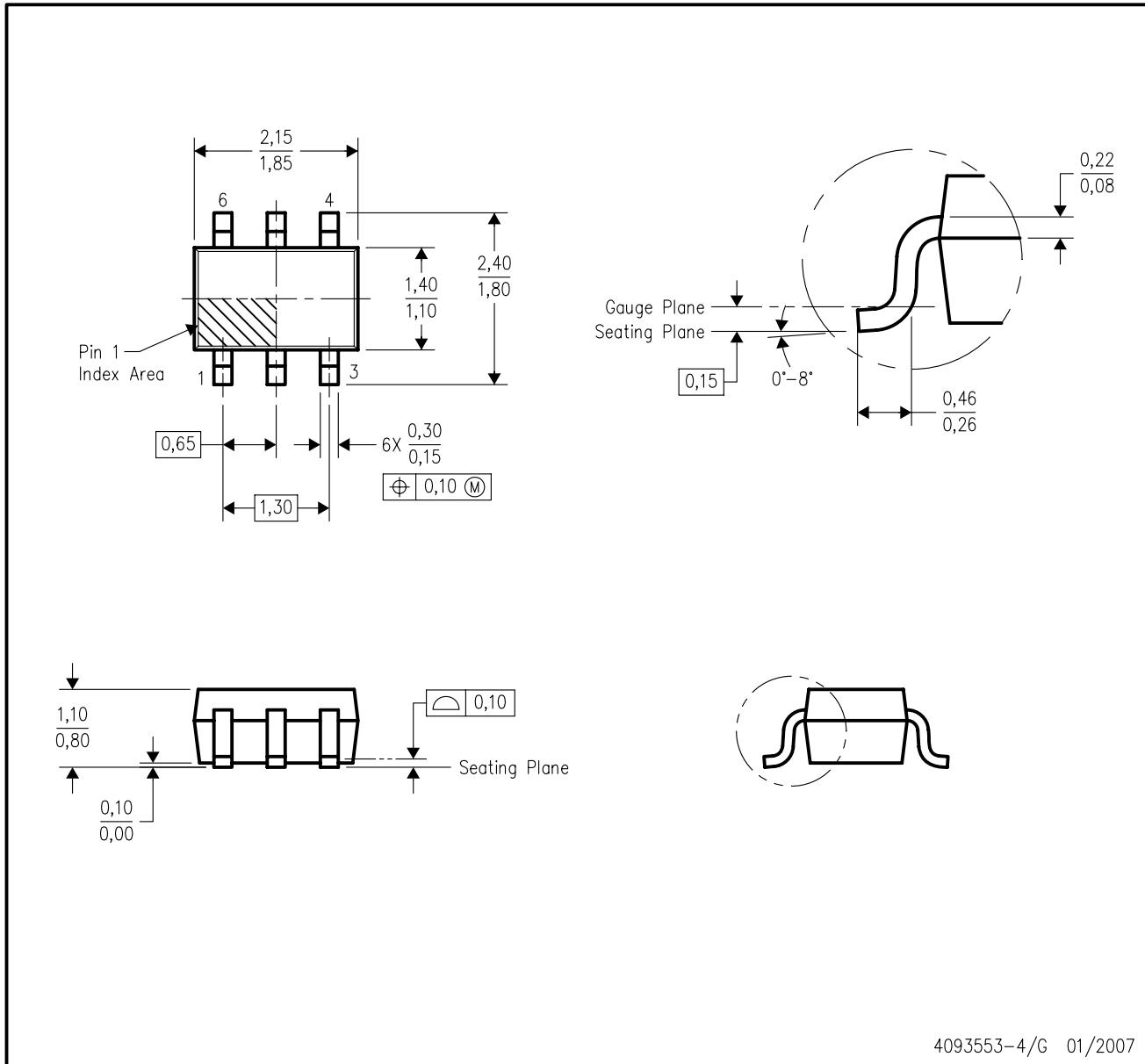


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-4/G 01/2007

NOTES:

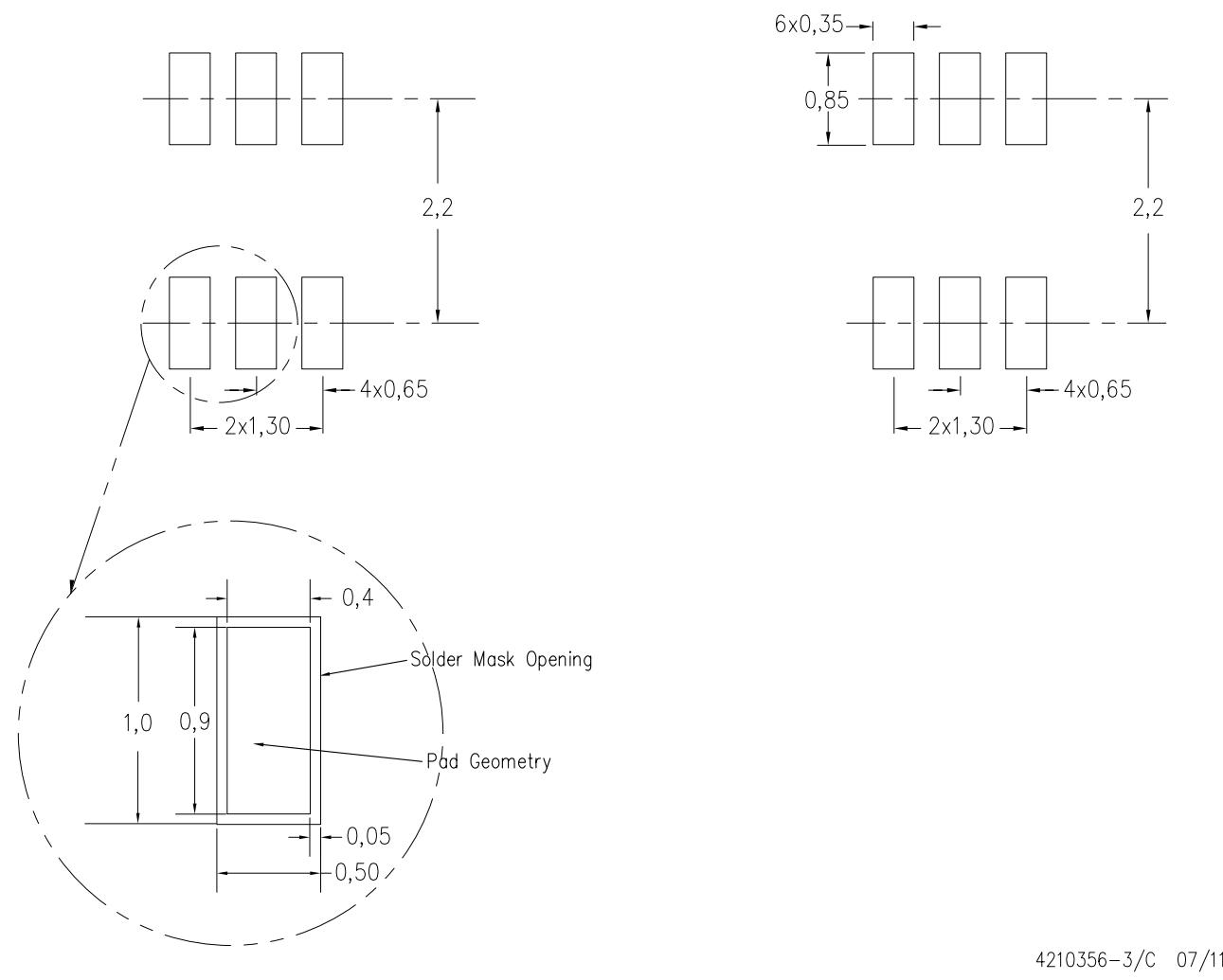
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

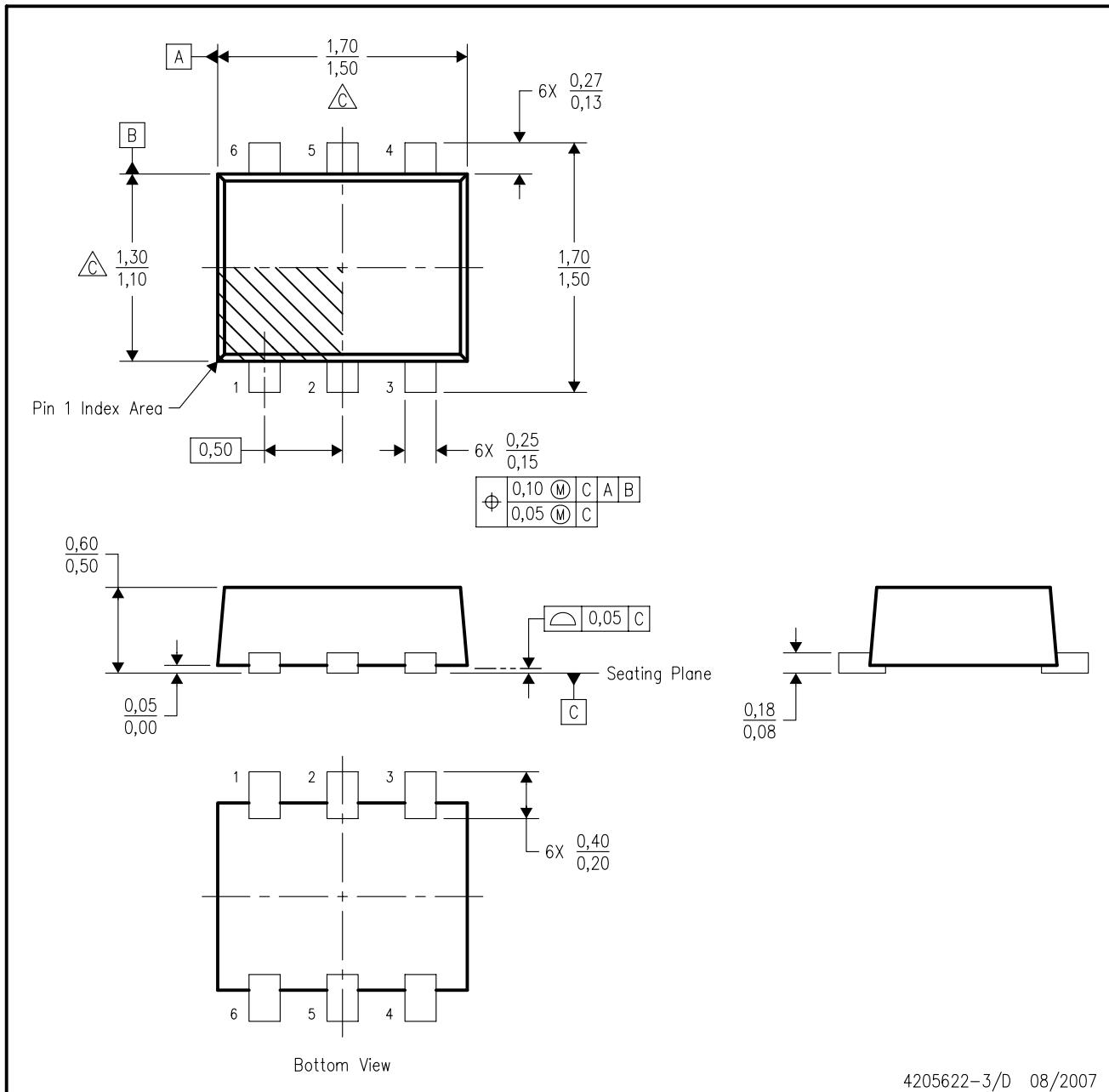


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

 This drawing is subject to change without notice.

 Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.

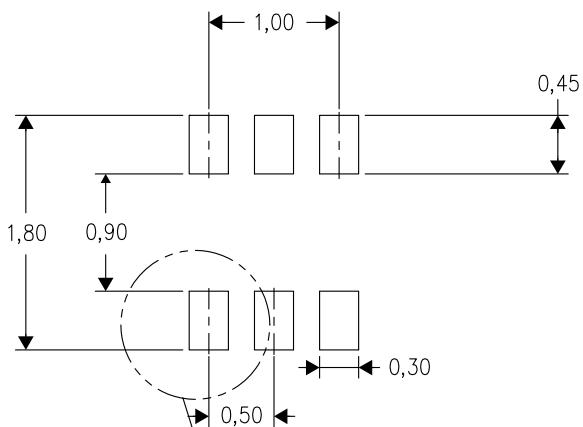
D. JEDEC package registration is pending.

D. JEDEC package registration is pending.

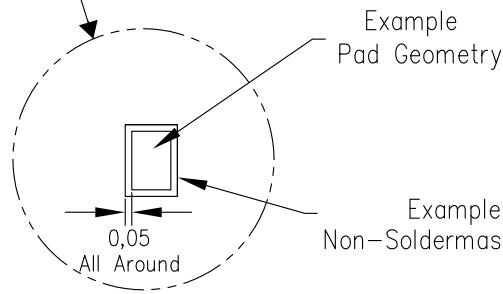
DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE

Example Board Layout

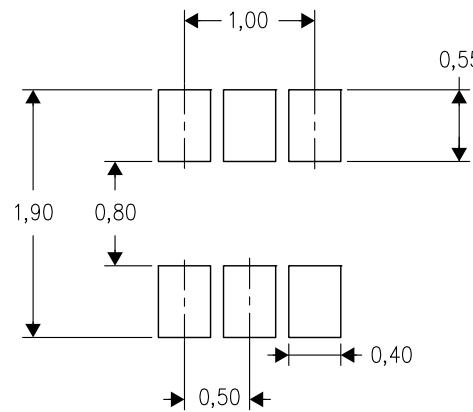


Example Non-Soldermask Defined Pad



Example Pad Geometry

Example Non-Soldermask Opening

Example Stencil Design
(Note E)

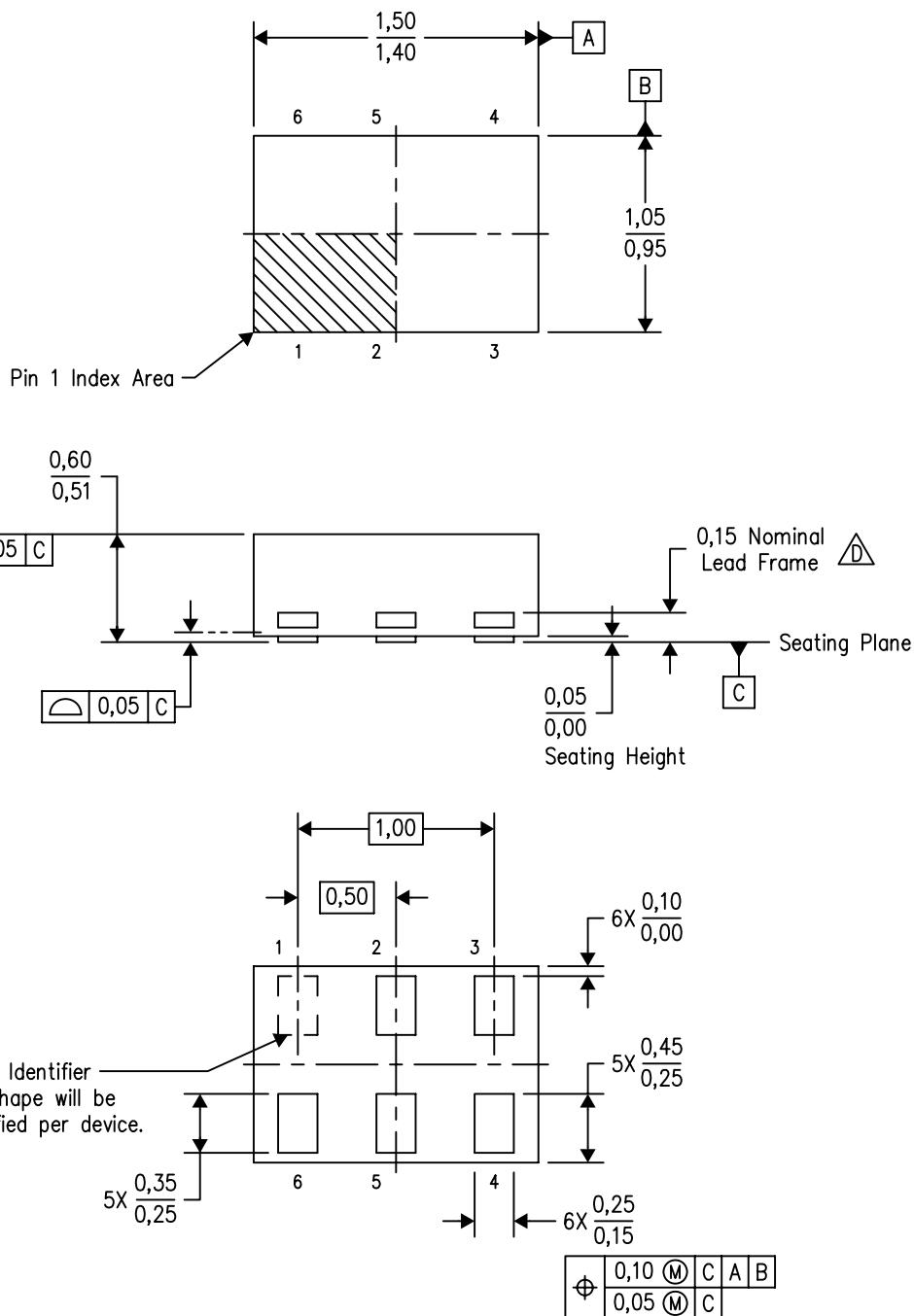
4208207-3/E 06/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Side aperture dimensions over-print land for acceptable area ratio > 0.66 . Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



Bottom View

4207181/F 12/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.

C. SON (Small Outline No-Lead) package configuration.

D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.

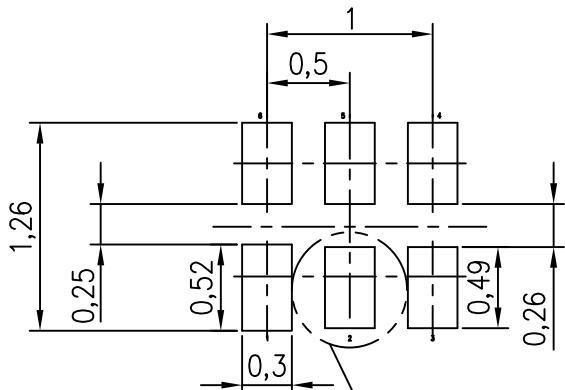
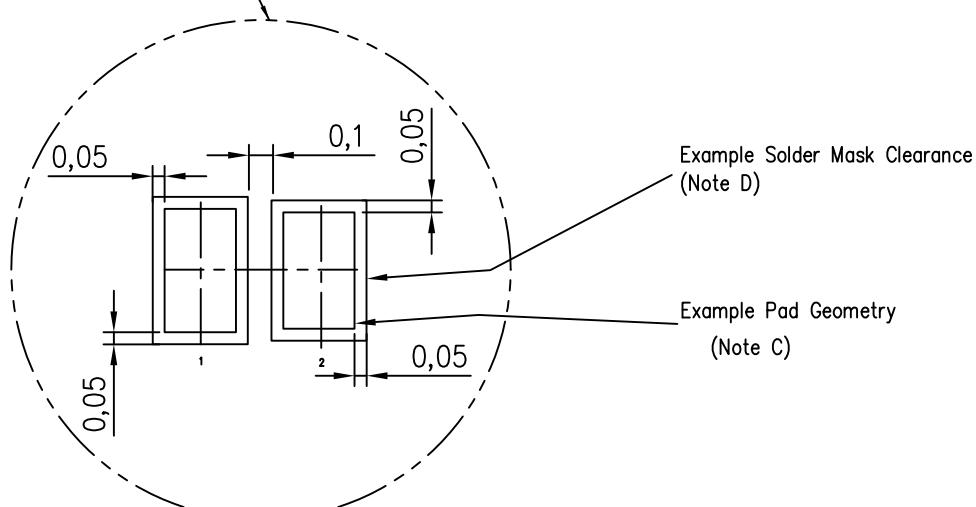
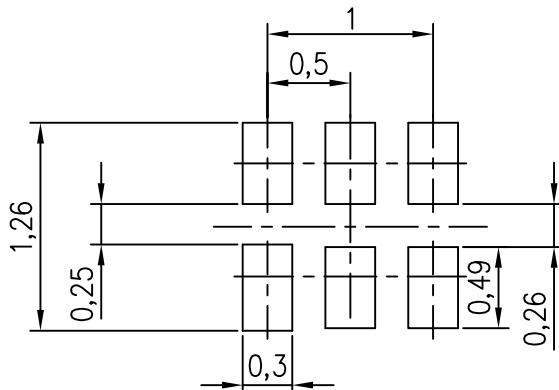
E. This package complies to JEDEC MO-287 variation UFAD.

F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

Example Board Layout

Example Stencil Design
(Note E, F, G)

4208310/E 02/13

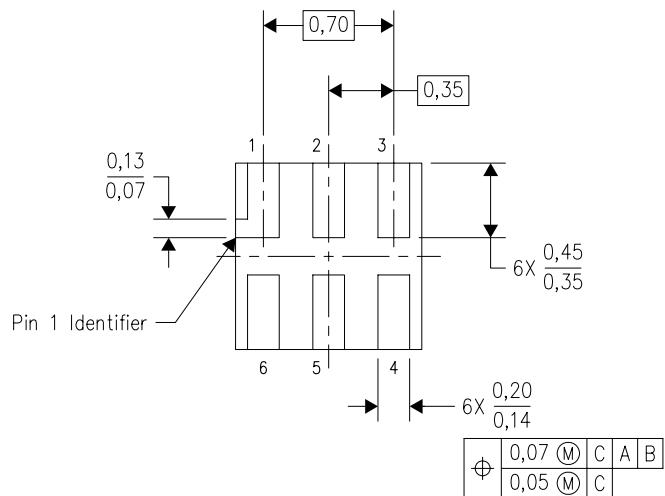
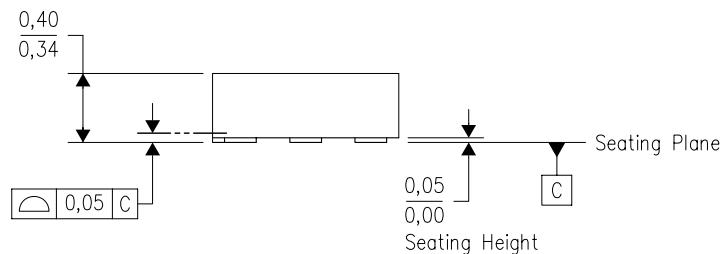
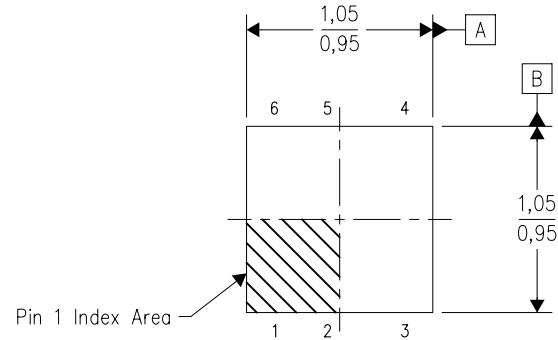
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Side aperture dimensions over-print land for acceptable area ratio > 0.66 . Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

MECHANICAL DATA

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



Bottom View

4208186/E 03/11

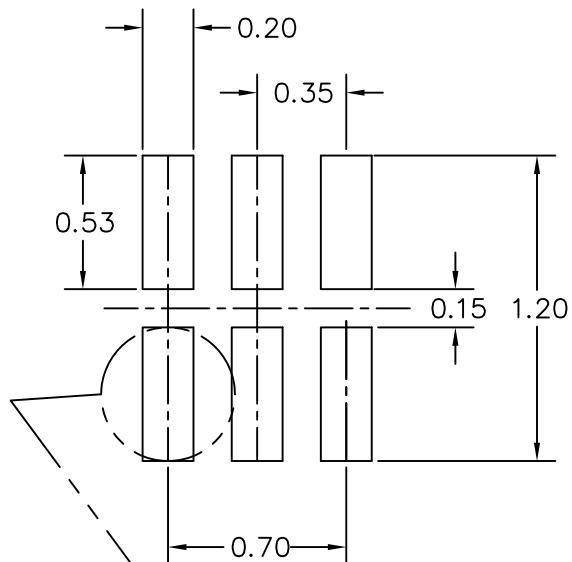
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- D. This package complies to JEDEC MO-287 variation X2AAF.

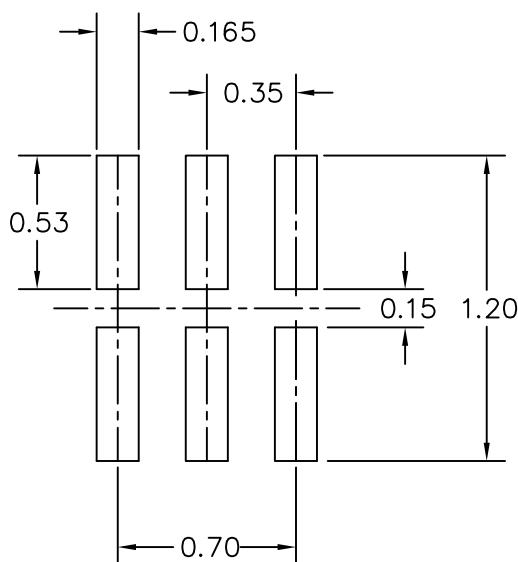
DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

Land Pattern



Stencil Pattern



Contact your PCB vendor for
allowable Solder Mask clearance (Notes C, D.)

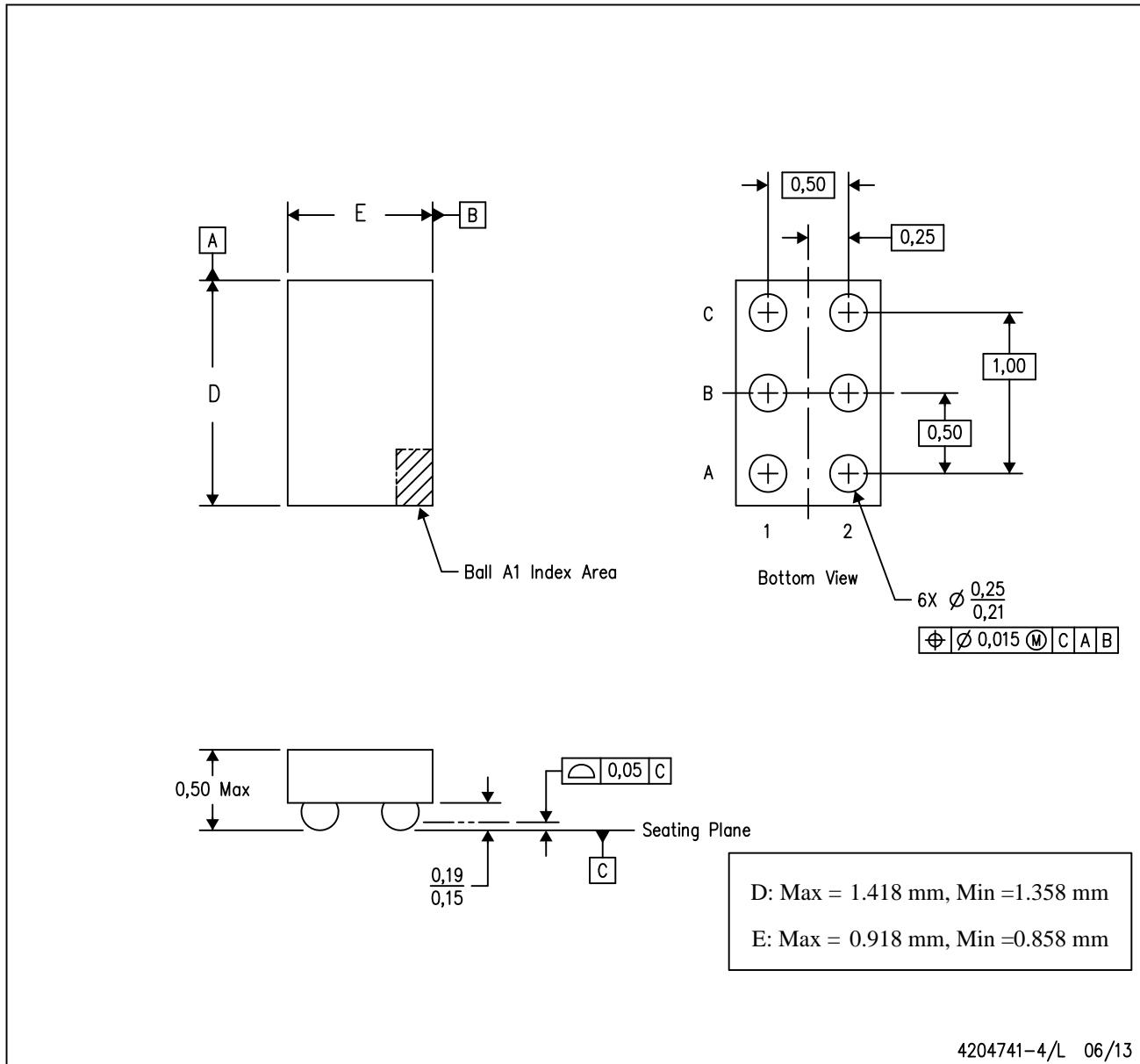
4210277/D 05/12

NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Publication IPC-7351 is recommended for alternate designs.
 D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
 E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 H. Component placement force should be minimized to prevent excessive paste block deformation.

MECHANICAL DATA

YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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