

TOSHIBA BI-DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

SM8GZ47, SM8JZ47, SM8GZ47A, SM8JZ47A

AC POWER CONTROL APPLICATIONS

- Repetitive Peak Off-State Voltage: $V_{DRM} = 400V, 600V$
- R.M.S On-State Current: $I_T (RMS) = 8A$
- High Commutating (dv / dt)
- Isolation Voltage: $V_{ISOL} = 1500V AC$

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC		SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage	SM8GZ47 SM8GZ47A	V_{DRM}	400	V
	SM8JZ47 SM8JZ47A		600	
R.M.S On-State Current (Full Sine Waveform $T_c = 83^\circ C$)		$I_T (RMS)$	8	A
Peak One Cycle Surge On-State Current (Non-Repetitive)		I_{TSM}	80 (50Hz)	A
			88 (60Hz)	
$I^2 t$ Limit Value		$I^2 t$	32	$A^2 s$
Critical Rate of Rise of On-State Current (Note 1)		di / dt	50	A / μs
Peak Gate Power Dissipation		P_{GM}	5	W
Average Gate Power Dissipation		$P_G (AV)$	0.5	W
Peak Gate Voltage		V_{GM}	10	V
Peak Gate Current		I_{GM}	2	A
Junction Temperature		T_j	-40~125	$^\circ C$
Storage Temperature Range		T_{stg}	-40~125	$^\circ C$
Isolation Voltage (AC, $t = 1min.$)		V_{ISOL}	1500	V

Note 1: di / dt Test Condition

$$V_{DRM} = 0.5 \times \text{Rated}$$

$$I_{TM} \leq 12A$$

$$t_{gw} \geq 10\mu s$$

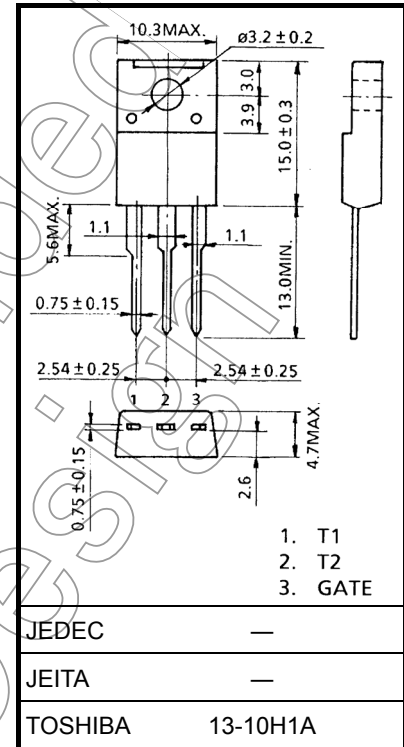
$$t_{gr} \leq 250ns$$

$$I_{GP} = I_{GT} \times 2.0$$

Note 2: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Unit: mm

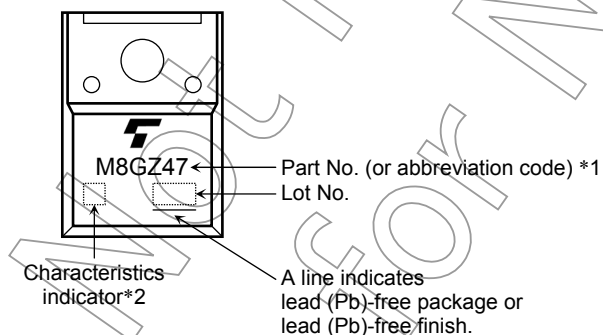


Weight: 1.7 g (typ.)

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

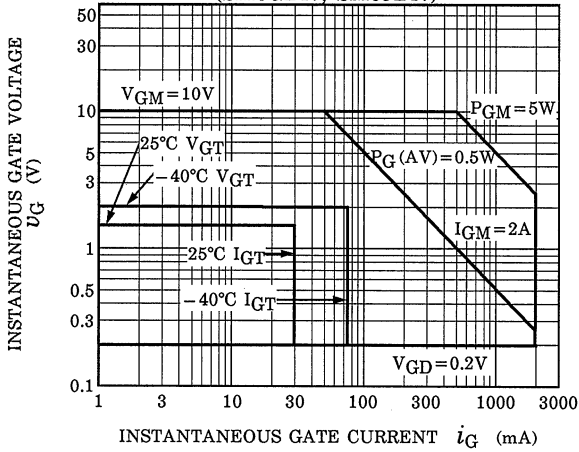
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT	
Repetitive Peak Off-State Current		I_{DRM}	$V_{DRM} = \text{Rated}$	—	—	20	μA	
Gate Trigger Voltage	I	V_{GT}	$V_D = 12\text{V}$ $R_L = 20\Omega$	T2 (+), Gate (+)	—	—	1.5	V
	II			T2 (+), Gate (-)	—	—	1.5	
	III			T2 (-), Gate (-)	—	—	1.5	
	IV			T2 (-), Gate (+)	—	—	—	
Gate Trigger Current	SM8GZ47 SM8JZ47	I_{GT}	$V_D = 12\text{V}$ $R_L = 20\Omega$	T2 (+), Gate (+)	—	—	30	mA
				T2 (+), Gate (-)	—	—	30	
				T2 (-), Gate (-)	—	—	30	
				T2 (-), Gate (+)	—	—	—	
	SM8GZ47A SM8JZ47A			T2 (+), Gate (+)	—	—	20	
				T2 (+), Gate (-)	—	—	20	
				T2 (-), Gate (-)	—	—	20	
				T2 (-), Gate (+)	—	—	—	
Peak On-State Voltage		V_{TM}	$I_{TM} = 12\text{A}$	—	—	1.5	V	
Gate Non-Trigger Voltage		V_{GD}	$V_D = \text{Rated}, T_c = 125^\circ\text{C}$	0.2	—	—	V	
Holding Current		I_H	$V_D = 12\text{V}, I_{TM} = 1\text{A}$	—	—	50	mA	
Thermal Resistance		$R_{th(j-c)}$	Junction to Case, AC	—	—	3.6	$^\circ\text{C} / \text{W}$	
Critical Rate of Rise of Off-State Voltage	SM8GZ47 SM8JZ47	dv/dt	$V_{DRM} = \text{Rated}, T_j = 125^\circ\text{C}$ Exponential Rise	—	300	—	V / μs	
	SM8GZ47A SM8JZ47A			—	200	—		
Critical Rate of Rise of Off-State Voltage at Commutation	SM8GZ47 SM8JZ47	$(dv/dt)_c$	$V_{DRM} = 400\text{V}, T_j = 125^\circ\text{C}$ $(di/dt)_c = -4.5\text{A/ms}$	10	—	—	V / μs	
	SM8GZ47A SM8JZ47A			4	—	—		

MARKING

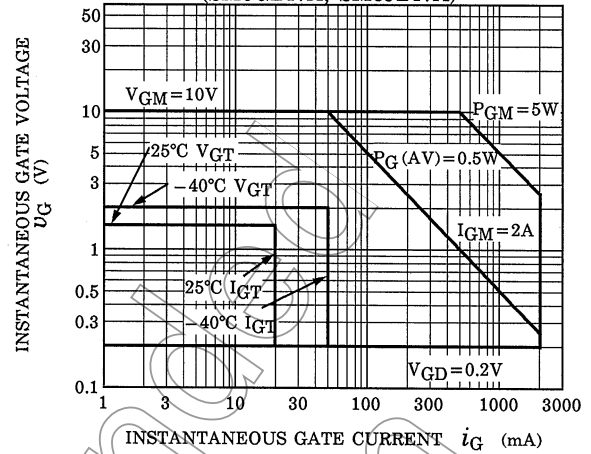


	Part No. (or abbreviation code)	Part No.
*1	M8GZ47	SM8GZ47, SM8GZ47A
	M8JZ47	SM8JZ47, SM8JZ47A
*2	Nothing	SM8GZ47, SM8JZ47
	A	SM8GZ47A, SM8JZ47A

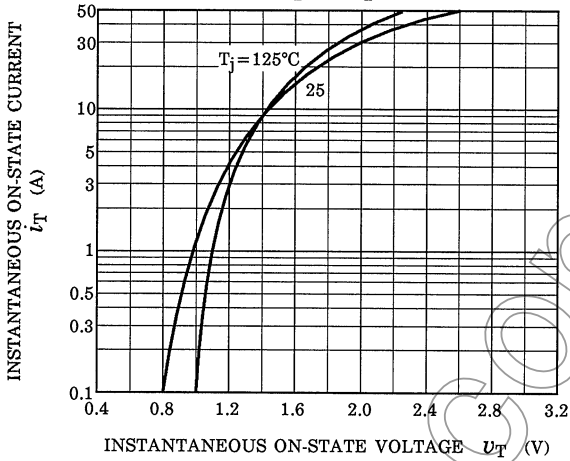
GATE TRIGGER CHARACTERISTIC
(SM8GZ47, SM8JZ47)



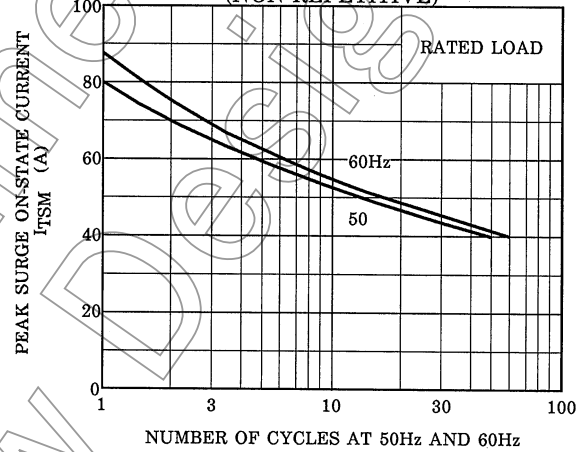
GATE TRIGGER CHARACTERISTIC
(SM8GZ47A, SM8JZ47A)



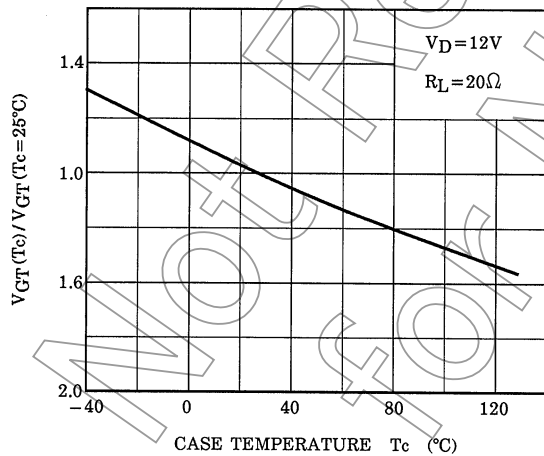
$i_T - v_T$



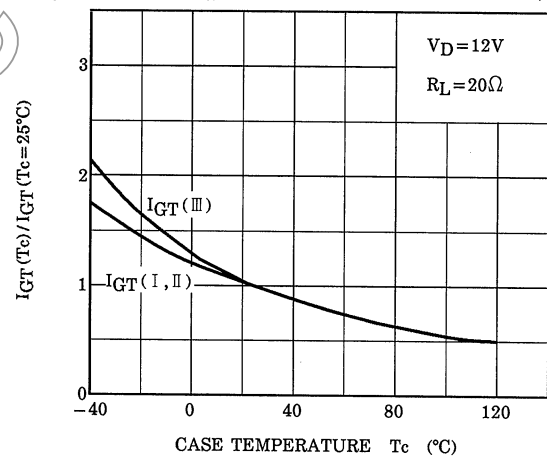
SURGE ON-STATE CURRENT
(NON-REPETITIVE)

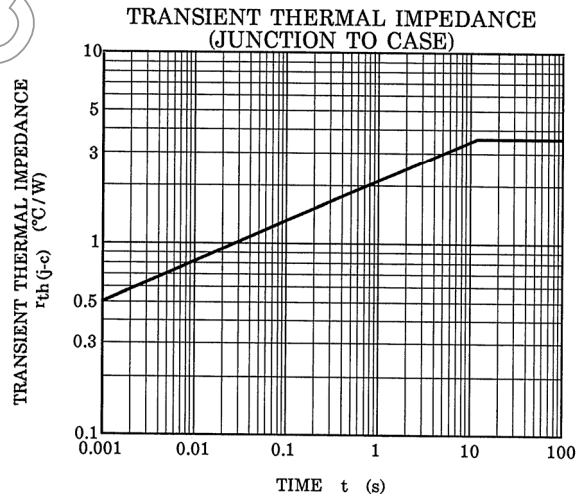
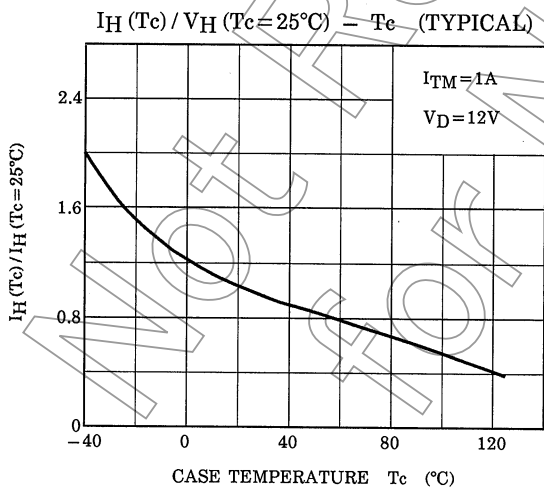
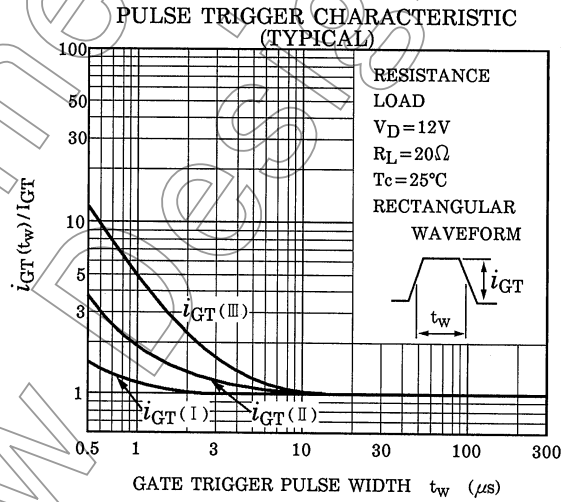
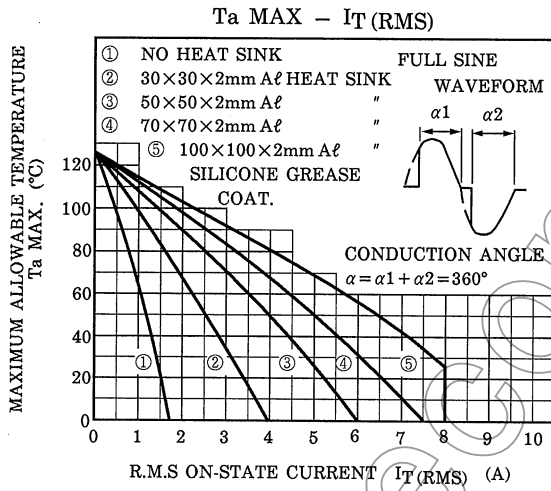
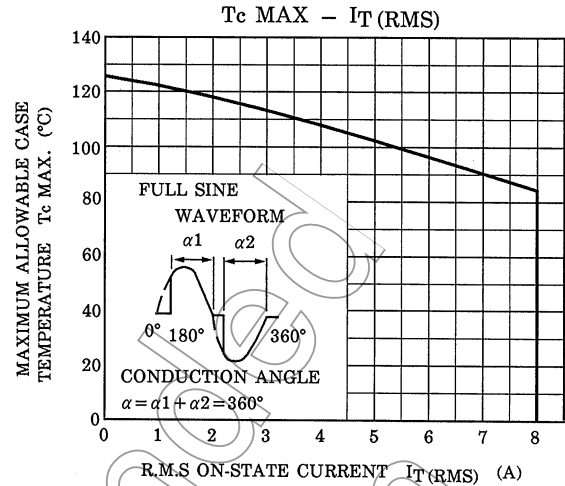
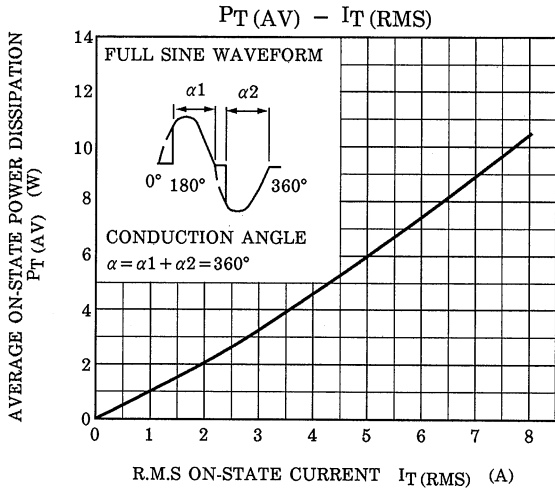


$V_{GT}(T_c) / V_{GT}(T_c=25^\circ\text{C}) - T_c$ (TYPICAL)



$I_{GT}(T_c) / I_{GT}(T_c=25^\circ\text{C}) - T_c$ (TYPICAL)





RESTRICTIONS ON PRODUCT USE

20070701-EN

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