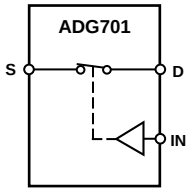
CMOS
Low Voltage 2 Ω SPST Switches

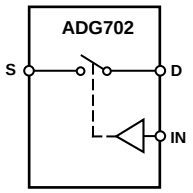
ADG701/ADG702

FEATURES
+1.8 V to +5.5 V Single Supply
2 Ω (Typ) On Resistance
Low On-Resistance Flatness
–3 dB Bandwidth >200 MHz
Rail-to-Rail Operation
6-Lead SOT-23
8-Lead μSOIC Package
Fast Switching Times
t_{ON} 18 ns
t_{OFF} 12 ns
Typical Power Consumption (<0.01 μW)
TTL/CMOS Compatible

APPLICATIONS
Battery Powered Systems
Communication Systems
Sample Hold Systems
Audio Signal Routing
Video Switching
Mechanical Reed Relay Replacement

FUNCTIONAL BLOCK DIAGRAMS





SWITCHES SHOWN FOR
A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG701/ADG702 are monolithic CMOS SPST switches. These switches are designed on an advanced submicron process that provides low power dissipation yet high switching speed, low on resistance, low leakage currents and –3 dB bandwidths of greater than 200 MHz can be achieved.

The ADG701/ADG702 can operate from a single +1.8 V to +5.5 V supply making it ideal for use in battery powered instruments and with the new generation of DACs and ADCs from Analog Devices.

As can be seen from the Functional Block Diagrams, with a logic input of "1" the switch of the ADG701 is closed, while that of the ADG702 is open. Each switch conducts equally well in both directions when ON.

The ADG701/ADG702 are available in 6-lead SOT-23 and 8-lead μSOIC packages.

PRODUCT HIGHLIGHTS

1. +1.8 V to +5.5 V Single Supply Operation. The ADG701/ADG702 offer high performance, including low on resistance and fast switching times and is fully specified and guaranteed with +3 V and +5 V supply rails.
2. Very Low R_{ON} (3 Ω max at 5 V, 5 Ω max at 3 V). At 1.8 V operation, R_{ON} is typically 40 Ω over the temperature range.
3. On-Resistance Flatness $R_{FLAT(ON)}$ (1 Ω max).
4. –3 dB Bandwidth >200 MHz.
5. Low Power Dissipation. CMOS construction ensures low power dissipation.
6. Fast t_{ON}/t_{OFF}.
7. Tiny 6-Lead SOT-23 and 8-Lead μSOIC.

REV. A

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ADG701/ADG702–SPECIFICATIONS[1] (V_{DD} = 5 V ± 10%, GND = 0 V. All specifications –40°C to +85°C unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	2		Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA;
	3	4	Ω max	Test Circuit 1
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA
		1.0	Ω max	
LEAKAGE CURRENTS				V_{DD} = +5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V;
	±0.25	±0.35	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V;
	±0.25	±0.35	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 1 V, or 4.5 V;
	±0.25	±0.35	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	12		ns typ	R_L = 300 Ω, C_L = 35 pF
		18	ns max	V_S = 3 V; Test Circuit 4
t_{OFF}	8		ns typ	R_L = 300 Ω, C_L = 35 pF
		12	ns max	V_S = 3 V; Test Circuit 4
Charge Injection	5		pC typ	V_S = 2 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 5
Off Isolation	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 6
Bandwidth –3 dB	200		MHz typ	R_L = 50 Ω, C_L = 5 pF; Test Circuit 7
C_S (OFF)	17		pF typ	
C_D (OFF)	17		pF typ	
C_D, C_S (ON)	38		pF typ	
POWER REQUIREMENTS				V_{DD} = +5.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.001		µA typ	
		1.0	µA max	

NOTES
[1]Temperature ranges are as follows: B Versions: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3 V ± 10%, GND = 0 V. All specifications –40°C to +85°C unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	3.5		Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA;
	5	6	Ω max	Test Circuit 1
On-Resistance Flatness ($R_{FLAT(ON)}$)	1.5		Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA
LEAKAGE CURRENTS				V_{DD} = +3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.25	±0.35	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.25	±0.35	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 1 V, or 3 V;
	±0.25	±0.35	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	14		ns typ	R_L = 300 Ω, C_L = 35 pF
		20	ns max	V_S = 2 V, Test Circuit 4
t_{OFF}	8		ns typ	R_L = 300 Ω, C_L = 35 pF
		13	ns max	V_S = 2 V, Test Circuit 4
Charge Injection	4		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 5
Off Isolation	–55		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–75		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 6
Bandwidth –3 dB	200		MHz typ	R_L = 50 Ω, C_L = 5 pF; Test Circuit 7
C_S (OFF)	17		pF typ	
C_D (OFF)	17		pF typ	
C_D, C_S (ON)	38		pF typ	
POWER REQUIREMENTS				V_{DD} = +3.3 V Digital Inputs = 0 V or 3 V
I_{DD}	0.001		µA typ	
		1.0	µA max	

NOTES
[1]Temperature ranges are as follows: B Versions: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V to +7 V
Analog, Digital Inputs[2] . . . . . –0.3 V to V_{DD} +0.3 V
or 30 mA, Whichever Occurs First
Continuous Current, S or D . . . . . 30 mA
Peak Current, S or D . . . . . 100 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
µSOIC Package, Power Dissipation . . . . . 315 mW
θ_{JA} Thermal Impedance . . . . . 206°C/W
θ_{JC} Thermal Impedance . . . . . 44°C/W
SOT-23 Package, Power Dissipation . . . . . 282 mW
θ_{JA} Thermal Impedance . . . . . 229.6°C/W
θ_{JC} Thermal Impedance . . . . . 91.99°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
ESD . . . . . 2 kV

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table I. Truth Table

ADG701 In	ADG702 In	Switch Condition
0	1	OFF
1	0	ON

ORDERING GUIDE

Model	Temperature Range	Brand*	Package Descriptions	Package Options
ADG701BRT	–40°C to +85°C	S3B	SOT-23 (Plastic Surface Mount)	RT-6
ADG702BRT	–40°C to +85°C	S4B	SOT-23 (Plastic Surface Mount)	RT-6
ADG701BRM	–40°C to +85°C	S3B	µSOIC (Small Outline)	RM-8
ADG702BRM	–40°C to +85°C	S4B	µSOIC (Small Outline)	RM-8

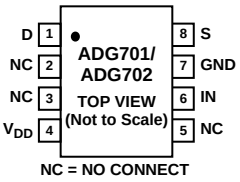
*Brand = Due to package size limitations, these three characters represent the part number.

CAUTION

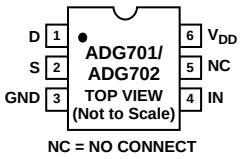
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG701/ADG702 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

8-Lead μSOIC (RM-8)



6-Lead Plastic Surface Mount (SOT-23) (RT-6)



TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R_{ON}	Ohmic Resistance Between D and S.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch "OFF."
I_D (OFF)	Drain Leakage Current with the Switch "OFF."
I_D, I_S (ON)	Channel Leakage Current with the Switch "ON."
V_D (V_S)	Analog Voltage on Terminals D, S.
C_S (OFF)	"OFF" Switch Source Capacitance.
C_D (OFF)	"OFF" Switch Drain Capacitance.
C_D, C_S (ON)	"ON" Switch Capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
t_{OFF}	Delay between applying the digital control input and the output switching off.
Off Isolation	A measure of Unwanted Signal Coupling Through an "OFF" Switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Bandwidth	The frequency at which the output is attenuated by –3 dBs.
On Response	The frequency response of the "ON" switch.
On Loss	The voltage drop across the "ON" switch seen on the On Response vs. Frequency plot as how many dBs the signal is away from 0 dB at very low frequencies.

ADG701/ADG702–Typical Performance Characteristics

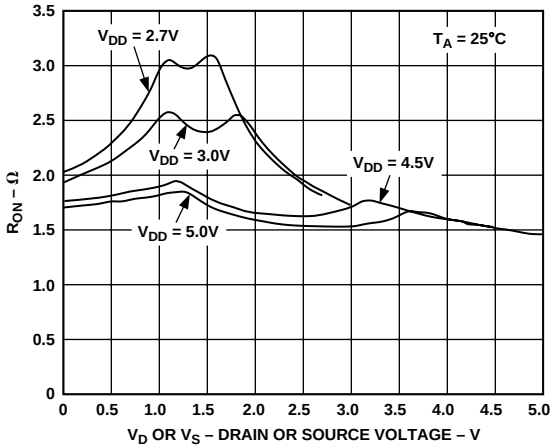


Figure 1. On Resistance as a Function of V_D (V_S) Single Supplies

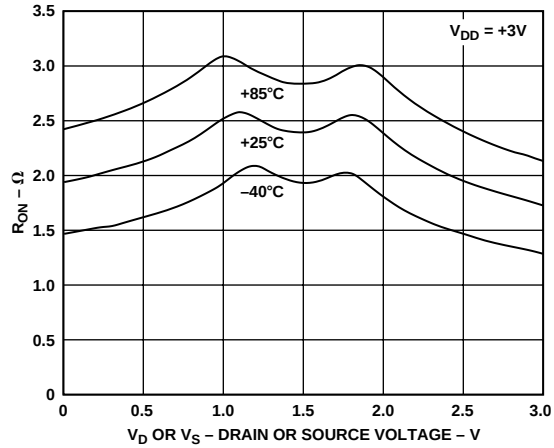


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures V_{DD} = 3 V

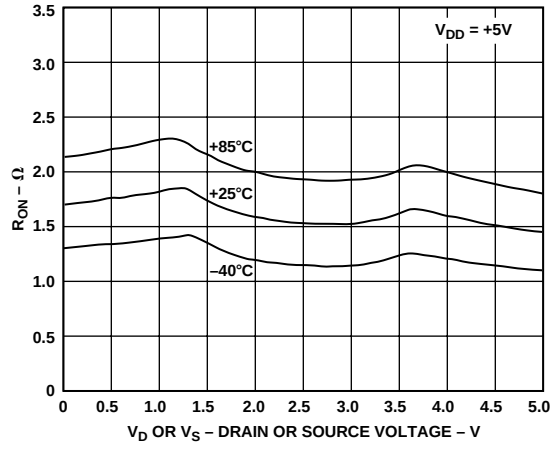


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures V_{DD} = 5 V

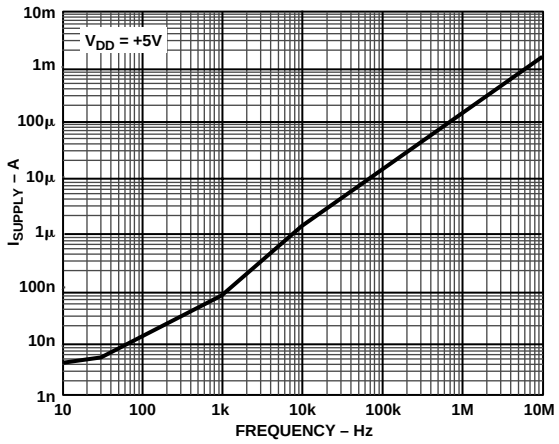


Figure 4. Supply Current vs. Input Switching Frequency

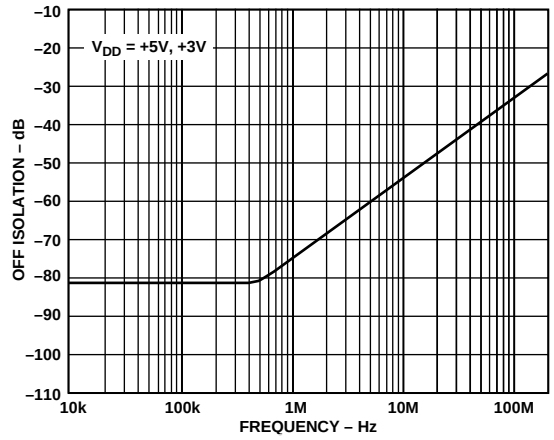


Figure 5. Off Isolation vs. Frequency

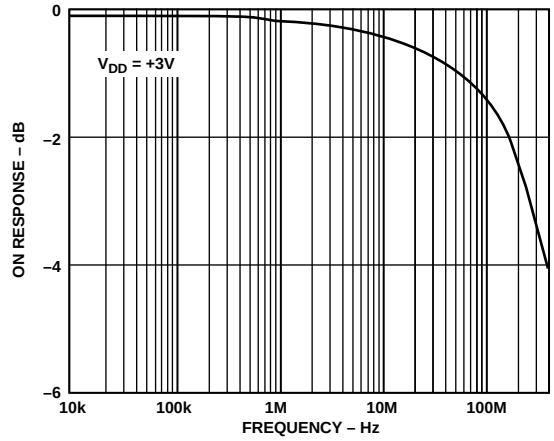
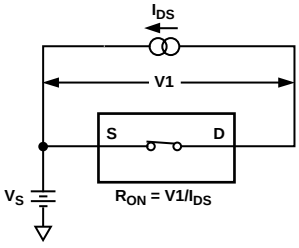
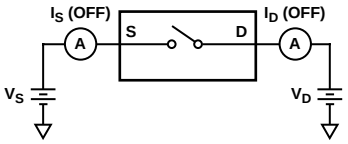


Figure 6. On Response vs. Frequency

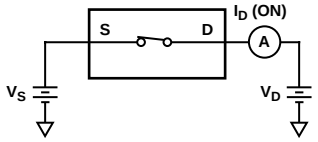
Test Circuits



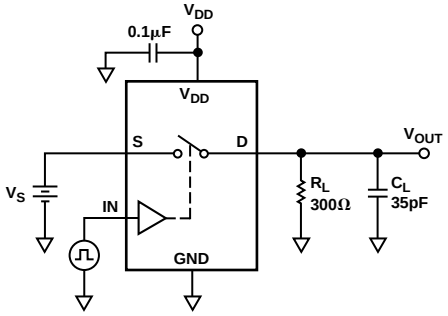
Test Circuit 1. On Resistance

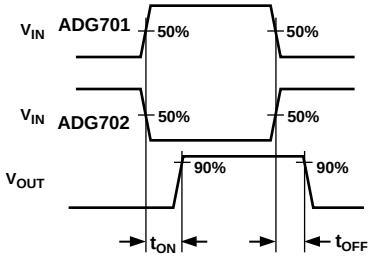


Test Circuit 2. Off Leakage

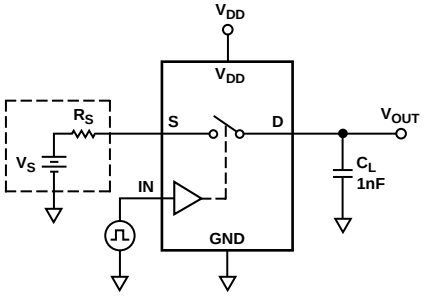


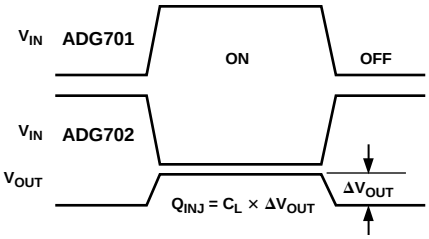
Test Circuit 3. On Leakage



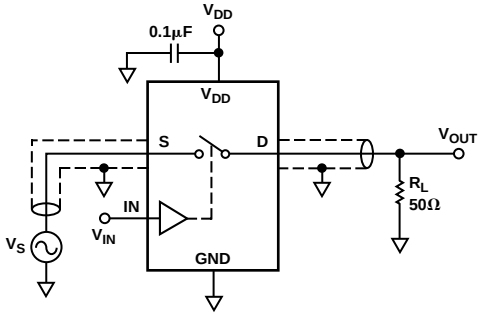


Test Circuit 4. Switching Times

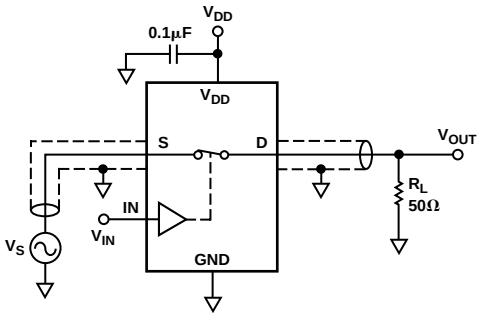




Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation



Test Circuit 7. Bandwidth

APPLICATIONS INFORMATION

The ADG701/ADG702 belongs to Analog Devices' new family of CMOS switches. This series of general purpose switches have improved switching times, lower on resistance, higher bandwidth, low power consumption and low leakage currents.

ADG701/ADG702 Supply Voltages

Functionality of the ADG701/ADG702 extends from +1.8 V to +5.5 V single supply, which makes it ideal for battery powered instruments, where important design parameters are power efficiency and performance.

It is important to note that the supply voltage effects the input signal range, the on resistance and the switching times of the part. By taking a look at the typical performance characteristics and the specifications, the effects of the power supplies can be clearly seen.

For V_{DD} = +1.8 V operation, R_{ON} is typically 40 Ω over the temperature range.

On Response vs. Frequency

Figure 7 illustrates the parasitic components that affect the ac performance of CMOS switches (the switch is shown surrounded by a box). Additional external capacitances will further degrade some performance. These capacitances affect feedthrough, crosstalk and system bandwidth.

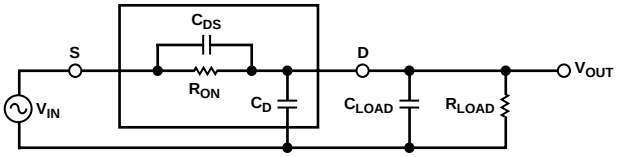


Figure 7. Switch Represented by Equivalent Parasitic Components

The transfer function that describes the equivalent diagram of the switch (Figure 7) is of the form (A)s shown below.

$$A(s) = R_T\left[\frac{s(R_{ON}\ C_{DS})+1}{s(R_{ON}\ C_T\ R_T)+1}\right]$$

where:

$C_T = C_{LOAD} + C_D + C_{DS}$

$R_T = R_{LOAD}/(R_{LOAD} + R_{ON})$

The signal transfer characteristic is dependent on the switch channel capacitance, C_{DS}. This capacitance creates a frequency zero in the numerator of the transfer function A(s). Because the switch on resistance is small, this zero usually occurs at high frequencies. The bandwidth is a function of the switch output capacitance combined with C_{DS} and the load capacitance. The frequency pole corresponding to these capacitances appears in the denominator of A(s).

The dominant effect of the output capacitance, C_D, causes the pole breakpoint frequency to occur first. Therefore, in order to maximize bandwidth a switch must have a low input and output capacitance and low on resistance. The On Response vs. Frequency plot for the ADG701/ADG702 can be seen in Figure 6.

Off Isolation

Off isolation is a measure of the input signal coupled through an off switch to the switch output. The capacitance, C_{DS}, couples the input signal to the output load, when the switch is off, as shown in Figure 8.

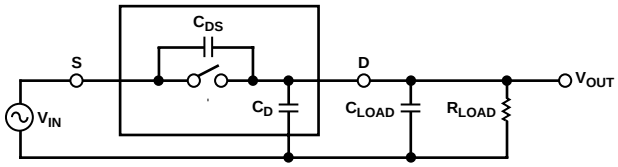


Figure 8. Off Isolation Is Affected by External Load Resistance and Capacitance

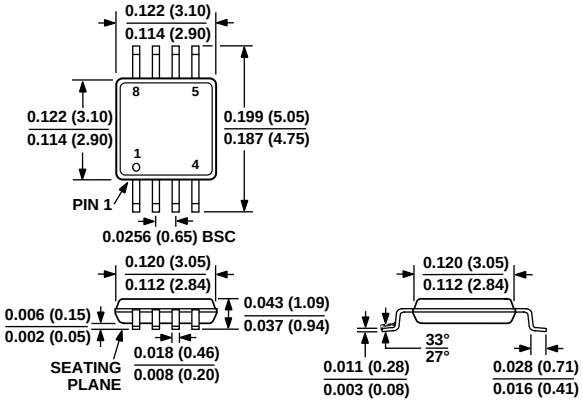
The larger the value of C_{DS}, larger values of feedthrough will be produced. The typical performance characteristic graph of Figure 5 illustrates the drop in off-isolation as a function of frequency. From dc to roughly 1 MHz, the switch shows better than –75 dB isolation. Up to frequencies of 10 MHz, the off isolation remains better than –55 dB. As the frequency increases, more and more of the input signal is coupled through to the output. Off-isolation can be maximized by choosing a switch with the smallest C_{DS} as possible. The values of load resistance and capacitance affect off isolation also, as they contribute to the coefficients of the poles and zeros in the transfer function of the switch when open.

$$A(s) = \left[\frac{s(R_{LOAD}\ C_{DS})}{s(R_{LOAD})(C_T)+1}\right]$$

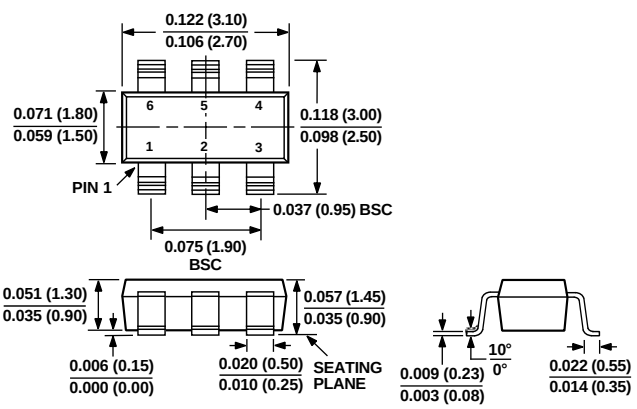
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead μSOIC
(RM-8)



6-Lead Plastic Surface Mount (SOT-23)
(RT-6)



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